CSD19538Q2 100V N 沟道 NexFET™ 功率 MOSFET

1 特性

- 超低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩级
- 无铅
- 符合 RoHS
- 无卤素
- SON 2mm × 2mm 塑料封装

2 应用

- 以太网供电 (PoE)
- 电源设备 (PSE)
- 电机控制

说明

这款 100V 49mΩ 2mm x 2mm SON NexFET™ 功率 MOSFET 旨在用于更大限度地降低功率转换应用中的损耗。

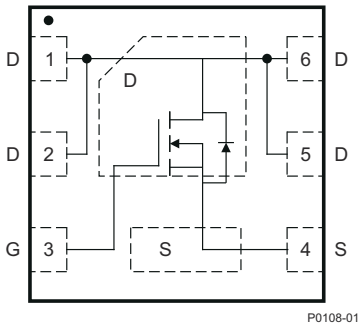


图 3-1. 顶视图

产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	100		V
Q_g	栅极电荷总量 (10V)	4.3		nC
Q_{gd}	栅极电荷（栅极到漏极）	0.8		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 6V	58	mΩ
		V_{GS} = 10V	49	
$V_{GS(th)}$	阈值电压	3.2		V

器件信息(1)

器件	数量	介质	封装	运输
CSD19538Q2	3000	7 英寸卷带	无引线小外形尺寸 (SON) 2.00mm x 2.00mm 塑料封装	卷带包装
CSD19538Q2T	250			
CSD19538Q2R	10,000	13 英寸卷带		

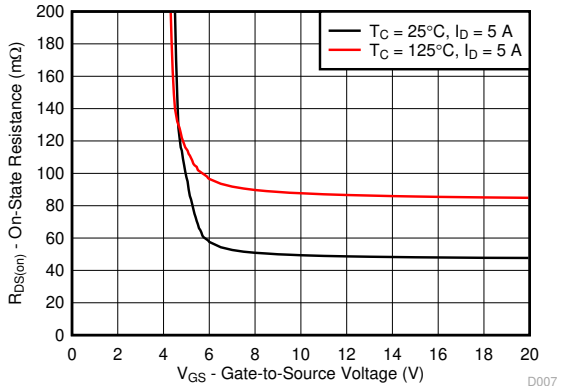
(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

绝对最大额定值

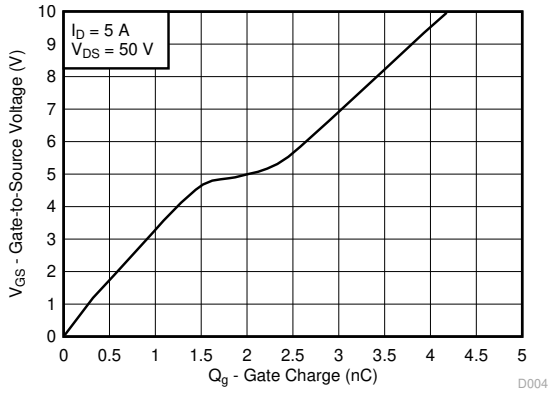
T_A = 25°C		值	单位
V_{DS}	漏源电压	100	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流（受封装限制）	14.4	A
	持续漏极电流（受器件限制），T_C = 25°C 时测得	13.1	
	持续漏极电流(1)	4.6	
I_{DM}	脉冲漏极电流(2)	34.4	A
P_D	功率耗散(1)	2.5	W
	功率耗散，T_C = 25°C	20.2	
T_J、T_{stg}	工作结温，贮存温度	-55 至 150	°C
E_{AS}	雪崩能量，单脉冲 I_D = 12.6A，L = 0.1mH，R_G = 25Ω	8	mJ

(1) 0.06 英寸厚 FR4 PCB 上 1 平方英寸、2oz. 铜焊盘上的 $R_{\theta JA}$ = 50°C/W（典型值）。

(2) 最大 $R_{\theta JC}$ = 6.2°C/W，脉冲持续时间 ≤ 100μs，占空比 ≤ 1%。



$R_{DS(on)}$ 与 V_{GS} 之间的关系



栅极电荷

Table of Contents

3 Specifications

3.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

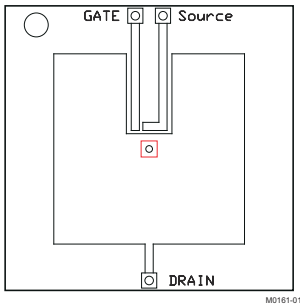
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0V, I_D = 250 μA	100			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0V, V_{DS} = 80V			1	μA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0V, V_{GS} = 20V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 μA	2.8	3.2	3.8	V
$R_{DS(on)}$	Drain-to-source on resistance	V_{GS} = 6V, I_D = 5A		58	72	mΩ
		V_{GS} = 10V, I_D = 5A		49	59	
g_{fs}	Transconductance	V_{DS} = 10V, I_D = 5A		19		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0V, V_{DS} = 50V, f = 1MHz		349	454	pF
C_{oss}	Output capacitance			69	90	pF
C_{rss}	Reverse transfer capacitance			12.6	16.4	pF
R_G	Series gate resistance			4.6	9.2	Ω
Q_g	Gate charge total (10V)	V_{DS} = 50V, I_D = 5A		4.3	5.6	nC
Q_{gd}	Gate charge gate-to-drain			0.8		nC
Q_{gs}	Gate charge gate-to-source			1.6		nC
$Q_{g(th)}$	Gate charge at V_{th}			1.0		nC
Q_{oss}	Output charge	V_{DS} = 50V, V_{GS} = 0V		12.3		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 50V, V_{GS} = 10V, I_{DS} = 5A, R_G = 0Ω		5		ns
t_r	Rise time			3		ns
$t_{d(off)}$	Turnoff delay time			7		ns
t_f	Fall time			2		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 5A, V_{GS} = 0V		0.85	1.0	V
Q_{rr}	Reverse recovery charge	V_{DS}= 50V, I_F = 5A, di/dt = 300A/μs		94		nC
t_{rr}	Reverse recovery time			32		ns

3.2 Thermal Information

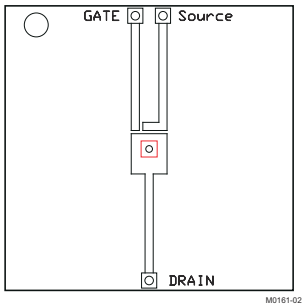
T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance(1)			6.2	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1) (2)			65	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1in² (6.45cm²), 2oz (0.071mm) thick Cu pad on a 1.5in × 1.5in (3.81cm × 3.81cm), 0.06in (1.52mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1in² (6.45cm²), 2oz (0.071mm) thick Cu.



Max $R_{\theta JA}$ = 65°C/W when mounted on 1in^2 (6.45cm^2) of 2oz (0.071mm) thick Cu.



Max $R_{\theta JA}$ = 250°C/W when mounted on a minimum pad area of 2oz (0.071mm) thick Cu.

3.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

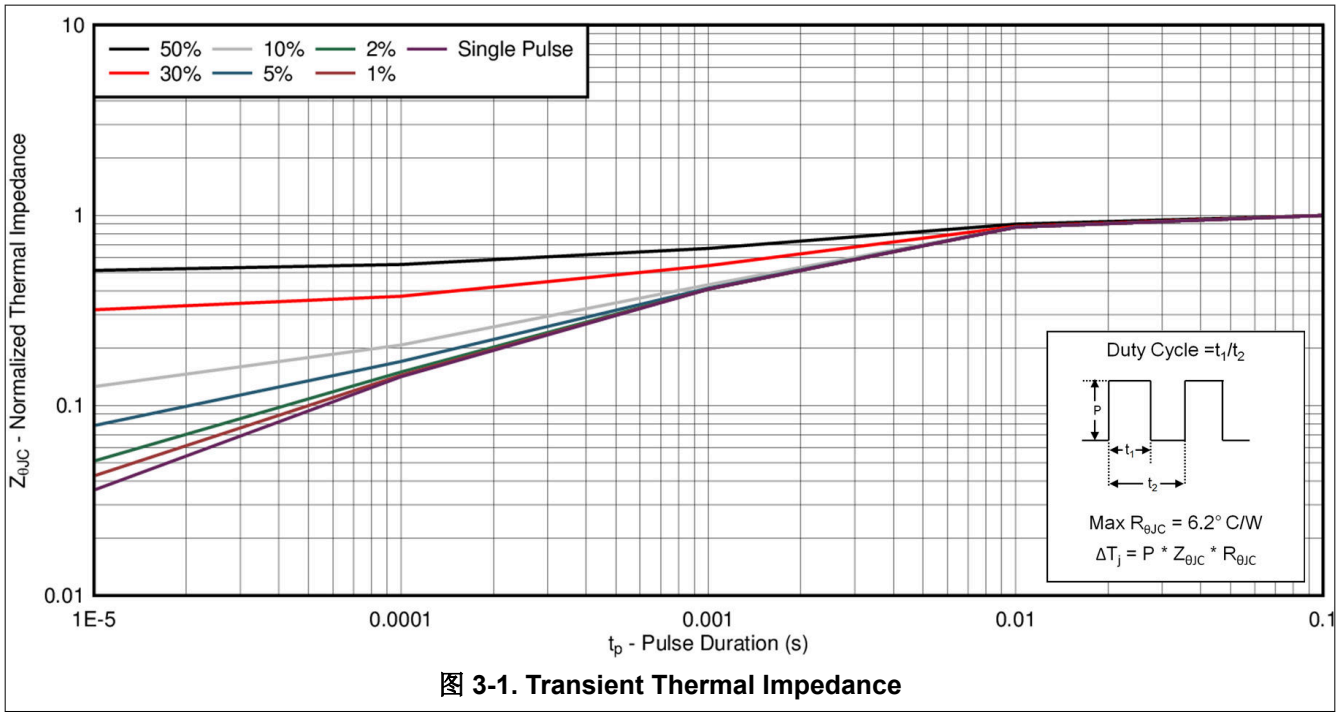


图 3-1. Transient Thermal Impedance

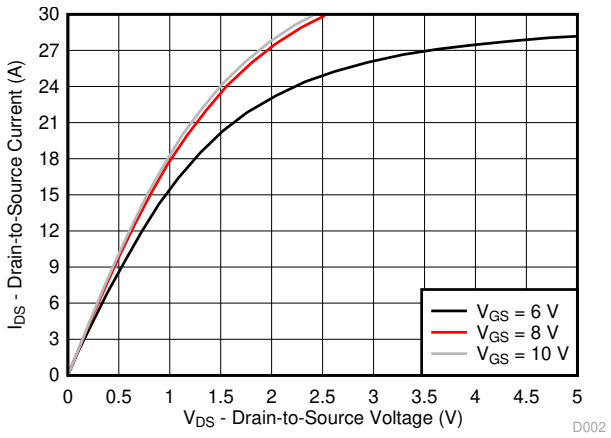
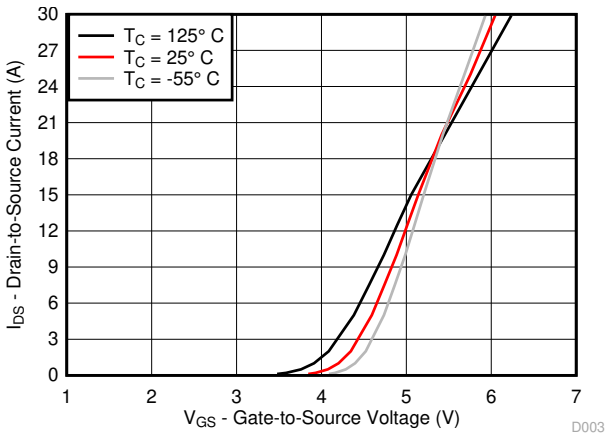
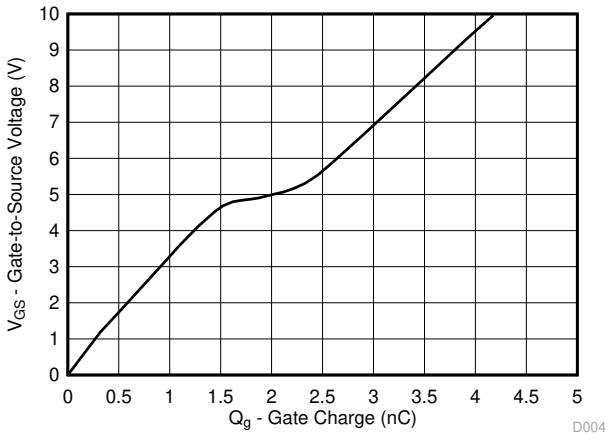


图 3-2. Saturation Characteristics



V_{DS} = 5V

图 3-3. Transfer Characteristics



I_D = 5A V_{DS} = 50V

图 3-4. Gate Charge

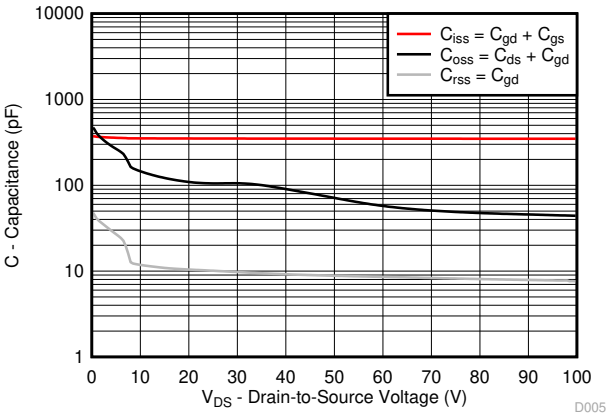
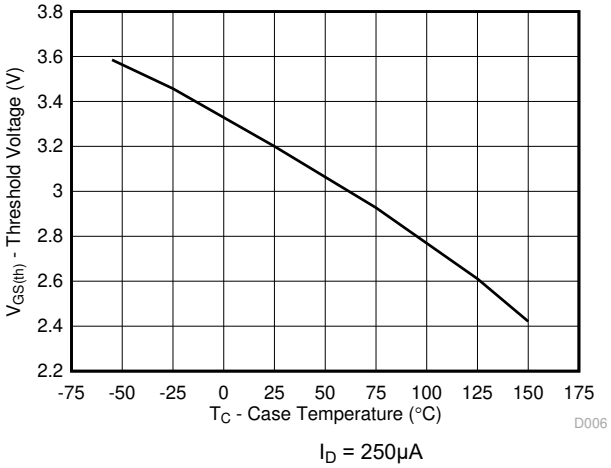


图 3-5. Capacitance



I_D = 250µA

图 3-6. Threshold Voltage vs Temperature

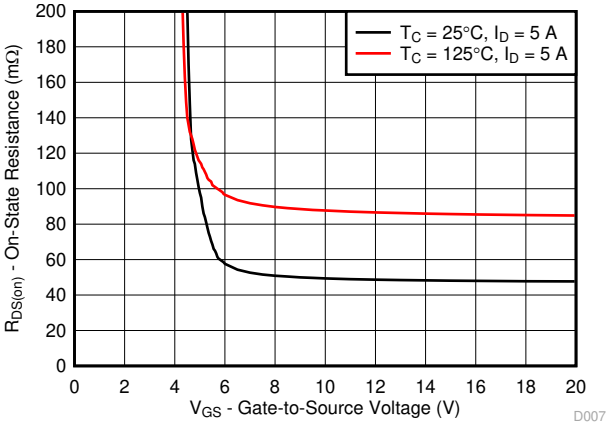
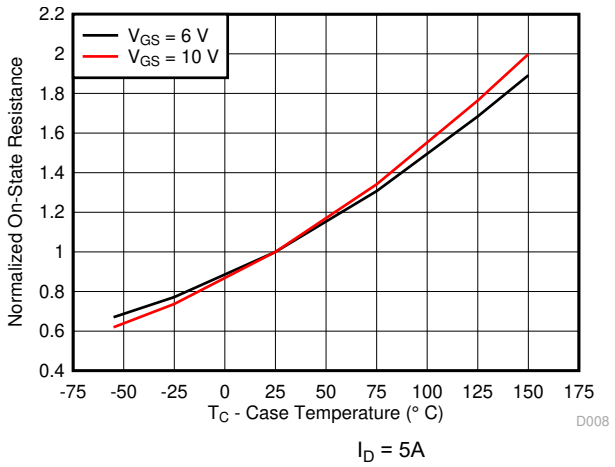


图 3-7. On-State Resistance vs Gate-to-Source Voltage



I_D = 5A

图 3-8. Normalized On-State Resistance vs Temperature

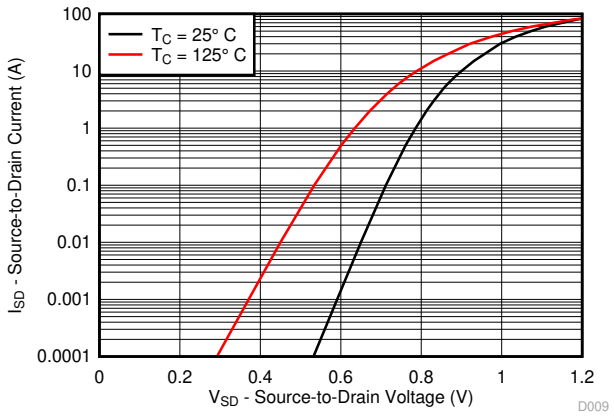
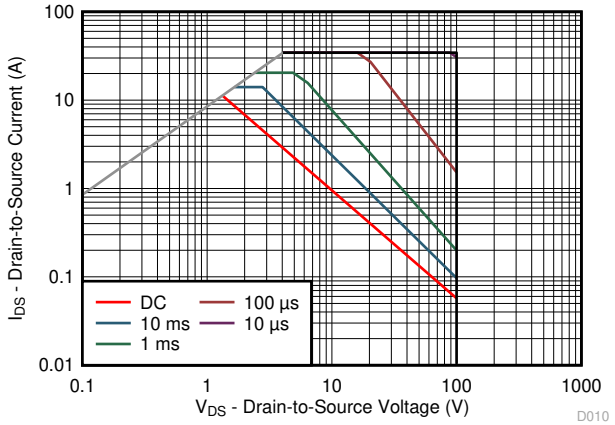


图 3-9. Typical Diode Forward Voltage



Single pulse, max $R_{\theta JC}$ = 6.2°C/W

图 3-10. Maximum Safe Operating Area

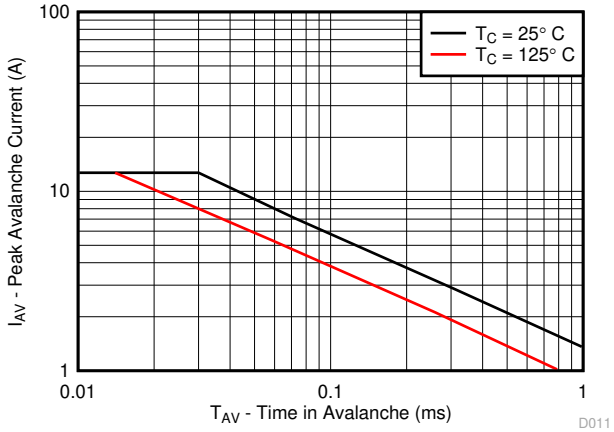


图 3-11. Single Pulse Unclamped Inductive Switching

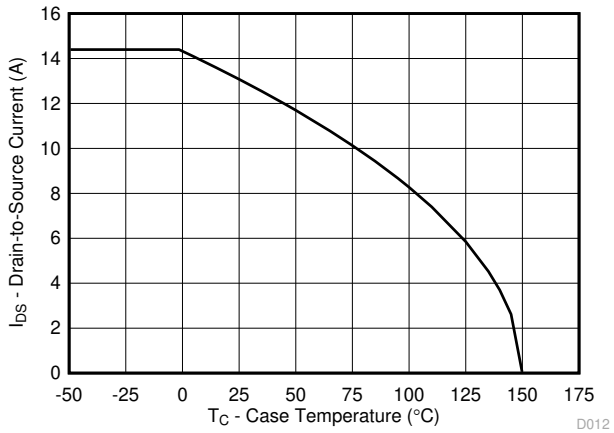


图 3-12. Maximum Drain Current vs Temperature

4 Device and Documentation Support

4.1 第三方产品免责声明

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4.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

4.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

4.4 Trademarks

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4.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

4.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

5 Revision History

Changes from Revision A (January 2017) to Revision B (March 2024)	Page
• 通篇更新了表格、图和交叉参考的编号格式	1

Changes from Revision * (July 2016) to Revision A (January 2017)	Page
• 将图 3-2 曲线中的测试电压 V_{DS} 从 100V 更改为 50V	1
• Changed test voltage V_{DS} from 100V : to 50V in 图 3-4	4

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD19538Q2	Active	Production	WSON (DQK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	1958
CSD19538Q2.B	Active	Production	WSON (DQK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	1958
CSD19538Q2G4.B	Active	Production	WSON (DQK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	1958
CSD19538Q2R	Active	Production	WSON (DQK) | 6	10000 | JUMBO T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	1958
CSD19538Q2R.B	Active	Production	WSON (DQK) | 6	10000 | JUMBO T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	1958
CSD19538Q2T	Active	Production	WSON (DQK) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	1958
CSD19538Q2T.B	Active	Production	WSON (DQK) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	1958

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

GENERIC PACKAGE VIEW

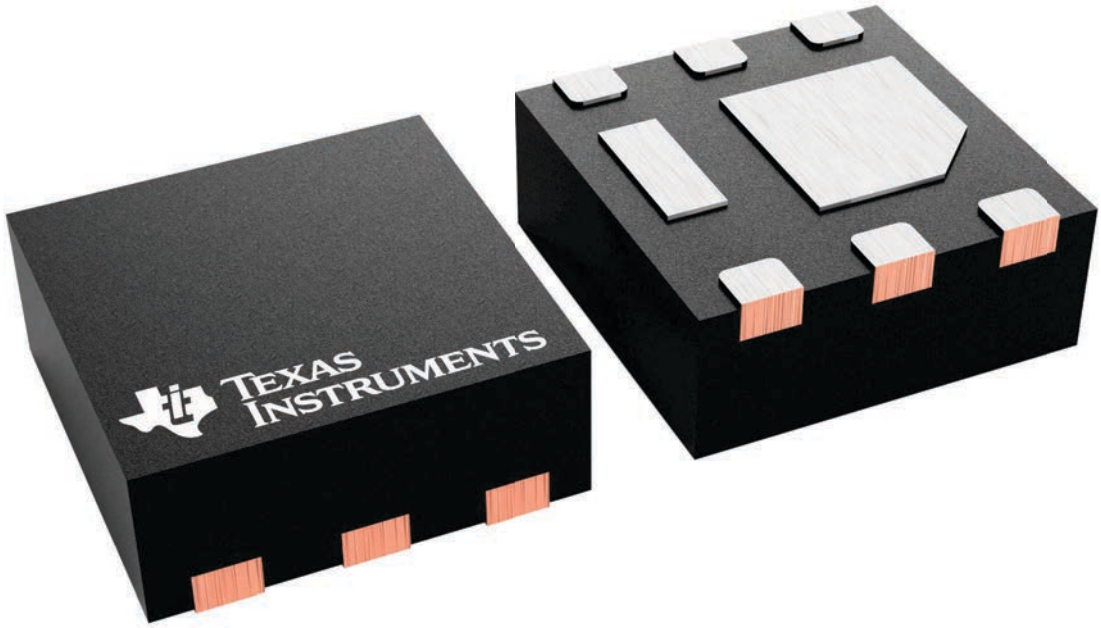
DQK 6

WSON - 0.8 mm max height

2 x 2, 0.65 mm pitch

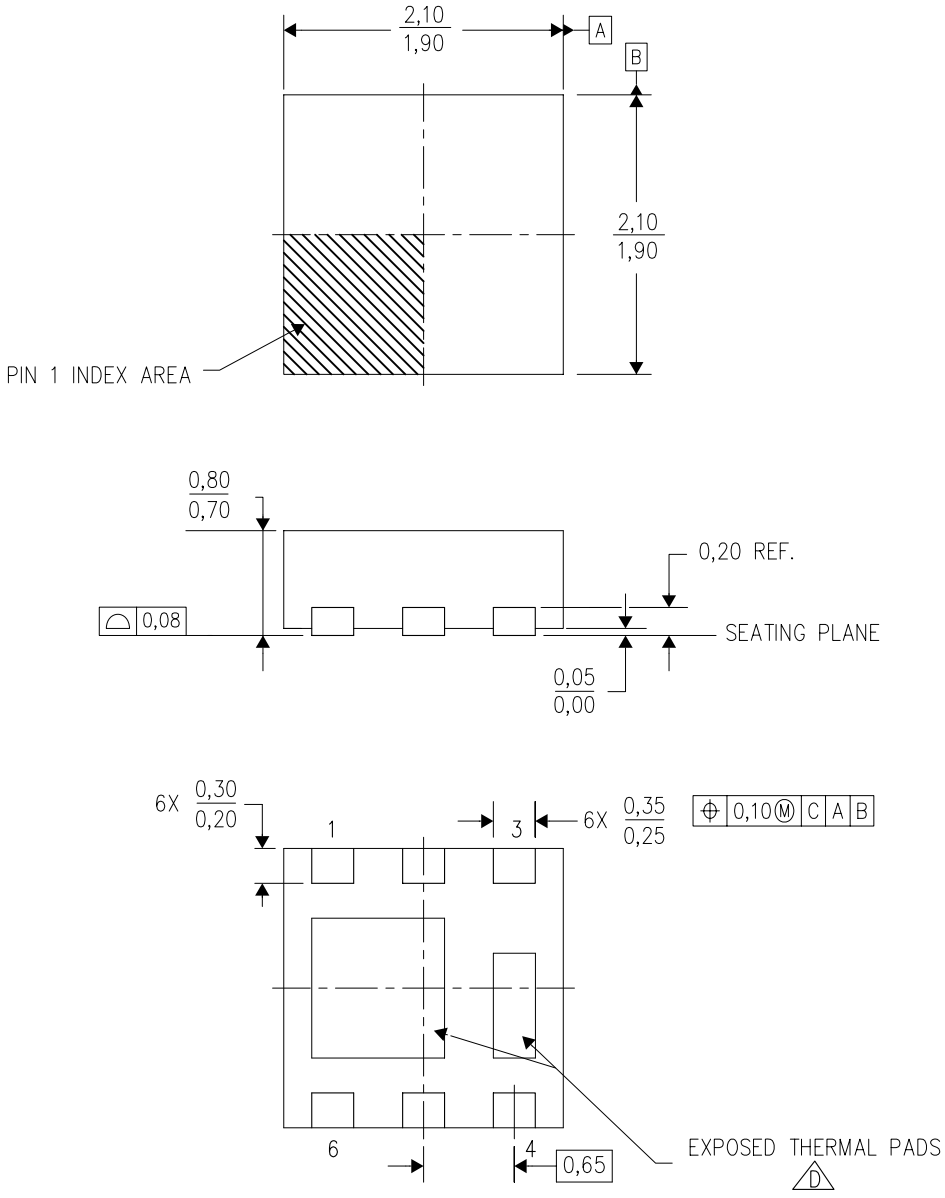
PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229807/A

DQK (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4210192/B 01/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pads must be soldered to the board for thermal and mechanical performance.

THERMAL PAD MECHANICAL DATA

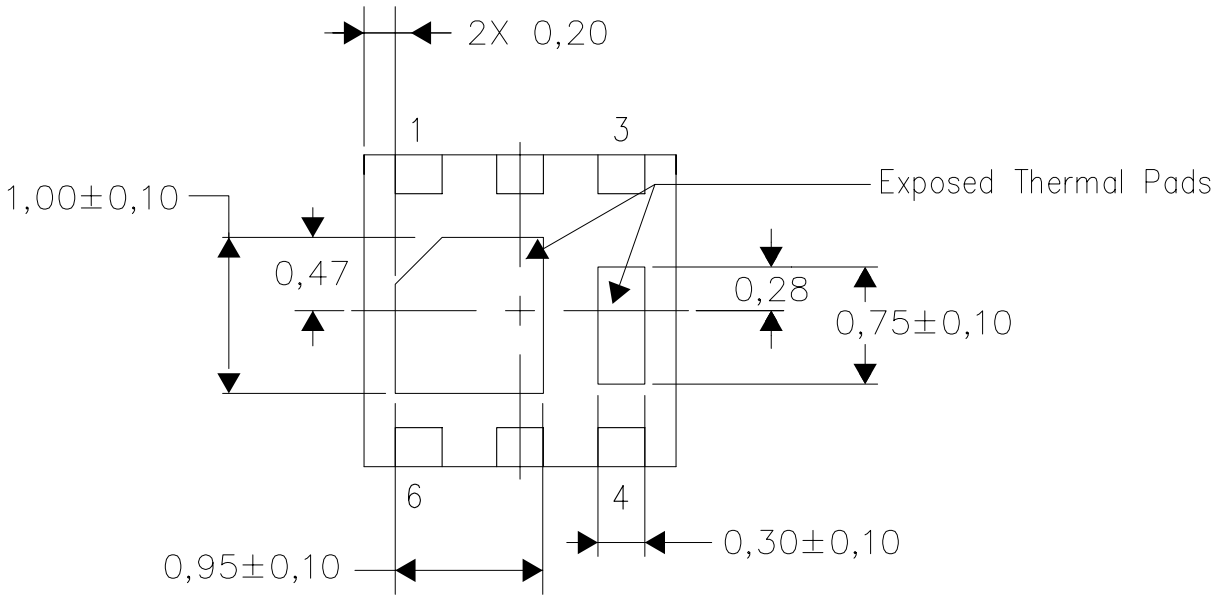
DQK (S–PWSON–N6)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

重要通知和免责声明

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