

CSD19535KTT 100V N 沟道 NexFET™ 功率 MOSFET

1 特性

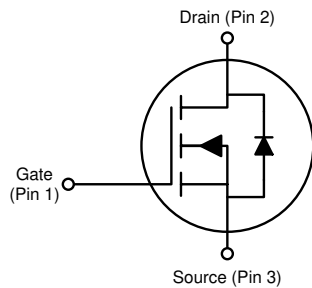
- 超低 Q_g 和 Q_{gd}
- 低热阻
- 具有雪崩能力
- 无铅端子镀层
- 符合 RoHS
- 无卤素
- D²PAK 塑料封装

2 应用

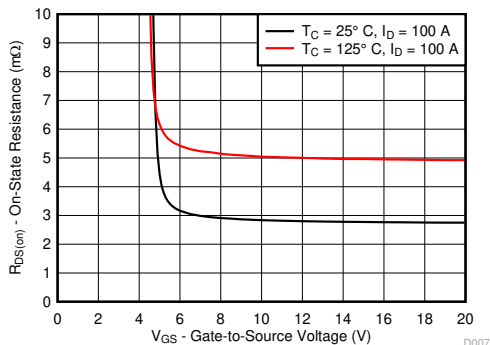
- 热插拔
- 电机控制
- 次级侧同步整流器

3 说明

这款 100V、 $2.8\text{m}\Omega$ 、D²PAK (TO-263) NexFET™ 功率 MOSFET 旨在用于更大限度地降低功率转换应用中的损耗。



引脚排列



$R_{DS(on)}$ 与 V_{GS} 之间的关系

产品概要

$T_A = 25^\circ\text{C}$		典型值	单位
V_{DS}	漏源电压	100	V
Q_g	栅极电荷总量 (10V)	75	nC
Q_{gd}	栅极电荷 (栅极到漏极)	11	nC
$R_{DS(on)}$	漏源导通电阻	$V_{GS} = 6\text{V}$	3.2
		$V_{GS} = 10\text{V}$	2.8
$V_{GS(th)}$	阈值电压	2.7	V

器件信息 (1)

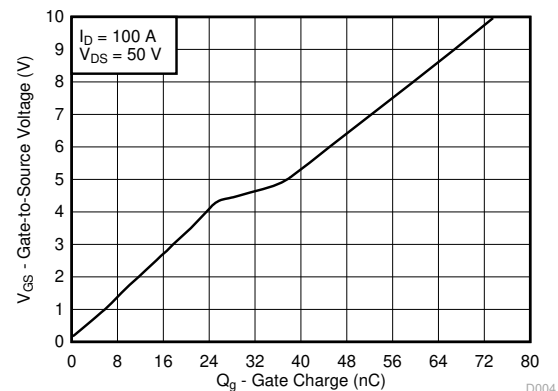
器件	数量	介质	封装	运输
CSD19535KTT	500	13 英寸卷带	D ² PAK 塑料封装	卷带包装
CSD19535KTTT	50			

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

绝对最大额定值

$T_A = 25^\circ\text{C}$		值	单位
V_{DS}	漏源电压	100	V
V_{GS}	栅源电压	± 20	V
I_D	持续漏极电流 (受封装限制)	200	A
	持续漏极电流 (受器件限制), $T_C = 25^\circ\text{C}$	197	
	持续漏极电流 (受器件限制), $T_C = 100^\circ\text{C}$	139	
I_{DM}	脉冲漏极电流 ⁽¹⁾	400	A
P_D	功率耗散, $T_C = 25^\circ\text{C}$	300	W
T_J, T_{stg}	工作结温, 贮存温度	-55 至 175	$^\circ\text{C}$
E_{AS}	雪崩能量, 单脉冲 $I_D = 95\text{A}, L = 0.1\text{mH}$	451	mJ

(1) 最大 $R_{\theta JC} = 0.5^\circ\text{C/W}$, 脉冲持续时间 $\leq 100\mu\text{s}$, 占空比 $\leq 1\%$ 。



栅极电荷



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4 规格

4.1 电气特性

$T_A = 25^\circ\text{C}$ (除非另外注明)

参数		测试条件		最小值	典型值	最大值	单位
静态特性							
BV _{DSS}	漏源电压	V _{GS} = 0V , I _D = 250 μ A		100			V
I _{DSS}	漏源漏电流	V _{GS} = 0V , V _{DS} = 80V				1	μ A
I _{GSS}	栅源漏电流	V _{DS} = 0V , V _{GS} = 20V				100	nA
V _{GS(th)}	栅源阈值电压	V _{DS} = V _{GS} , I _D = 250 μ A		2.2	2.7	3.4	V
R _{DS(on)}	漏源导通电阻	V _{GS} = 6V , I _D = 100A			3.2	4.1	m Ω
		V _{GS} = 10V , I _D = 100A			2.8	3.4	
g _{fs}	跨导	V _{DS} = 10V , I _D = 100A		301			S
动态特性							
C _{iss}	输入电容	V _{GS} = 0V , V _{DS} = 50V , f = 1MHz		6100	7930		pF
C _{oss}	输出电容			1160	1510		pF
C _{rss}	反向传输电容			29	38		pF
R _G	串联栅极电阻			1.4	2.8		Ω
Q _g	栅极电荷总量 (10V)	V _{DS} = 50V , I _D = 100A		75	98		nC
Q _{gd}	栅极电荷 (栅极到漏极)			11			nC
Q _{gs}	栅极电荷 (栅漏极)			25			nC
Q _{g(th)}	V _{th} 下的栅极电荷			16			nC
Q _{oss}	输出电荷	V _{DS} = 50V , V _{GS} = 0V		210			nC
t _{d(on)}	导通延迟时间	V _{DS} = 50V , V _{GS} = 10V , I _{DS} = 100A , R _G = 0Ω		9			ns
t _r	上升时间			18			ns
t _{d(off)}	关断延迟时间			21			ns
t _f	下降时间			15			ns
二极管特性							
V _{SD}	二极管正向电压	I _{SD} = 100A , V _{GS} = 0V		0.9	1.1		V
Q _{rr}	反向恢复电荷	V _{DS} = 50V , I _F = 100A , di/dt = 300A/ μ s		435			nC
t _{rr}	反向恢复时间			85			ns

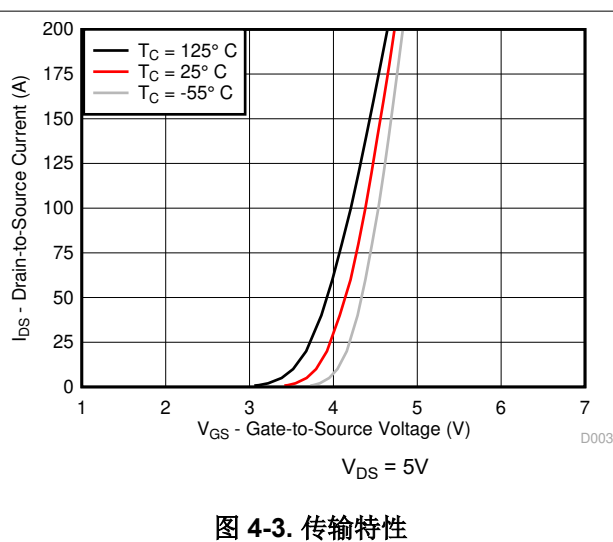
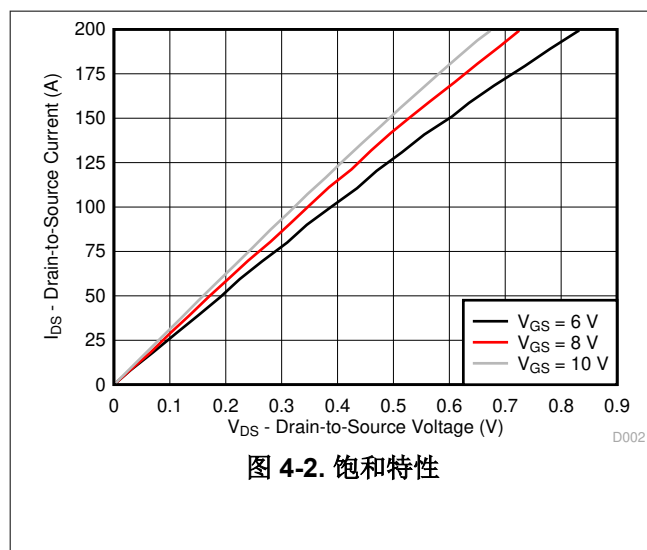
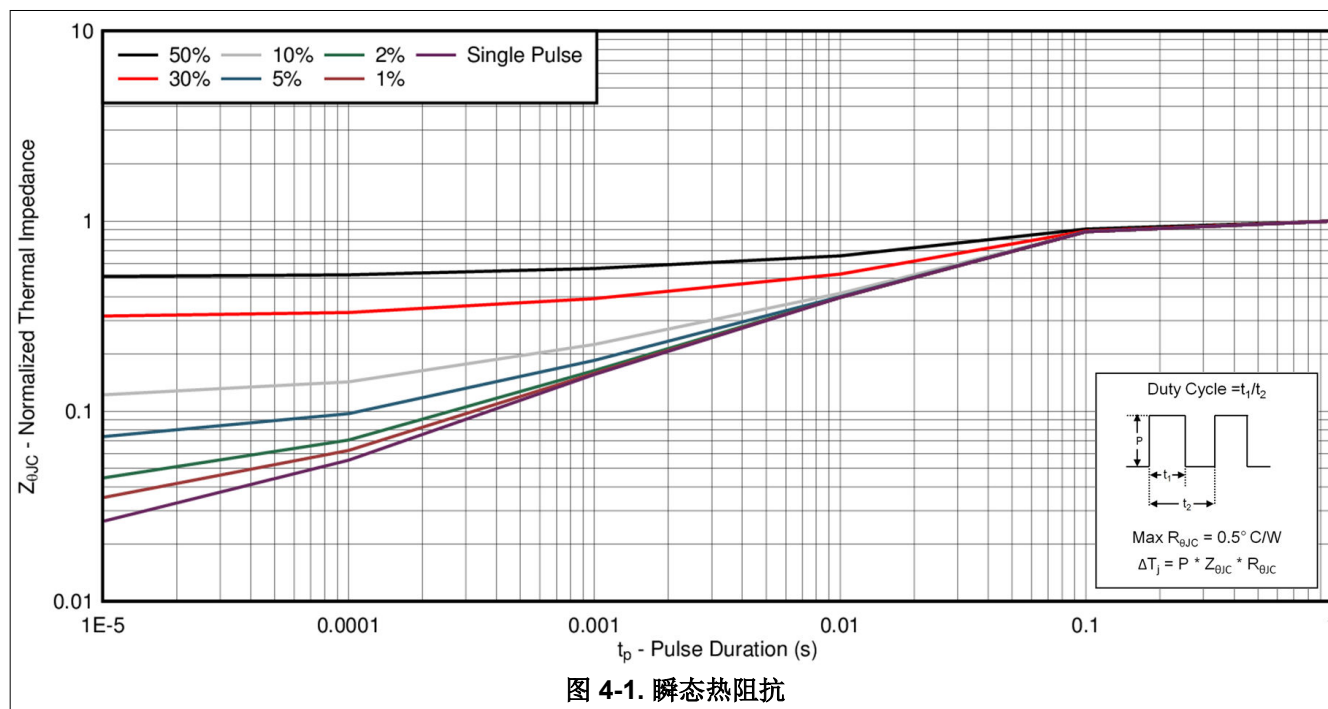
4.2 热性能信息

$T_A = 25^\circ\text{C}$ (除非另外注明)

热指标	最小值	典型值	最大值	单位
$R_{\theta JC}$ 结至外壳热阻			0.5	$^\circ\text{C/W}$
$R_{\theta JA}$ 结至环境热阻			62	$^\circ\text{C/W}$

4.3 典型 MOSFET 特性

$T_A = 25^\circ\text{C}$ (除非另外注明)



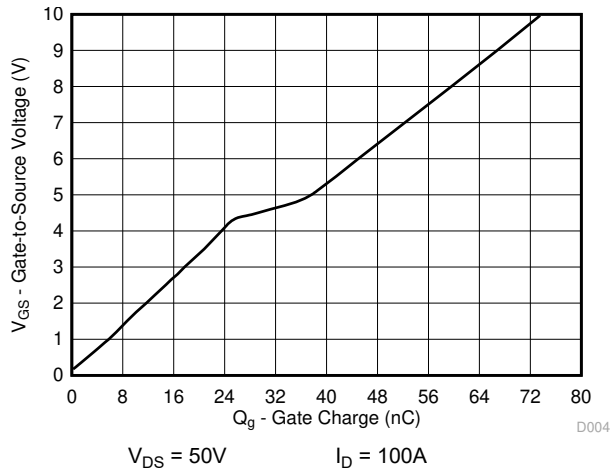


图 4-4. 栅极电荷

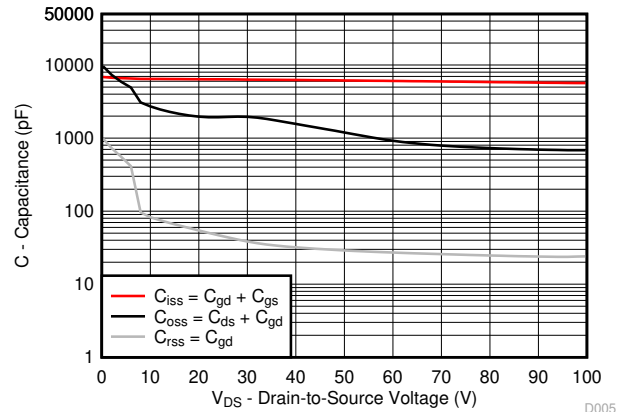


图 4-5. 电容

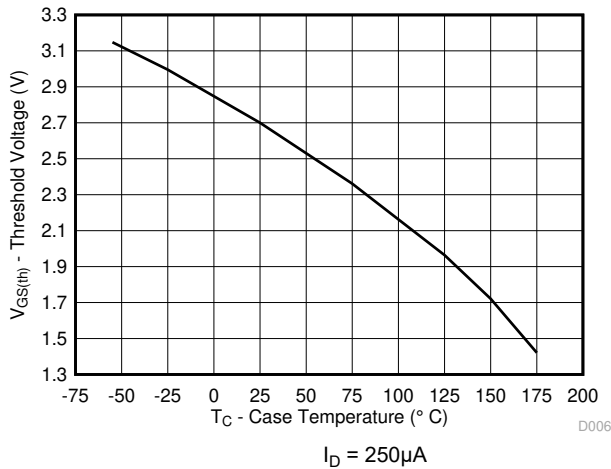


图 4-6. 阈值电压与温度间的关系

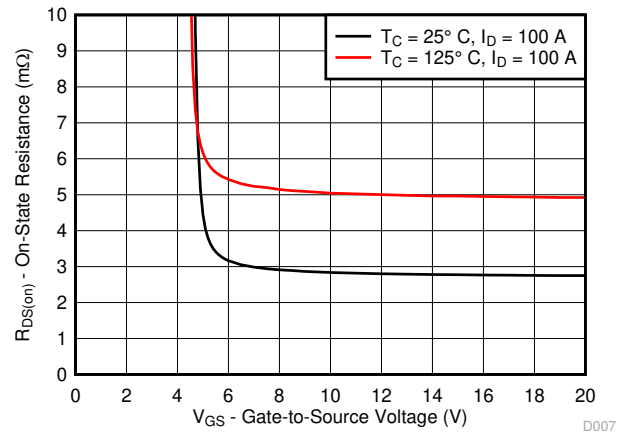


图 4-7. 导通电阻与栅源电压

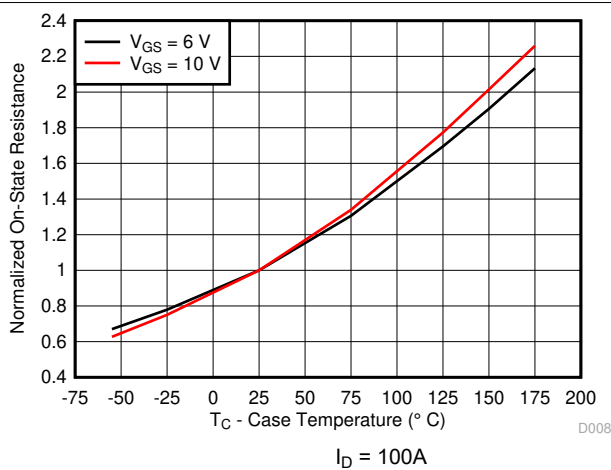


图 4-8. 标准化通态电阻与温度的关系

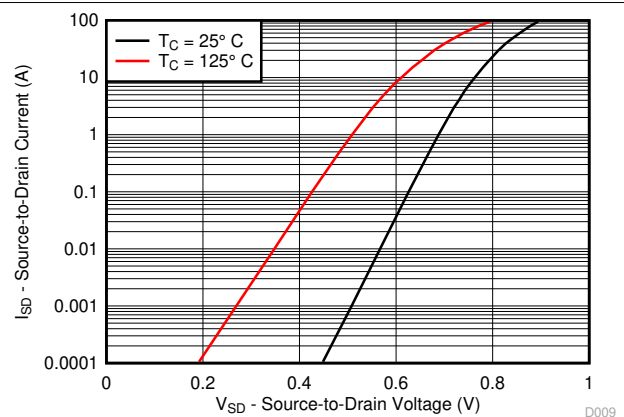


图 4-9. 典型二极管正向电压

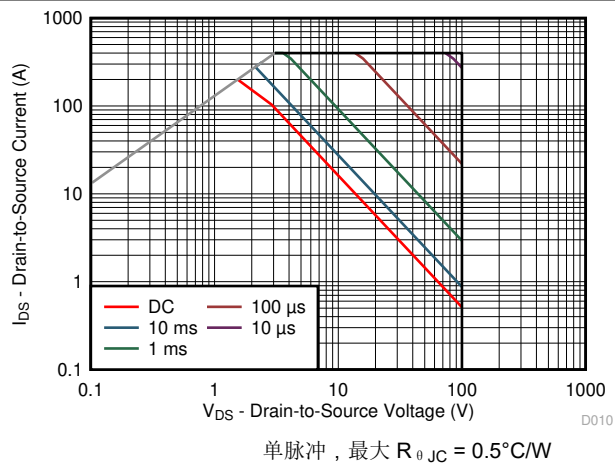


图 4-10. 最大安全工作区

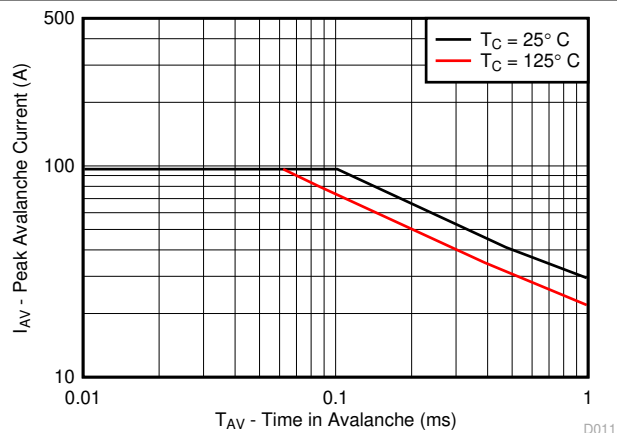


图 4-11. 单脉冲非钳位电感式开关

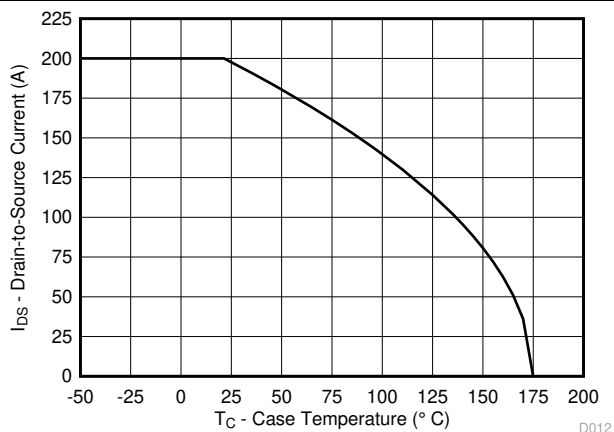


图 4-12. 最大漏极电流与温度间的关系

5 器件和文档支持

5.1 第三方产品免责声明

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5.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

5.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

5.4 商标

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TI E2E™ is a trademark of Texas Instruments.

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5.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

5.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

6 修订历史记录

Changes from Revision B (January 2017) to Revision C (May 2025)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1

7 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD19535KTT	Active	Production	DDPAK/ TO-263 (KTT) 2	500 LARGE T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 175	CSD19535KTT
CSD19535KTT.B	Active	Production	DDPAK/ TO-263 (KTT) 2	500 LARGE T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 175	CSD19535KTT
CSD19535KTTT	Active	Production	DDPAK/ TO-263 (KTT) 2	50 SMALL T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 175	CSD19535KTT
CSD19535KTTT.B	Active	Production	DDPAK/ TO-263 (KTT) 2	50 SMALL T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 175	CSD19535KTT

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD19535KTT	DDPAK/ TO-263	KTT	2	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
CSD19535KTTT	DDPAK/ TO-263	KTT	2	50	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2

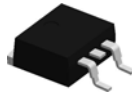
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD19535KTT	DDPAK/TO-263	KTT	2	500	340.0	340.0	38.0
CSD19535KTTT	DDPAK/TO-263	KTT	2	50	340.0	340.0	38.0

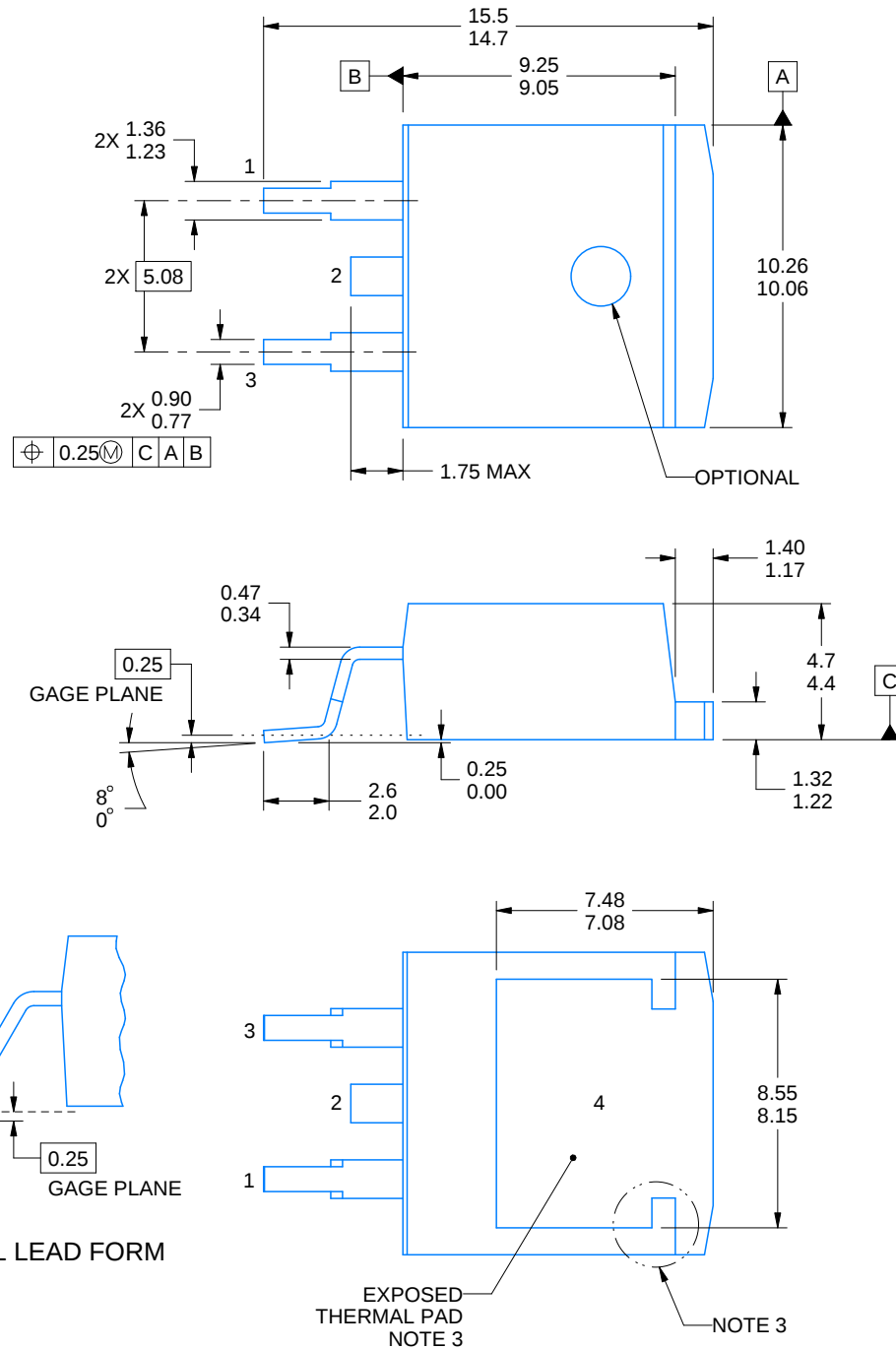
KTT0002A



PACKAGE OUTLINE

TO-263 - 4.7 mm max height

TRANSISTOR OUTLINE



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NOTES:

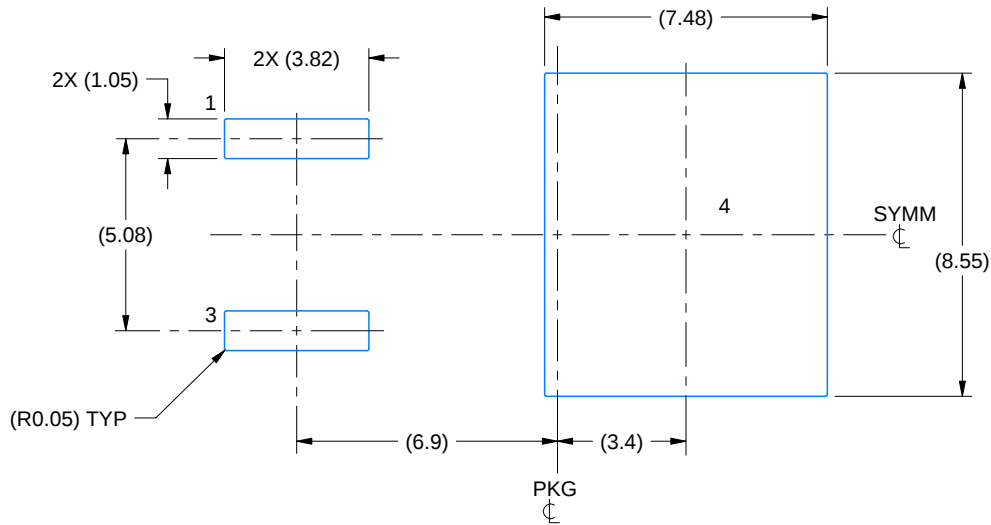
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Features may not exist and shape may vary per different assembly sites. Pin 2 and Pin 4 connected.
4. Reference JEDEC registration TO-263.

EXAMPLE BOARD LAYOUT

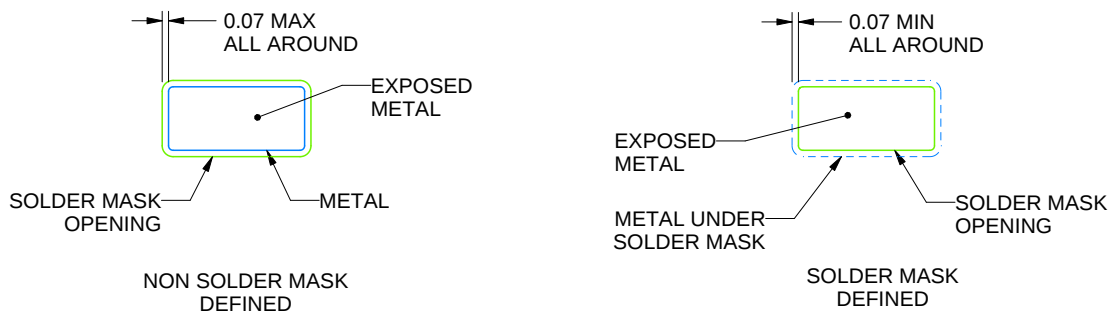
KTT0002A

TO-263 - 4.7 mm max height

TRANSISTOR OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:5X



SOLDER MASK DETAILS

4222117/D 08/2025

NOTES: (continued)

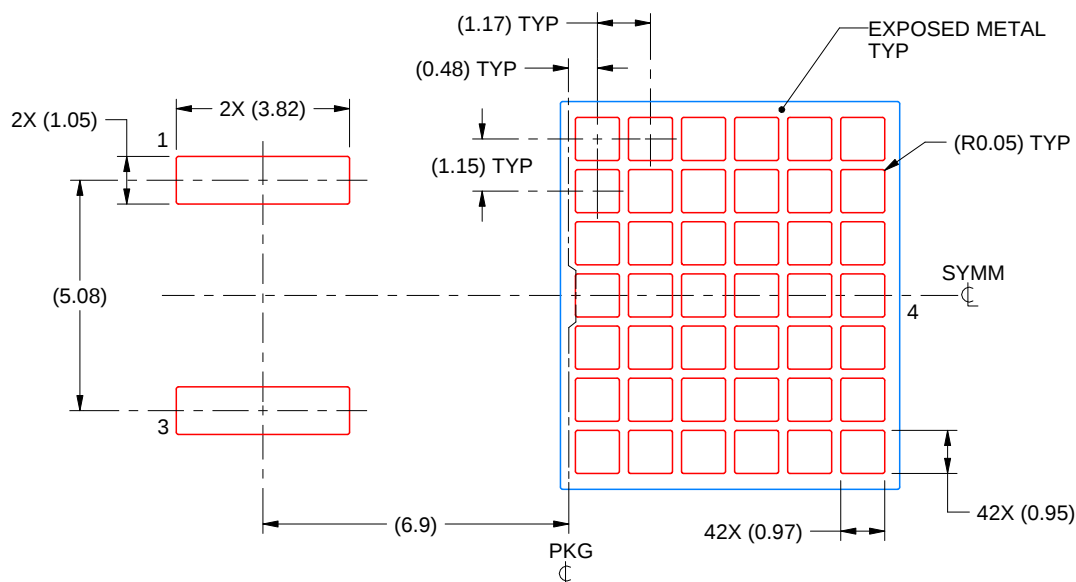
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

KTT0002A

TO-263 - 4.7 mm max height

TRANSISTOR OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
60.5% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

4222117/D 08/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

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