# CSD18541F5 60V N 沟道 FemtoFET™ MOSFET

## 1 特性

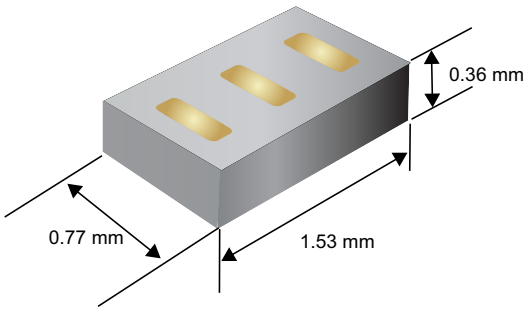
- 低导通电阻
- 超低 $Q_g$ 和 $Q_{gd}$
- 超小尺寸
  - 1.53mm × 0.77mm
- 薄型封装
  - 厚度为 0.36mm
- 集成型 ESD 保护二极管
- 无铅且无卤素
- 符合 RoHS

## 2 应用

- 针对工业负载开关应用进行了优化
- 针对通用开关应用进行了优化

## 3 说明

该 54mΩ、60V N 沟道 FemtoFET™ MOSFET 技术经过设计和优化，能够最大限度地减小在空间受限的工业负载开关应用中占用的空间。这项技术能够在替代标准小信号 MOSFET 的同时大幅减小封装尺寸。




典型器件尺寸

**产品概要**

| $T_A$ = 25°C | | 典型值 | | 单位 |
|---|---|---|---|---|
| $V_{DS}$ | 漏源电压 | 60 | | V |
| $Q_g$ | 栅极电荷总量 (10V) | 11 | | nC |
| $Q_{gd}$ | 栅极电荷 ( 栅极到漏极 ) | 1.6 | | nC |
| $R_{DS(on)}$ | 漏源导通电阻 | $V_{GS}$ = 4.5V | 57 | mΩ |
| | | $V_{GS}$ = 10V | 54 | |
| $V_{GS(th)}$ | 阈值电压 | 1.75 | | V |

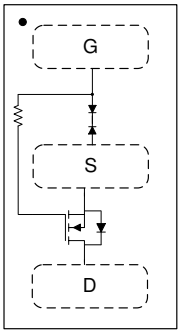
**器件信息**

| 器件 | 数量 | 介质 | 封装 | 配送 |
|---|---|---|---|---|
| CSD18541F5 | 3000 | 7 英寸卷带 | Femto 1.53mm × 0.77mm 无引线 SMD | 卷带包装 |
| CSD18541F5T | 250 | | | |

1. 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

**绝对最大额定值**

| $T_A$ = 25°C | | 值 | 单位 |
|---|---|---|---|
| $V_{DS}$ | 漏源电压 | 60 | V |
| $V_{GS}$ | 栅源电压 | ±20 | V |
| $I_D$ | 持续漏极电流 | 2.2 | A |
| $I_{DM}$ | 脉冲漏极电流 (1)(2) | 21 | A |
| $P_D$ | 功率耗散 | 500 | mW |
| $T_J$、$T_{stg}$ | 工作结温，贮存温度 | –55 至 150 | °C |
| $E_{AS}$ | 雪崩能量，单脉冲 $I_D$ = 12.8A，L = 0.1mH，$R_G$ = 25Ω | 8.2 | mJ |




顶视图

# Table of Contents

**1 特性**.....1
**2 应用**.....1
**3 说明**.....1
**4 Revision History**.....2
**5 Specifications**.....3
5.1 Electrical Characteristics.....3
5.2 Thermal Information.....3
5.3 Typical MOSFET Characteristics.....3
**6 Device and Documentation Support**.....7
6.1 Receiving Notification of Documentation Updates.....7
6.2 Community Resources.....7
6.3 Trademarks.....7
**7 Mechanical, Packaging, and Orderable Information**.....8
7.1 Mechanical Dimensions.....8
7.2 Recommended Minimum PCB Layout.....9
7.3 Recommended Stencil Pattern.....9

## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision A (December 2016) to Revision B (February 2022) | Page |
|---|---|
| • 将超薄型封装要点中的厚度从 0.35mm 更改为 0.36mm | 1 |
| • 将超薄型封装图片中的厚度从 0.35mm 更新为 0.36mm | 1 |
| • Changed ultra-low profile image height from 0.35 mm to 0.36 mm | 8 |
| • Added FemtoFET Surface Mount Guide note | 9 |

| Changes from Revision * (May 2016) to Revision A (August 2017) | Page |
|---|---|
| • Added the *节 6.1* section to *节 6* | 7 |
| • Added *表 7-1* to the *节 7.1* section | 8 |
| • Updated the *节 7.2* | 9 |
| • Updated the *节 7.3* | 9 |

# 5 Specifications

## 5.1 Electrical Characteristics

$T_A$ = 25°C (unless otherwise stated)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **STATIC CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain-to-source voltage | $V_{GS}$ = 0 V, $I_{DS}$ = 250 μA | 60 | | | V |
| $I_{DSS}$ | Drain-to-source leakage current | $V_{GS}$ = 0 V, $V_{DS}$ = 48 V | | | 1 | μA |
| $I_{GSS}$ | Gate-to-source leakage current | $V_{DS}$ = 0 V, $V_{GS}$ = 20 V | | | 10 | μA |
| $V_{GS(th)}$ | Gate-to-source threshold voltage | $V_{DS}$ = $V_{GS}$, $I_{DS}$ = 250 μA | 1.4 | 1.75 | 2.2 | V |
| $R_{DS(on)}$ | Drain-to-source on-resistance | $V_{GS}$ = 4.5 V, $I_{DS}$ = 1 A | | 57 | 75 | mΩ |
| | | $V_{GS}$ = 10 V, $I_{DS}$ = 1 A | | 54 | 65 | |
| $g_{fs}$ | Transconductance | $V_{DS}$ = 6 V, $I_{DS}$ = 1 A | | 7.7 | | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input capacitance | $V_{GS}$ = 0 V, $V_{DS}$ = 30 V, $f$ = 1 MHz | | 598 | 777 | pF |
| $C_{oss}$ | Output capacitance | | | 47 | 61 | pF |
| $C_{rss}$ | Reverse transfer capacitance | | | 8.1 | 10.5 | pF |
| $R_G$ | Series gate resistance | | | 1200 | 1600 | Ω |
| $Q_g$ | Gate charge total (10 V) | $V_{DS}$ = 30 V, $I_{DS}$ = 1 A | | 11 | 14 | nC |
| $Q_{gd}$ | Gate charge gate-to-drain | | | 1.6 | | nC |
| $Q_{gs}$ | Gate charge gate-to-source | | | 1.5 | | nC |
| $Q_{g(th)}$ | Gate charge at $V_{th}$ | | | 0.8 | | nC |
| $Q_{oss}$ | Output charge | $V_{DS}$ = 30 V, $V_{GS}$ = 0 V | | 3.2 | | nC |
| $t_{d(on)}$ | Turnon delay time | $V_{DS}$ = 30 V, $V_{GS}$ = 4.5 V, $I_{DS}$ = 1 A, $R_G$ = 0 Ω | | 572 | | ns |
| $t_r$ | Rise time | | | 540 | | ns |
| $t_{d(off)}$ | Turnoff delay time | | | 1076 | | ns |
| $t_f$ | Fall time | | | 496 | | ns |
| **DIODE CHARACTERISTICS** | | | | | | |
| $V_{SD}$ | Diode forward voltage | $I_{SD}$ = 1 A, $V_{GS}$ = 0 V | | 0.8 | 1 | V |

## 5.2 Thermal Information

$T_A$ = 25°C (unless otherwise stated)

| THERMAL METRIC | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance(1) | | 85 | | °C/W |
| | Junction-to-ambient thermal resistance(2) | | 245 | | |

(1) Device mounted on FR4 material with 1-in$^2$ (6.45-cm$^2$), 2-oz (0.071-mm) thick Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

## 5.3 Typical MOSFET Characteristics

$T_A$ = 25°C (unless otherwise stated)

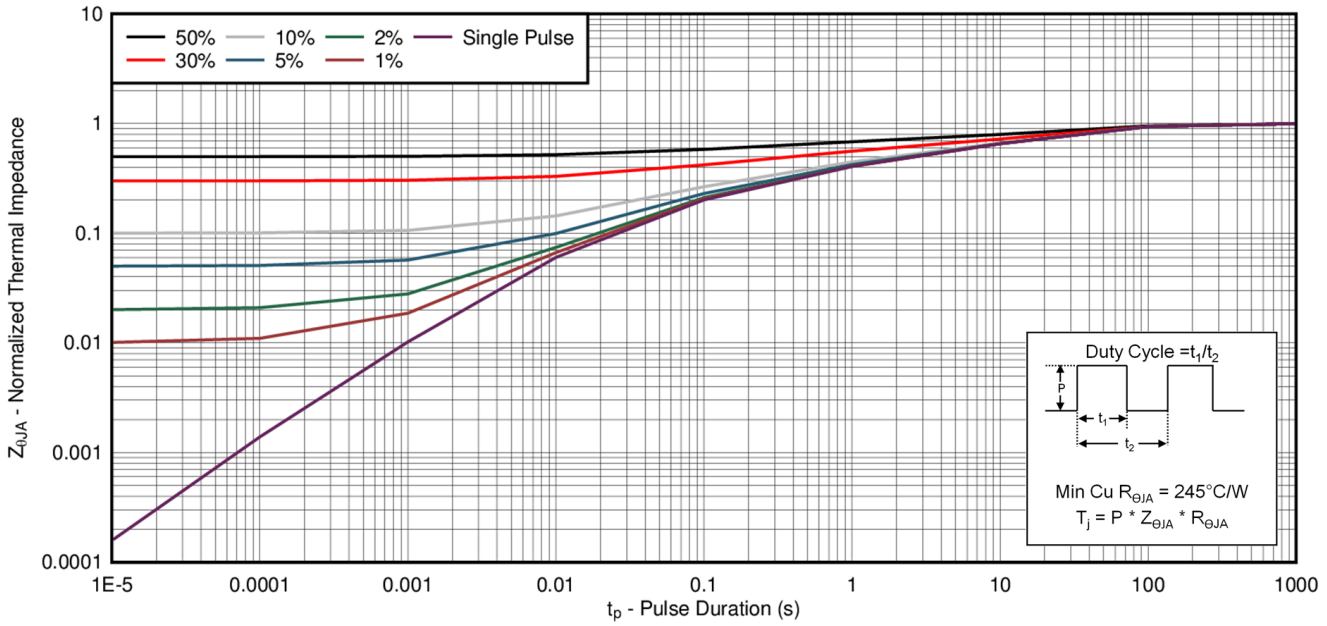



**图 5-1. Transient Thermal Impedance**

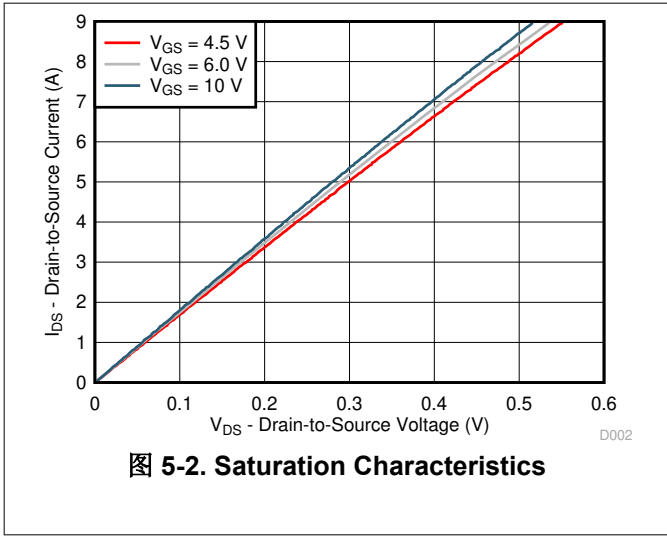
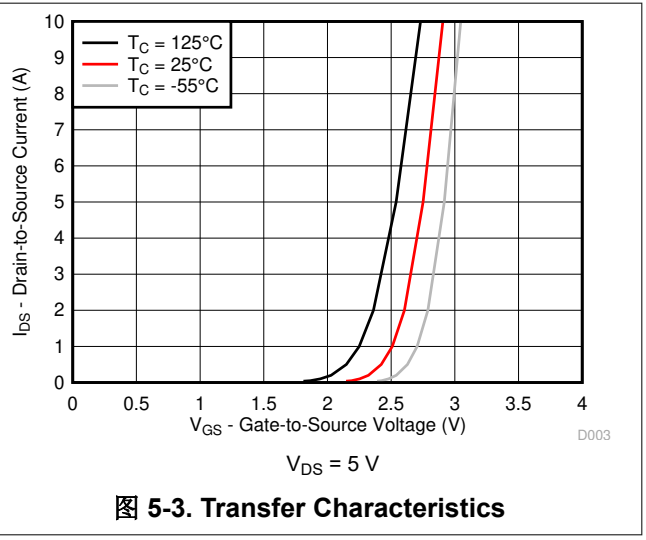
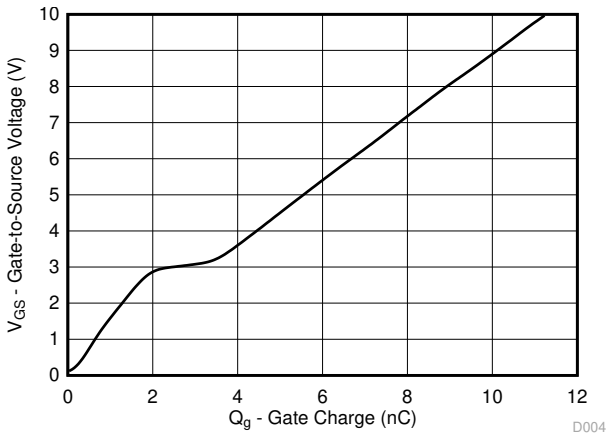



**图 5-2. Saturation Characteristics**




VDS = 5 V

**图 5-3. Transfer Characteristics**




$I_D$ = 1 A $V_{DS}$ = 30 V

**图 5-4. Gate Charge**

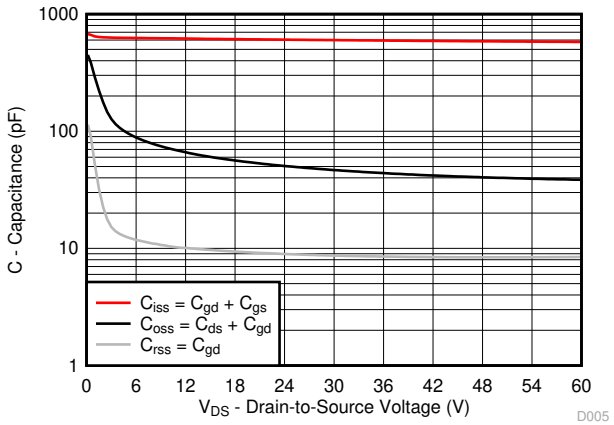
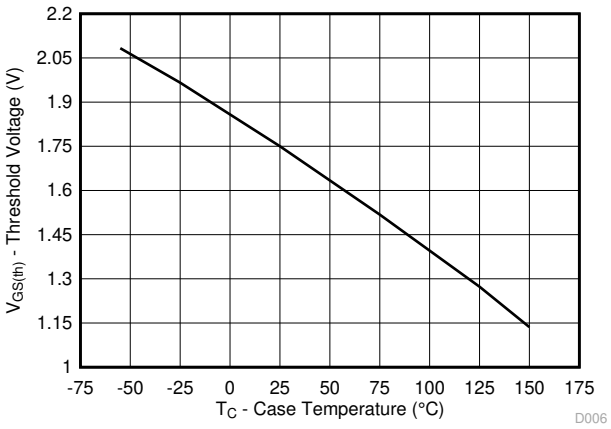



**图 5-5. Capacitance**




$I_D$ = 250 µA

**图 5-6. Threshold Voltage vs Temperature**

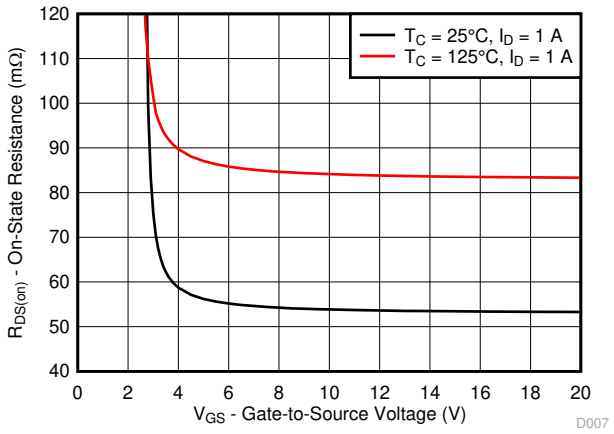
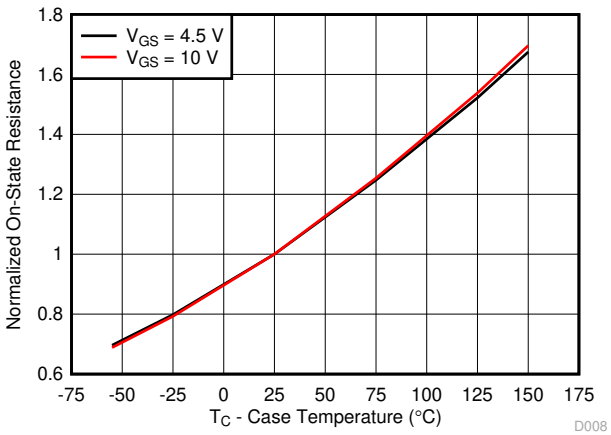



**图 5-7. On-State Resistance vs Gate-to-Source Voltage**




$I_D$ = 1 A

**图 5-8. Normalized On-State Resistance vs Temperature**

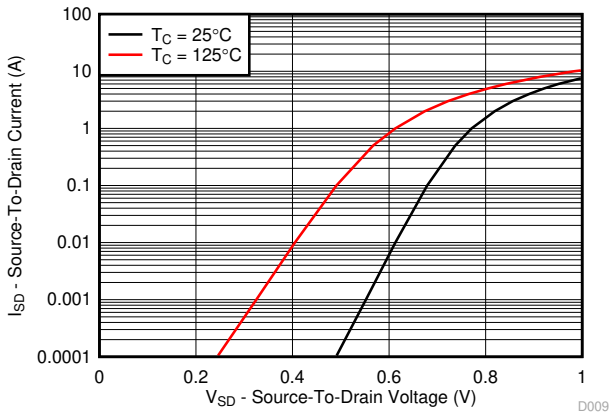
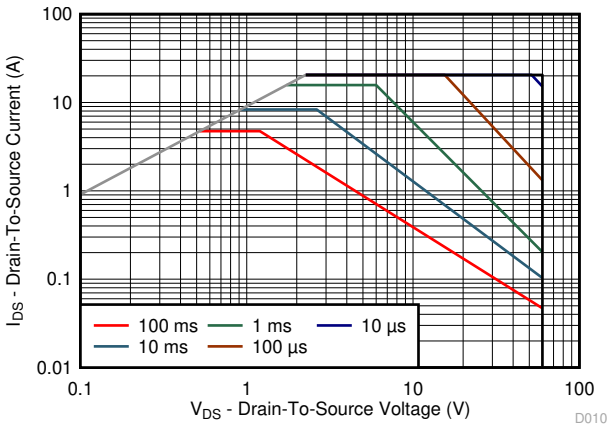



**图 5-9. Typical Diode Forward Voltage**




Single pulse, typ $R_{\theta JA}$ = 245°C/W

**图 5-10. Maximum Safe Operating Area (SOA)**

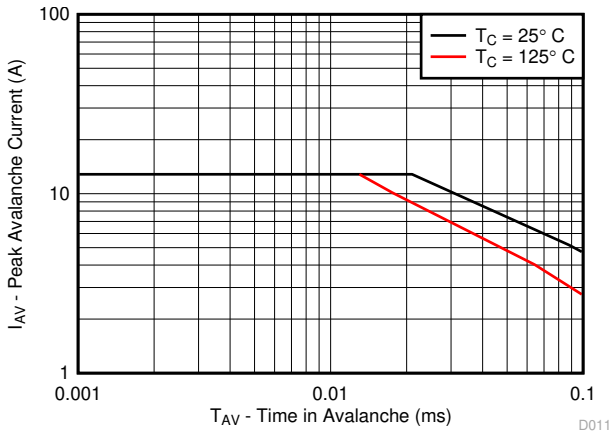



**图 5-11. Single Pulse Unclamped Inductive Switching**

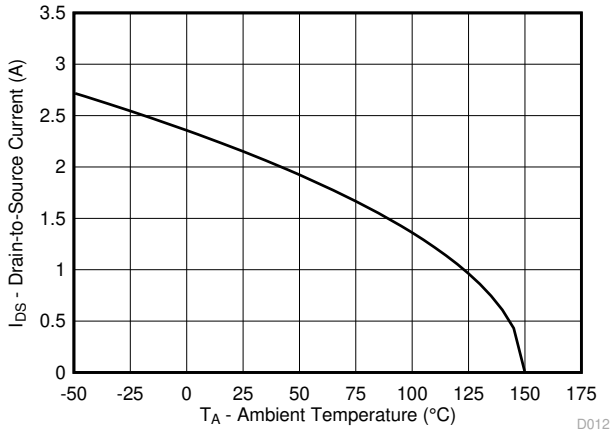



**图 5-12. Maximum Drain Current vs Temperature**

# 6 Device and Documentation Support

## 6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 6.2 Community Resources

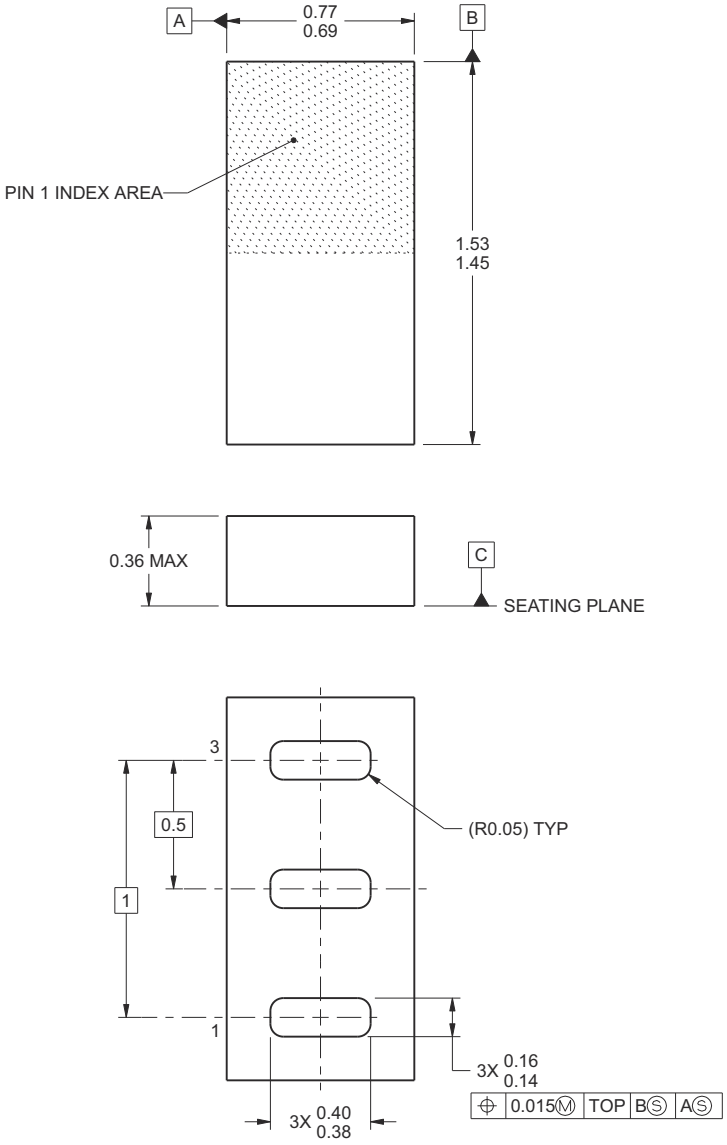
## 6.3 Trademarks

FemtoFET™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

# 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 7.1 Mechanical Dimensions

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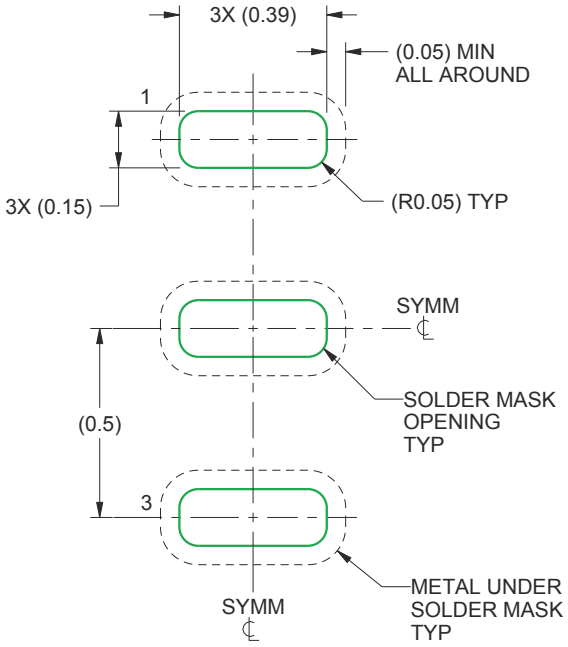
A. All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
B. This drawing is subject to change without notice.
C. This package is a PB-free solder land design.

**表 7-1. Pin Configuration**

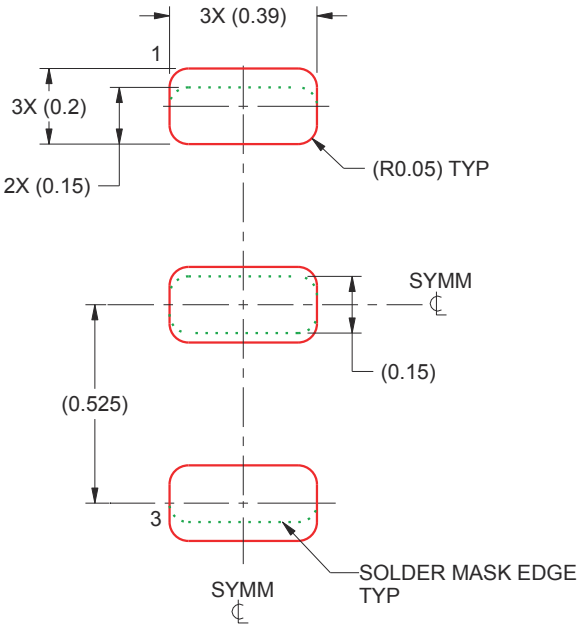
| POSITION | DESIGNATION |
|---|---|
| Pin 1 | Gate |
| Pin 2 | Source |
| Pin 3 | Drain |

## 7.2 Recommended Minimum PCB Layout




A. All dimensions are in millimeters.
B. For more information, see *FemtoFET Surface Mount Guide* (SLRA003D).

## 7.3 Recommended Stencil Pattern




A. All dimensions are in millimeters.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| CSD18541F5 | Active | Production | PICOSTAR (YJK) \| 3 | 3000 \| LARGE T&R | Yes | NIAU | Level-1-260C-UNLIM | -55 to 150 | 1T |
| CSD18541F5.B | Active | Production | PICOSTAR (YJK) \| 3 | 3000 \| LARGE T&R | Yes | NIAU | Level-1-260C-UNLIM | -55 to 150 | 1T |
| CSD18541F5T | Active | Production | PICOSTAR (YJK) \| 3 | 250 \| SMALL T&R | Yes | NIAU | Level-1-260C-UNLIM | -55 to 150 | 1T |
| CSD18541F5T.B | Active | Production | PICOSTAR (YJK) \| 3 | 250 \| SMALL T&R | Yes | NIAU | Level-1-260C-UNLIM | -55 to 150 | 1T |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

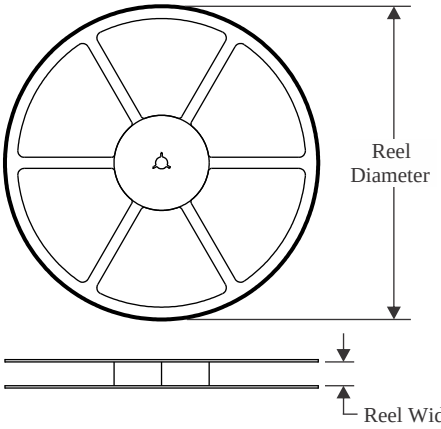
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

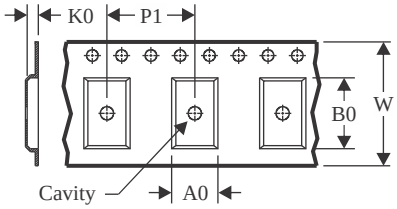
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

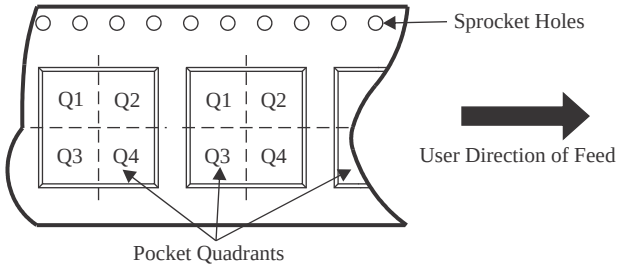



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

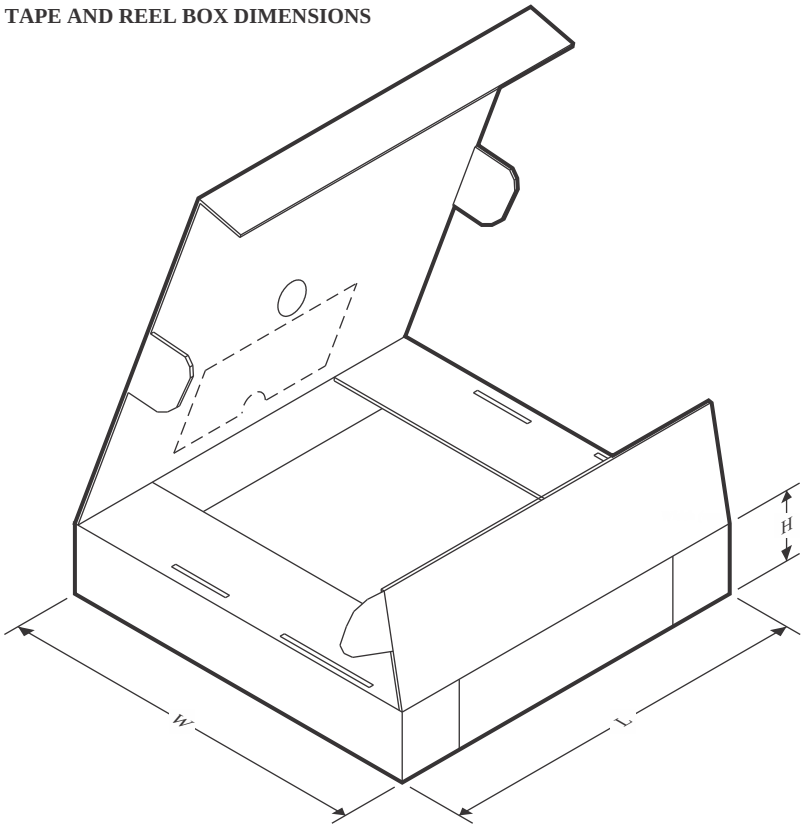
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

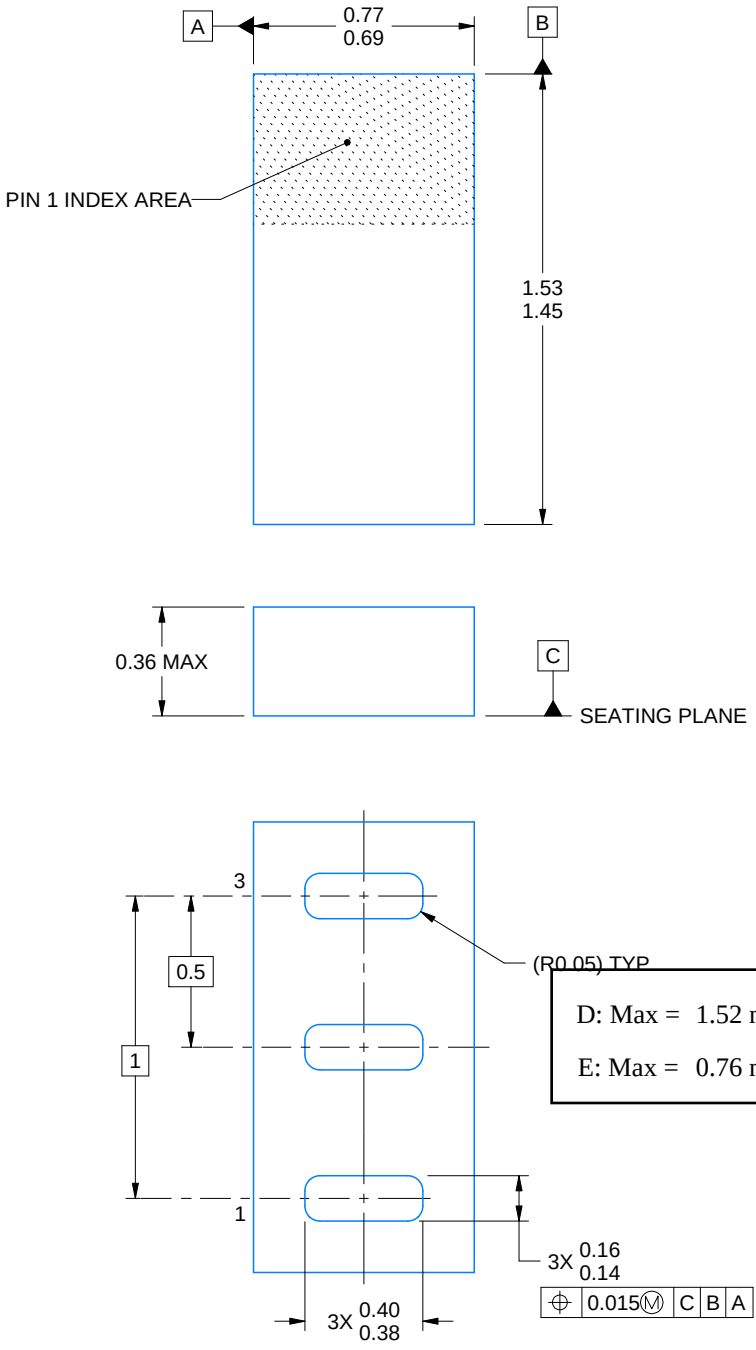
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CSD18541F5 | PICOSTAR | YJK | 3 | 3000 | 180.0 | 8.4 | 0.92 | 1.68 | 0.42 | 4.0 | 8.0 | Q1 |
| CSD18541F5T | PICOSTAR | YJK | 3 | 250 | 180.0 | 8.4 | 0.92 | 1.68 | 0.42 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CSD18541F5 | PICOSTAR | YJK | 3 | 3000 | 182.0 | 182.0 | 20.0 |
| CSD18541F5T | PICOSTAR | YJK | 3 | 250 | 182.0 | 182.0 | 20.0 |

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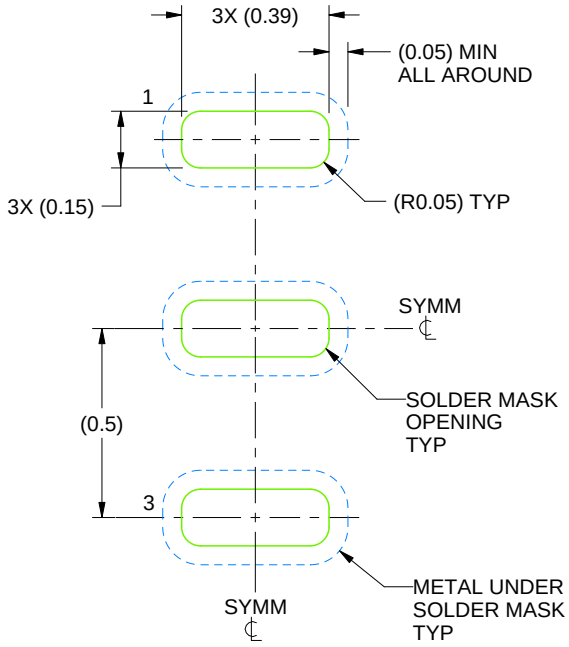
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.
3. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device datasheet or contact a local TI representative.




LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:50X

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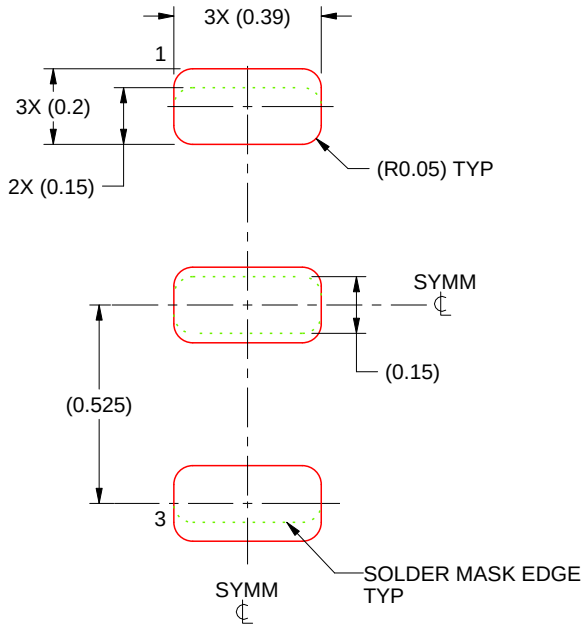
NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).




SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:50X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# 重要通知和免责声明

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