CSD18536KTT 60V N 沟道 NexFET™ 功率 MOSFET

1 特性

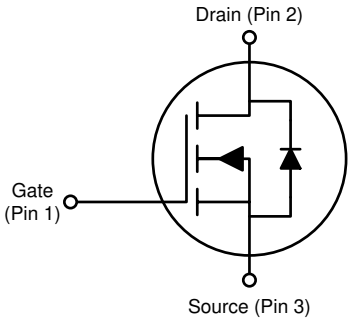
- 超低 Q_g 和 Q_{gd}
- 低热阻
- 具有雪崩能力
- 无铅端子镀层
- 符合 RoHS
- 无卤素
- D^2PAK 塑料封装

2 应用

- 次级侧同步整流器
- 电机控制

3 说明

这款 60V、1.3mΩ、D^2PAK (TO-263) NexFET™ 功率 MOSFET 旨在用于更大限度地降低功率转换应用中的损耗。



产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	60		V
Q_g	栅极电荷总量 (10V)	108		nC
Q_{gd}	栅极电荷（栅极到漏极）	14		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 4.5V	1.7	mΩ
		V_{GS} = 10V	1.3	mΩ
$V_{GS(th)}$	阈值电压	1.8		V

订购信息 (1)

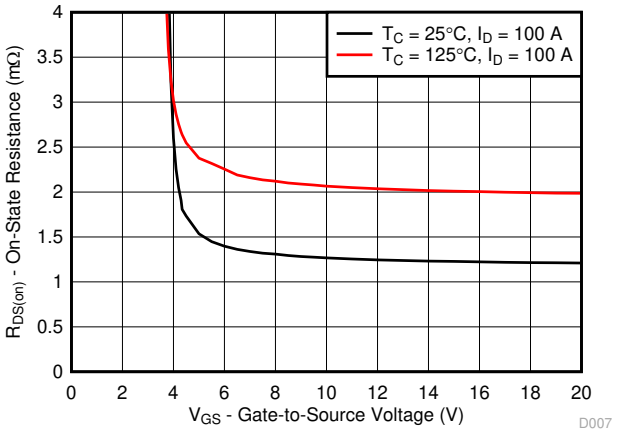
器件	数量	介质	封装	运输
CSD18536KTT	500	13 英寸卷带	D^2PAK 塑料封装	卷带包装
CSD18536KTTT	50			

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

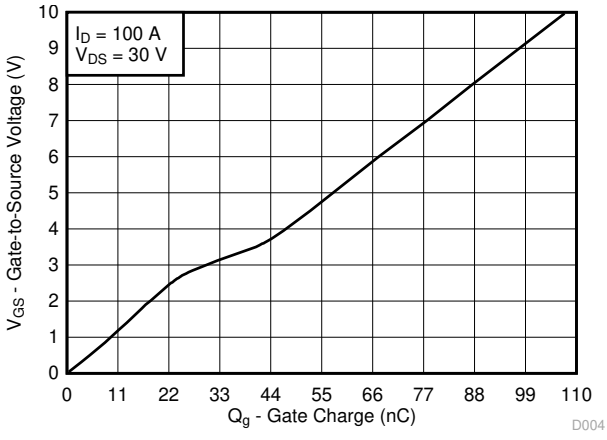
绝对最大额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	60	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流（受封装限制）	200	A
	持续漏极电流（受器件限制），T_C = 25°C 时测得	349	A
	持续漏极电流（受器件限制），T_C = 100°C 时测得	247	A
I_{DM}	脉冲漏极电流(1)	400	A
P_D	功率耗散	375	W
T_J、T_{stg}	工作结温和贮存温度	-55 至 175	°C
E_{AS}	雪崩能量，单脉冲 I_D = 128A，L = 0.1mH，R_G = 25Ω	819	mJ

(1) 最大 $R_{\theta JC}$ = 0.4°C/W，脉冲持续时间 ≤ 100μs，占空比 ≤ 1%



$R_{DS(on)}$ 与 V_{GS} 之间的关系



栅极电荷

内容

4 规格

4.1 电气特性

（T_A = 25°C 时测得，除非另有说明）

参数		测试条件	最小值	典型值	最大值	单位
静态特性						
BV_{DSS}	漏源电压	V_{GS} = 0V，I_D = 250 μA	60			V
I_{DSS}	漏源漏电流	V_{GS} = 0V，V_{DS} = 48V			1	μA
I_{GSS}	栅源漏电流	V_{DS} = 0V，V_{GS} = 20V			100	nA
$V_{GS(th)}$	栅源阈值电压	V_{DS} = V_{GS}，I_D = 250 μA	1.4	1.8	2.2	V
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 4.5V，I_D = 100A		1.7	2.2	mΩ
		V_{GS} = 10V，I_D = 100A		1.3	1.6	mΩ
g_{fs}	跨导	V_{DS} = 6V，I_D = 100A		312		S
动态特性						
C_{iss}	输入电容	V_{GS} = 0V，V_{DS} = 30V，f = 1MHz		8790	11430	pF
C_{oss}	输出电容			1410	1840	pF
C_{rss}	反向传输电容			39	51	pF
R_G	串联栅极电阻			0.7	1.4	Ω
Q_g	栅极电荷总量 (10V)	V_{DS} = 30V，I_D = 100A		108	140	nC
Q_{gd}	栅极电荷（栅极到漏极）			14		nC
Q_{gs}	栅极电荷（栅漏极）			18		nC
$Q_{g(th)}$	V_{th} 下的栅极电荷			17		nC
Q_{oss}	输出电荷	V_{DS} = 30V，V_{GS} = 0V		230		nC
$t_{d(on)}$	导通延时时间	V_{DS} = 30V，V_{GS} = 10V，I_{DS} = 100A，R_G = 0Ω		11		ns
t_r	上升时间			5		ns
$t_{d(off)}$	关闭延时时间			24		ns
t_f	下降时间			4		ns
二极管特性						
V_{SD}	二极管正向电压	I_{SD} = 100A，V_{GS} = 0V		0.9	1.0	V
Q_{rr}	反向恢复电荷	V_{DS}= 30V，I_F = 100A，di/dt = 300A/μs		323		nC
t_{rr}	反向恢复时间			86		ns

4.2 热性能信息

（T_A = 25°C 时测得，除非另有说明）

热指标		最小值	典型值	最大值	单位
$R_{\theta JC}$	结至外壳热阻			0.4	°C/W
$R_{\theta JA}$	结至环境热阻			62	°C/W

4.3 典型 MOSFET 特性

（T_A = 25°C 时测得，除非另有说明）

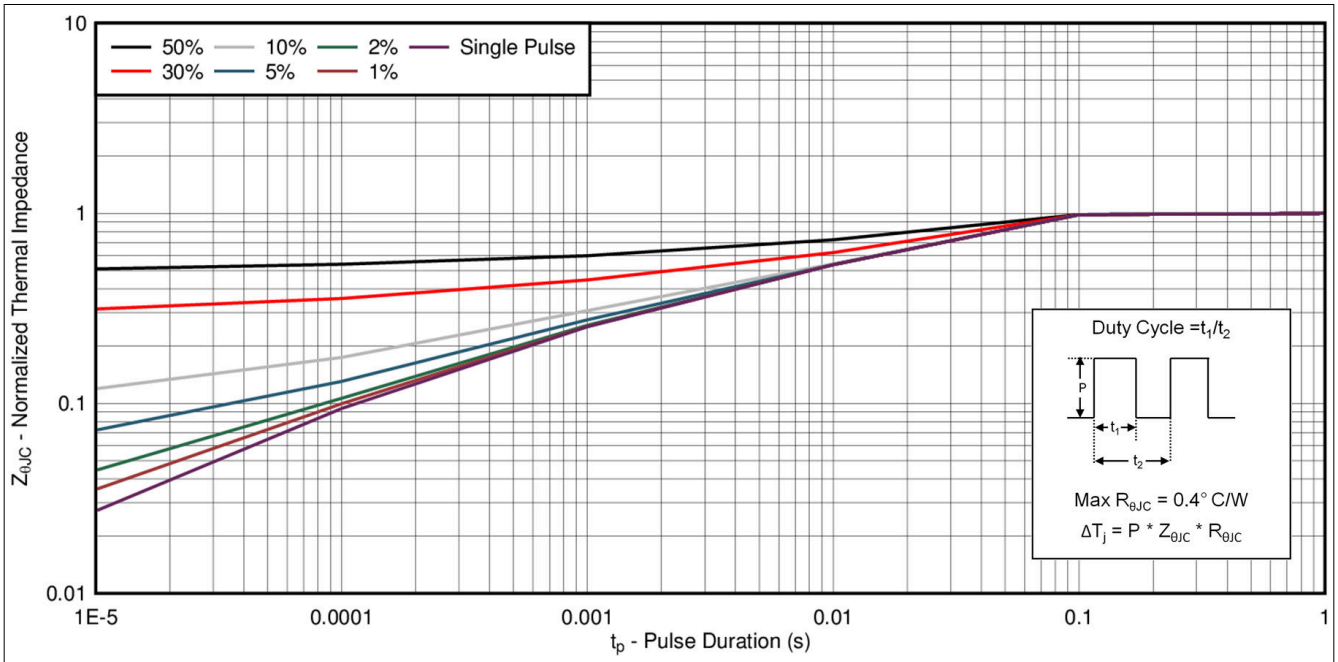


图 4-1. 瞬态热阻抗

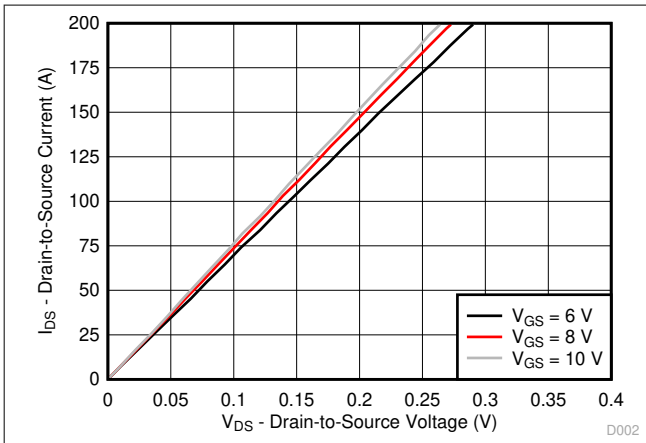
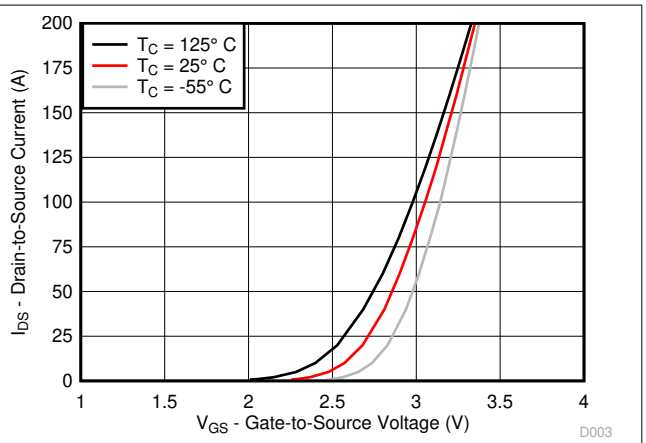


图 4-2. 饱和特性



VDS = 5V

图 4-3. 传输特性

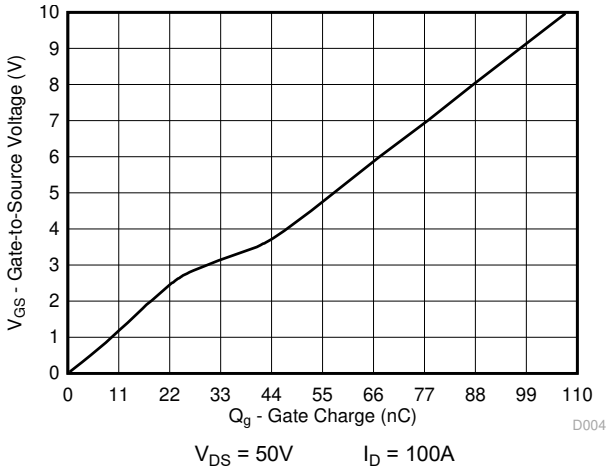


图 4-4. 栅极电荷

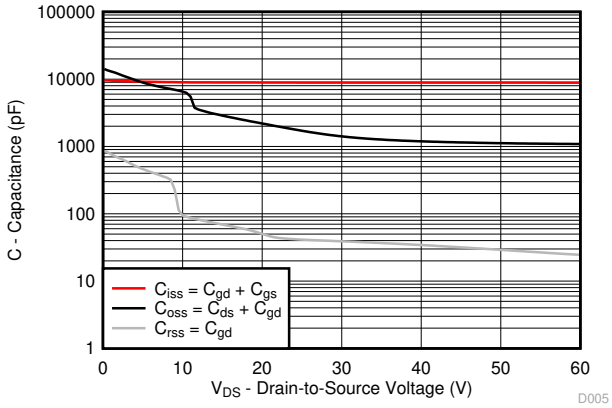


图 4-5. 电容

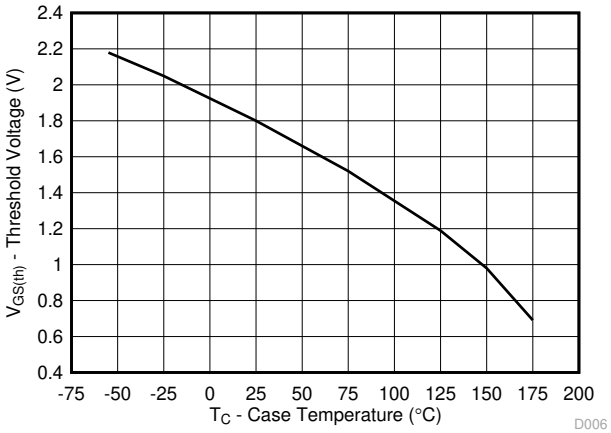


图 4-6. 阈值电压与温度间的关系

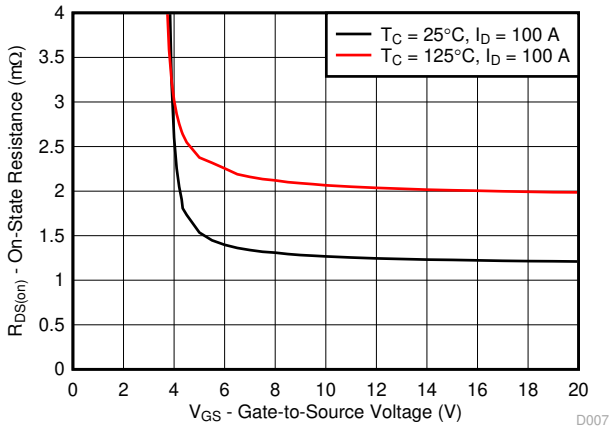


图 4-7. 导通电阻与栅源电压

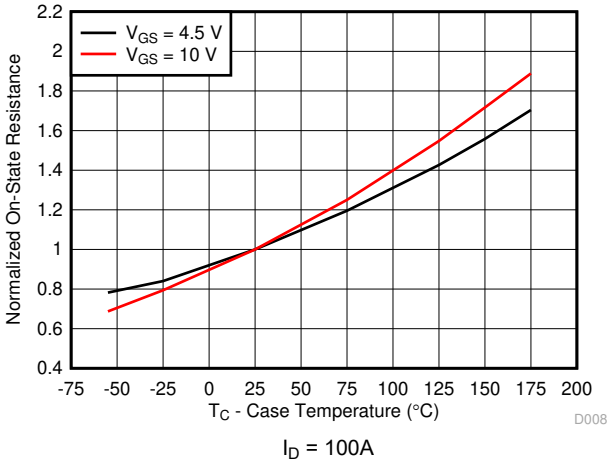


图 4-8. 标准化通态电阻与温度的关系

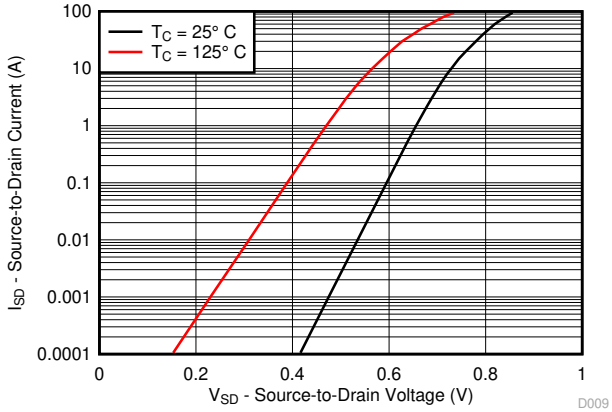
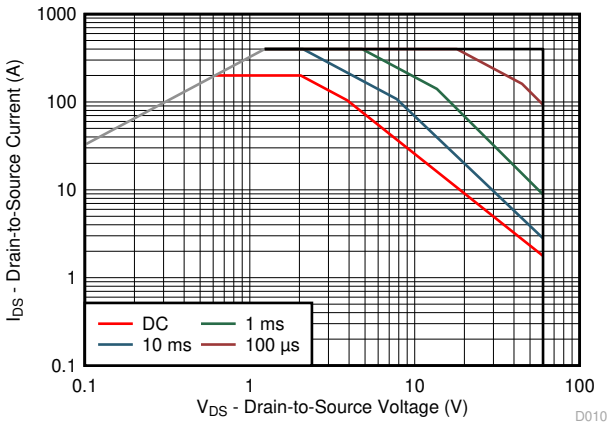


图 4-9. 典型二极管正向电压



单脉冲最大 $R_{\theta JC}$ = 0.4°C/W

图 4-10. 最大安全工作区

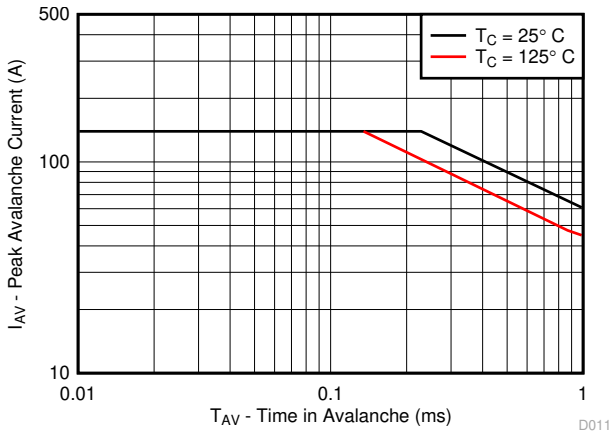


图 4-11. 单脉冲非钳位电感式开关

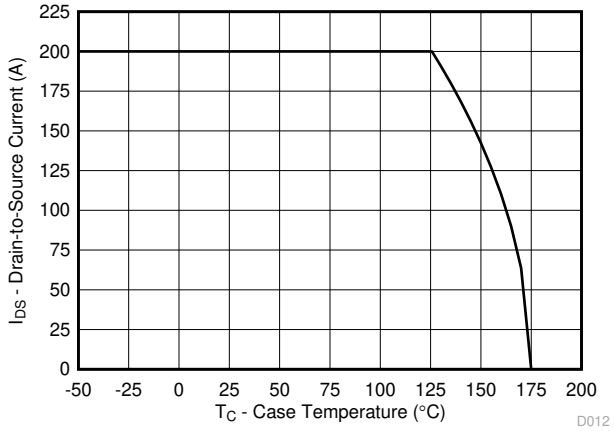


图 4-12. 最大漏极电流与温度间的关系

5 器件和文档支持

5.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

5.2 文档支持

5.2.1 相关文档

5.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

5.4 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

5.5 商标

NexFET™ is a trademark of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

5.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

5.7 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

6 修订历史记录

Changes from Revision * (March 2016) to Revision A (June 2025)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1

7 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD18536KTT	Active	Production	DDPAK/ TO-263 (KTT) | 2	500 | LARGE T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 175	CSD18536KTT
CSD18536KTT.B	Active	Production	DDPAK/ TO-263 (KTT) | 2	500 | LARGE T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 175	CSD18536KTT
CSD18536KTTT	Active	Production	DDPAK/ TO-263 (KTT) | 2	50 | SMALL T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 175	CSD18536KTT
CSD18536KTTT.B	Active	Production	DDPAK/ TO-263 (KTT) | 2	50 | SMALL T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 175	CSD18536KTT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

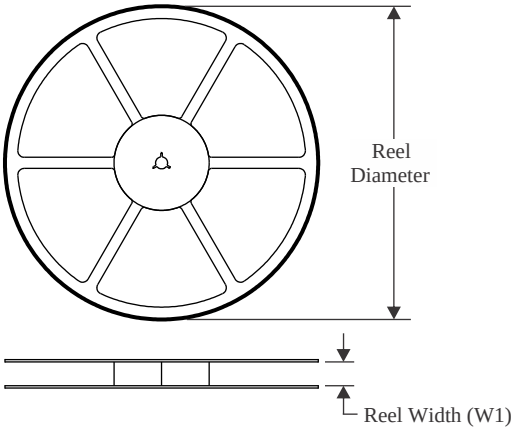
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

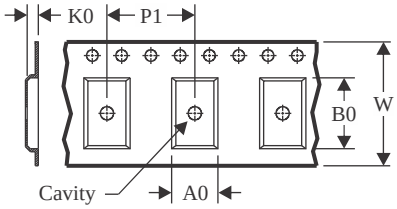
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

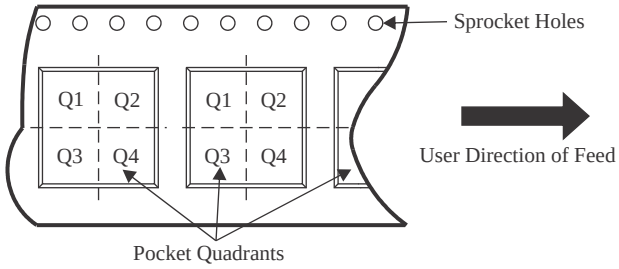


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

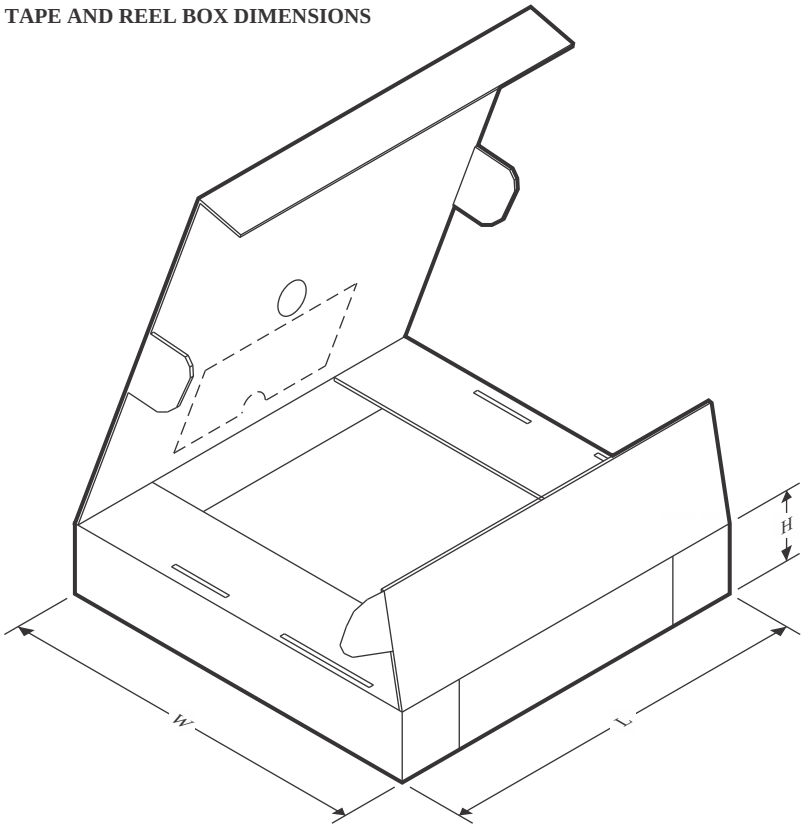
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD18536KTT	DDPAK/ TO-263	KTT	2	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
CSD18536KTTT	DDPAK/ TO-263	KTT	2	50	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2

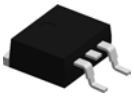
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD18536KTT	DDPAK/TO-263	KTT	2	500	340.0	340.0	38.0
CSD18536KTTT	DDPAK/TO-263	KTT	2	50	340.0	340.0	38.0

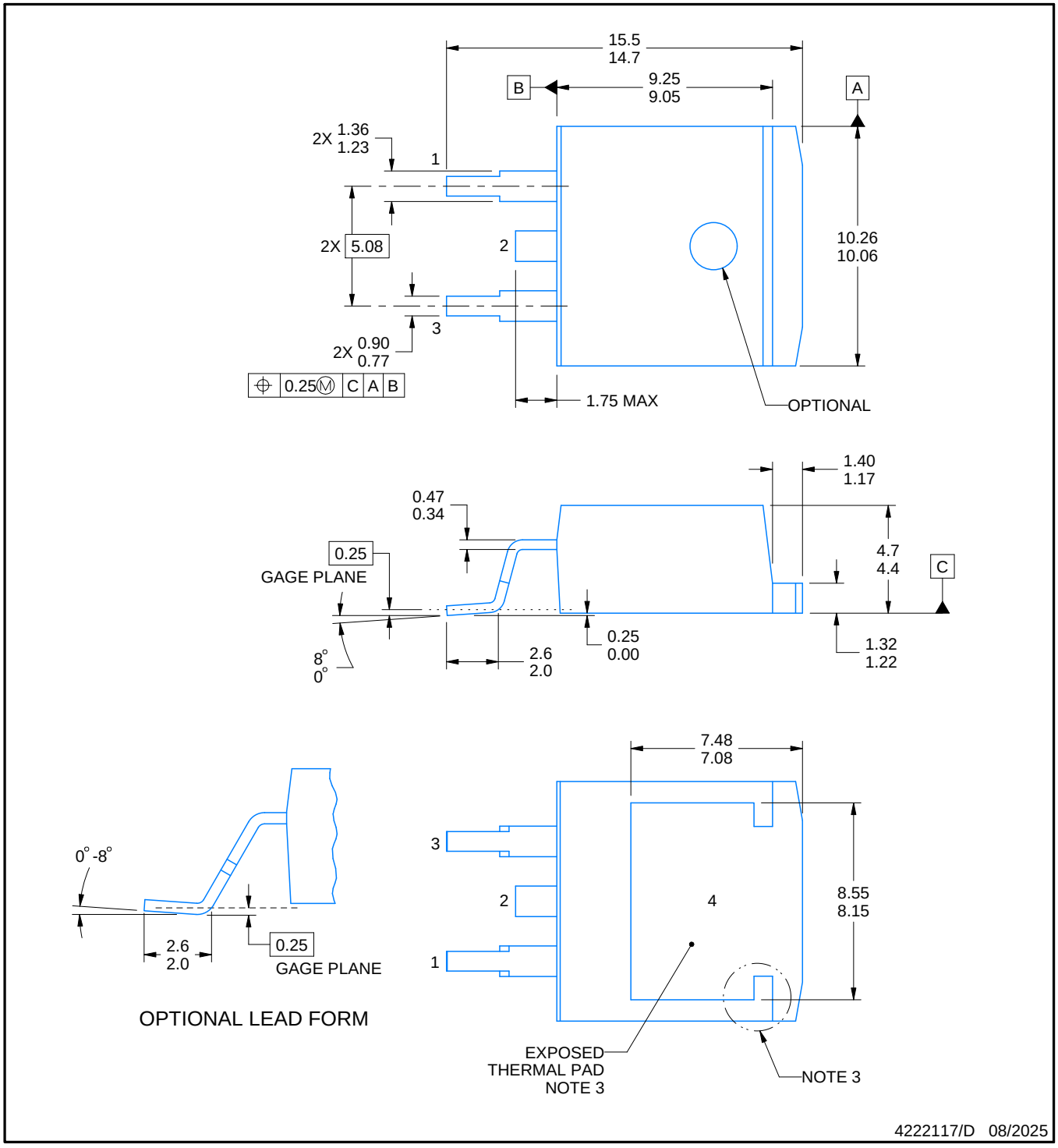
KTT0002A



PACKAGE OUTLINE

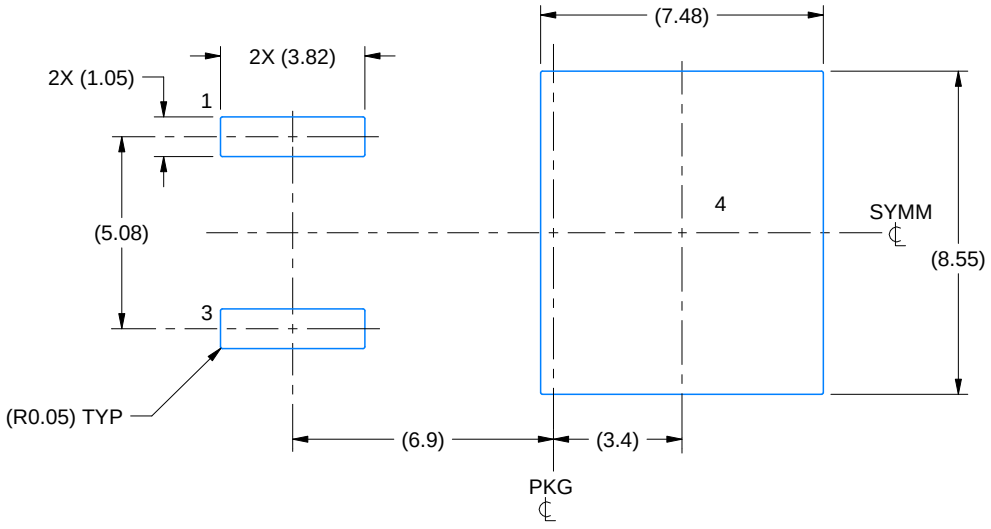
TO-263 - 4.7 mm max height

TRANSISTOR OUTLINE

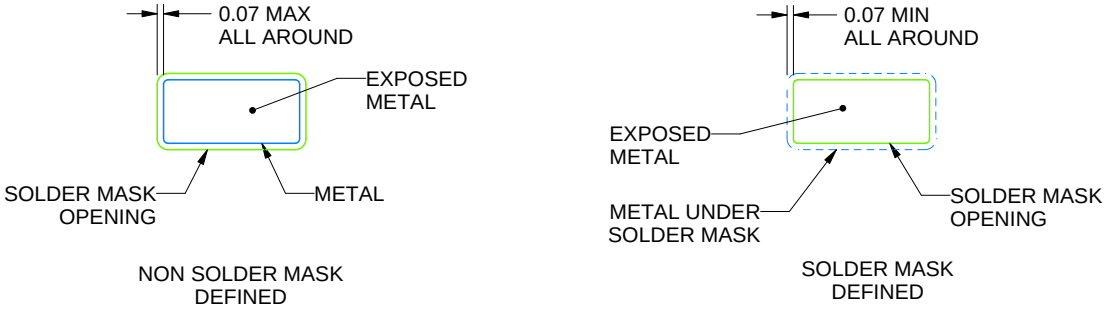


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Features may not exist and shape may vary per different assembly sites. Pin 2 and Pin 4 connected.
4. Reference JEDEC registration TO-263.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:5X

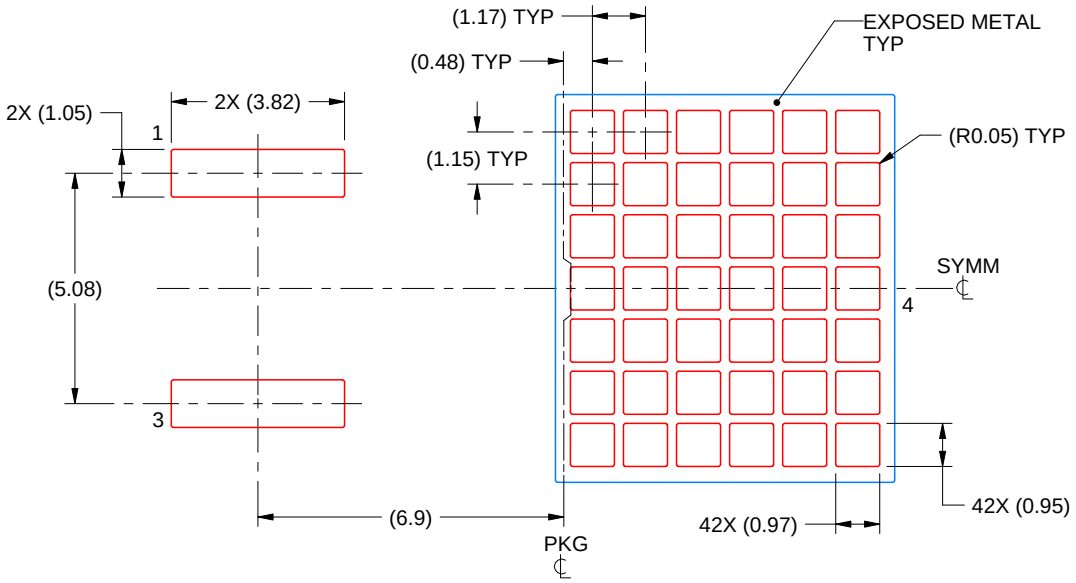


SOLDER MASK DETAILS

4222117/D 08/2025

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
60.5% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

4222117/D 08/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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