

CSD18509Q5B N 通道 NexFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET)

1 特性

- 超低导通电阻
- 低热阻
- 雪崩额定值
- 逻辑电平
- 无铅引脚镀层
- 符合 RoHS 标准
- 无卤素
- SON 5mm × 6mm 塑料封装

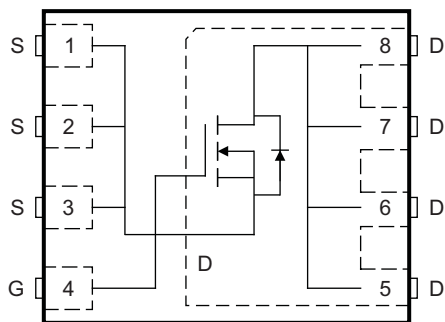
2 应用

- 直流 - 直流转换
- 次级侧同步整流器
- 电机控制

3 说明

这个 40V, 1mΩ, SON5x6 NexFET™ 功率 MOSFET 的设计旨在追求以最大限度降低功率转换应用中的功率损耗。

顶视图



P0093-01

产品概要

T _A = 25°C		典型值		单位
V _{DS}	漏源电压	40		V
Q _g	栅极电荷总量 (10V)	150		nC
Q _{gd}	栅极电荷 栅极到漏极	17		nC
R _{DS(on)}	漏源导通电阻	V _{GS} = 4.5V	1.3	mΩ
		V _{GS} = 10V	1.0	mΩ
V _{GS(th)}	阈值电压	1.8		V

订购信息⁽¹⁾

器件	数量	介质	封装	出货
CSD18509Q5B	2500	13 英寸卷带	SON 5mm x 6mm 塑料封装	卷带封装
CSD18509Q5BT	250	7 英寸卷带		

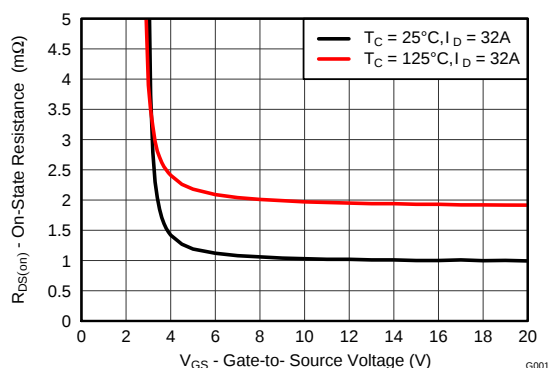
(1) 要了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

绝对最大额定值

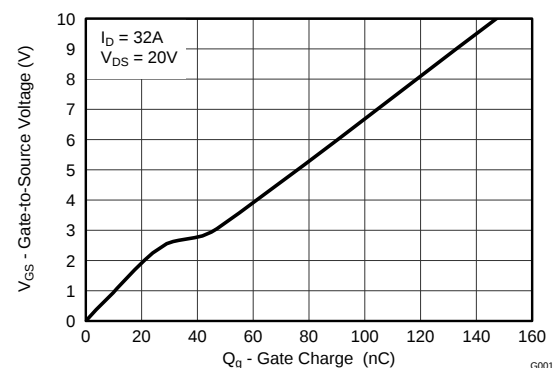
T _A = 25°C		值	单位
V _{DS}	漏源电压	40	V
V _{GS}	栅源电压	±20	V
I _D	持续漏极电流 (受封装限制)	100	A
	持续漏极电流 (受芯片限制), T _C = 25°C 时测得	299	
	持续漏极电流 ⁽¹⁾	38	
I _{DM}	脉冲漏极电流, T _A = 25°C 时测得 ⁽²⁾	400	A
P _D	功率耗散 ⁽¹⁾	3.1	W
	功率耗散, T _C = 25°C	195	
T _J , T _{stg}	运行结温和储存温度范围	-55 至 150	°C
E _{AS}	雪崩能量, 单脉冲 I _D = 83, L = 0.1mH, R _G = 25Ω	345	mJ

(1) R_{θJA} = 40°C/W, 这是在一个厚度 0.06 英寸环氧树脂 (FR4) 印刷电路板 (PCB) 上的 1 英寸², 2 盎司的铜过渡垫片上测得的典型值。

(2) 最大 R_{θJC} = 0.8°C/W, 脉冲持续时间 ≤ 100μs, 占空比 ≤ 1%

R_{DS(on)} 与 V_{GS} 对比

栅极电荷



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4 修订历史记录

Changes from Original (June 2014) to Revision A	Page
• 已添加 “接收文档更新通知”和“社区资源”部分添加到了“器件和文档支持”。	7
• 已更改 将“建议 PCB 布局”部分方框图中	9

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-Source Voltage	V _{GS} = 0 V, I _D = 250 μA	40			V
I _{DSS}	Drain-to-Source Leakage Current	V _{GS} = 0 V, V _{DS} = 32 V			1	μA
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = 20 V			100	nA
V _{GS(th)}	Gate-to-Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	1.4	1.8	2.2	V
R _{DS(on)}	Drain-to-Source On Resistance	V _{GS} = 4.5 V, I _D = 32 A	1.3		1.7	mΩ
		V _{GS} = 10 V, I _D = 32 A	1		1.2	mΩ
g _{fs}	Transconductance	V _{DS} = 4 V, I _D = 32 A	180			S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input Capacitance	V _{GS} = 0 V, V _{DS} = 20 V, f = 1 MHz	10700	13900		pF
C _{oss}	Output Capacitance		821	1070		pF
C _{rss}	Reverse Transfer Capacitance		272	354		pF
R _G	Series Gate Resistance		0.8	1.6		Ω
Q _g	Gate Charge Total (4.5 V)	V _{DS} = 20 V, I _D = 32 A	70	91		nC
Q _g	Gate Charge Total (10 V)		150	195		nC
Q _{gd}	Gate Charge Gate-to-Drain		17			nC
Q _{gs}	Gate Charge Gate-to-Source		29			nC
Q _{g(th)}	Gate Charge at V _{th}		18			nC
Q _{oss}	Output Charge	V _{DS} = 20 V, V _{GS} = 0 V	39			nC
t _{d(on)}	Turn On Delay Time	V _{DS} = 20 V, V _{GS} = 10 V, I _{DS} = 32 A, R _G = 0 Ω	9			ns
t _r	Rise Time		19			ns
t _{d(off)}	Turn Off Delay Time		57			ns
t _f	Fall Time		11			ns
DIODE CHARACTERISTICS						
V _{SD}	Diode Forward Voltage	I _{SD} = 32 A, V _{GS} = 0 V	0.8	1		V
Q _{rr}	Reverse Recovery Charge	V _{DS} = 20 V, I _F = 32 A, di/dt = 300 A/μs	40			nC
t _{rr}	Reverse Recovery Time		23			ns

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

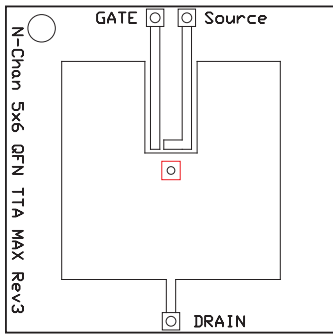
THERMAL METRIC		MIN	TYP	MAX	UNIT
R _{θJC}	Junction-to-Case Thermal Resistance ⁽¹⁾			0.8	°C/W
R _{θJA}	Junction-to-Ambient Thermal Resistance ⁽¹⁾⁽²⁾			50	

- (1) R_{θJC} is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inches × 1.5-inches (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. R_{θJC} is specified by design, whereas R_{θJA} is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.

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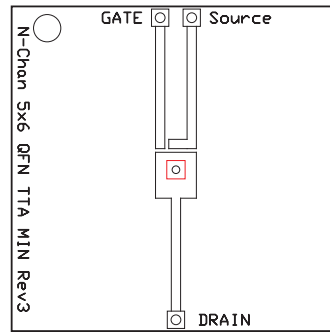
ZHCSC1A – JUNE 2014 – REVISED MAY 2017

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Max $R_{\theta JA} = 50^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of
2-oz. (0.071-mm thick)
Cu.

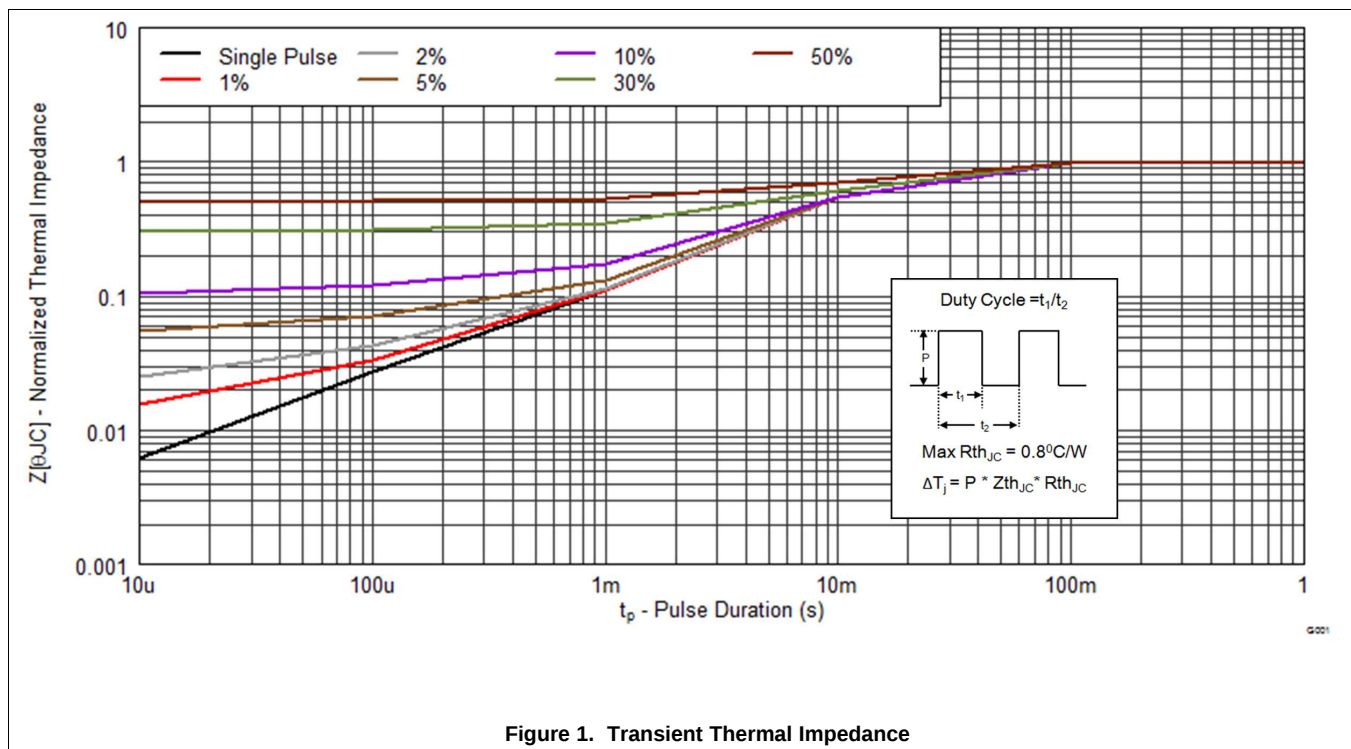


M0137-02

Max $R_{\theta JA} = 125^{\circ}\text{C/W}$
when mounted on a
minimum pad area of
2-oz. (0.071-mm thick)
Cu.

5.3 Typical MOSFET Characteristics

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)



Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

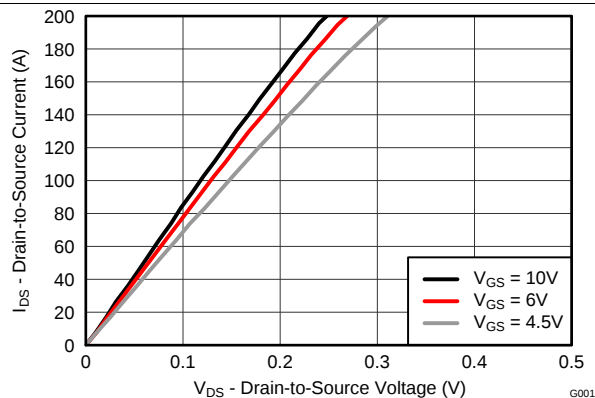


Figure 2. Saturation Characteristics

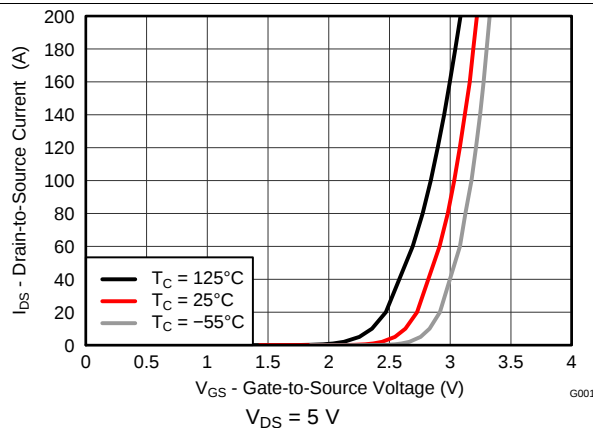


Figure 3. Transfer Characteristics

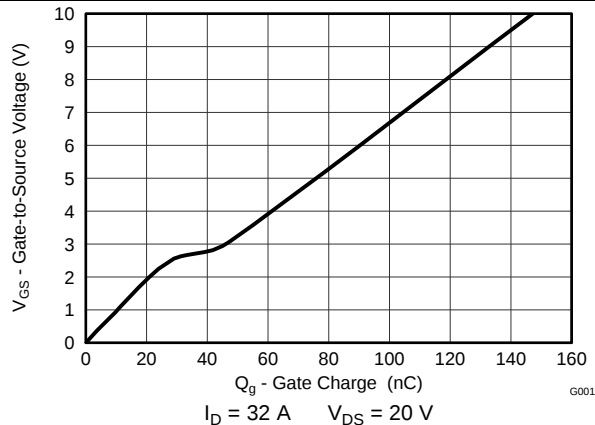


Figure 4. Gate Charge

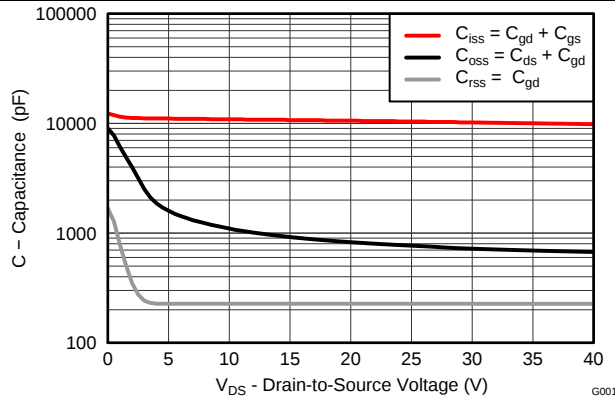


Figure 5. Capacitance

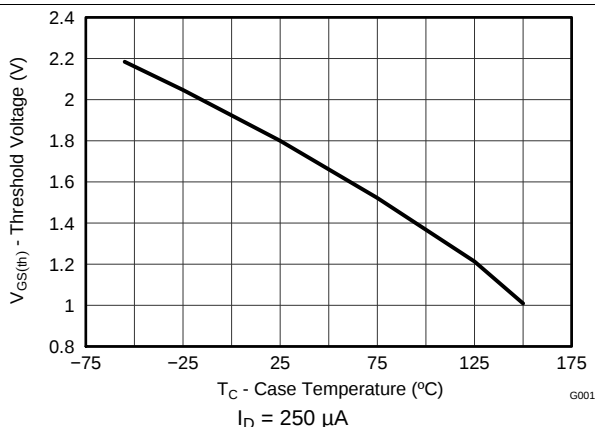


Figure 6. Threshold Voltage vs Temperature

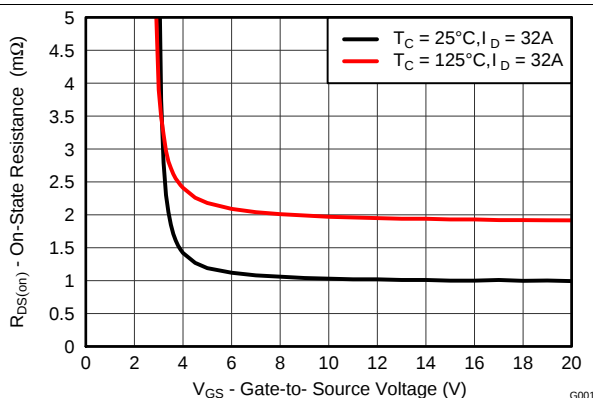


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

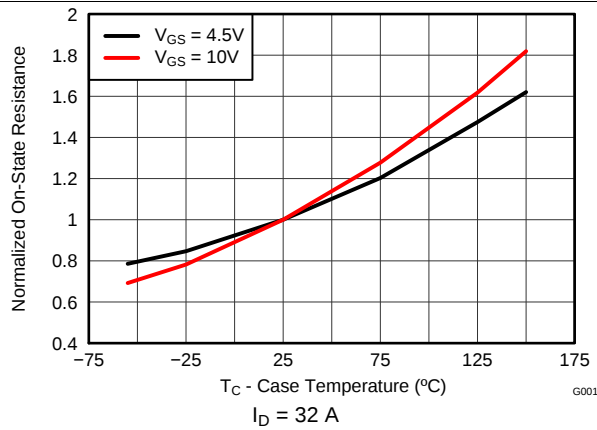


Figure 8. Normalized On-State Resistance vs Temperature

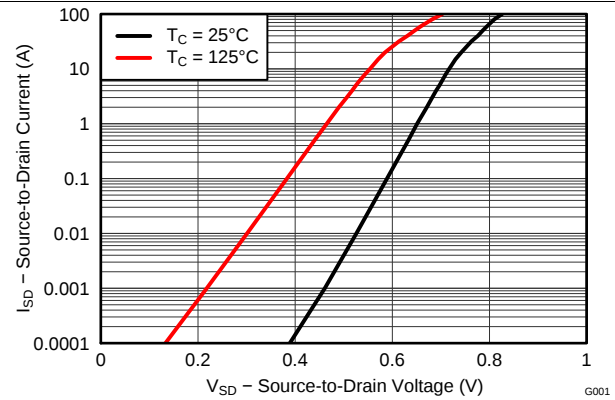


Figure 9. Typical Diode Forward Voltage

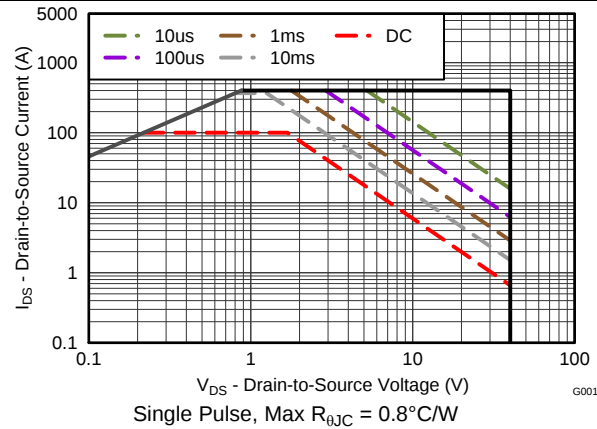


Figure 10. Maximum Safe Operating Area

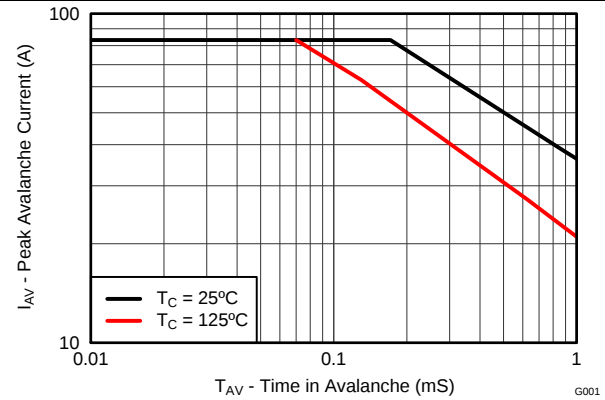


Figure 11. Single Pulse Unclamped Inductive Switching

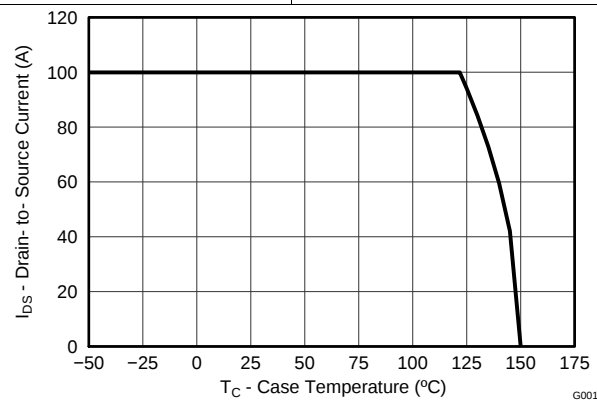


Figure 12. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。请单击右上角的通知我进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

6.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 商标

NexFET, E2E are trademarks of Texas Instruments.

6.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.5 Glossary

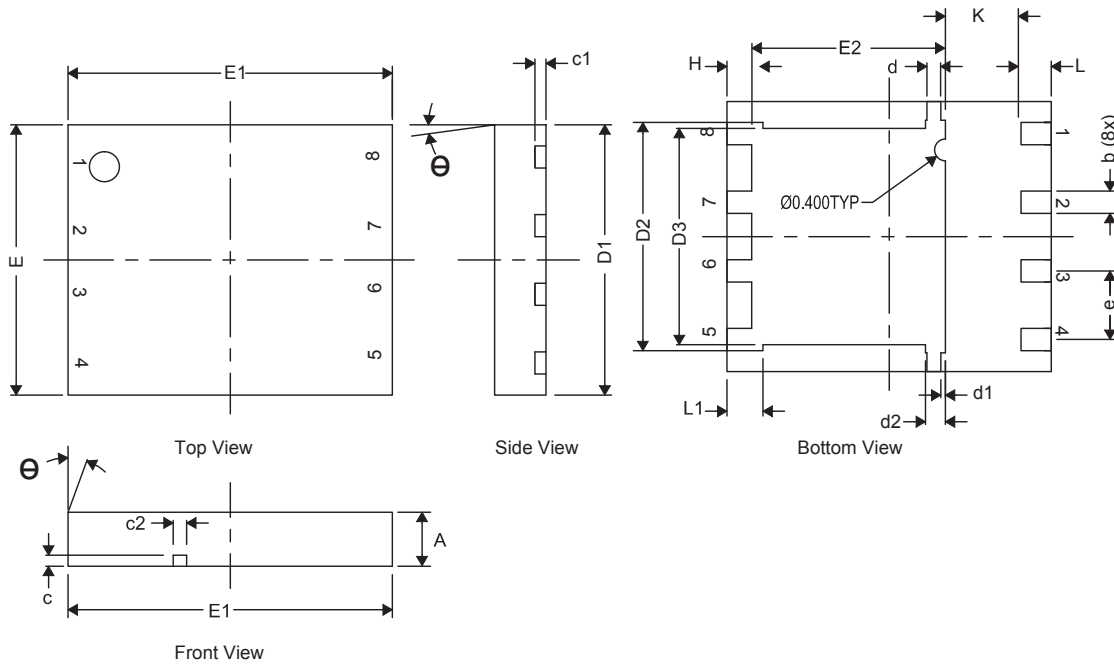
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 机械、封装和可订购信息

以下页中包括机械封装、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

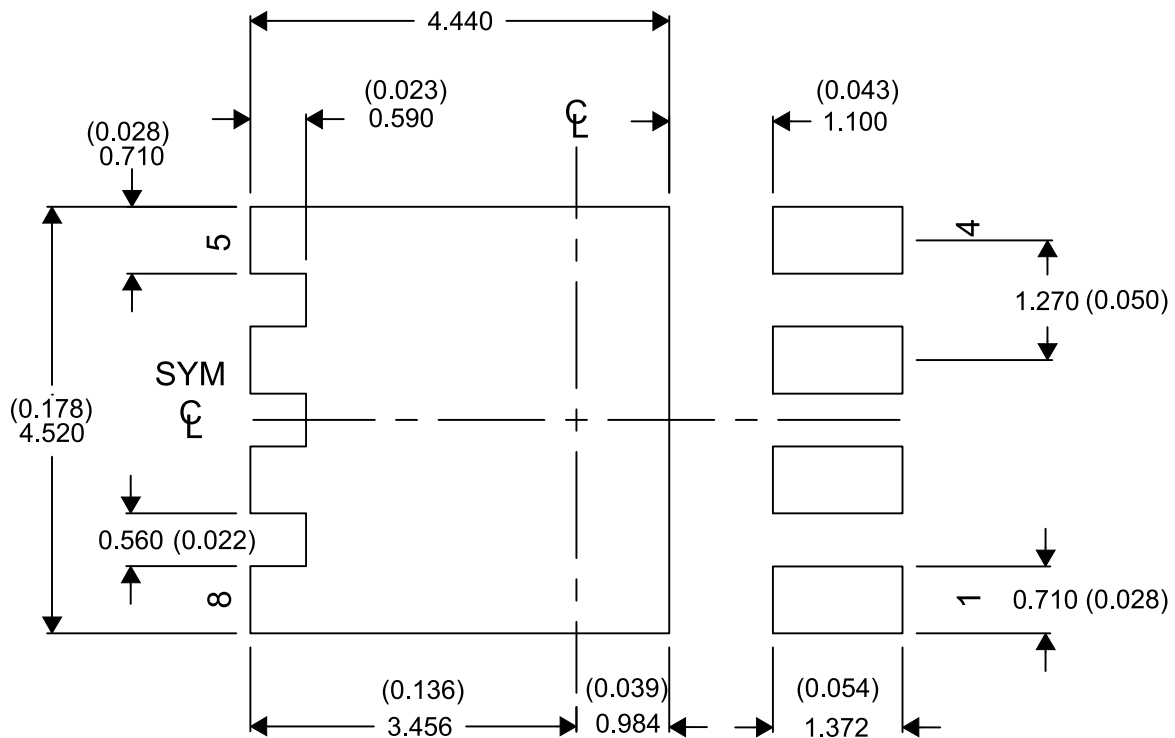
7.1 Q5B 封装尺寸



DIM	毫米		
	最小值	标称值	最大值
A	0.80	1.00	1.05
b	0.36	0.41	0.46
c	0.15	0.20	0.25
c1	0.15	0.20	0.25
c2	0.20	0.25	0.30
D1	4.90	5.00	5.10
D2	4.12	4.22	4.32
D3	3.90	4.00	4.10
d	0.20	0.25	0.30
d1	0.085 典型值		
d2	0.319	0.369	0.419
E	4.90	5.00	5.10
E1	5.90	6.00	6.10
E2	3.48	3.58	3.68
e	1.27 典型值		
H	0.36	0.46	0.56
L	0.46	0.56	0.66
L1	0.57	0.67	0.77
θ	0°	—	—
K	1.40 典型值		

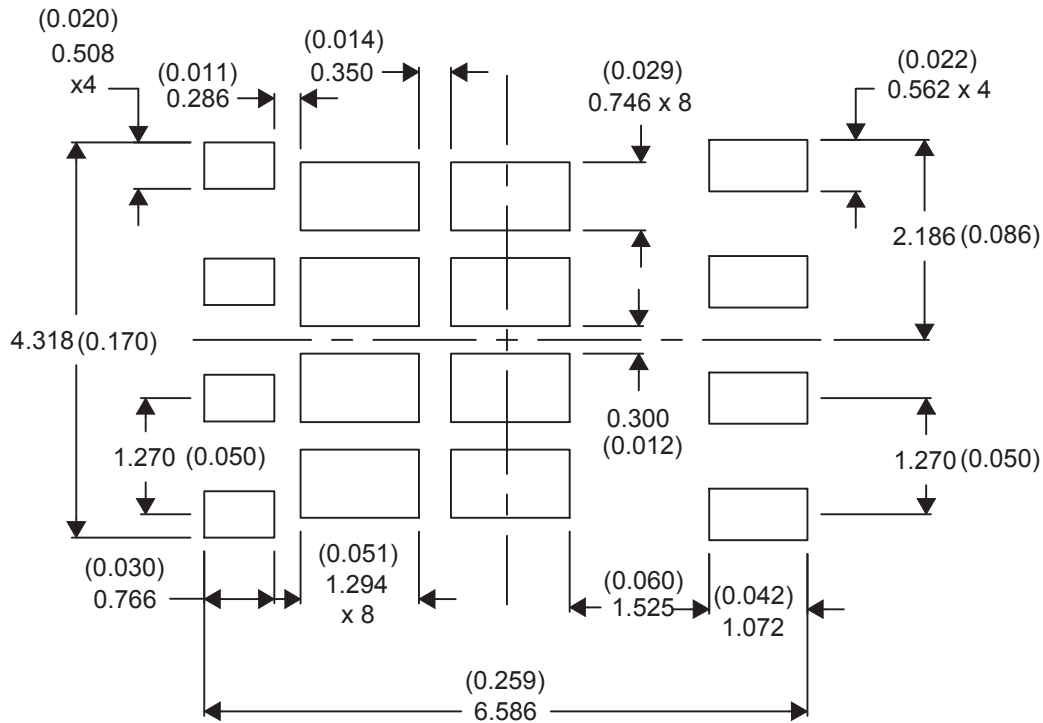
7.2 建议 PCB 布局

，焊盘 3 和 4 之间的尺寸从 0.028 英寸更改为 0.050 英寸
(0.175)

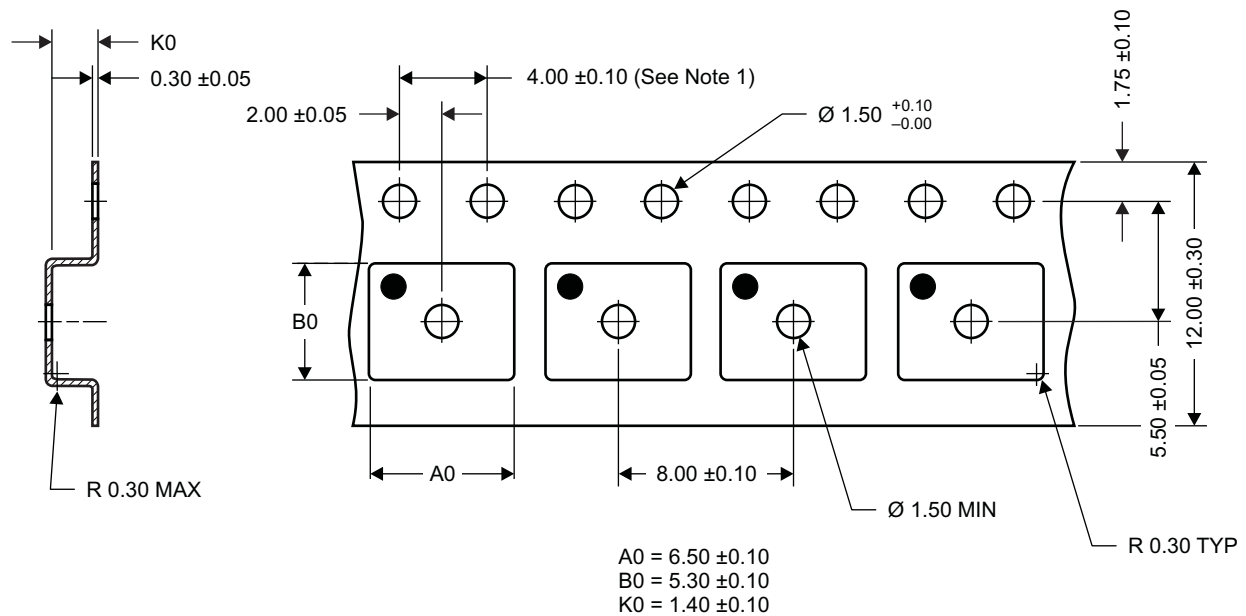


要获得与印刷电路板 (PCB) 设计相关的建议电路布局布线，请参见《应用说明》[SLPA005 - 通过 PCB 布局布线技巧来减少振铃](#)。

7.3 建议模板布局



7.4 Q5B 卷带信息



M0138-01

注释:

- 10 个链齿孔的累积容差为 ± 0.2
- 每 100mm 长度的翘曲不能超过 1mm, 在 250mm 长度上不累积
- 材料: 黑色抗静电聚苯乙烯
- 全部尺寸单位为 mm (除非另外注明)。
- 高于孔眼底部 0.3mm 的平面上测量得到 A0 和 B0 值

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD18509Q5B	Active	Production	VSON-CLIP (DNK) 8	2500 LARGE T&R	ROHS Exempt	NIPDAU SN	Level-1-260C-UNLIM	-55 to 150	CSD18509
CSD18509Q5B.B	Active	Production	VSON-CLIP (DNK) 8	2500 LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	CSD18509
CSD18509Q5BG4	Active	Production	VSON-CLIP (DNK) 8	2500 LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	CSD18509
CSD18509Q5BG4.B	Active	Production	VSON-CLIP (DNK) 8	2500 LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	CSD18509
CSD18509Q5BT	Active	Production	VSON-CLIP (DNK) 8	250 SMALL T&R	ROHS Exempt	NIPDAU SN	Level-1-260C-UNLIM	-55 to 150	CSD18509
CSD18509Q5BT.B	Active	Production	VSON-CLIP (DNK) 8	250 SMALL T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	CSD18509

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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