

CSD18502Q5B 40V N 通道 NexFET™ 功率 MOSFET

1 特性

- 超低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩额定值
- 逻辑电平
- 无铅引脚镀层
- 符合 RoHS 环保标准
- 无卤素
- 小外形尺寸无引线 (SON) 5mm x 6mm 塑料封装

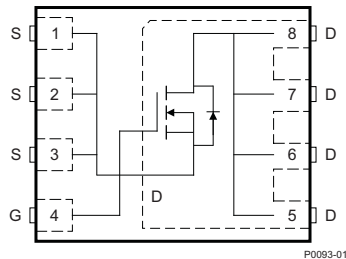
2 应用

- 直流 - 直流转换
- 次级侧同步整流器
- 电机控制

3 说明

此 40V、1.8mΩ、5mm × 6mm NexFET™ 功率 MOSFET 被设计成在功率转换应用中大大降低损耗。

顶视图



P0093-01

产品概要

$T_A = 25^\circ\text{C}$		典型值		单位
V_{DS}	漏源电压	40		V
Q_g	栅极电荷总量 (4.5V)	25		nC
Q_{gd}	栅漏栅极电荷	8.4		nC
$R_{DS(on)}$	漏源导通电阻	$V_{GS} = 4.5\text{V}$	2.5	mΩ
		$V_{GS} = 10\text{V}$	1.8	mΩ
$V_{GS(th)}$	阈值电压	1.8		V

订购信息^(a)

器件	数量	包装介质	封装	运输
CSD18502Q5B	2500	13 英寸卷带	SON 5mm × 6mm 塑料封装	卷带封装
CSD18502Q5BT	250	7 英寸卷带		

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

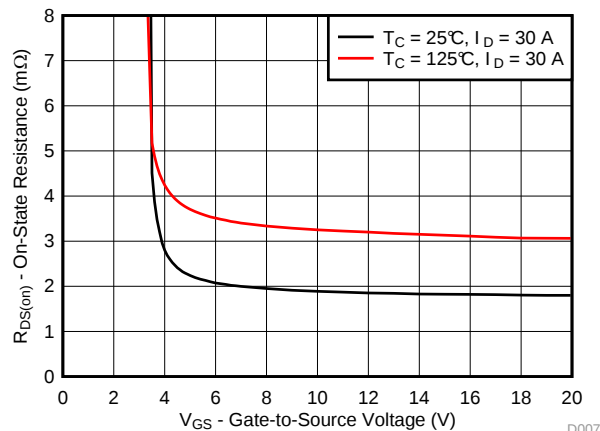
绝对最大额定值

$T_A = 25^\circ\text{C}$		值	单位
V_{DS}	漏源电压	40	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流 (受封装限制)	100	A
	持续漏极电流 (受芯片限制), $T_C = 25^\circ\text{C}$ 时测得	204	
	持续漏极电流 ⁽¹⁾	26	
I_{DM}	脉冲漏极电流 ⁽²⁾	400	A
P_D	功率耗散 ⁽¹⁾	3.2	W
	功率损耗, $T_C = 25^\circ\text{C}$	156	
T_J	工作结温	-55 至 150	°C
T_{stg}	存储温度	-55 至 150	°C
E_{AS}	雪崩能量, 单一脉冲 $I_D = 88\text{A}$, $L = 0.1\text{mH}$, $R_G = 25\Omega$	387	mJ

(1) $R_{\theta JA} = 40^\circ\text{C/W}$ 。这是在厚度为 0.06 英寸的环氧板 (FR4) 印刷电路板 (PCB) 上的 1 英寸² 2 盎司的铜焊盘上测得的典型值。

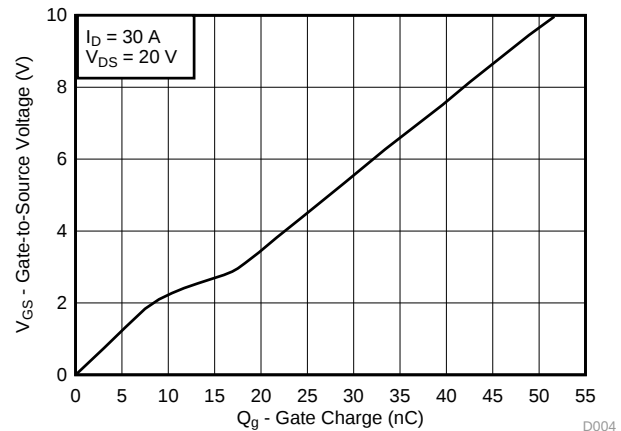
(2) 最大 $R_{\theta JC} = 0.8^\circ\text{C/W}$ ，脉冲持续时间 $\leq 100\mu\text{s}$ ，占空比 $\leq 1\%$

$R_{DS(on)}$ 与 V_{GS} 对比



D007

栅极电荷



D004



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (May 2015) to Revision B	Page
• 已添加 接收文档更新通知 部分。	7
• 已更改 在建议 PCB 布局 部分方框图中将焊盘 3 和 4 之间的尺寸从 0.028 英寸更改为了 0.050 英寸	9

Changes from Original (November 2012) to Revision A	Page
• 在标题中添加了部件编号。	1
• 向订购信息 中添加了 7 英寸卷带。	1
• 向绝对最大额定值 中添加了 $T_C = 25^{\circ}\text{C}$ 时的功率损耗。	1
• 在绝对最大额定值 中更新了脉冲漏极电流条件。	1
• Updated Figure 1 to normalized $R_{\theta JC}$ curves.	4
• Updated SOA in Figure 10.	6
• 添加了 社区资源。	8
• 更新了机械图纸以显示其他尺寸。	8

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

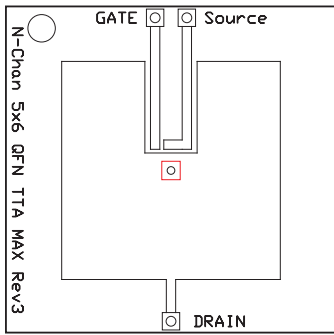
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{DSS}	Drain to source voltage	V _{GS} = 0 V, I _D = 250 μA	40			V
I _{DSS}	Drain to source leakage current	V _{GS} = 0 V, V _{DS} = 32 V			1	μA
I _{GSS}	Gate to source leakage current	V _{DS} = 0 V, V _{GS} = 20 V			100	nA
V _{GS(th)}	Gate to source threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	1.5	1.8	2.2	V
R _{DS(on)}	Drain to source on resistance	V _{GS} = 4.5 V, I _D = 30 A	2.5		3.3	mΩ
		V _{GS} = 10 V, I _D = 30 A	1.8		2.3	mΩ
g _{fs}	Transconductance	V _{DS} = 20 V, I _D = 30 A	143			S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input capacitance	V _{GS} = 0 V, V _{DS} = 20 V, f = 1 MHz	3900		5070	pF
C _{oss}	Output capacitance		900		1170	pF
C _{rss}	Reverse transfer capacitance		21		27	pF
R _G	Series gate resistance		1.2	2.4		Ω
Q _g	Gate charge total (4.5 V)	V _{DS} = 20 V, I _D = 30 A	25		33	nC
Q _g	Gate charge total (10 V)		52		68	nC
Q _{gd}	Gate charge gate to drain		8.4			nC
Q _{gs}	Gate charge gate to source		10.3			nC
Q _{g(th)}	Gate charge at V _{th}		6.9			nC
Q _{oss}	Output charge	V _{DS} = 20 V, V _{GS} = 0 V	59			nC
t _{d(on)}	Turn on delay time	V _{DS} = 20 V, V _{GS} = 10 V, I _{DS} = 30 A, R _G = 0 Ω	5.3			ns
t _r	Rise time		6.8			ns
t _{d(off)}	Turn off delay time		23			ns
t _f	Fall time		4			ns
DIODE CHARACTERISTICS						
V _{SD}	Diode forward voltage	I _{SD} = 30 A, V _{GS} = 0 V	0.8		1	V
Q _{rr}	Reverse recovery charge	V _{DS} = 20 V, I _F = 30 A, di/dt = 300 A/μs	88			nC
t _{rr}	Reverse recovery time		44			ns

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

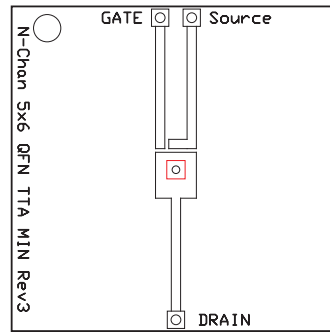
THERMAL METRIC		MIN	TYP	MAX	UNIT
R _{θJC}	Junction-to-case (top of package) thermal resistance ⁽¹⁾			0.8	°C/W
R _{θJA}	Junction-to-ambient thermal resistance ⁽¹⁾⁽²⁾			50	°C/W

- (1) R_{θJC} is determined with the device mounted on a 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inch × 1.5 inch (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB. R_{θJC} is specified by design, whereas R_{θJA} is determined by the user's board design.
- (2) Device mounted on FR4 material with 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu.



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Max $R_{\theta JA} = 50^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of 2
oz. (0.071 mm thick)
Cu.

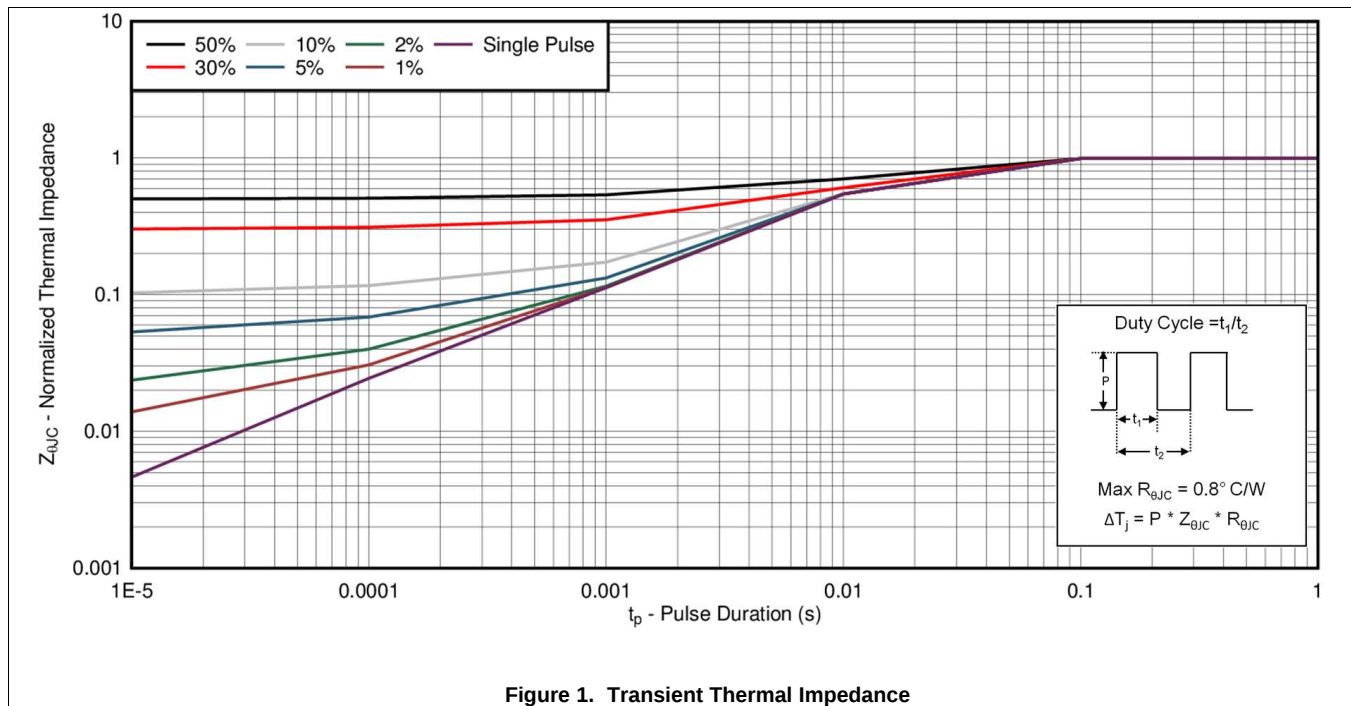


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Max $R_{\theta JA} = 125^{\circ}\text{C/W}$
when mounted on a
minimum pad area of 2
oz. (0.071 mm thick)
Cu.

5.3 Typical MOSFET Characteristics

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)



Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

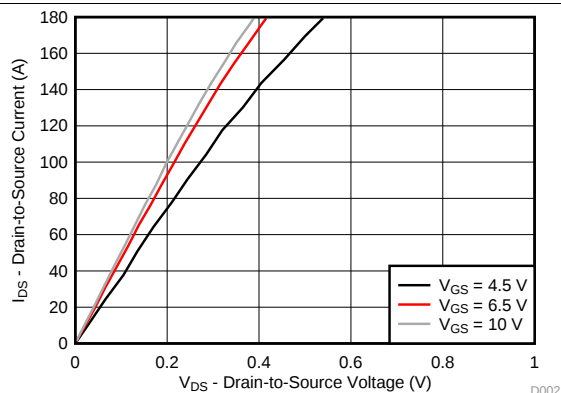


Figure 2. Saturation Characteristics

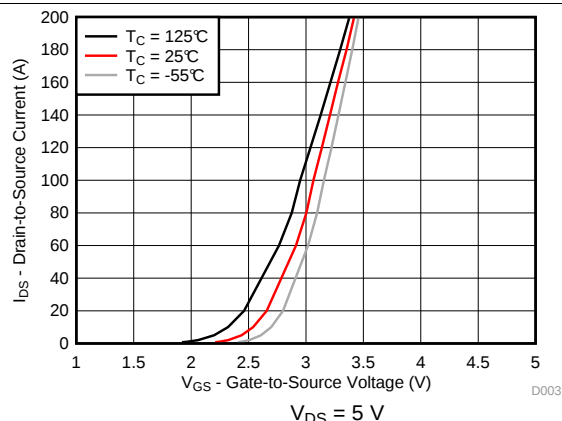


Figure 3. Transfer Characteristics

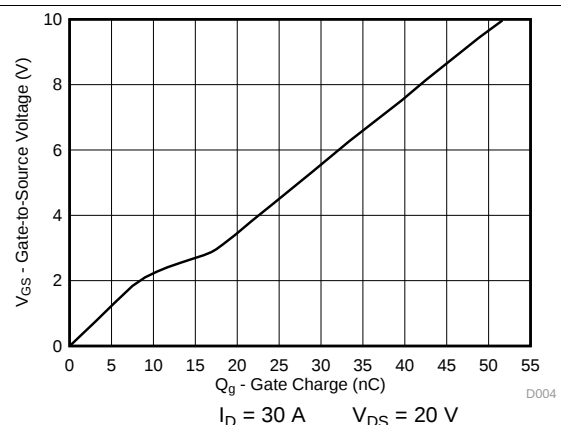


Figure 4. Gate Charge

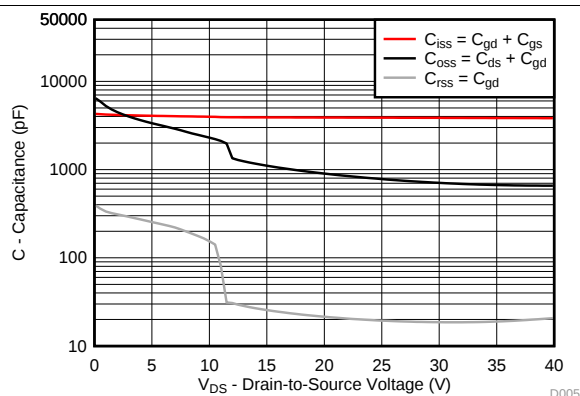


Figure 5. Capacitance

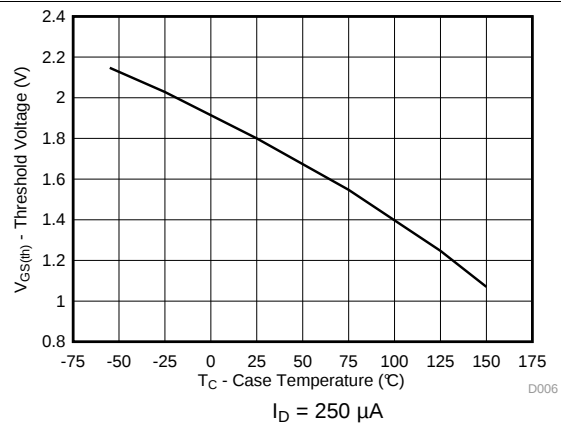


Figure 6. Threshold Voltage vs Temperature

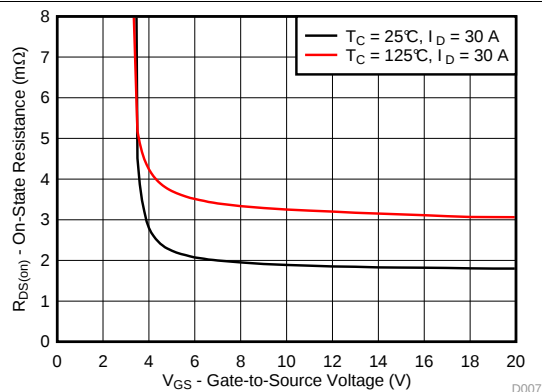


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

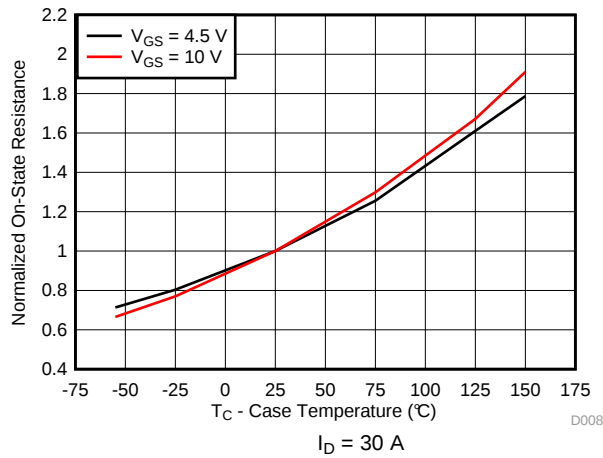


Figure 8. Normalized On-State Resistance vs Temperature

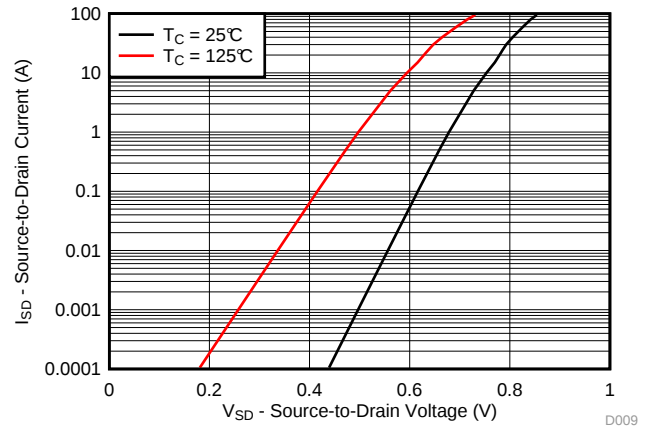


Figure 9. Typical Diode Forward Voltage

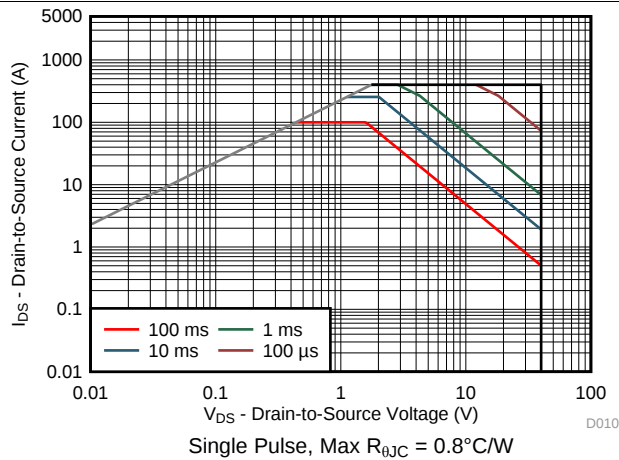


Figure 10. Maximum Safe Operating Area

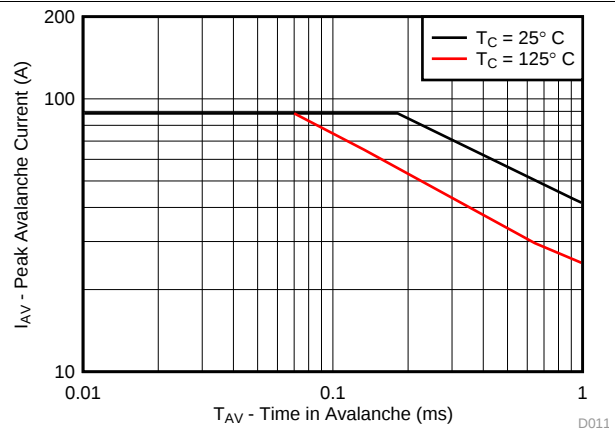


Figure 11. Single Pulse Unclamped Inductive Switching

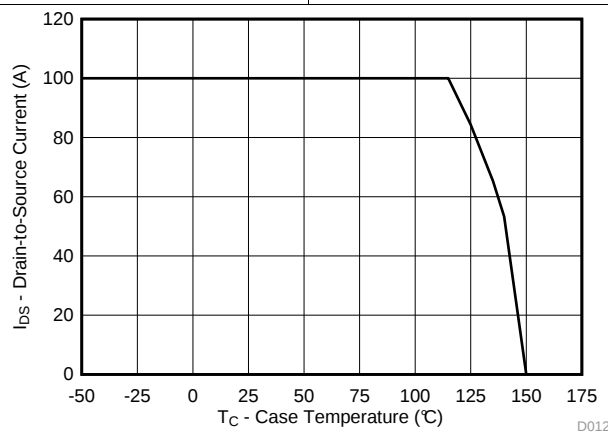


Figure 12. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的提醒我 (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

6.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 商标

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6.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

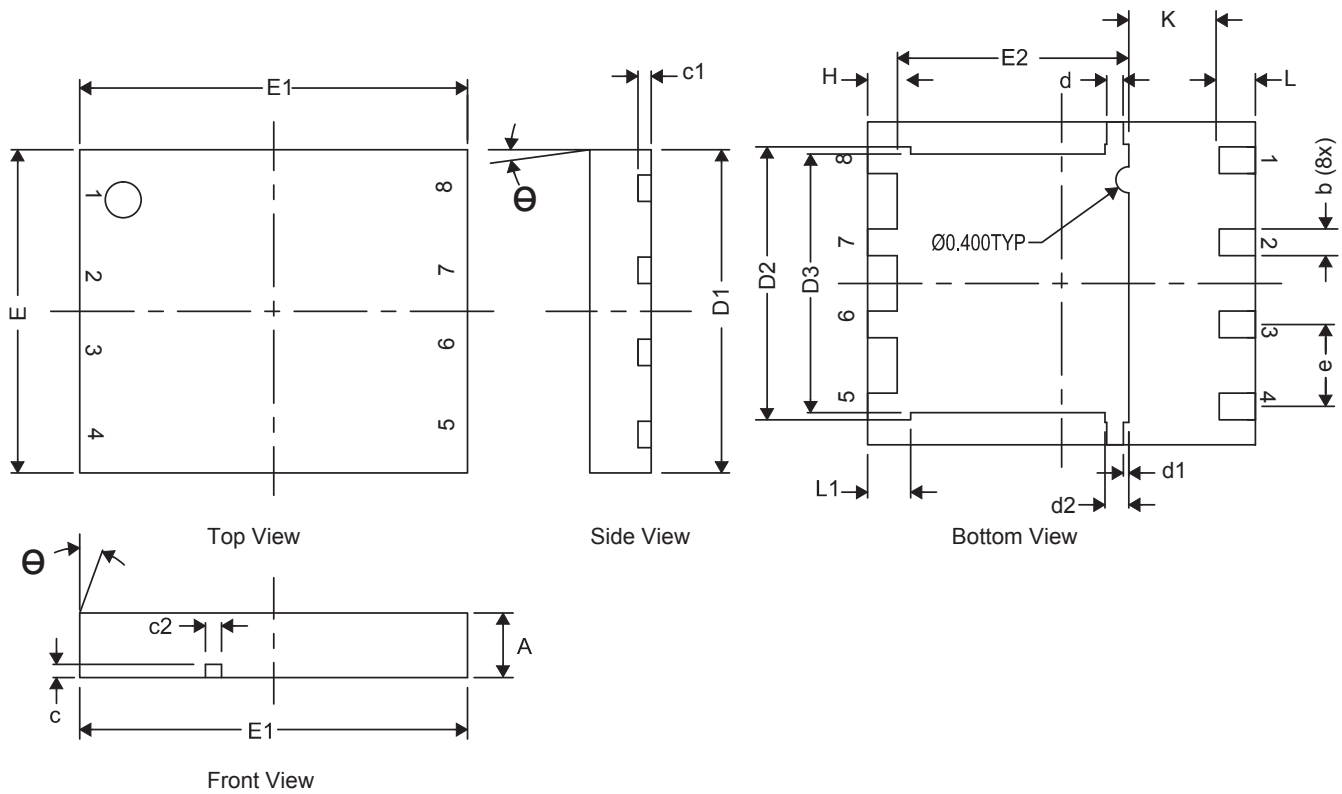
6.5 Glossary

SLYZ022 — *TI Glossary*.

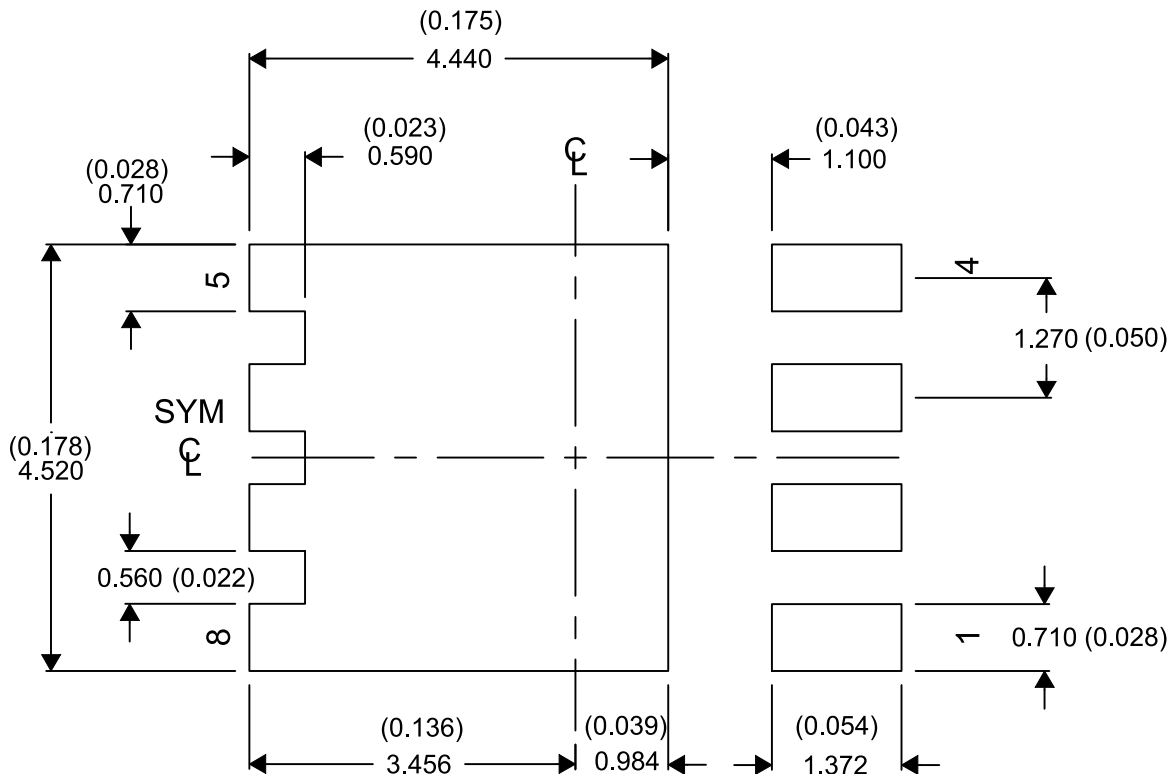
This glossary lists and explains terms, acronyms, and definitions.

7 机械、封装和可订购信息

7.1 Q5B 封装尺寸

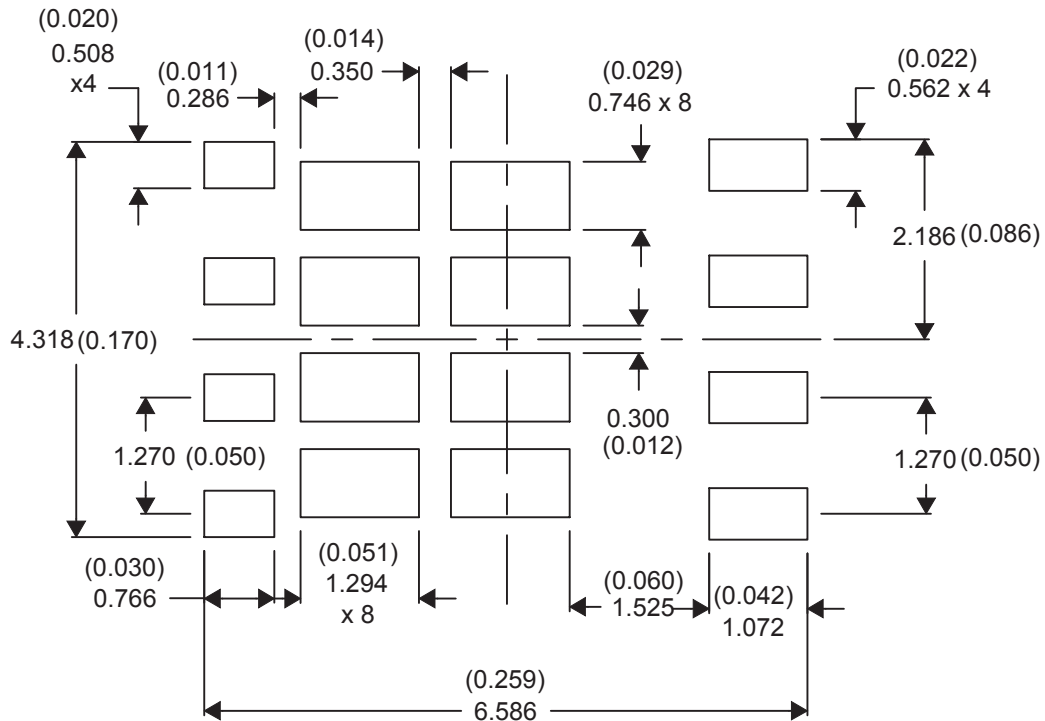


7.2 建议 PCB 布局

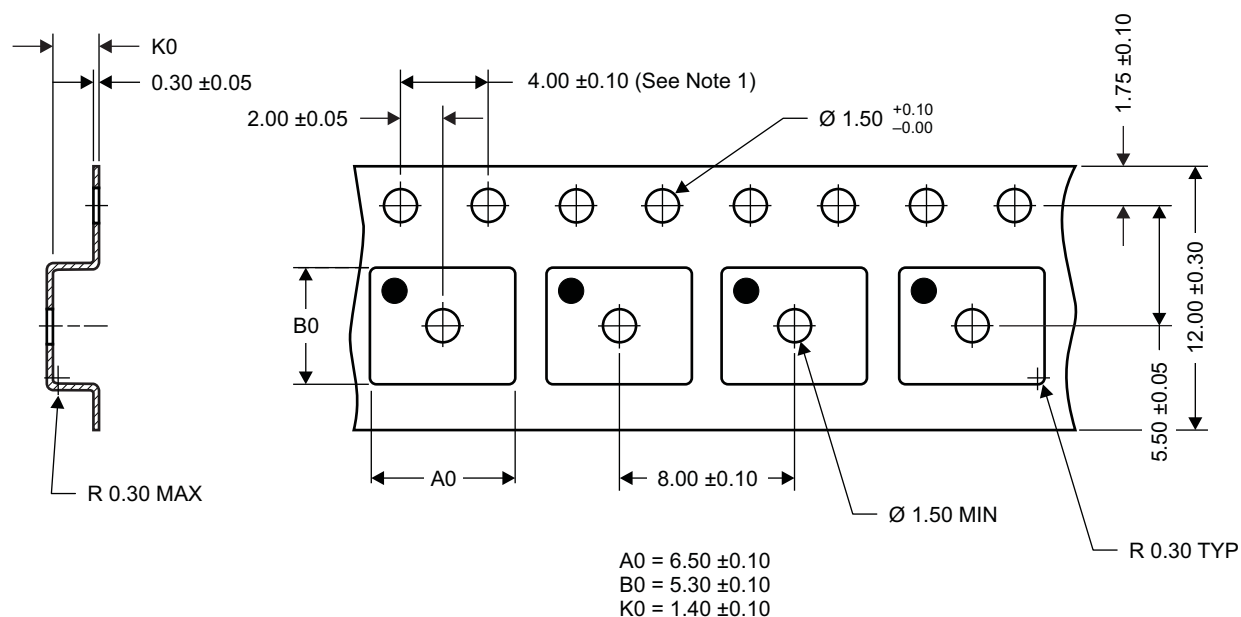


要获得与 PCB 设计相关的建议电路布局，请参见《通过 PCB 布局技巧来减少振铃》(SLPA005)。

7.3 建议模板布局



7.4 Q5B 卷带信息



M0138-01

注释:

1. 10 个链齿孔的累积容差为 ± 0.2
2. 每 100mm 长度的翘曲不能超过 1mm，在 250mm 长度上不累积
3. 材料：黑色抗静电聚苯乙烯
4. 全部尺寸单位为 mm（除非另外注明）
5. 高于孔眼底部 0.3mm 的平面上测量得到 A0 和 B0 值

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD18502Q5B	Active	Production	VSON-CLIP (DNK) 8	2500 LARGE T&R	ROHS Exempt	NIPDAU SN	Level-1-260C-UNLIM	-	CSD18502
CSD18502Q5B.B	Active	Production	VSON-CLIP (DNK) 8	2500 LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	CSD18502
CSD18502Q5BT	Active	Production	VSON-CLIP (DNK) 8	250 SMALL T&R	ROHS Exempt	NIPDAU SN	Level-1-260C-UNLIM	-55 to 150	CSD18502
CSD18502Q5BT.B	Active	Production	VSON-CLIP (DNK) 8	250 SMALL T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	CSD18502

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD18502Q5B	VSON-CLIP	DNK	8	2500	330.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1
CSD18502Q5BT	VSON-CLIP	DNK	8	250	180.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD18502Q5B	VSON-CLIP	DNK	8	2500	346.0	346.0	33.0
CSD18502Q5BT	VSON-CLIP	DNK	8	250	182.0	182.0	20.0

重要通知和免责声明

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