CSD17577Q3A 30V N 通道 NexFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET)

1 特性

- 低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩额定值
- 无铅
- 符合 RoHS 环保标准
- 无卤素
- 小外形尺寸无引线 (SON) 3.3mm × 3.3mm 封装

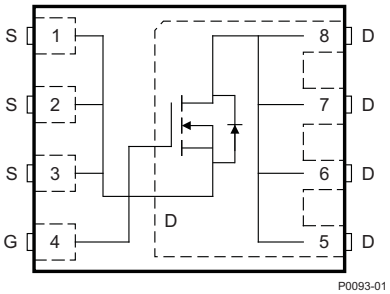
2 应用范围

- 网络互联、电信和计算系统中的负载点同步降压
- 针对控制和同步 FET 应用进行了优化

3 说明

这款 30V，4.0mΩ，SON 3.3mm × 3.3mm NexFET™ 功率 MOSFET 被设计成在功率转换应用中以最大程度降低电阻。

顶部图标



P0093-01

产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	30		V
Q_g	栅极电荷总量 (4.5V)	12		nC
Q_{gd}	栅漏栅极电荷	2.5		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 4.5V	5.3	mΩ
		V_{GS} = 10V	4	mΩ
$V_{GS(th)}$	阈值电压	1.4		V

订购信息(1)

器件	数量	介质	封装	出货
CSD17577Q3A	2500	13 英寸卷带	SON 3.3mm x 3.3mm 塑料封装	卷带封装
CSD17577Q3AT	250	7 英寸卷带		

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

最大绝对额定值

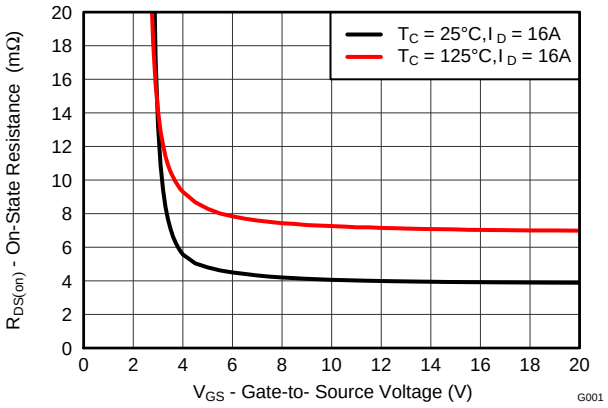
T_A = 25°C		值	单位
V_{DS}	漏源电压	30	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流（受封装限制）	35	A
	持续漏极电流（受芯片限制），T_C = 25°C 时测得	83	
	持续漏极电流 (1)	19	
I_{DM}	脉冲漏极电流 (2)	239	A
P_D	功率耗散(1)	2.8	W
	功率耗散，T_C = 25°C	53	
T_J，T_{stg}	运行结温和储存温度范围	-55 至 150	°C
E_{AS}	雪崩能量，单一脉冲 I_D = 28A，L = 0.1mH，R_G = 25Ω	39	mJ

(1) $R_{\theta JA}$ = 50°C/W，这是在一个厚度 0.06 英寸环氧树脂 (FR4) 印刷电路板 (PCB) 上的 1 英寸^2，2 盎司 的铜焊盘上测得的典型值
。

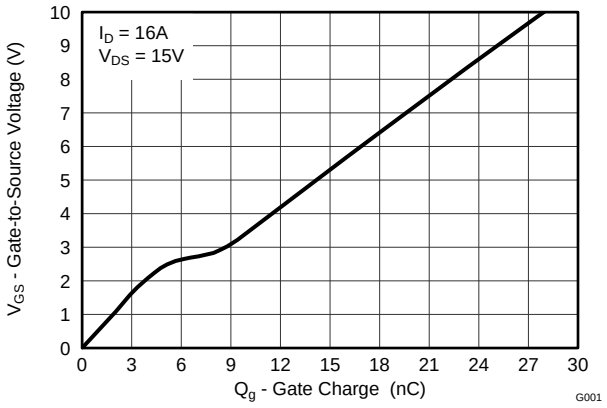
(2) 最大 $R_{\theta JC}$ = 3.0°C/W，脉冲持续时间 ≤ 100μs，占空比 ≤ 1%

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

$R_{DS(on)}$ 与 V_{GS} 间的关系



栅极电荷



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目录

4 修订历史记录

日期	修订版本	注释
2014 年 8 月	*	最初发布。

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5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 24 V			1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1.1	1.4	1.8	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 4.5 V, I_D = 10 A		5.3	6.4	mΩ
		V_{GS} = 10 V, I_D = 16 A		4	4.8	mΩ
g_{fs}	Transconductance	V_{DS} = 15 V, I_D = 16 A		76		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		1780	2310	pF
C_{oss}	Output Capacitance			208	270	pF
C_{rss}	Reverse Transfer Capacitance			79	103	pF
R_G	Series Gate Resistance			1.4	2.8	Ω
Q_g	Gate Charge Total (4.5 V)	V_{DS} = 15 V, I_D = 16 A		13	17	nC
Q_g	Gate Charge Total (10 V)			27	35	nC
Q_{gd}	Gate Charge Gate-to-Drain			2.8		nC
Q_{gs}	Gate Charge Gate-to-Source			5.1		nC
$Q_{g(th)}$	Gate Charge at V_{th}			2.5		nC
Q_{oss}	Output Charge	V_{DS} = 15 V, V_{GS} = 0 V		6		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 15 V, V_{GS} = 10 V, I_{DS} = 16 A, R_G = 0 Ω		4		ns
t_r	Rise Time			31		ns
$t_{d(off)}$	Turn Off Delay Time			20		ns
t_f	Fall Time			4		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{SD} = 16 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= 15 V, I_F = 16 A, di/dt = 300 A/µs		8.2		nC
t_{rr}	Reverse Recovery Time			8.6		ns

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance(1)			3.0	°C/W
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance(1)(2)			55	

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inches × 1.5-inches (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.

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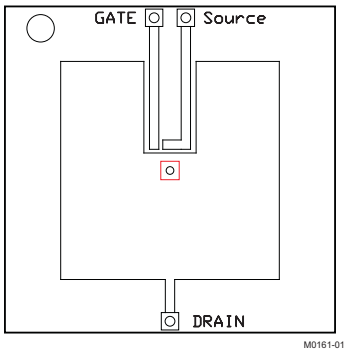
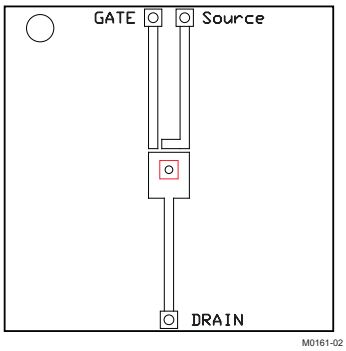


Max $R_{\theta JA}$ = 55°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 190°C/W when mounted on a minimum pad area of 2-oz. (0.071-mm thick) Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

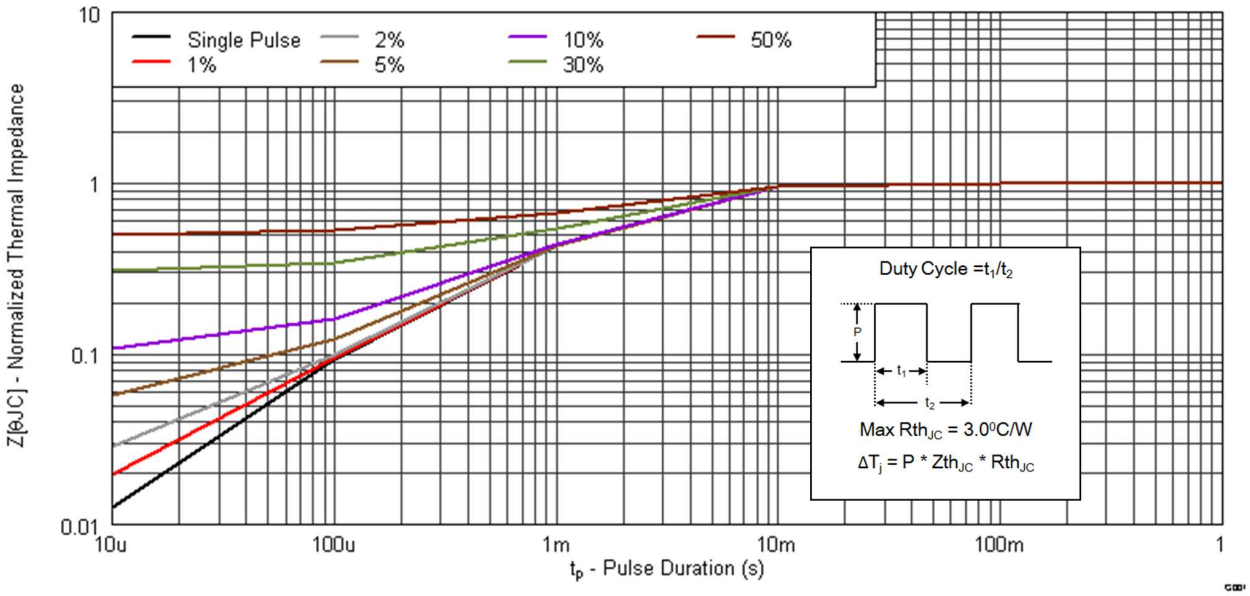


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

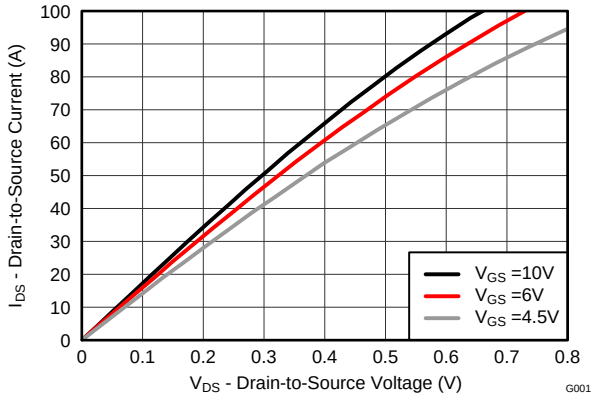


Figure 2. Saturation Characteristics

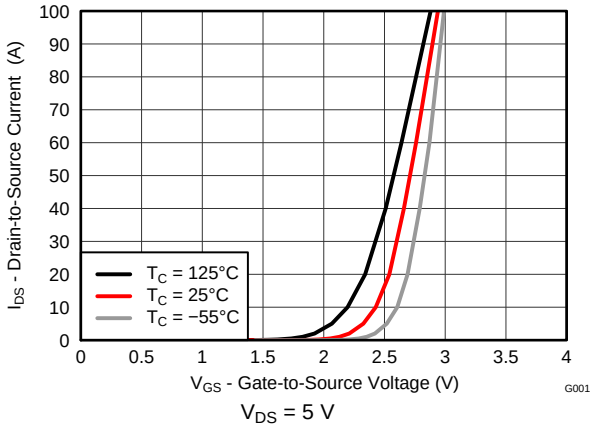


Figure 3. Transfer Characteristics

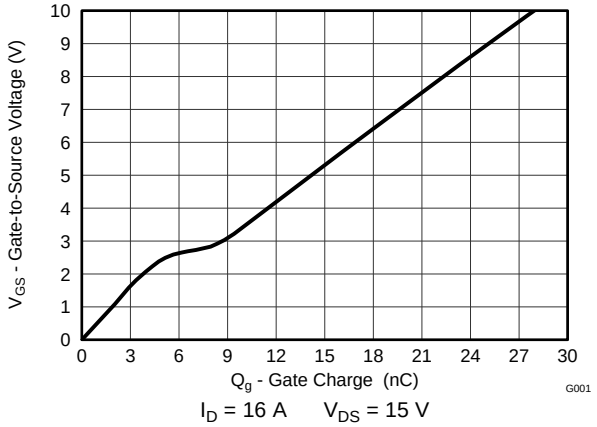


Figure 4. Gate Charge

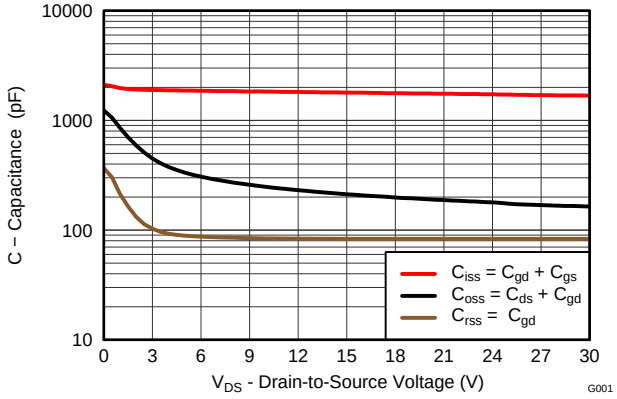


Figure 5. Capacitance

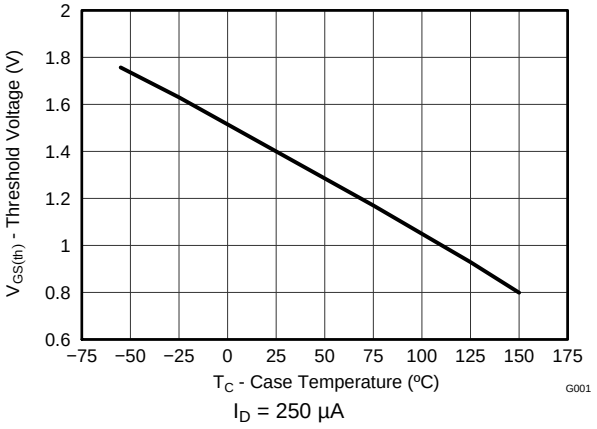


Figure 6. Threshold Voltage vs Temperature

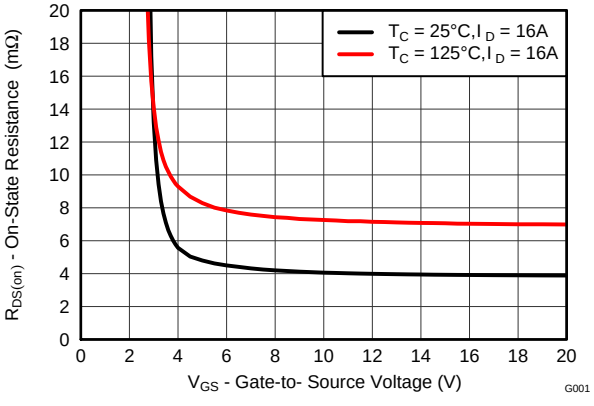


Figure 7. On-State Resistance vs Gate-to-Source Voltage

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Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

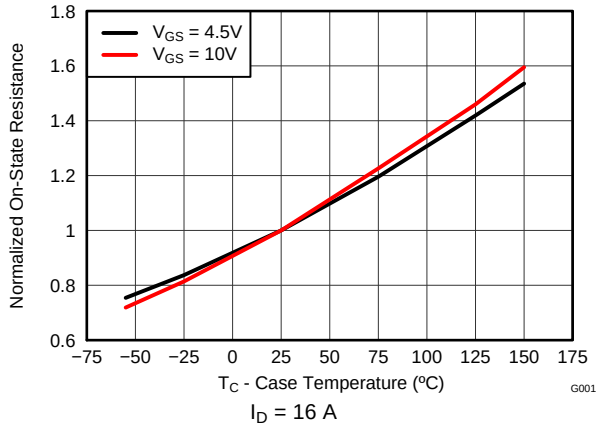

Figure 8. Normalized On-State Resistance vs Temperature

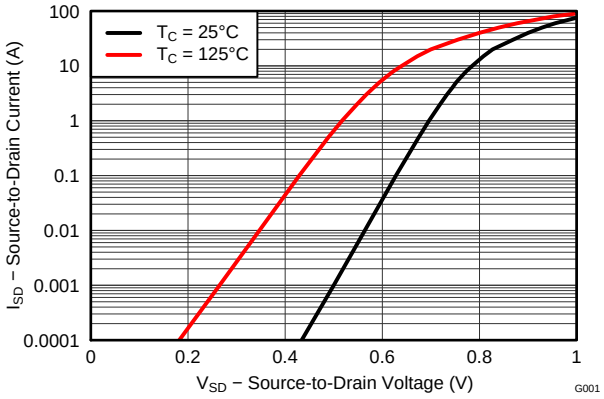

Figure 9. Typical Diode Forward Voltage

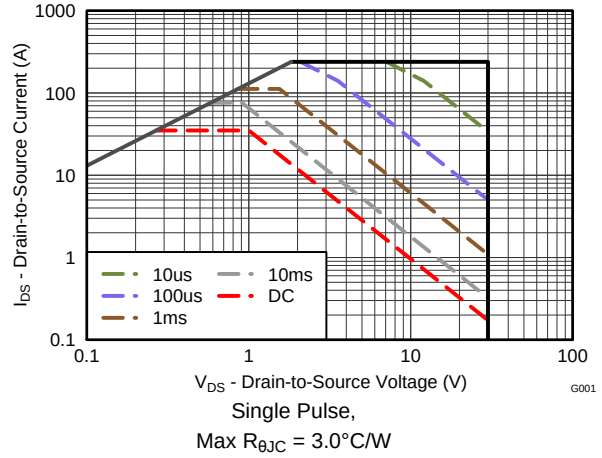

Figure 10. Maximum Safe Operating Area

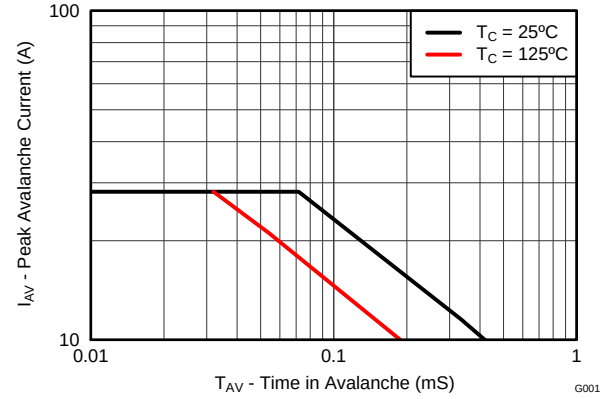

Figure 11. Single Pulse Unclamped Inductive Switching

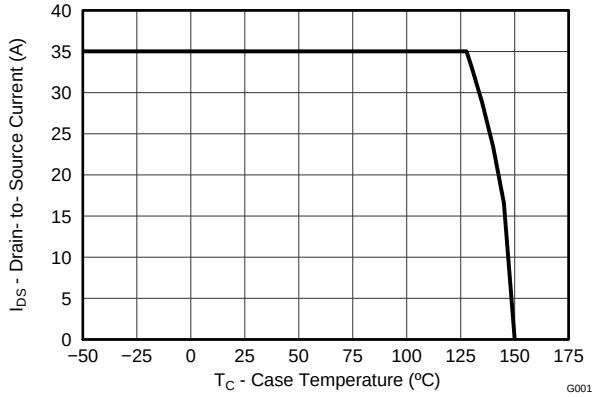

Figure 12. Maximum Drain Current vs Temperature

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6 器件和文档支持

6.1 Trademarks

NexFET is a trademark of Texas Instruments.

6.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

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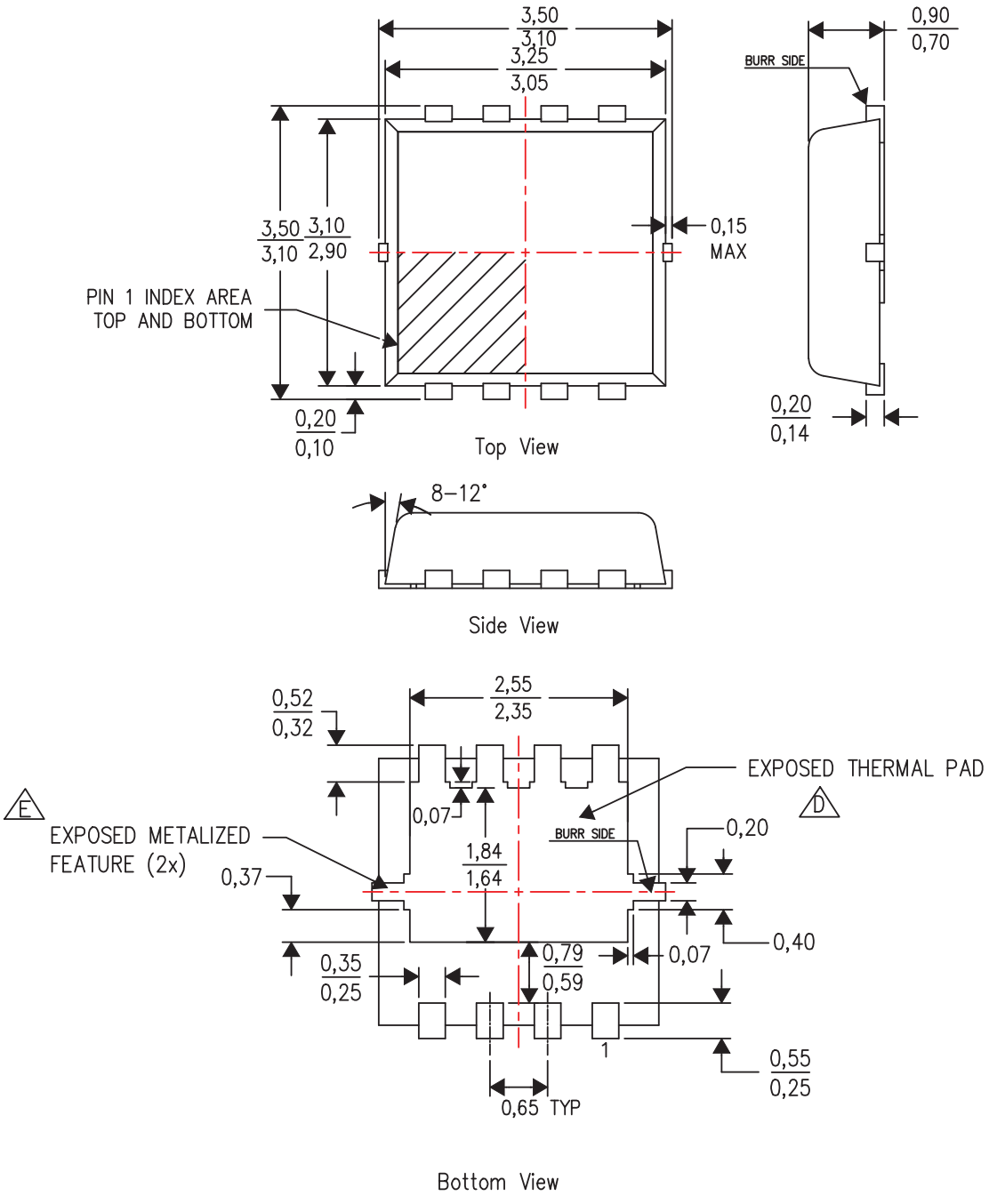
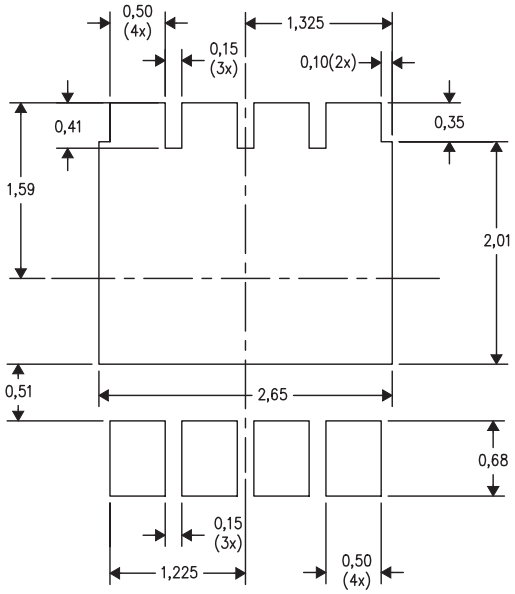
7 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

7.1 Q3A 封装尺寸

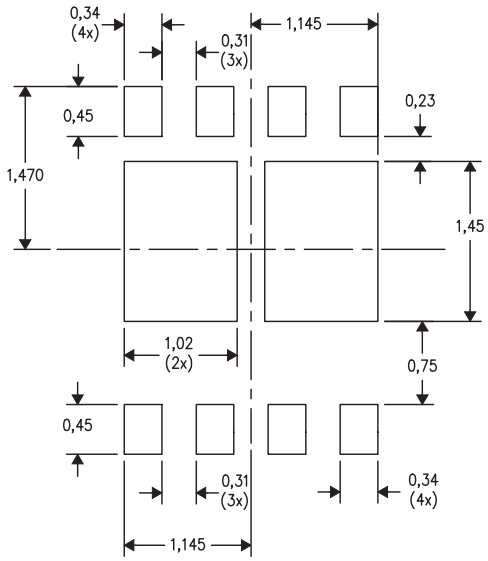


7.2 Q3A 建议的 PCB 布局



要获得与印刷电路板 (PCB) 设计相关的建议电路布局布线，请参见《应用说明》SLPA005 - *通过 PCB 布局布线技巧来减少振铃*。

7.3 Q3A 建议的模板布局



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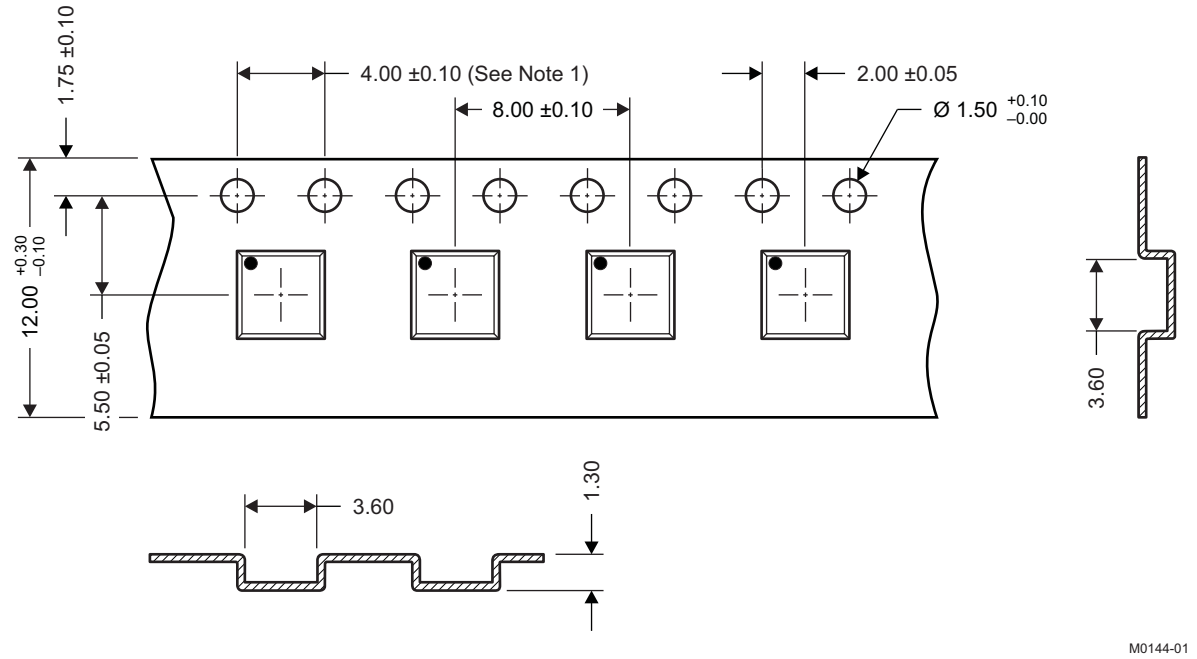
7.4 Q3A 卷带信息



Notes: 1. 10 链轮孔距累积容差 ±0.2

2. 每 100mm 长度的翘曲不能超过 1mm，在 250mm 长度上不累积
3. 材料：黑色抗静电聚苯乙烯
4. 全部尺寸单位为 mm，除非另外注明。
5. 厚度：0.30 ± 0.05mm
6. MSL1 260°C（红外 (IR) 和传导）PbF 回流焊兼容

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD17577Q3A	Active	Production	VSONP (DNH) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 150	17577
CSD17577Q3A.B	Active	Production	VSONP (DNH) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 150	17577
CSD17577Q3AT	Active	Production	VSONP (DNH) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 150	17577
CSD17577Q3AT.B	Active	Production	VSONP (DNH) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-55 to 150	17577

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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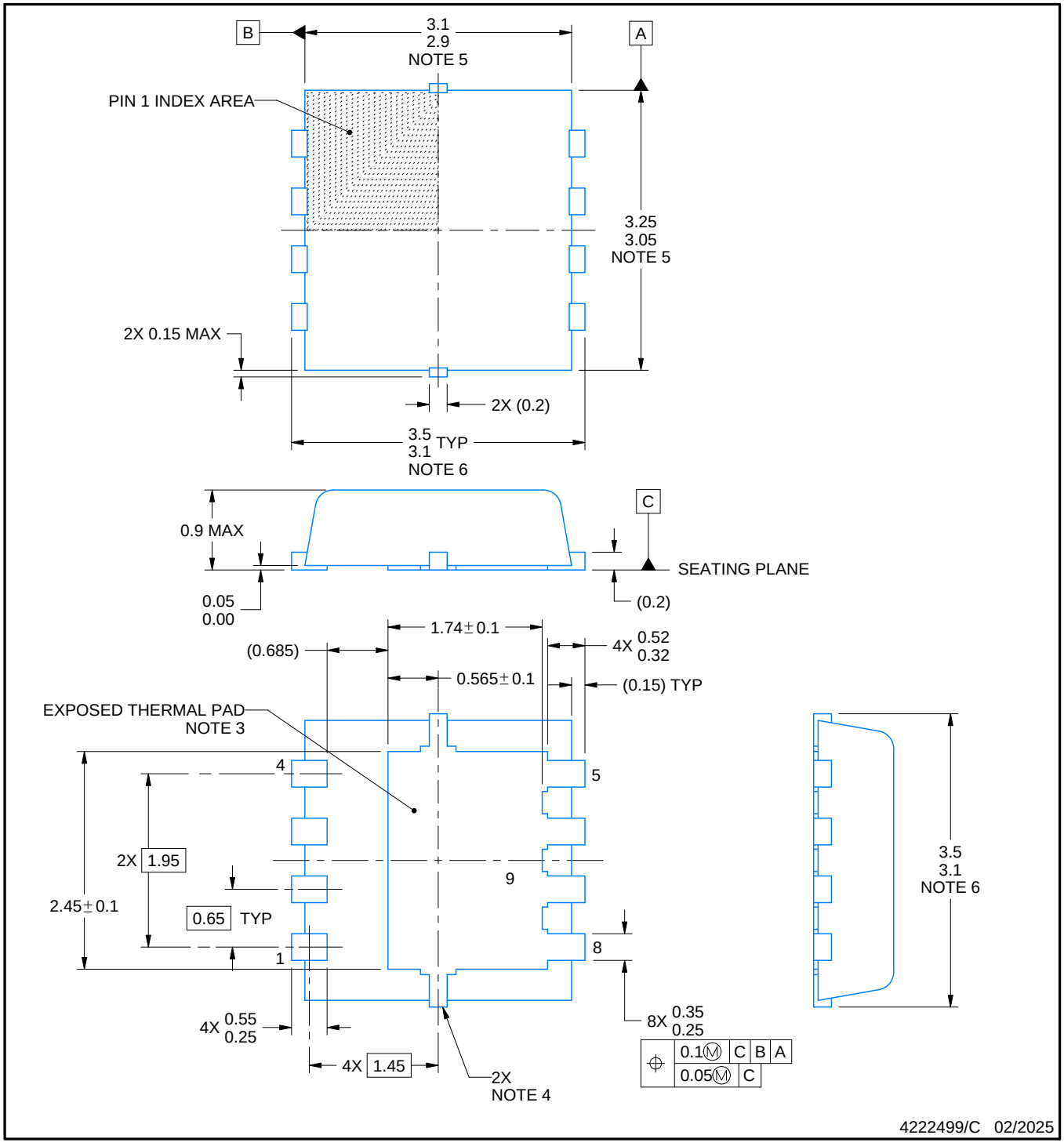
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

DNH0008A

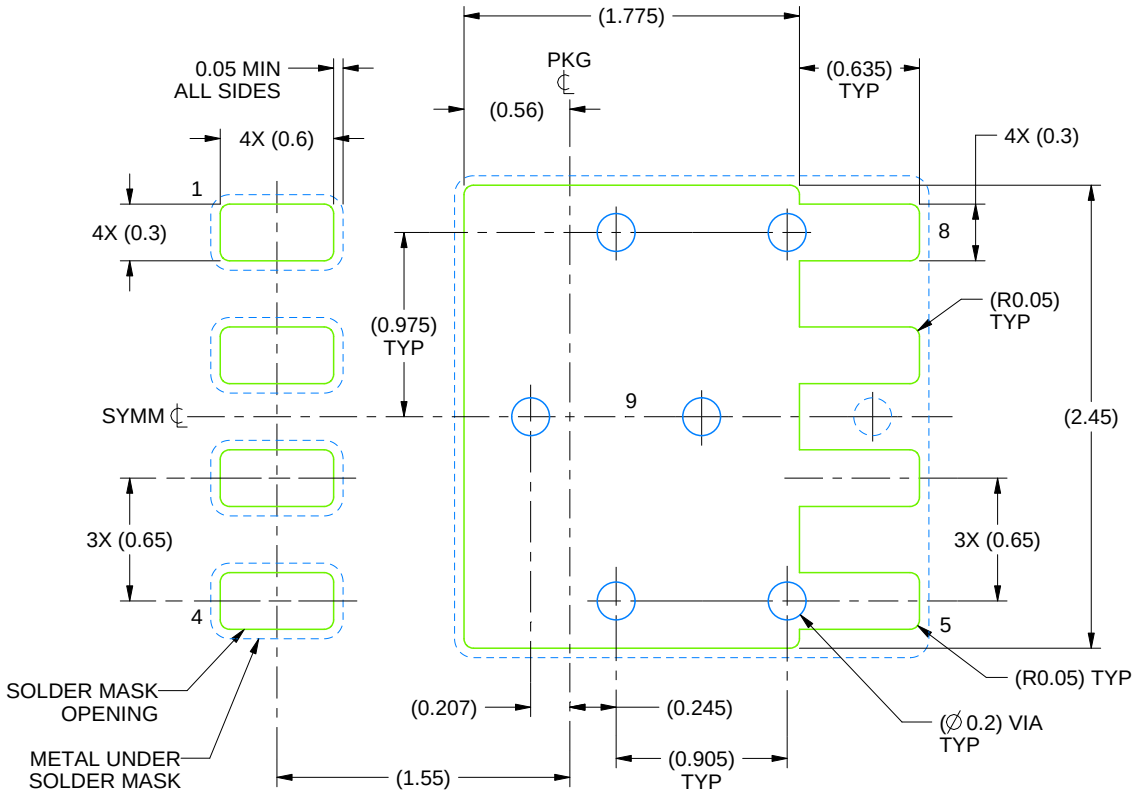
VSONP - 0.9 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Metalized features are supplier options and may not be on the package.
5. These dimensions do not include mold flash protrusions or gate burrs.
6. These dimensions include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE: 25X

4222499/C 02/2025

NOTES: (continued)

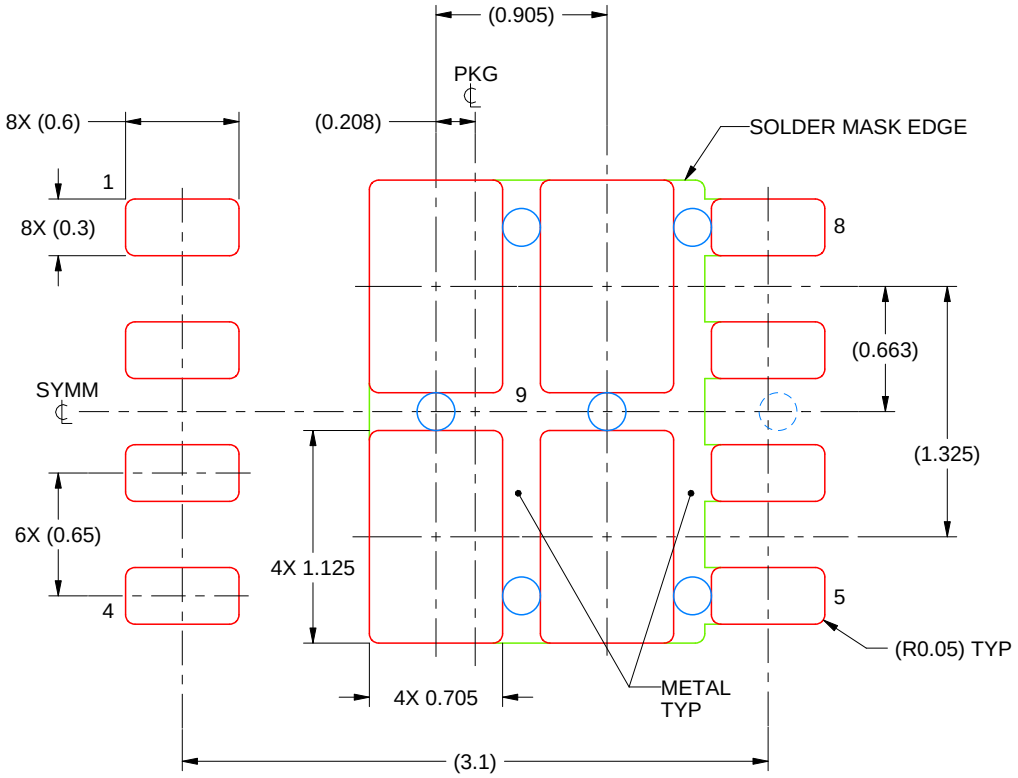
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DNH0008A

VSONP - 0.9 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 25X

4222499/C 02/2025

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

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