CSD17573Q5B 30V N 通道 NexFET™功率 MOSFET

1 特性

- 低 Q_g 和 Q_{gd}
- 超低导通电阻 $R_{DS(on)}$
- 低热阻
- 雪崩额定值
- 无铅引脚镀层
- 符合 RoHS 环保标准
- 无卤素
- SON 5mm × 6mm 塑料封装

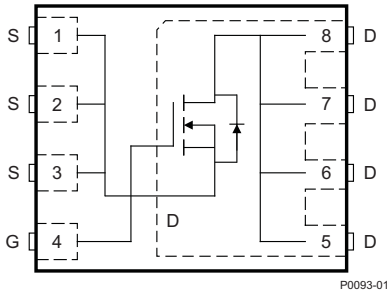
2 应用范围

- 用于网络互联、电信和计算系统的 负载点 同步降压转换器
- 已针对同步 FET 应用进行 优化

3 说明

此 0.84mΩ、30V、SON 5mm × 6mm NexFET™功率 MOSFET 被设计成在功率转换应用中大大降低 损耗。

俯视图



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产品概要

T_A=25°C		典型值		单位
V_{DS}	漏源极电压	30		V
Q_g	栅极电荷总量 (4.5V)	49		nC
Q_{gd}	栅极电荷（栅极到漏极）	11.9		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 4.5V	1.19	mΩ
		V_{GS} = 10V	0.84	
$V_{GS(th)}$	阈值电压	1.4		V

器件信息(1)

器件	数量	包装介质	封装	运输
CSD17573Q5B	2500	13 英寸卷带	SON 5.00-mm × 6.00-mm 塑料封装	卷带封装
CSD17573Q5BT	250	7 英寸卷带		

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

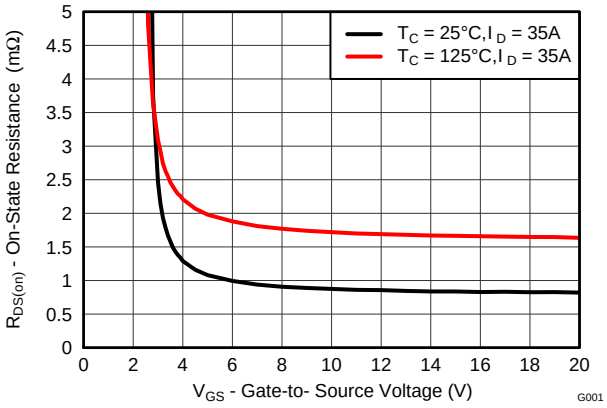
绝对最大额定值

T_A = 25°C		值	单位
V_{DS}	漏源极电压	30	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流（受封装限制）	100	A
	持续漏极电流（受芯片限制），T_C = 25°C 时测得	332	
	持续漏极电流(1)	43	
I_{DM}	脉冲漏极电流(2)	400	A
P_D	功率耗散(1)	3.2	W
	功率耗散，T_C = 25°C	195	
T_J, T_{stg}	工作结温，储存温度	-55 至 150	°C
E_{AS}	雪崩能量，单一脉冲 I_D = 76，L = 0.1mH，R_G = 25Ω	289	mJ

(1) $R_{\theta JA}$ = 40°C/W，这是在一块厚度为 0.06 英寸环氧树脂 (FR4) 印刷电路板 (PCB) 上的 1 英寸^2，2 盎司铜焊盘上测得的典型值。

(2) 最大 $R_{\theta JC}$ = 0.8°C/W，脉冲持续时间 ≤ 100µs，占空比 ≤ 1%。

$R_{DS(on)}$ 与 V_{GS} 间的关系



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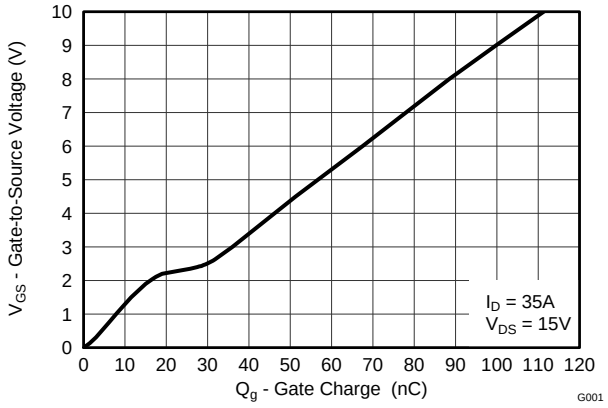
栅极电荷



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4 修订历史记录

Changes from Revision A (February 2015) to Revision B **Page**

- Changed Figure 10 in *Typical MOSFET Characteristics* section ... 4
- 已添加 *接收文档更新通知*和*社区资源*添加到*器件和文档支持*部分 ... 7
- 已更改 更正了*建议 PCB 布局*部分方框图中的拼写错误 ... 9

Changes from Original (June 2014) to Revision A **Page**

- 已将“阈值电压”单位更正为“V” ... 1

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

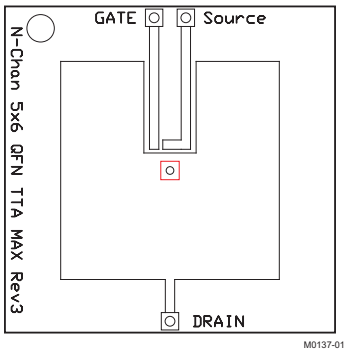
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 μA	30			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 24 V			1	μA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 μA	1.1	1.4	1.8	V
$R_{DS(on)}$	Drain-to-source on resistance	V_{GS} = 4.5 V, I_D = 35 A		1.19	1.45	mΩ
		V_{GS} = 10 V, I_D = 35 A		0.84	1.00	
g_{fs}	Transconductance	V_{DS} = 15 V, I_D = 35 A		181		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		6920	9000	pF
C_{oss}	Output capacitance			769	1000	pF
C_{rss}	Reverse transfer capacitance			300	390	pF
R_G	Series gate resistance			0.9	1.8	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 15 V, I_D = 35 A		49	64	nC
Q_{gd}	Gate charge gate-to-drain			11.9		nC
Q_{gs}	Gate charge gate-to-source			17.1		nC
$Q_{g(th)}$	Gate charge at V_{th}			8.6		nC
Q_{oss}	Output charge	V_{DS} = 30 V, V_{GS} = 0 V		21		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 15 V, V_{GS} = 10 V, I_{DS} = 35 A, R_G = 0 Ω		6		ns
t_r	Rise time			20		ns
$t_{d(off)}$	Turnoff delay time			40		ns
t_f	Fall Time			7		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 35 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse recovery charge	V_{DS}= 15 V, I_F = 35 A, di/dt = 300 A/μs		29		nC
t_{rr}	Reverse recovery time			21		ns

5.2 Thermal Information

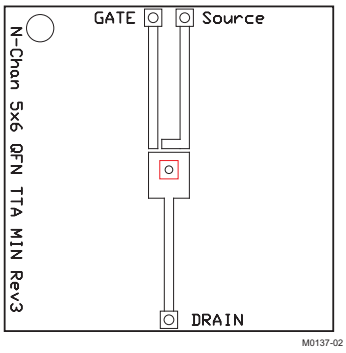
T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance(1)			0.8	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)(2)			50	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 50°C/W when mounted on 1 in^2 (6.45 cm^2) of 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on a minimum pad area of 2-oz (0.071-mm) thick Cu.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

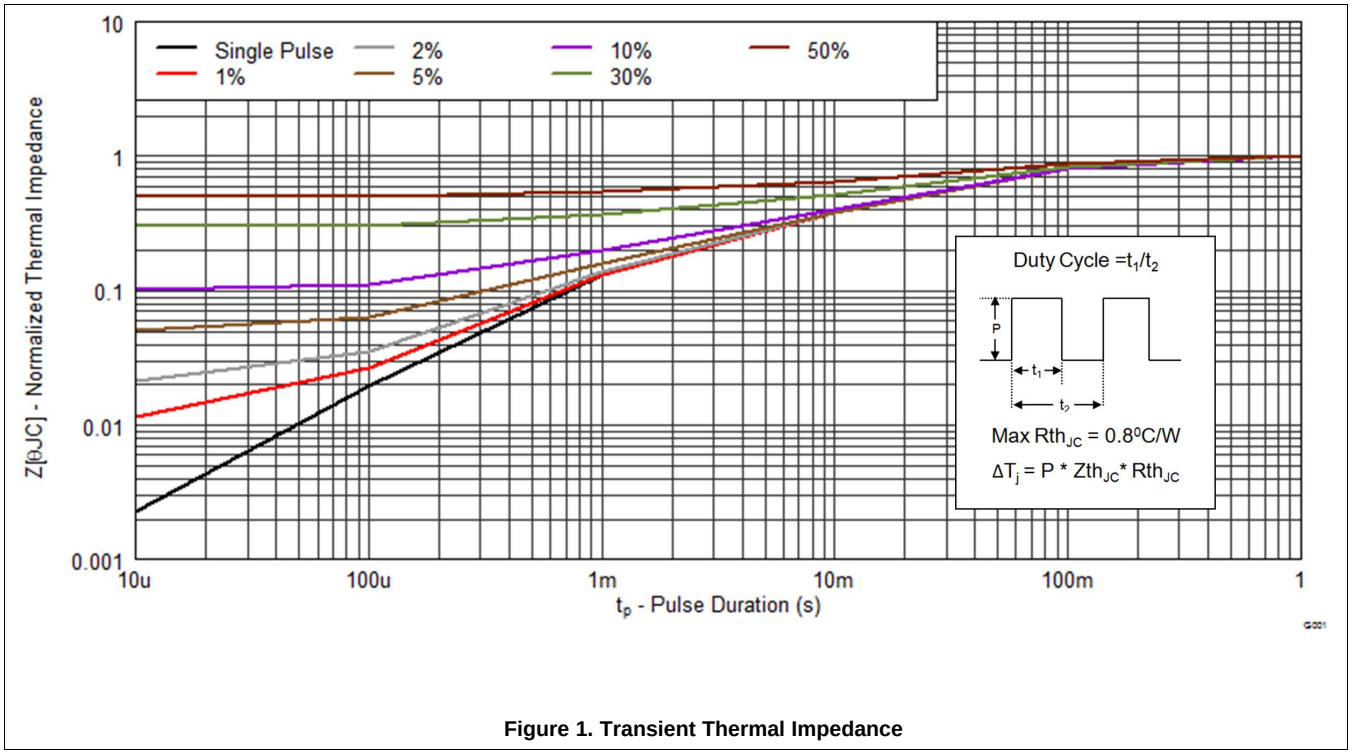


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

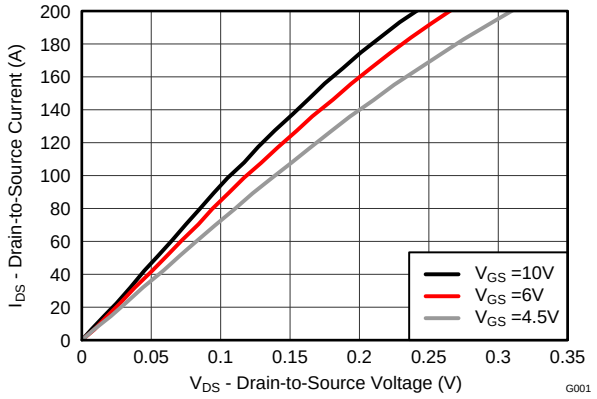


Figure 2. Saturation Characteristics

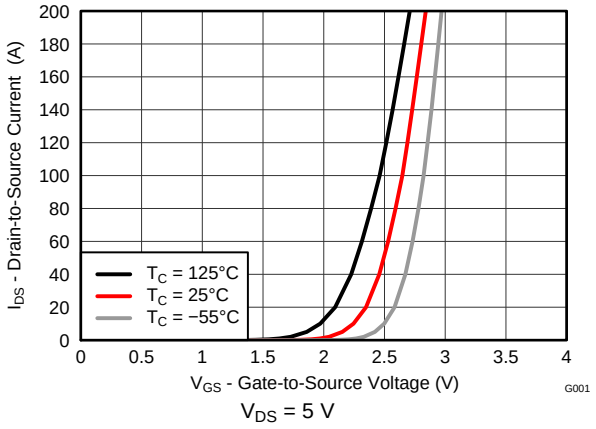


Figure 3. Transfer Characteristics

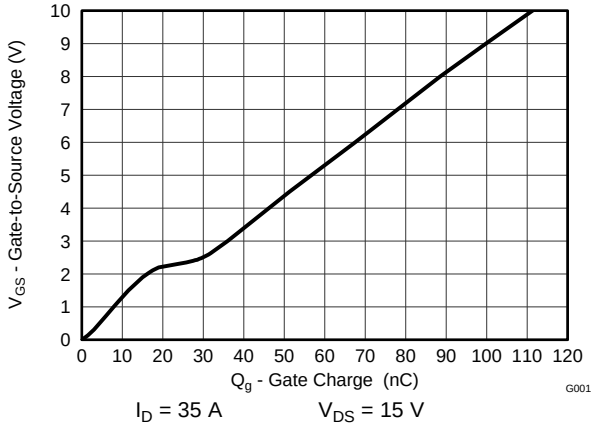


Figure 4. Gate Charge

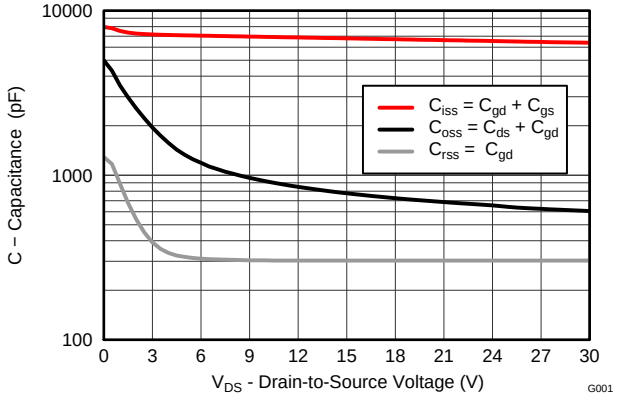


Figure 5. Capacitance

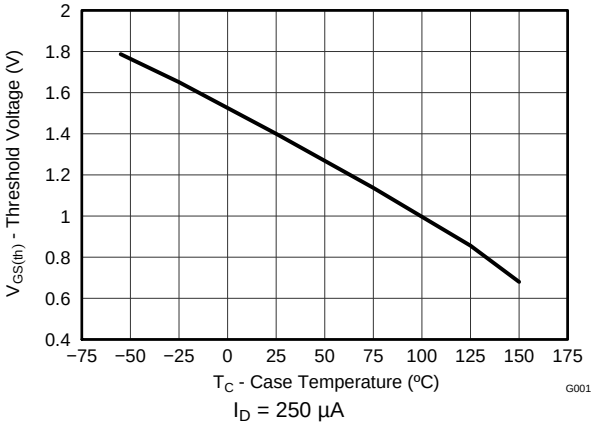


Figure 6. Threshold Voltage vs Temperature

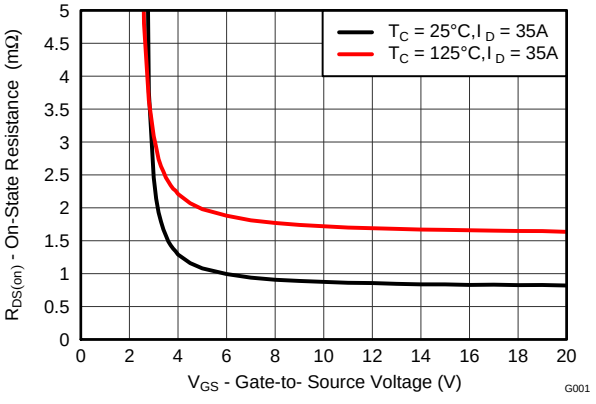


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

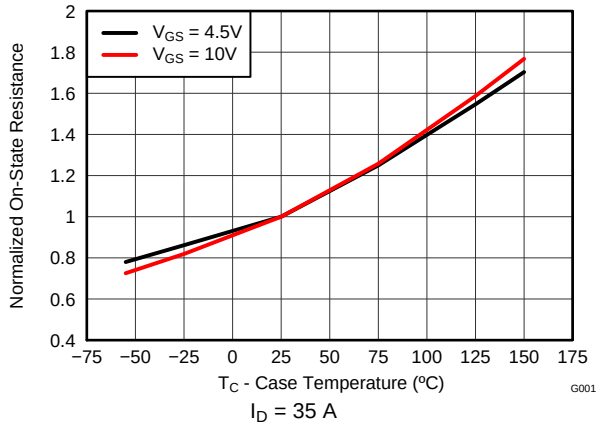


Figure 8. Normalized On-State Resistance vs Temperature

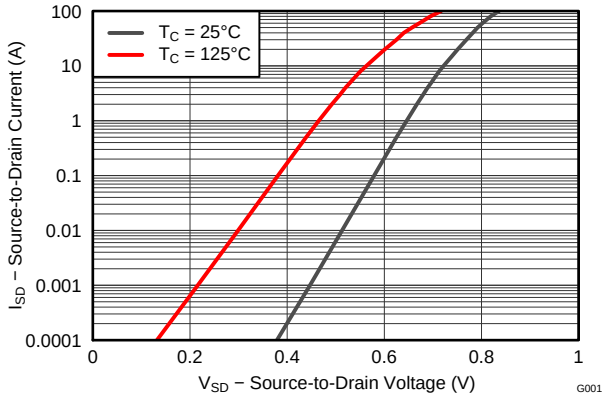


Figure 9. Typical Diode Forward Voltage

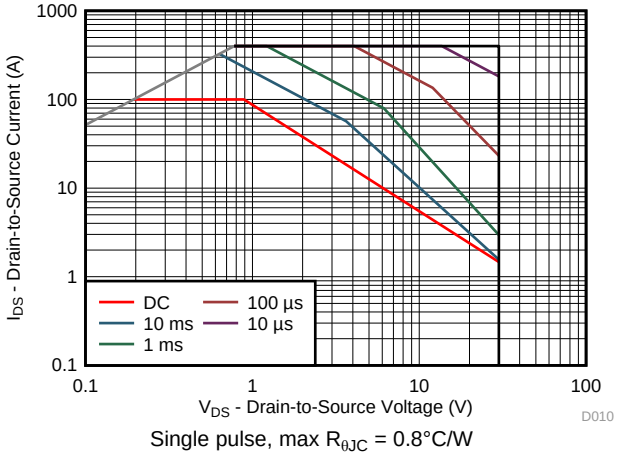


Figure 10. Maximum Safe Operating Area

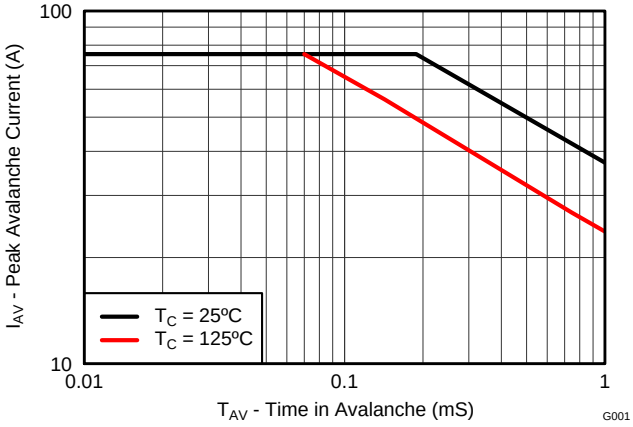


Figure 11. Single Pulse Unclamped Inductive Switching

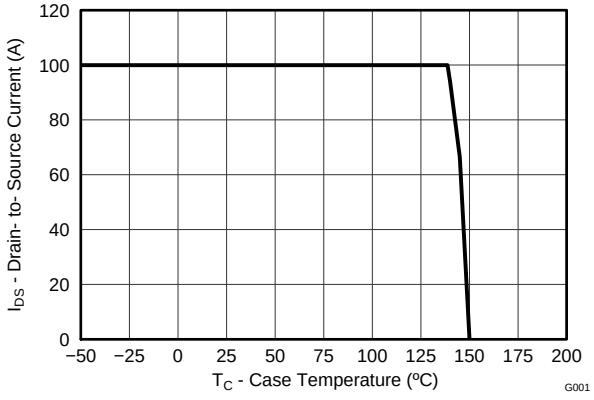


Figure 12. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

6.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 商标

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6.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.5 Glossary

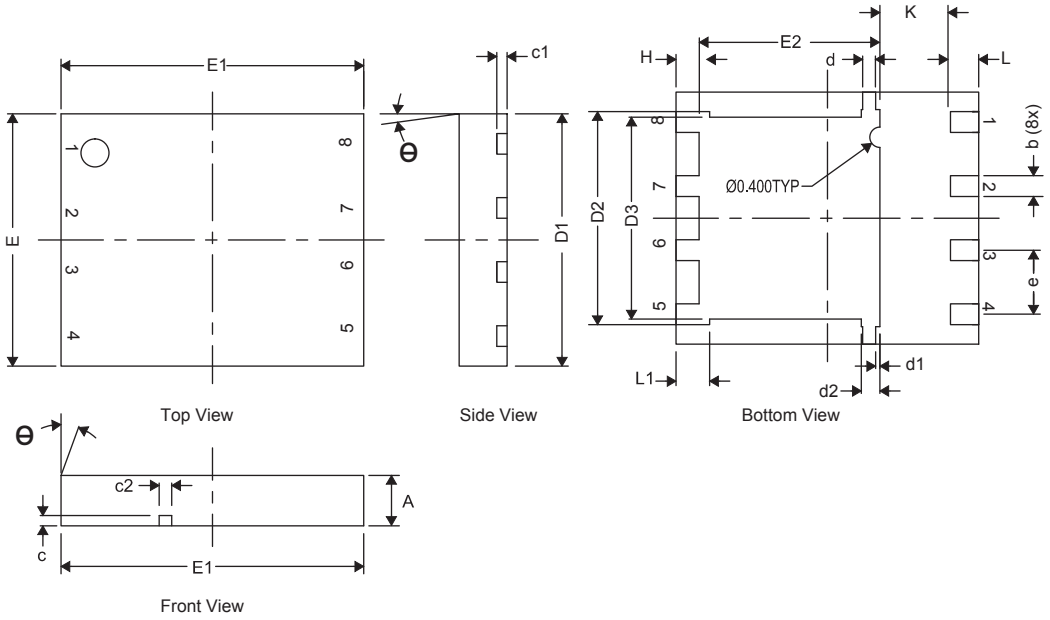
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。要获得这份数据表的浏览器版本，请查阅左侧的导航栏。

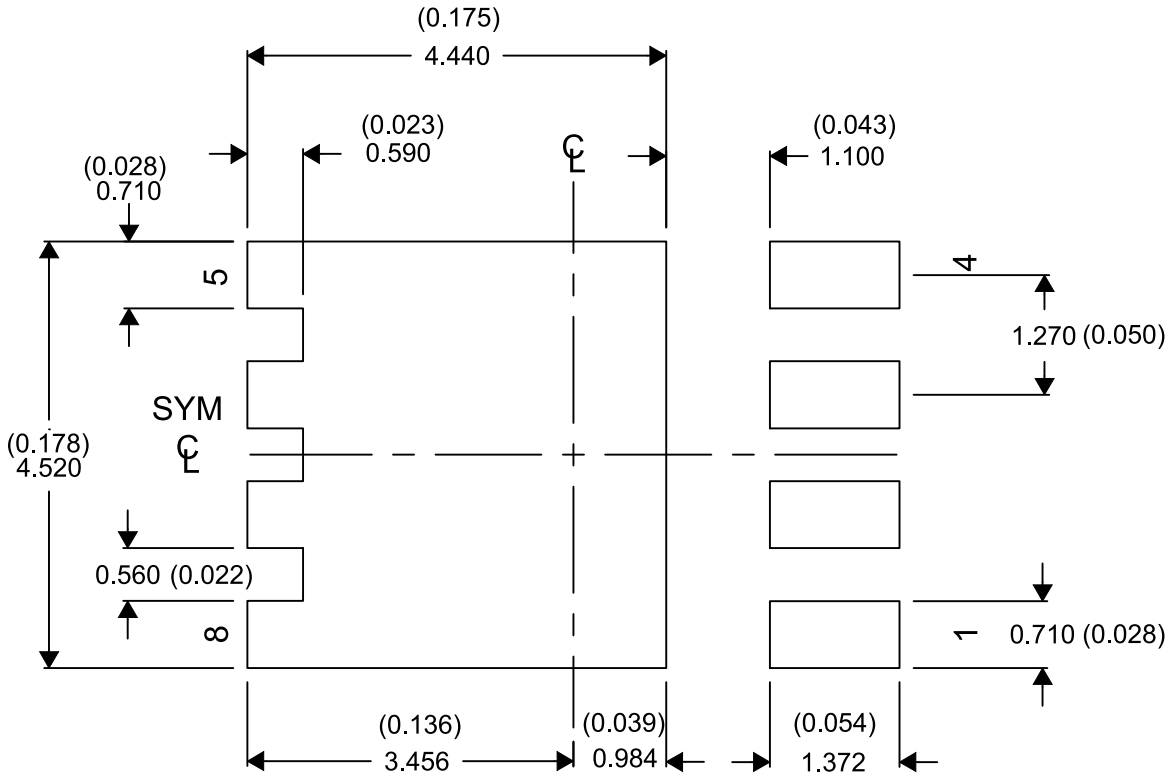
7.1 Q5B 封装尺寸



DIM	毫米		
	最小值	标称值	最大值
A	0.80	1.00	1.05
b	0.36	0.41	0.46
c	0.15	0.20	0.25
c1	0.15	0.20	0.25
c2	0.20	0.25	0.30
D1	4.90	5.00	5.10
D2	4.12	4.22	4.32
D3	3.90	4.00	4.10
d	0.20	0.25	0.30
d1	0.085 典型值		
d2	0.319	0.369	0.419
E	4.90	5.00	5.10
E1	5.90	6.00	6.10
E2	3.48	3.58	3.68
e	1.27 典型值		
H	0.36	0.46	0.56
L	0.46	0.56	0.66
L1	0.57	0.67	0.77
θ	0°	—	—
K	1.40 典型值		

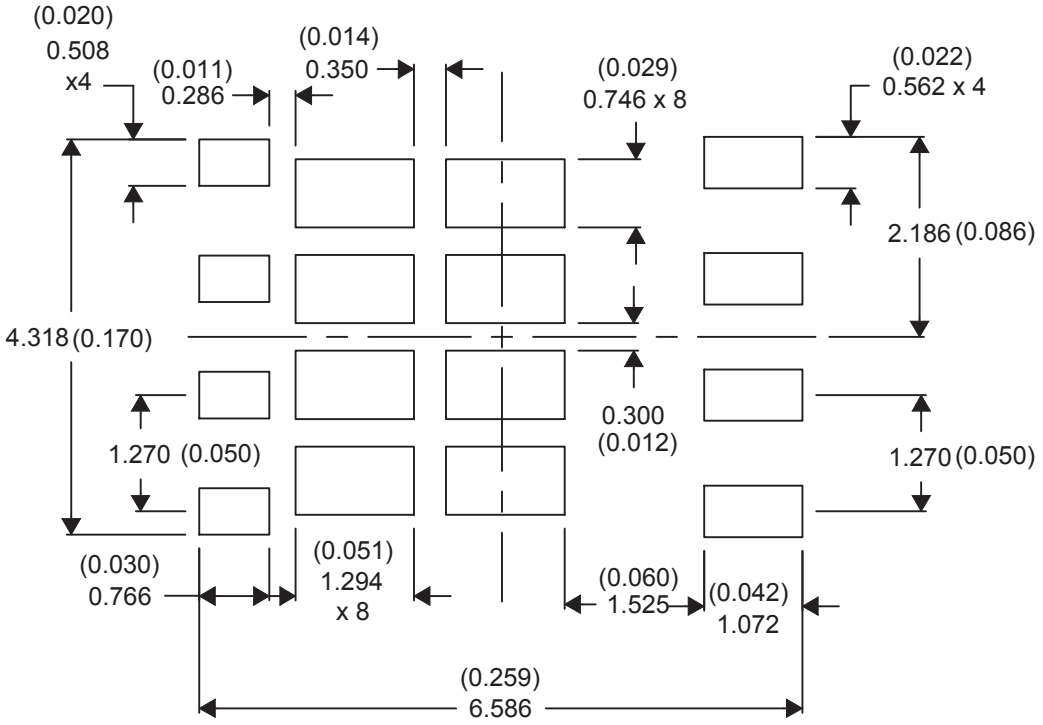
，已将焊盘 3 和 4 之间的尺寸从 0.028 英寸更改为 0.050 英寸

7.2 建议 PCB 布局

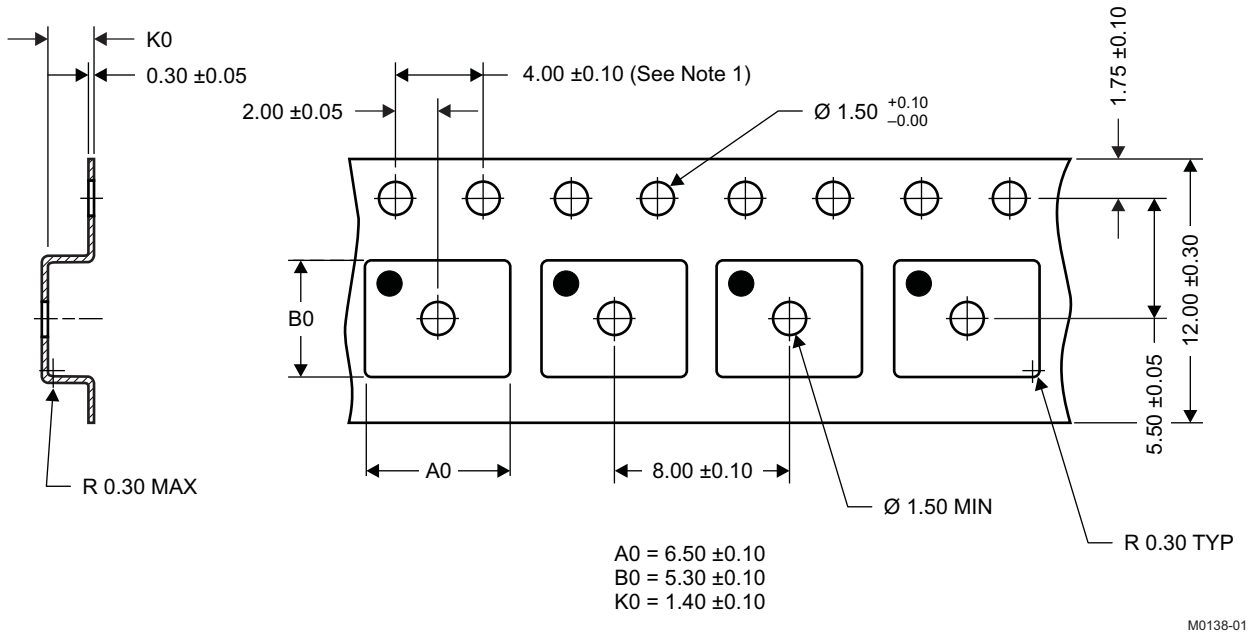


有关针对 PCB 设计的建议电路布局布线，请参见《通过 PCB 布局布线技巧来减少振铃》（文献编号：SLPA005）。

7.3 建议模板布局



7.4 Q5B 卷带信息



注释：

1. 10 链齿孔距累积容差 ±0.2。
2. 每 100mm 长度的翘曲不能超过 1mm，在 250mm 长度上不累积。
3. 材料：黑色抗静电聚苯乙烯。
4. 全部尺寸单位为 mm（除非另外注明）
5. 高于孔眼底部 0.3mm 的平面上测量得到 A0 和 B0 值.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD17573Q5B	Active	Production	VSON-CLIP (DNK) | 8	2500 | LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	CSD17573
CSD17573Q5B.B	Active	Production	VSON-CLIP (DNK) | 8	2500 | LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	CSD17573
CSD17573Q5BG4.B	Active	Production	VSON-CLIP (DNK) | 8	2500 | LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	CSD17573
CSD17573Q5BT	Active	Production	VSON-CLIP (DNK) | 8	250 | SMALL T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	CSD17573
CSD17573Q5BT.B	Active	Production	VSON-CLIP (DNK) | 8	250 | SMALL T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	CSD17573

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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