

30V、N 沟道 NexFET™ 功率 MOSFET

查询样品: [CSD17322Q5A](#)

特性

- 针对 5V 栅极驱动而优化
- 超低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩额定
- 无铅终端镀层
- 符合 RoHS 标准
- 无卤素
- SON 5 毫米 × 6 毫米塑料封装

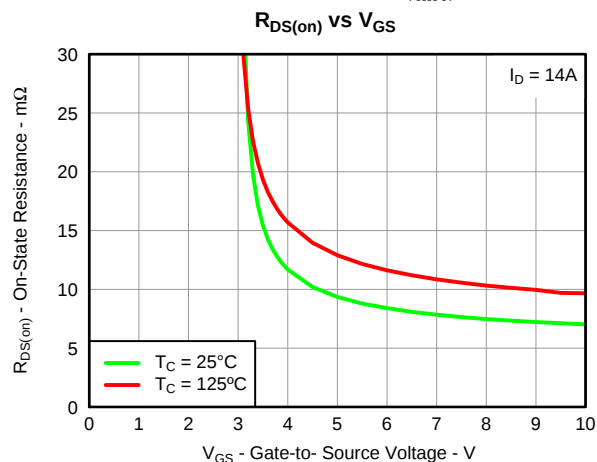
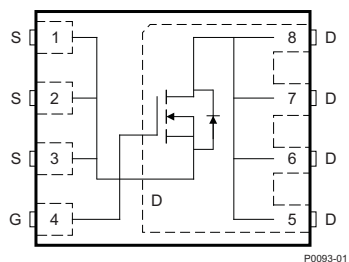
应用

- 笔记本电脑负载点
- 网络、电信和计算系统中的负载点同步降压

说明

此 NexFET™ 功率 MOSFET 专为最大限度地减少功率转换应用中的损耗而设计，并针对 5V 栅极驱动应用进行了优化。

图 1. 顶视图



产品汇总

V_{DS}	漏极至源极电压	30	V
Q_g	总栅极电荷 (4.5V)	3.6	nC
Q_{gd}	栅极电荷 (栅极至漏极)	1.1	nC
$R_{DS(on)}$	漏极至源极导通电阻	$V_{GS} = 4.5\text{V}$	10 mΩ
		$V_{GS} = 8\text{V}$	7.3 mΩ
$V_{GS(th)}$	门限电压	1.6	V

订购信息

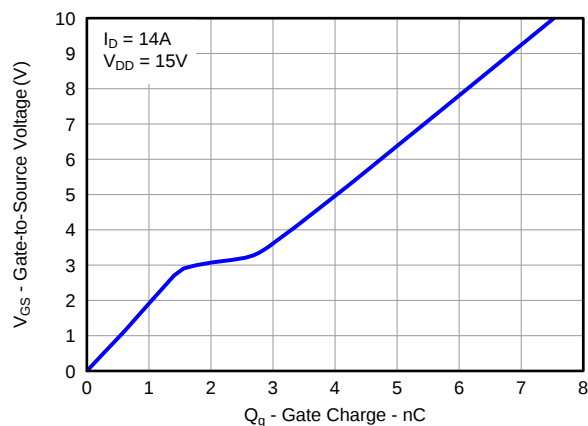
器件	封装	介质	数量	出货
CSD17322Q5A	SON 5 毫米 × 6 毫米塑料封装	13 英寸卷带	2500	卷带封装

最大绝对额定值

$T_A = 25^\circ\text{C}$, 除非另有说明。		数值	单位
V_{DS}	漏极至源极电压	30	V
V_{GS}	漏极至源极电压	+10 / -10	V
I_D	连续漏极电流, $T_C = 25^\circ\text{C}$	87	A
	连续漏极电流 ⁽¹⁾	16	A
I_{AS}	脉冲漏极电流, $T_A = 25^\circ\text{C}$ ⁽²⁾	104	A
P_D	功耗 ⁽¹⁾	3	W
T_J, T_{STG}	工作结温及存储温度范围	-55 至 150	$^\circ\text{C}$
E_{AS}	雪崩能量, 单脉冲 $I_D = 33\text{A}$, $L = 0.1\text{mH}$, $R_G = 25\Omega$	54	mJ

- (1) 典型 $R_{\theta JA} = 41^\circ\text{C/W}$, 在一个 1 英寸² (6.45-cm²)、2 盎司 (0.071-mm 厚) 铜焊盘上, 该焊盘位于一块厚度为 0.06 英寸 (1.52-mm) 的 FR4 PCB 之上。
- (2) 脉冲持续时间 $\leq 300\mu\text{s}$, 占空比 $\leq 2\%$

GATE CHARGE



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NexFET is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2011, Texas Instruments Incorporated
English Data Sheet: [SLPS330](#)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

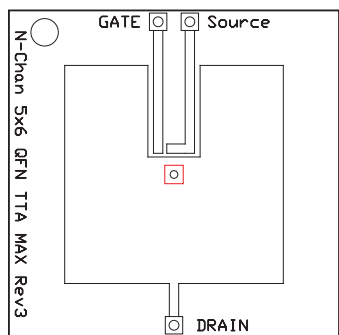
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV _{DSS}	Drain to Source Voltage	V _{GS} = 0V, I _D = 250μA	30			V
I _{DSS}	Drain to Source Leakage Current	V _{GS} = 0V, V _{DS} = 24V			1	μA
I _{GSS}	Gate to Source Leakage Current	V _{DS} = 0V, V _{GS} = +10 / −10V			100	nA
V _{GS(th)}	Gate to Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	1.1	1.6	2.0	V
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 4.5V, I _D = 14A		10	12.4	mΩ
		V _{GS} = 8V, I _D = 14A		7.3	8.8	mΩ
g _{fs}	Transconductance	V _{DS} = 15V, I _D = 14A		37		S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		580	695	pF
C _{oss}	Output Capacitance			390	470	pF
C _{rss}	Reverse Transfer Capacitance			35	44	pF
R _G	Series Gate Resistance			4.7		Ω
Q _g	Gate Charge Total (4.5V)	V _{DS} = 15V, I _D = 14A		3.6	4.3	nC
Q _{gd}	Gate Charge Gate to Drain			1.1		nC
Q _{gs}	Gate Charge Gate to Source			1.6		nC
Q _{g(th)}	Gate Charge at V _{th}			0.9		nC
Q _{oss}	Output Charge	V _{DS} = 13V, V _{GS} = 0V		8.6		nC
t _{d(on)}	Turn On Delay Time	V _{DS} = 15V, V _{GS} = 4.5V, I _{DS} = 14A, R _G = 2Ω		6.7		ns
t _r	Rise Time			12		ns
t _{d(off)}	Turn Off Delay Time			10.5		ns
t _f	Fall Time			3.7		ns
Diode Characteristics						
V _{SD}	Diode Forward Voltage	I _{SD} = 14A, V _{GS} = 0V	0.85		1	V
Q _{rr}	Reverse Recovery Charge	V _{DD} = 13V, I _F = 14A, di/dt = 300A/μs	19.6			nC
t _{rr}	Reverse Recovery Time		17.8			ns

THERMAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

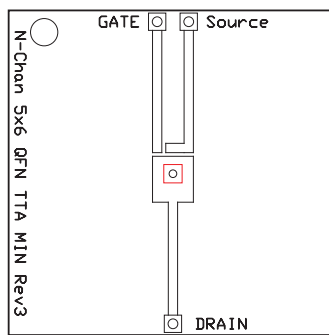
PARAMETER		MIN	TYP	MAX	UNIT
R _{θJC}	Thermal Resistance Junction to Case ⁽¹⁾			1.8	°C/W
R _{θJA}	Thermal Resistance Junction to Ambient ⁽¹⁾⁽²⁾			51	°C/W

- (1) R_{θJC} is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. R_{θJC} is specified by design, whereas R_{θJA} is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



M0137-01

Max $R_{\theta JA} = 51^\circ\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of
2-oz. (0.071-mm thick)
Cu.

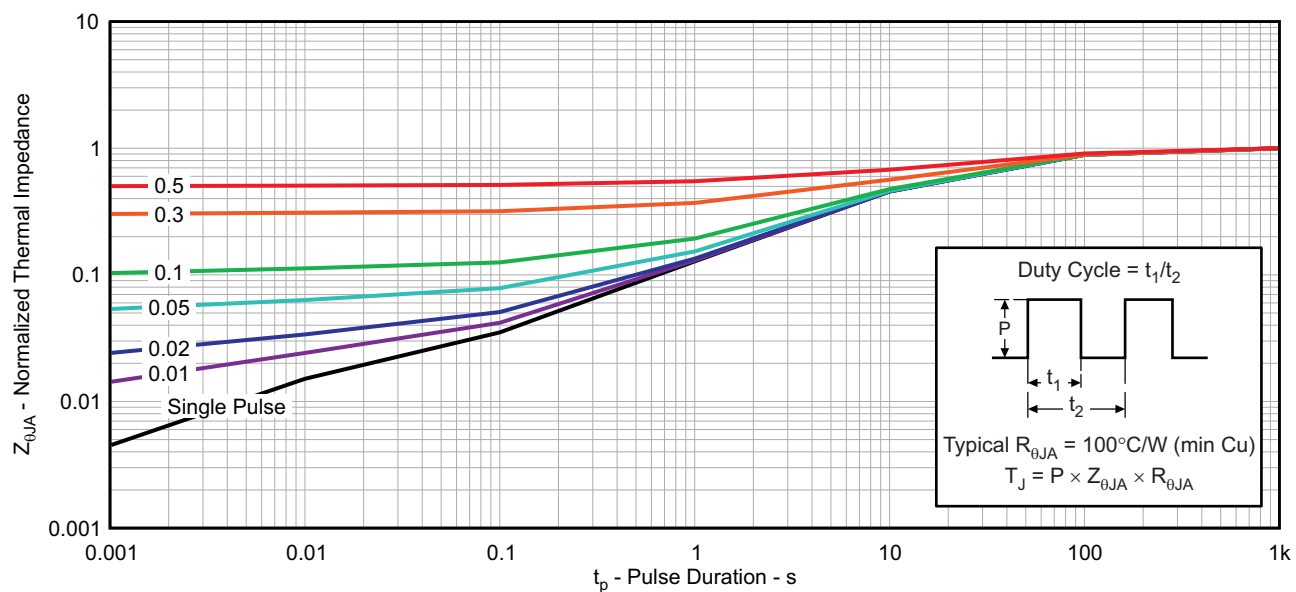


M0137-02

Max $R_{\theta JA} = 125^\circ\text{C/W}$
when mounted on a
minimum pad area of
2-oz. (0.071-mm thick)
Cu.

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)



G012

Figure 2. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

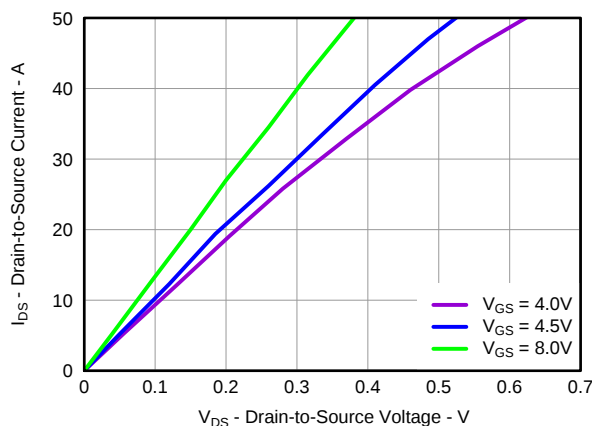


Figure 3. Saturation Characteristics

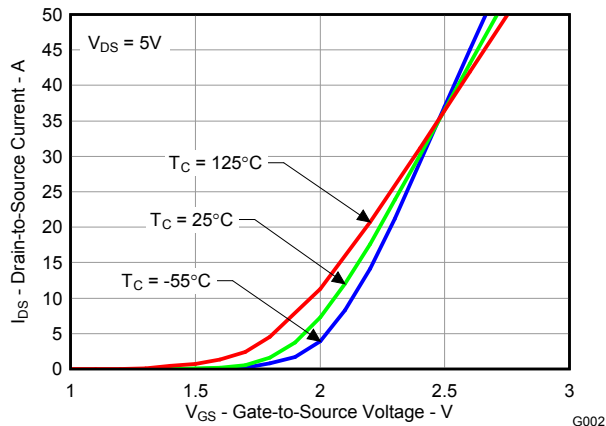


Figure 4. Transfer Characteristics

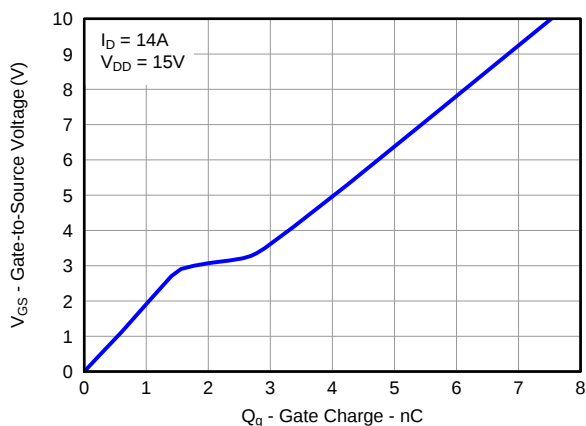


Figure 5. Gate Charge

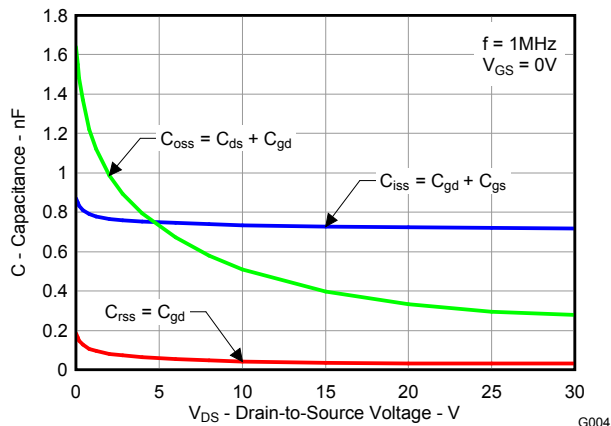


Figure 6. Capacitance

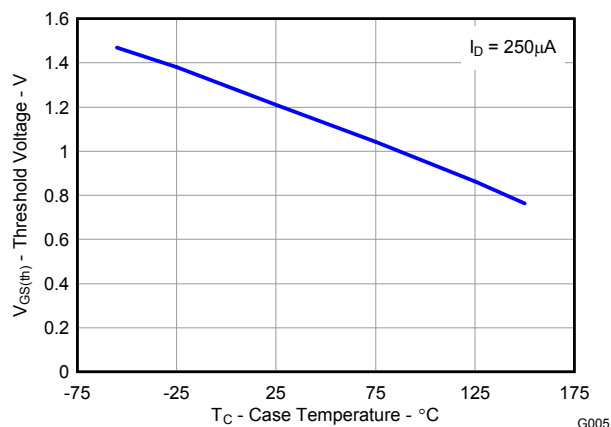


Figure 7. Threshold Voltage vs. Temperature

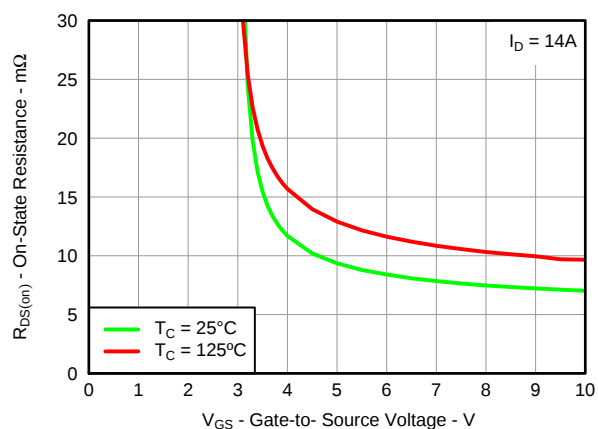


Figure 8. On-State Resistance vs. Gate-to-Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

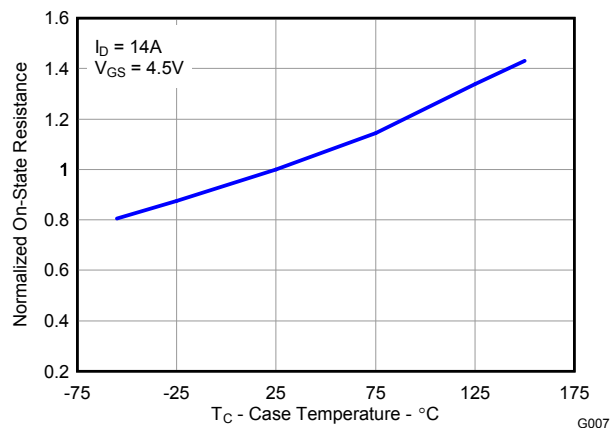


Figure 9. Normalized On-State Resistance vs. Temperature

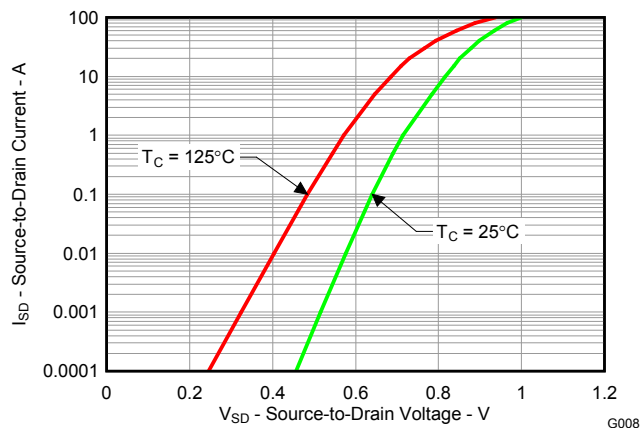


Figure 10. Typical Diode Forward Voltage

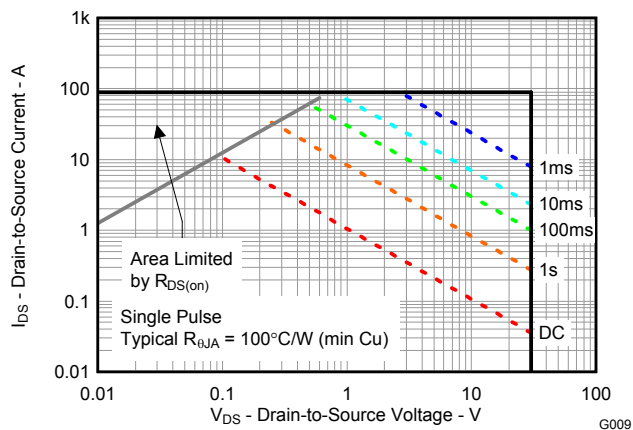


Figure 11. Maximum Safe Operating Area

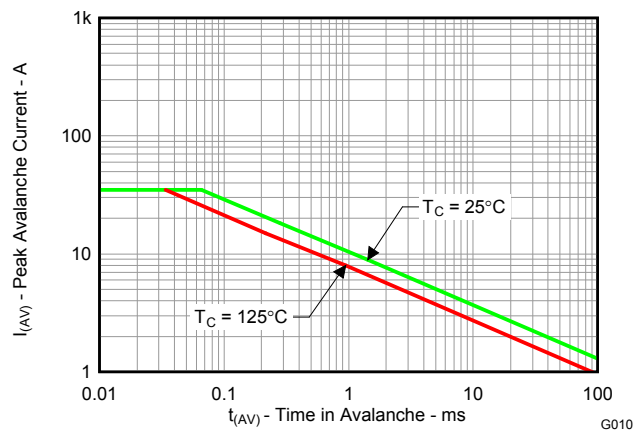


Figure 12. Single Pulse Unclamped Inductive Switching

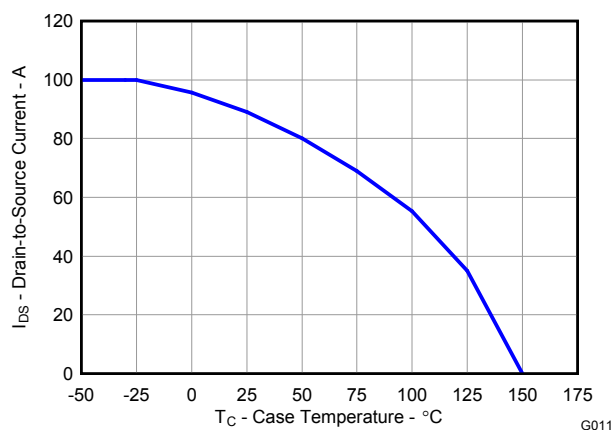
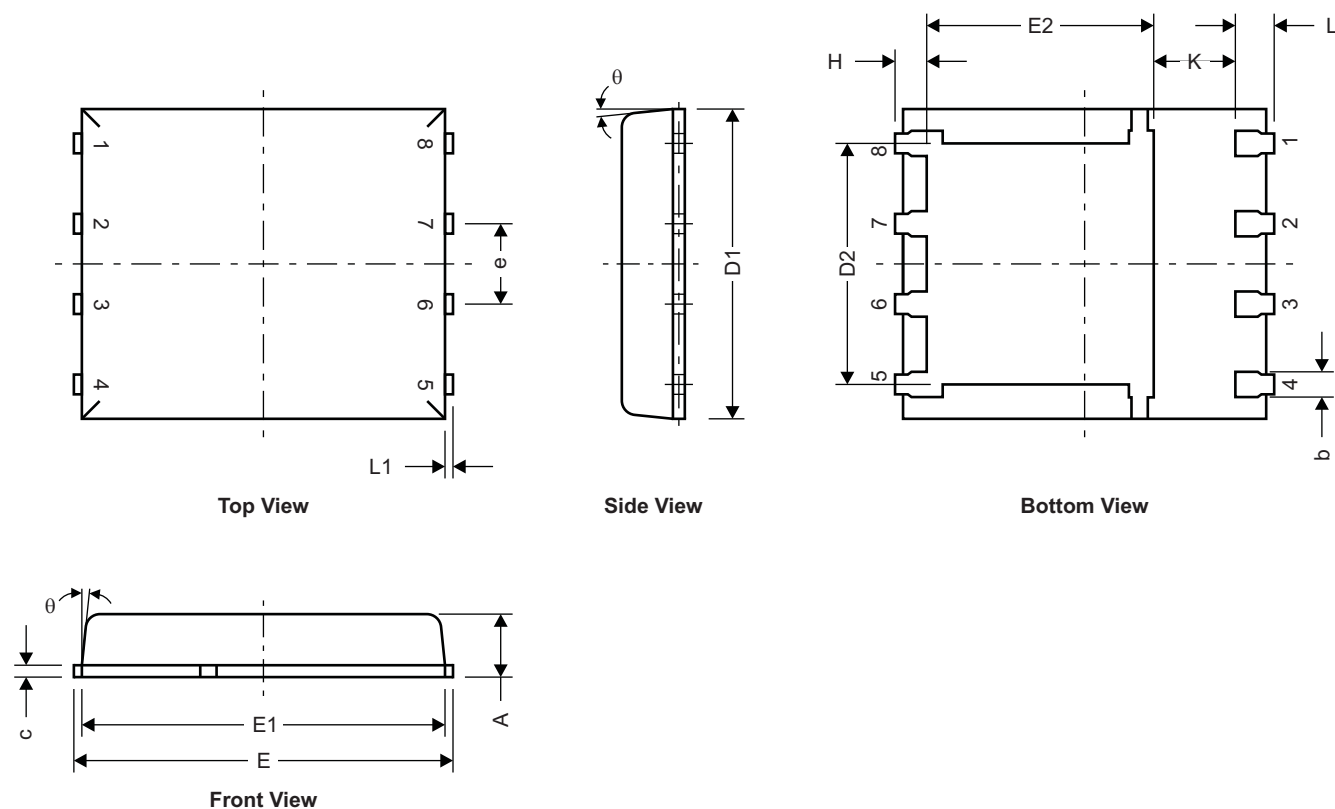


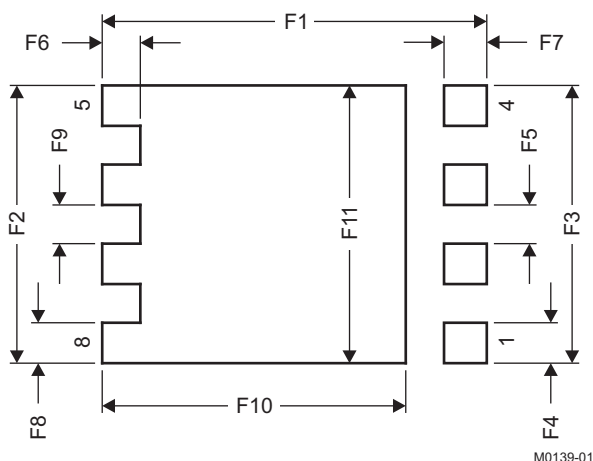
Figure 13. Maximum Drain Current vs. Temperature

MECHANICAL DATA**Q5A Package Dimensions**

M0135-01

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.34
D1	4.80	4.90	5.00
D2	3.61	3.81	4.02
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.17	1.27	1.37
H	0.41	0.56	0.71
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
θ	0°		12°

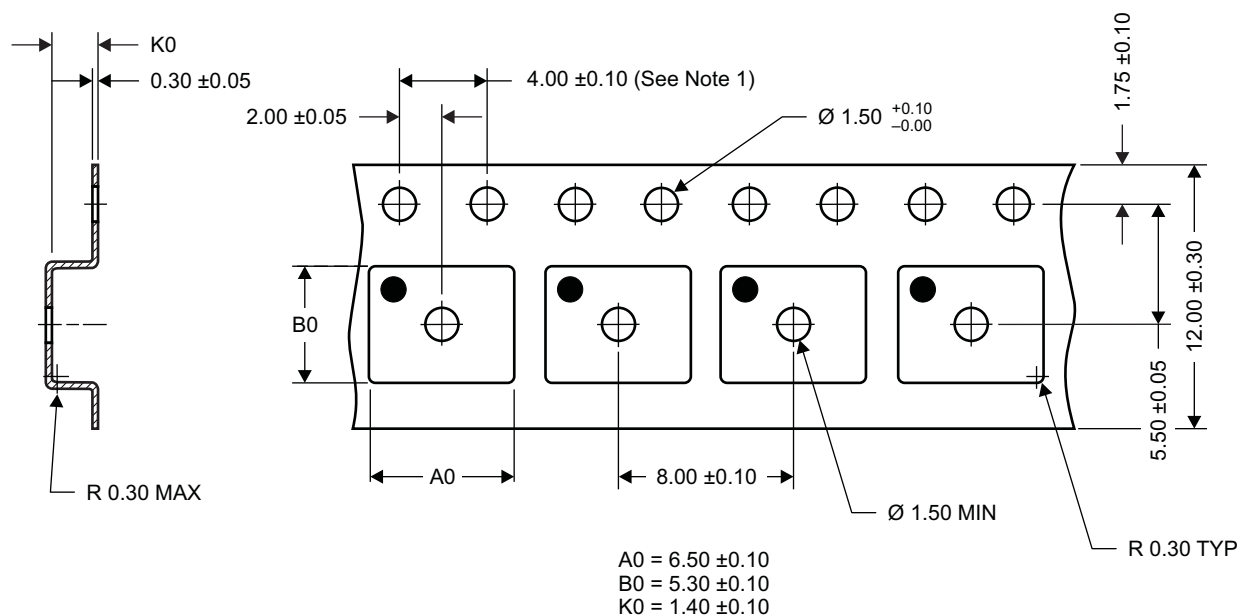
Figure 14. Recommended PCB Pattern



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

Q5A Tape and Reel Information



M0138-01

Notes:

- 10-sprocket hole-pitch cumulative tolerance ± 0.2
- Camber not to exceed 1mm in 100mm, noncumulative over 250mm
- Material: black static-dissipative polystyrene
- All dimensions are in mm (unless otherwise specified)
- A0 and B0 measured on a plane 0.3mm above the bottom of the pocket

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD17322Q5A	Active	Production	VSONP (DQJ) 8	2500 LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17322
CSD17322Q5A.B	Active	Production	VSONP (DQJ) 8	2500 LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17322

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

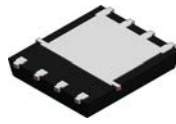
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

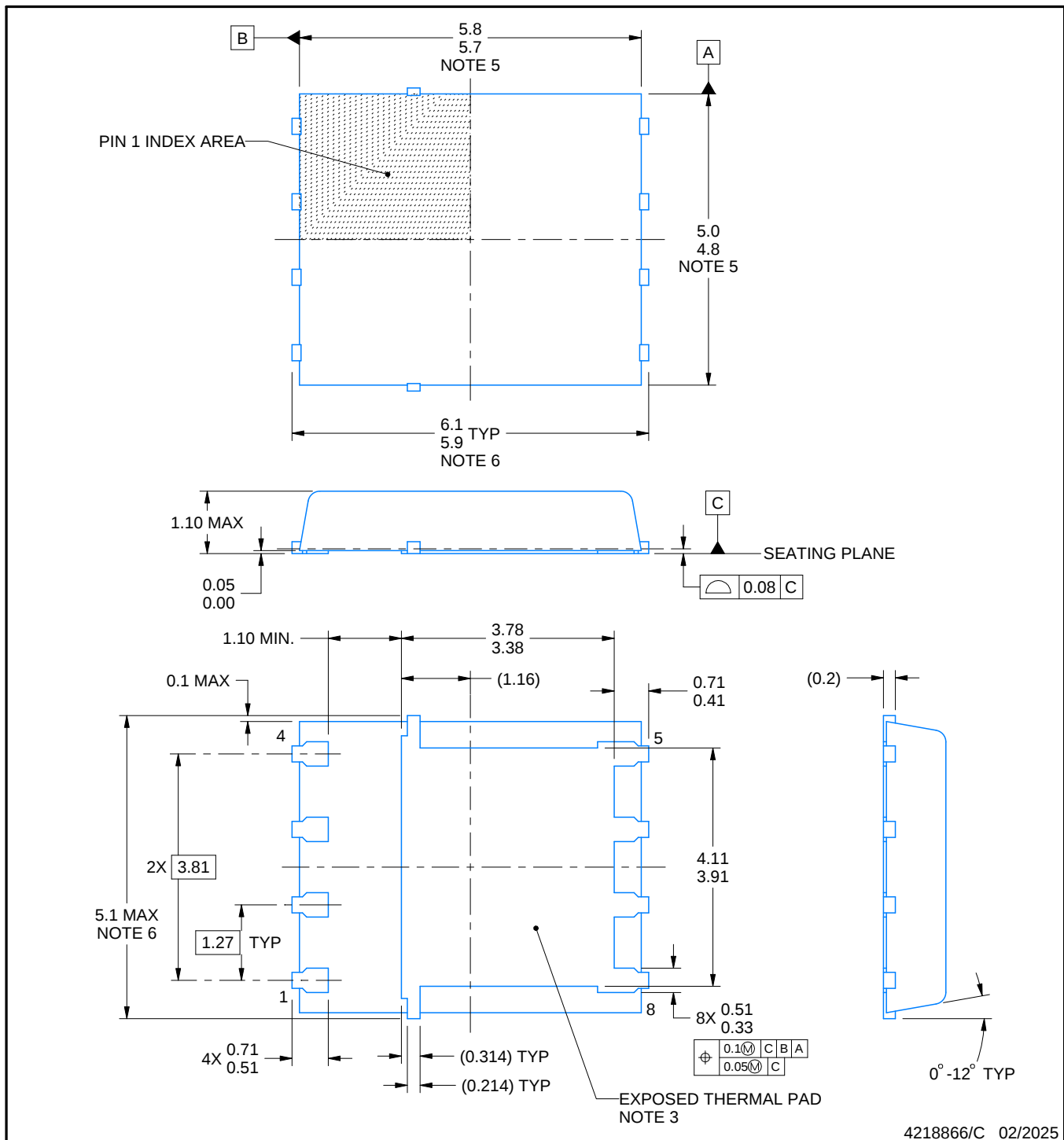
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DQJ0008A**PACKAGE OUTLINE****VSONP - 1.1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



4218866/C 02/2025

NOTES:

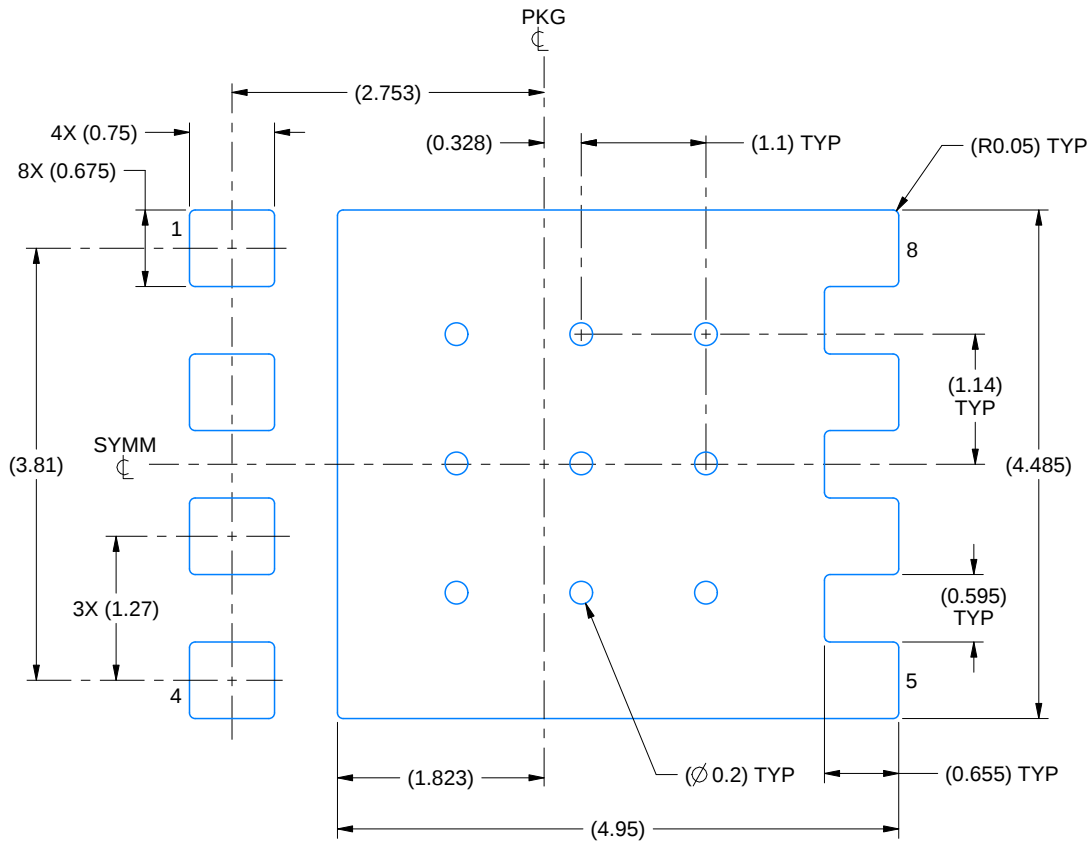
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Metalized features are supplier options and may not be on the package.
5. These dimensions do not include mold flash protrusions or gate burrs.
6. These dimensions include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25 mm per side.

EXAMPLE BOARD LAYOUT

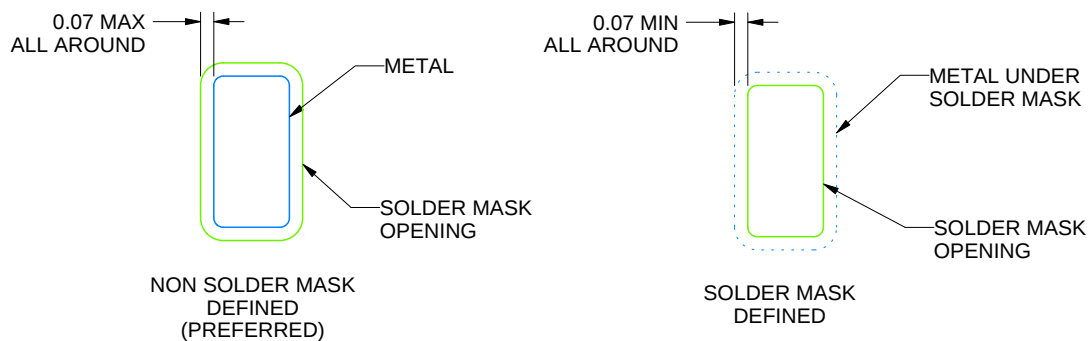
DQJ0008A

VSONP - 1.1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE: 15X



SOLDER MASK DETAILS

4218866/C 02/2025

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).

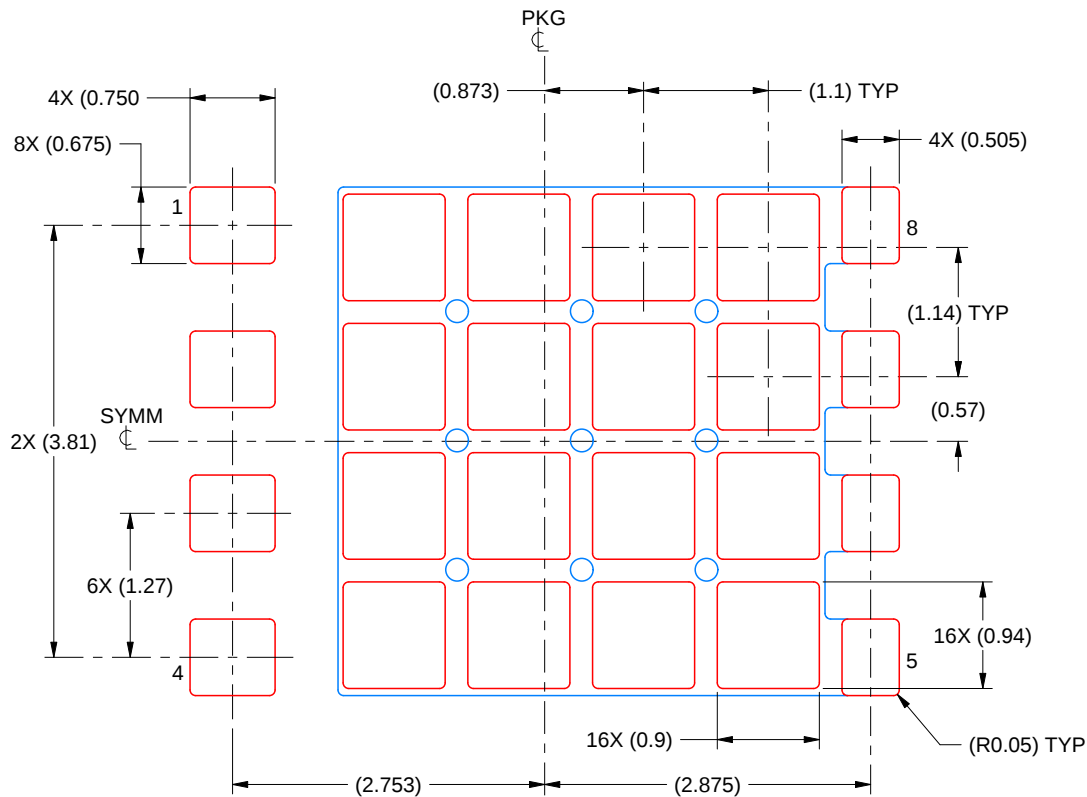
8. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DQJ0008A

VSONP - 1.1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD:
70% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 15X

4218866/C 02/2025

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
版权所有 © 2025，德州仪器 (TI) 公司