CSD17313Q2Q1 30V N 沟道 NexFET™ 功率 MOSFET

1 特性

- 符合汽车应用 应用
- 针对 5V 栅极驱动器进行了优化
- 超低 Q_g 和 Q_{gd}
- 低热阻
- 无铅
- 符合 RoHS 环保标准
- 无卤素
- 小外形尺寸无引线 (SON) 2mm x 2mm 塑料封装

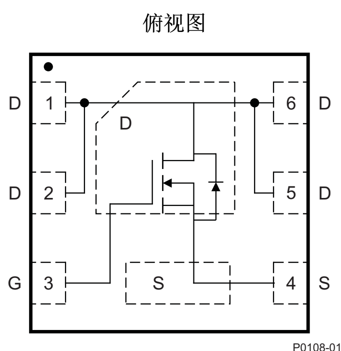
2 应用

- 直流/直流转换器
- 电池和负载管理

3 说明

该 30V、24mΩ、2mm x 2mm SON NexFET™功率 MOSFET 旨在用于最大程度降低功率转换应用中的 并针对 5V 栅极驱动器应用进行了优化 应用中， 2mm x 2mm SON 针对封装尺寸提供了出色的散热性能。

俯视图



产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	30		V
Q_g	总栅极电荷 (4.5V)	2.1		nC
Q_{gd}	栅极电荷（栅极到漏极）	0.4		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 3V	31	mΩ
		V_{GS} = 4.5V	26	mΩ
		V_{GS} = 8V	24	mΩ
$V_{GS(th)}$	阈值电压	1.3		V

订购信息(1)

器件编号	数量	包装介质	封装	发货
CSD17313Q2Q1	3000	13 英寸卷带	SON 2mm × 2mm 塑料封装	卷带封装
CSD17313Q2Q1T	250	7 英寸卷带		

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

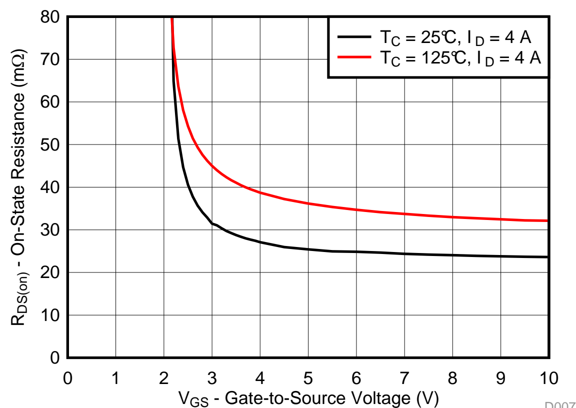
绝对最大额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	30	V
V_{GS}	栅源电压	+10 / –8	V
I_D	持续漏极电流（受封装限制）	5	A
	持续漏极电流（受器件限制），T_C = 25°C	19	
	持续漏极电流(1)	7.3	
I_{DM}	脉冲漏极电流，T_A = 25°C(2)	57	A
P_D	功率耗散(1)	2.4	W
	功率耗散，T_C = 25°C	17	
T_J，T_{STG}	运行结温和储存温度范围	–55 至 150	°C
E_{AS}	雪崩能量，单一脉冲，I_D=19A，L=0.1mH，R_G=25Ω	18	mJ

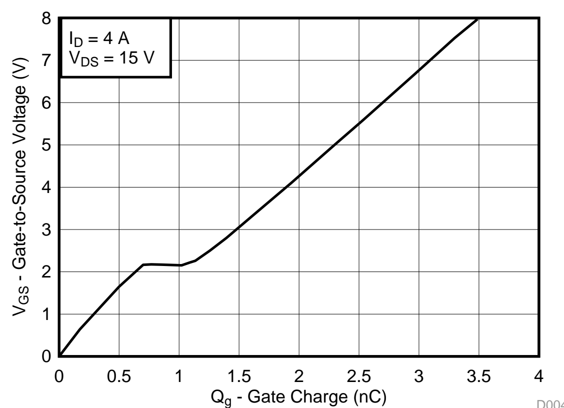
(1) $R_{θJA}$ = 53°C/W，这是在 0.06 英寸厚 FR4 PCB 上的 1 平方英寸 2 盎司的铜焊盘上测得的典型值。

(2) 最大 $R_{θJC}$ = 7.4°C/W，脉冲持续时间 ≤ 100μs，占空比 ≤ 1%。

导通电阻与源极电压



栅极电荷



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (March 2013) to Revision D	Page
• 改进了 说明	1
• 向*订购信息* 表中添加了 7 英寸卷带	1
• 更新了持续漏极电流	1
• 更新了脉冲电流条件	1
• Updated Figure 1 to show $R_{\theta JC}$ curves	4
• Added V_{GS} = 4.5 V line in Figure 8	5
• Updated the SOA in Figure 10	6
• 添加了*器件和文档* 部分。	9

Changes from Revision B (January 2013) to Revision C	Page
• Changed Figure 10, Maximum Safe Operating Area	5

Changes from Revision A (November 2012) to Revision B	Page
• 更改了建议的 PCB 布局	9
• 添加了建议的模版布局	9

Changes from Original (October 2012) to Revision A	Page
• 将器件编号从 CSD17313Q2-Q1 更改成了 CSD17313Q2Q1	1

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5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 μA	30			V
I_{DSS}	Drain-to-source leakage	V_{GS} = 0 V, V_{DS} = 24 V			1	μA
I_{GSS}	Gate-to-source leakage	V_{DS} = 0 V, V_{GS} = +10 / -8 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 μA	0.9	1.3	1.8	V
$R_{DS(on)}$	Drain-to-source on resistance	V_{GS} = 3 V, I_D = 4 A		31	42	mΩ
		V_{GS} = 4.5 V, I_D = 4 A		26	32	mΩ
		V_{GS} = 8 V, I_D = 4 A		24	30	mΩ
g_{fs}	Transconductance	V_{DS} = 15 V, I_D = 4 A		16		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 15 V, ƒ = 1 MHz		260	340	pF
C_{oss}	Output capacitance			140	180	pF
C_{rss}	Reverse transfer capacitance			13	17	pF
R_G	Series gate resistance			1.3	2.6	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 15 V, I_D = 4 A		2.1	2.7	nC
Q_{gd}	Gate charge – gate-to-drain			0.4		nC
Q_{gs}	Gate charge – gate-to-source			0.7		nC
$Q_{g(th)}$	Gate charge at Vth			0.3		nC
Q_{oss}	Output charge	V_{DS} = 13.5 V, V_{GS} = 0 V		3.8		nC
$t_{d(on)}$	Turn on delay time	V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 4 A, R_G = 2 Ω		2.8		ns
t_r	Rise time			3.9		ns
$t_{d(off)}$	Turn off delay time			4.2		ns
t_f	Fall time			1.3		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 4 A, V_{GS} = 0V		0.85	1	V
Q_{rr}	Reverse recovery charge	V_{DD}= 13.5 V, I_F = 4 A, di/dt = 300 A/μs		6.4		nC
t_{rr}	Reverse recovery time			12.9		ns

5.2 Thermal Information

T_A = 25°C (unless otherwise noted)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal resistance junction-to-case[1]			7.4	°C/W
$R_{\theta JA}$	Thermal resistance junction-to-ambient[1][2]			67	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071=mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.

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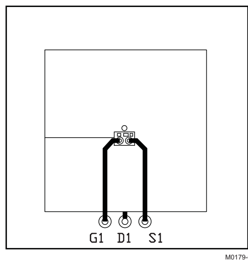
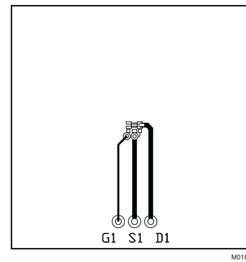


Max $R_{\theta JA}$ = 67°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2 oz. (0.071 mm thick) Cu.



Max $R_{\theta JA}$ = 228°C/W when mounted on a minimum pad area of 2 oz. (0.071 mm thick) Cu.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise noted)

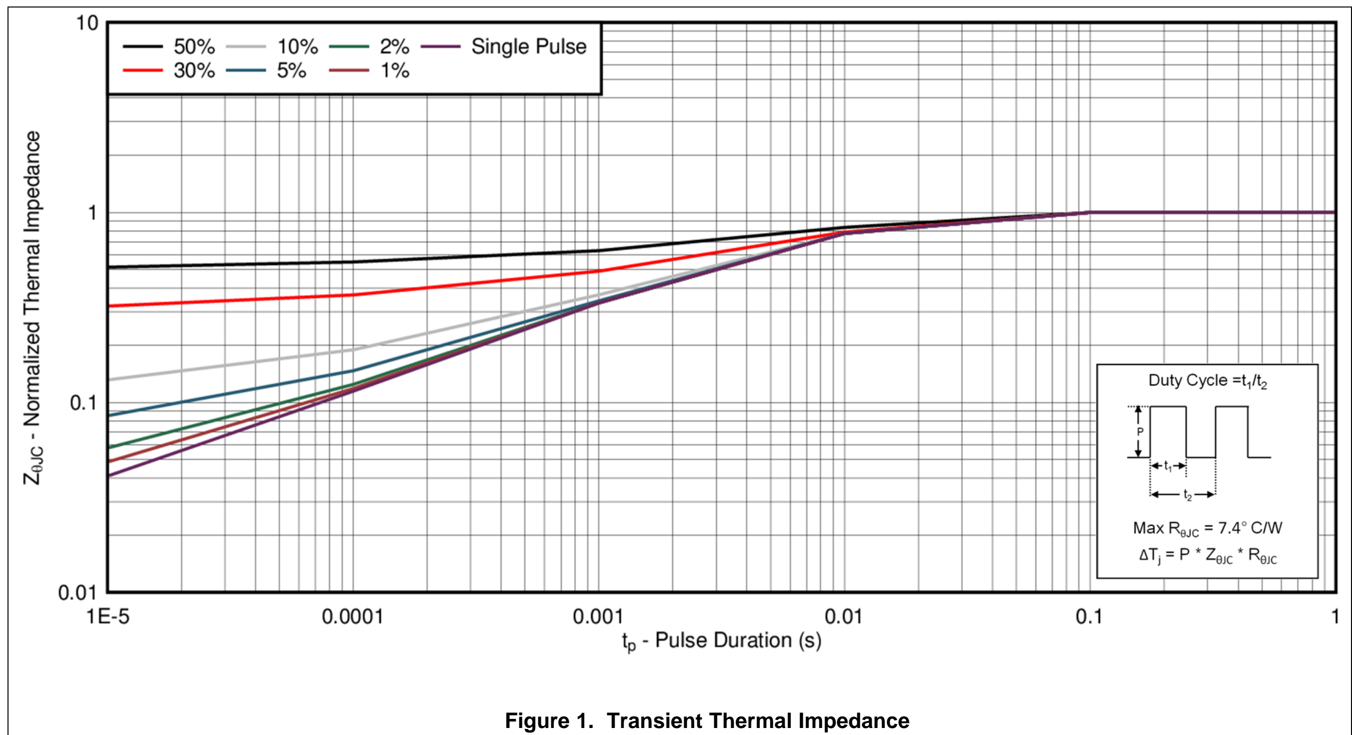


Figure 1. Transient Thermal Impedance

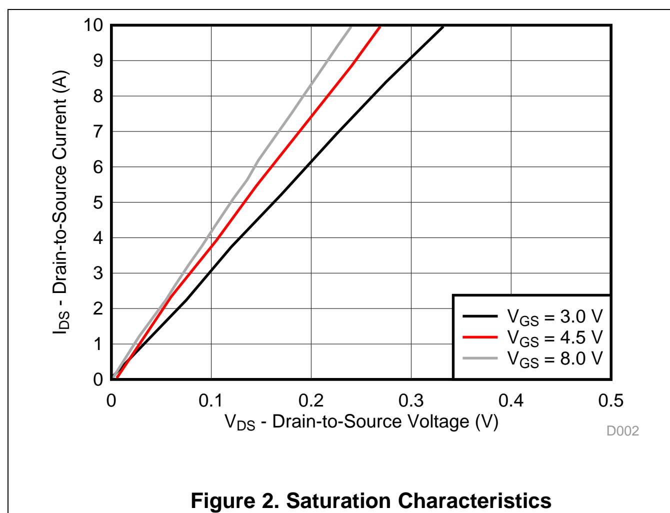


Figure 2. Saturation Characteristics

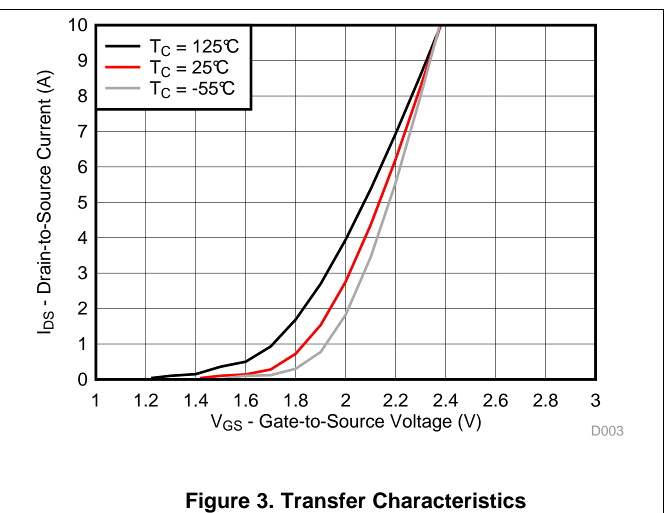


Figure 3. Transfer Characteristics

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Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise noted)

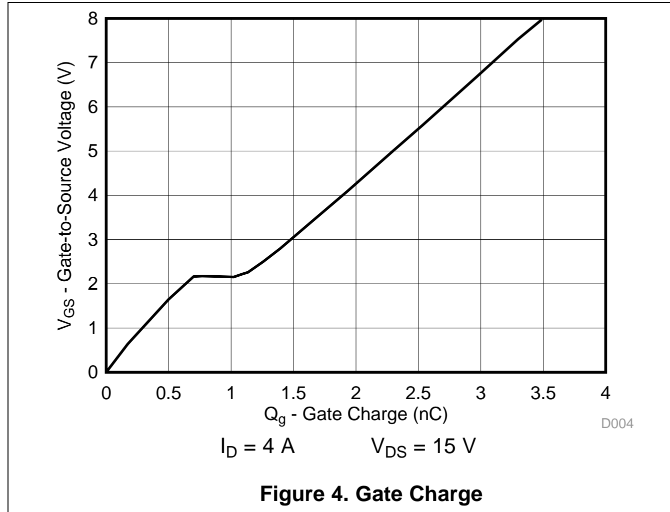

Figure 4. Gate Charge

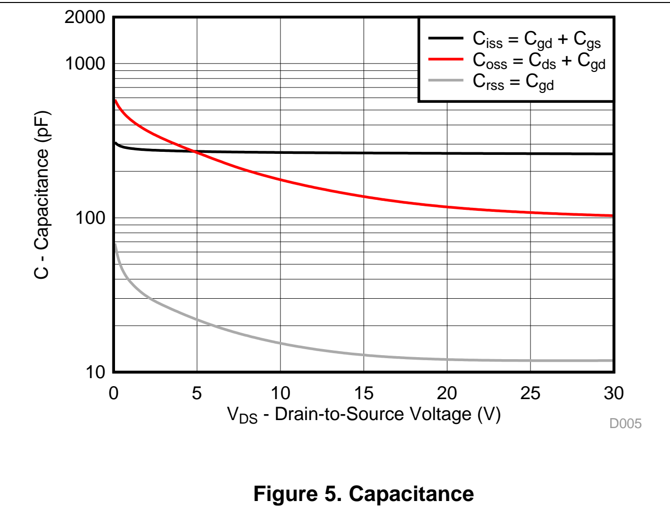

Figure 5. Capacitance

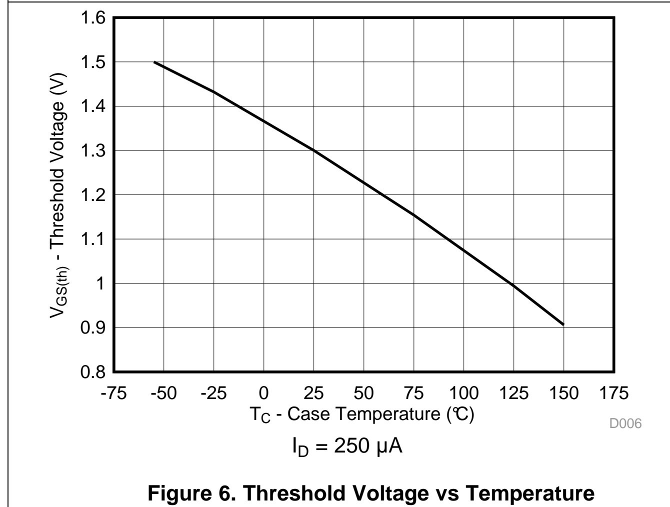

Figure 6. Threshold Voltage vs Temperature

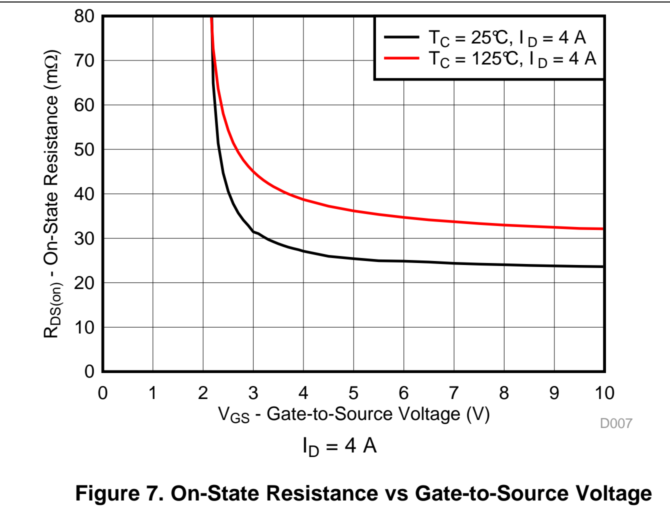

Figure 7. On-State Resistance vs Gate-to-Source Voltage

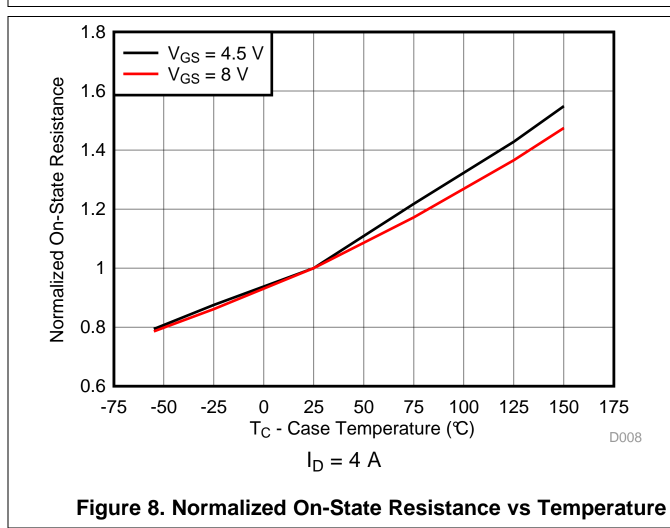

Figure 8. Normalized On-State Resistance vs Temperature

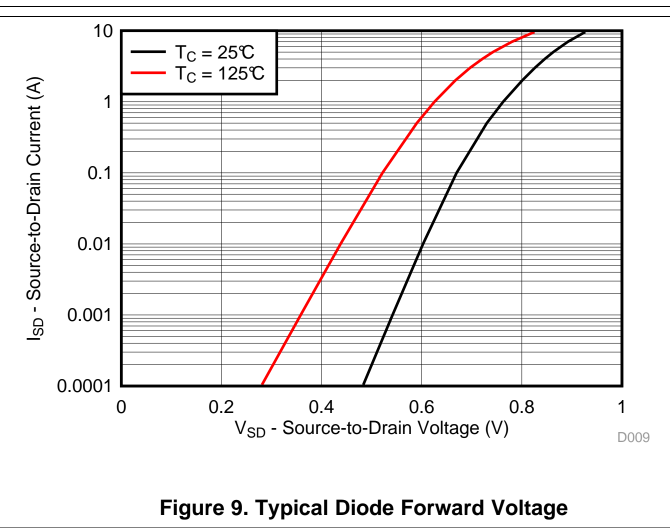

Figure 9. Typical Diode Forward Voltage

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Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise noted)

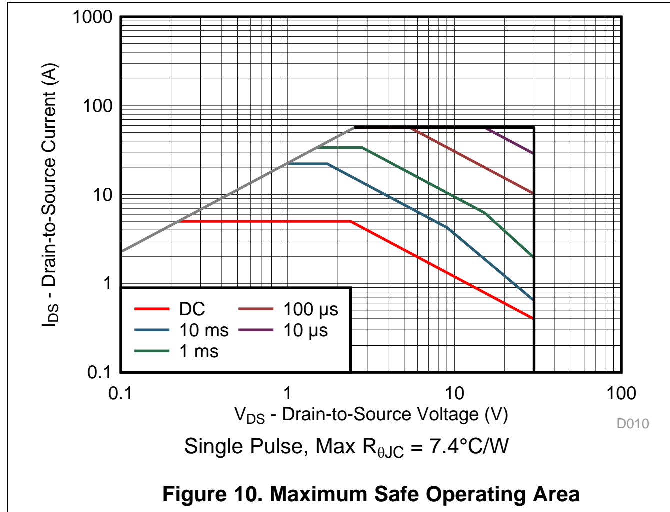

Figure 10. Maximum Safe Operating Area

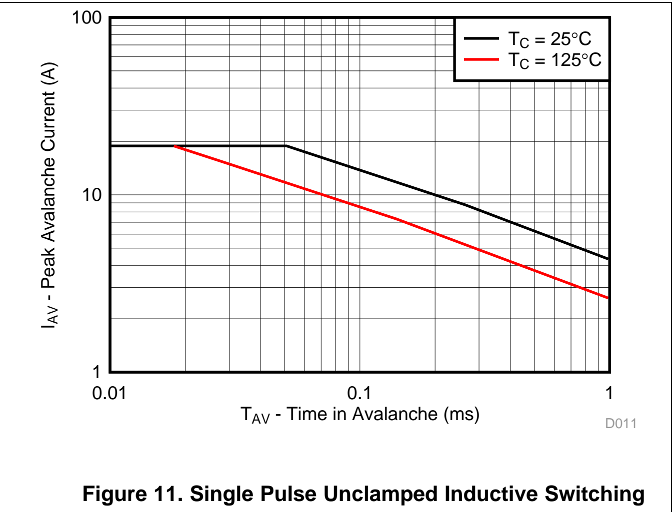

Figure 11. Single Pulse Unclamped Inductive Switching

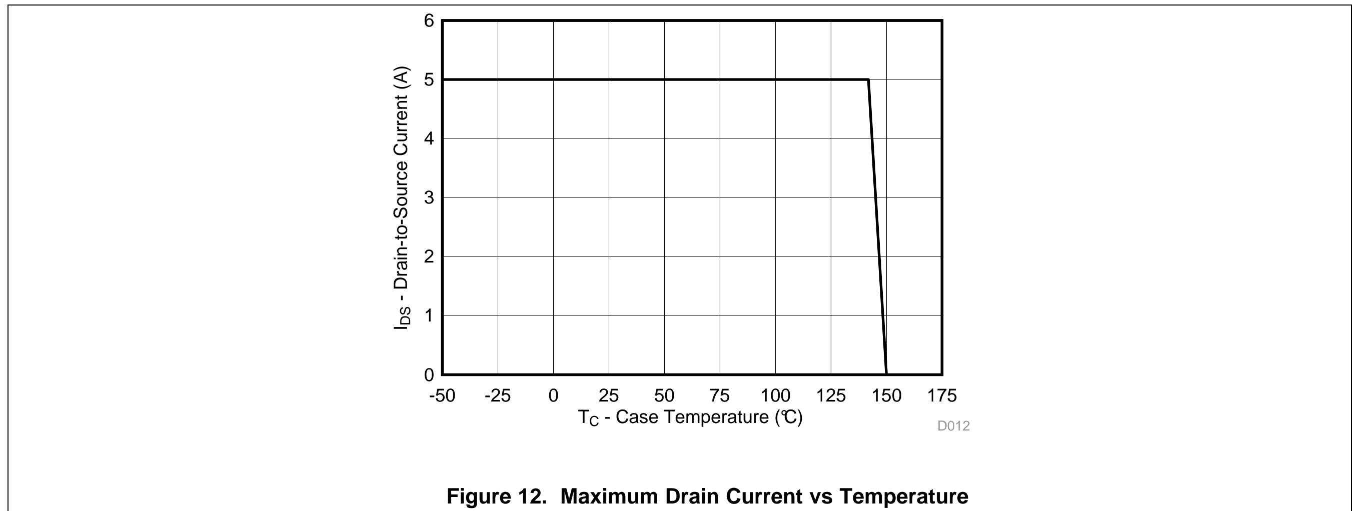

Figure 12. Maximum Drain Current vs Temperature

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6 器件和文档支持

6.1 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

6.2 商标

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All other trademarks are the property of their respective owners.

6.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

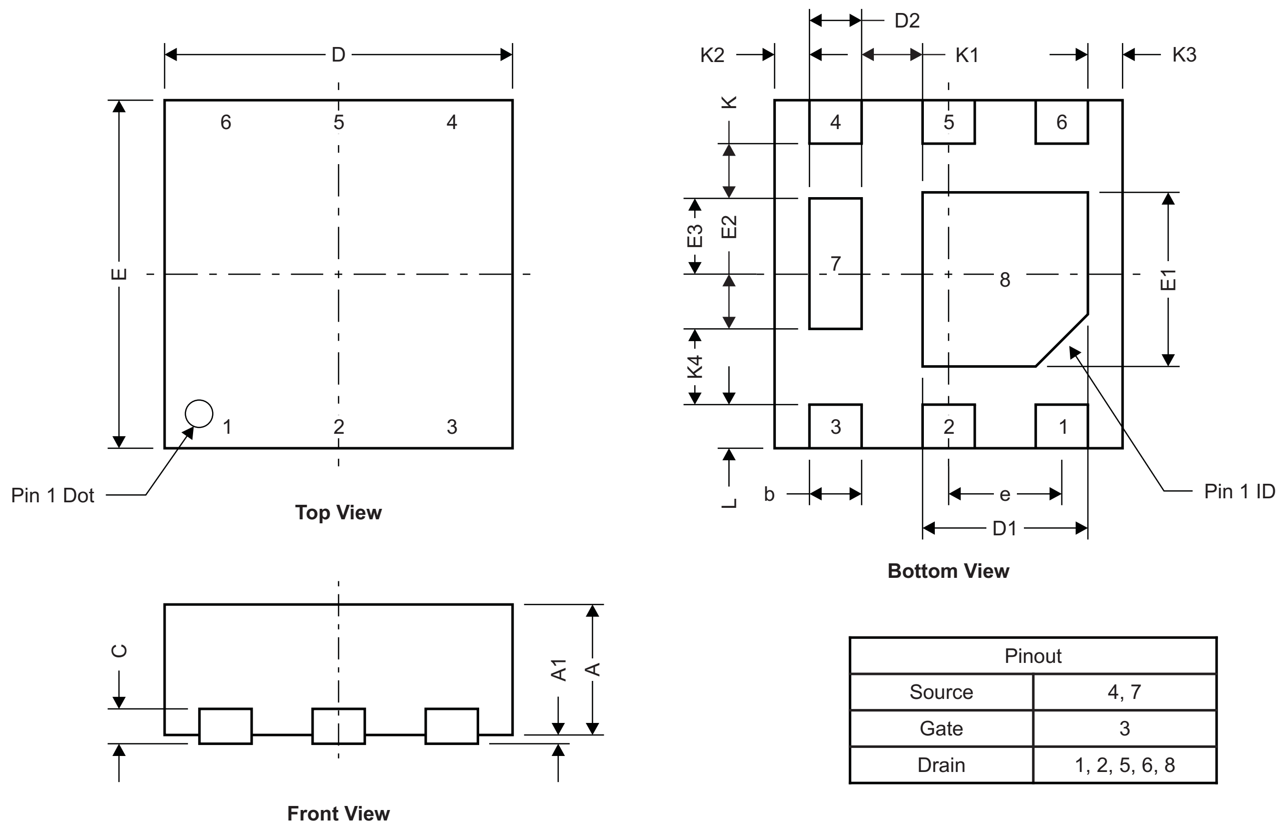
6.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 机械、封装和可订购信息

7.1 Q2 封装尺寸



DIM	毫米			英寸		
	最小值	标称值	最大值	最小值	标称值	最大值
A	0.700	0.750	0.800	0.028	0.030	0.032
A1	0.000		0.050	0.000		0.002
b	0.250	0.300	0.350	0.010	0.012	0.014
C		0.203 典型值			0.008 典型值	
D		2.000 典型值			0.080 典型值	
D1	0.900	0.950	1.000	0.036	0.038	0.040
D2		0.300 典型值			0.012 典型值	
E		2.000 典型值			0.080 典型值	
E1	0.900	1.000	1.100	0.036	0.040	0.044
E2		0.280 典型值			0.0112 典型值	
E3		0.470 典型值			0.0188 典型值	
e		0.650 BSC			0.026 典型值	
K		0.280 典型值			0.0112 典型值	
K1		0.350 典型值			0.014 典型值	
K2		0.200 典型值			0.008 典型值	
K3		0.200 典型值			0.008 典型值	
K4		0.470 典型值			0.0188 典型值	
L	0.200	0.25	0.300	0.008	0.010	0.012

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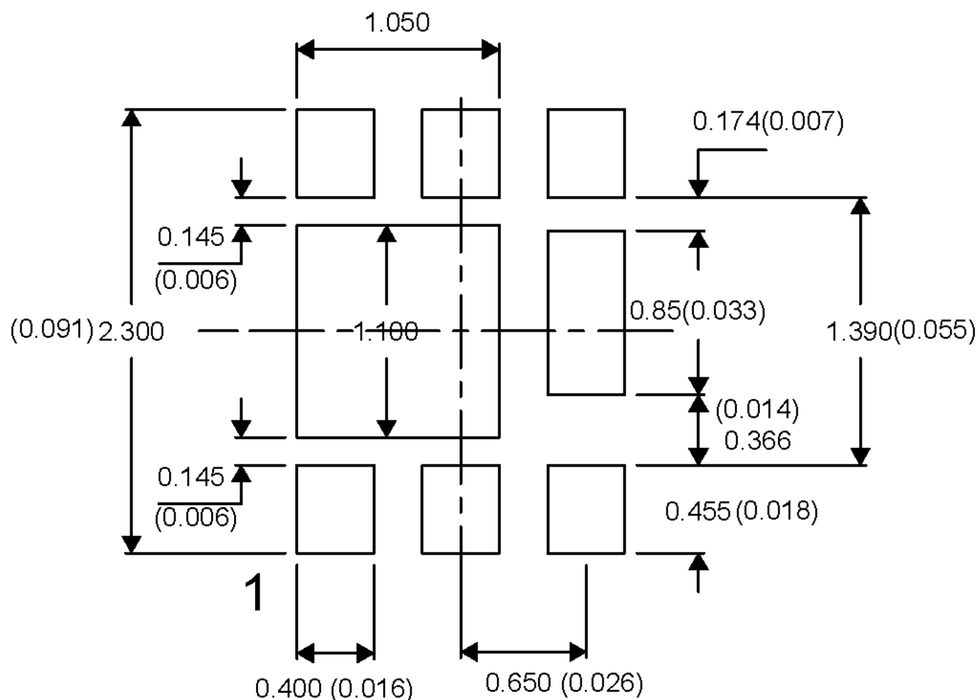
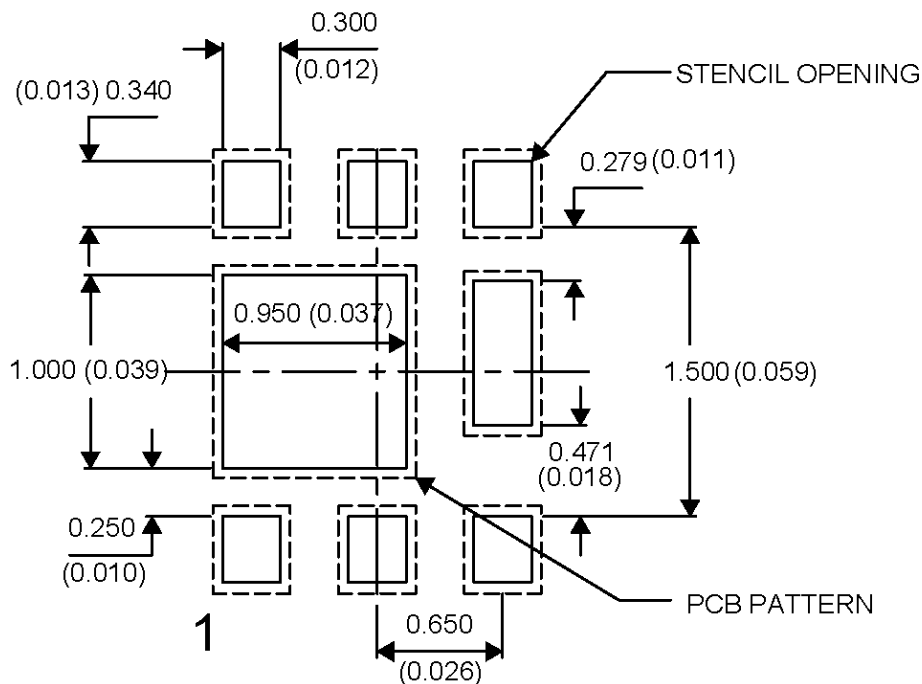
7.2 建议 PCB 布局



如需了解针对 PCB 设计的建议电路布局，请参阅应用手册《*通过 PCB 布局技巧来减少振铃*》，（SLPA005）。

7.3 建议的模版布局



Note: 全部尺寸单位为 mm，除非另外注明。

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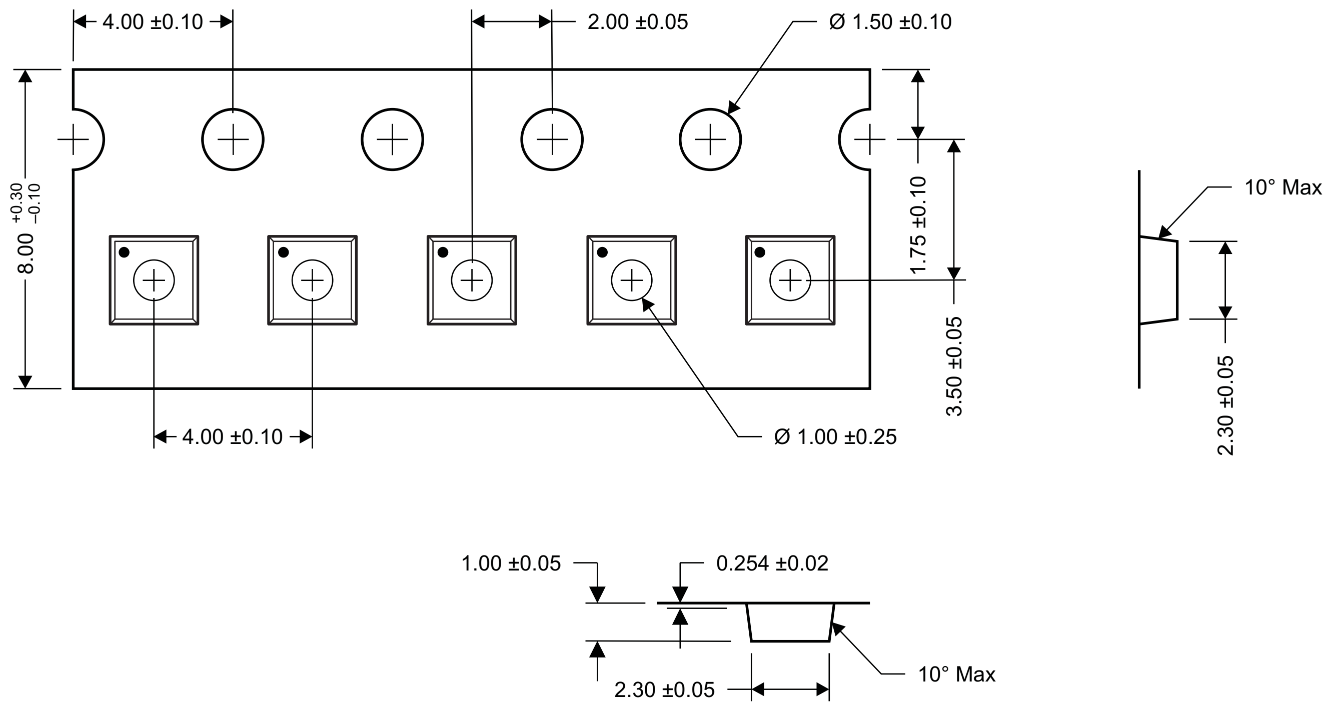
7.4 Q2 卷带信息



Notes:
1. 测自链齿孔中心线到孔眼中心线
2. 10 个链齿孔的累积容差为 ±0.20
3. 其他材料可用
4. 卷带的 SR 典型值最大为 10^8 OHM/SQ
5. 除非另有说明，否则所有尺寸单位均为 mm。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17313Q2Q1T	OBSOLETE	WSON	DQK	6		TBD	Call TI	Call TI	0 to 0	733Q	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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