CSD17308Q3 30V N 沟道 NexFET™ 功率 MOSFET

1 特性

- 针对 5V 栅极驱动器进行了优化
- 超低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩级
- 无铅端子镀层
- 符合 RoHS
- 无卤素
- VSON 3.3mm × 3.3mm 塑料封装

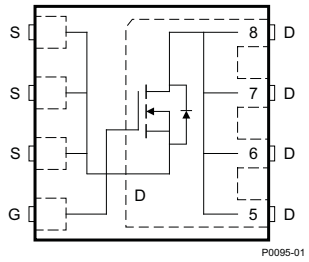
2 应用

- 笔记本电脑负载点
- 网络、电信和计算系统的负载点同步降压

3 说明

此 30V、8.2mΩ、3.3mm × 3.3mm VSON NexFET™ 功率 MOSFET 旨在用于最大程度降低功率转换 应用中的损耗并针对 5V 栅极驱动器 应用进行了优化。

俯视图



产品概要

T_A = 25°C		值	单位
V_{DS}	漏源电压	30	V

产品概要 (接下页)

T_A = 25°C		值		单位
Q_g	栅极电荷总量 (4.5V)	3.9		nC
Q_{gd}	栅极电荷（栅极到漏极）	0.8		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 3V	12.5	mΩ
		V_{GS} = 4.5V	9.4	
		V_{GS} = 8V	8.2	
$V_{GS(th)}$	阈值电压	1.3		V

器件信息(1)

器件	数量	包装介质	封装	配送
CSD17308Q3	2500	13 英寸卷带	SON 3.30mm × 3.30mm 塑料封装	卷带封装

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

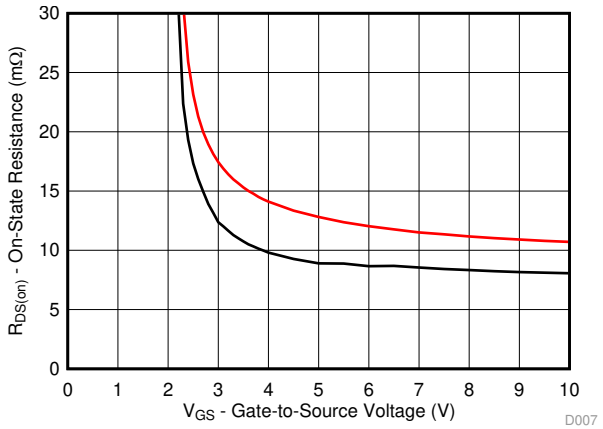
绝对最大额定值

T_A = 25°C 时测得，除非另外注明		值	单位
V_{DS}	漏源电压	30	V
V_{GS}	栅源电压	+10 / –8	V
I_D	持续漏极电流（受封装限制）	50	A
	持续漏极电流，T_C = 25°C	44	
	持续漏极电流(1)	14	
I_{DM}	脉冲漏极电流，T_A = 25°C(2)	167	A
P_D	功耗(1)	2.7	W
	功率耗散，T_C = 25°C	28	
T_J, T_{stg}	工作结温和贮存温度	–55 至 150	°C
E_{AS}	雪崩能量，单脉冲 I_D = 36A，L = 0.1mH，R_G = 25Ω	65	mJ

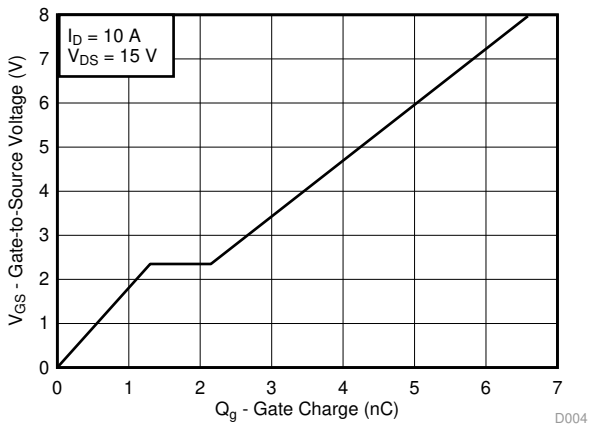
(1) 典型 $R_{\theta JA}$ = 46°C/W（当在 0.06 英寸 (1.52mm) 厚的 FR4 PCB 上将其安装在 1 平方英寸 (6.45cm²) 2oz (0.071mm) 厚的铜焊盘上时）。

(2) 最大 $R_{\theta JC}$ = 4.5°C/W，脉冲持续时间 ≤ 100µs，占空比 ≤ 1%。

$R_{DS(on)}$ 与 V_{GS} 对比



栅极电荷



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (October 2015) to Revision C **Page**

- Changed $V_{GS(th)}$ MAX specification in the *Electrical Characteristics* table, From 1.8 V : To 1.6 V ... 3

Changes from Revision A (February 2010) to Revision B **Page**

- 已添加 向标题中添加了部件编号 ... 1
- 已添加 受封装限制的持续漏极电流 ... 1
- 已添加 在*绝对最大额定值* 表格中添加了“功率耗散，T_C = 25°C”行 ... 1
- 更新了脉冲电流条件 ... 1
- Updated Figure 1 to show $R_{\theta JC}$ curves ... 5
- Added 4.5 V curve in Figure 8 ... 6
- Updated Figure 10 ... 7
- 已添加 添加了*器件和文档支持* 部分 ... 8
- 更新了机械、封装和可订购信息部分 ... 9

Changes from Original (February 2010) to Revision A **Page**

- 已删除 删除了“封装标记信息”部分 ... 11

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5 Specifications

5.1 Electrical Characteristics

T_A = 25°C unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 μA	30			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 24 V			1	μA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = +10 / –8 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 μA	0.9	1.3	1.6	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 3 V, I_D = 10 A		12.5	16.5	mΩ
		V_{GS} = 4.5 V, I_D = 10 A		9.4	11.8	
		V_{GS} = 8 V, I_D = 10 A		8.2	10.3	
g_{fs}	Transconductance	V_{DS} = 15 V, I_D = 10 A		37		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input capacitance	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		540	700	pF
C_{OSS}	Output capacitance			280	365	pF
C_{RSS}	Reverse transfer capacitance			27	35	pF
R_g	Series gate resistance			0.9	1.8	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 15 V, I_D = 10 A		3.9	5.1	nC
Q_{gd}	Gate charge gate-to-drain			0.8		nC
Q_{gs}	Gate charge gate-to-source			1.3		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.7		nC
Q_{OSS}	Output charge	V_{DS} = 13 V, V_{GS} = 0 V		7.4		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 10 A, R_G = 2 Ω		4.5		ns
t_r	Rise time			5.7		ns
$t_{d(off)}$	Turnoff delay time			9.9		ns
t_f	Fall time			2.3		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{DS} = 10 A, V_{GS} = 0 V		0.85	1	V
Q_{rr}	Reverse recovery charge	V_{DD} = 13 V, I_F = 10 A, di/dt = 300 A/μs		9.3		nC
t_{rr}	Reverse recovery time			14.3		ns

5.2 Thermal Information

T_A = 25°C unless otherwise stated

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance (1)			4.5	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1) (2)			58	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.

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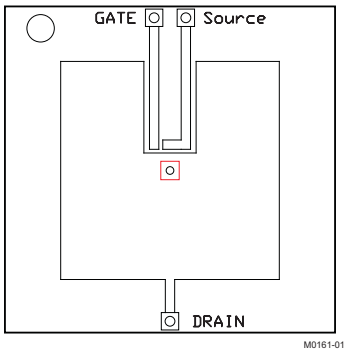
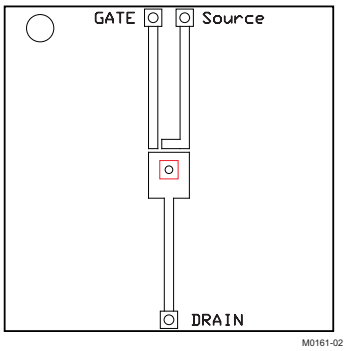


Max $R_{\theta JA}$ = 58°C/W when mounted on 1 in^2 (6.45 cm^2) of 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 165°C/W when mounted on a minimum pad area of 2-oz (0.071-mm) thick) Cu.

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5.3 Typical MOSFET Characteristics

T_A = 25°C unless otherwise stated

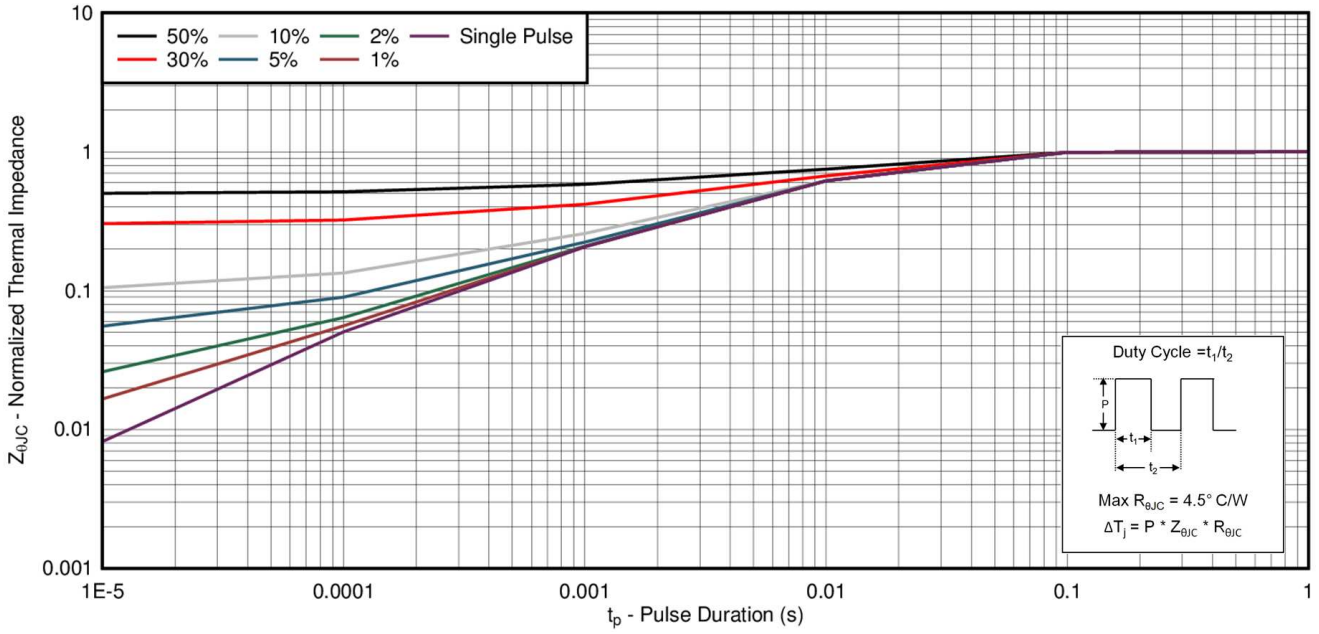

Figure 1. Transient Thermal Impedance

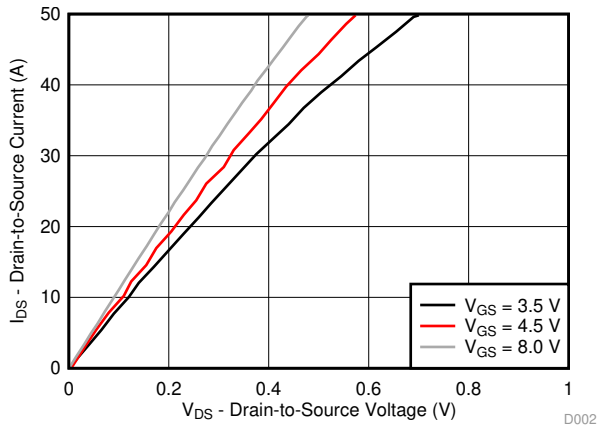

Figure 2. Saturation Characteristics

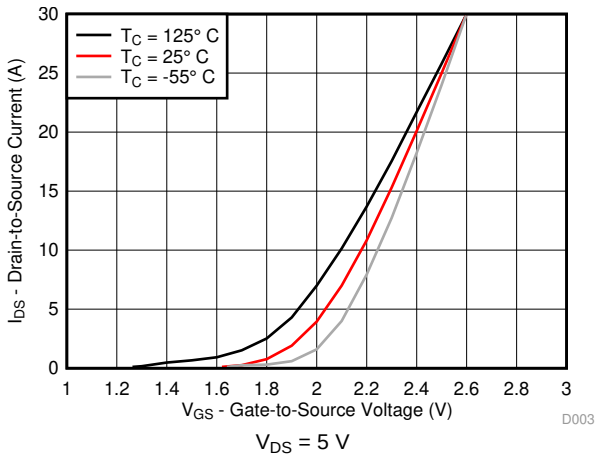

Figure 3. Transfer Characteristics

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Typical MOSFET Characteristics (continued)

T_A = 25°C unless otherwise stated

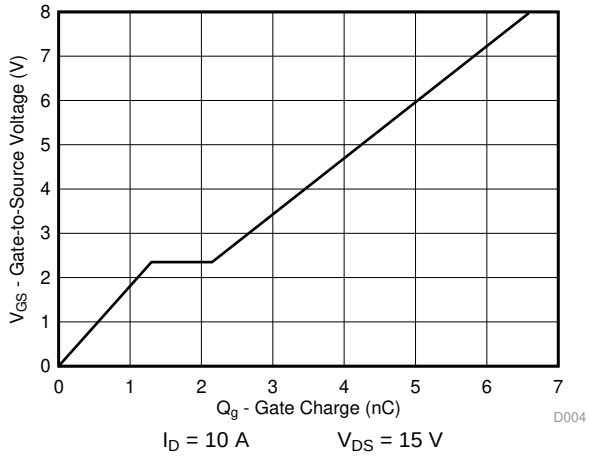

Figure 4. Gate Charge

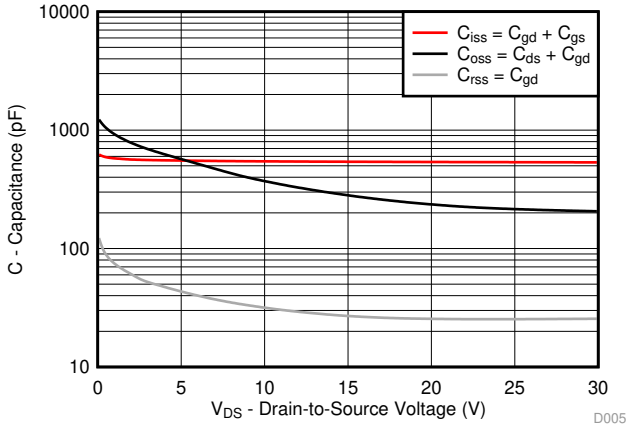

Figure 5. Capacitance

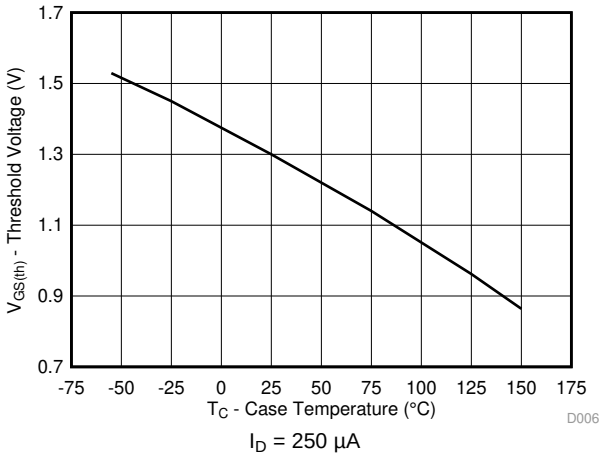

Figure 6. Threshold Voltage vs Temperature

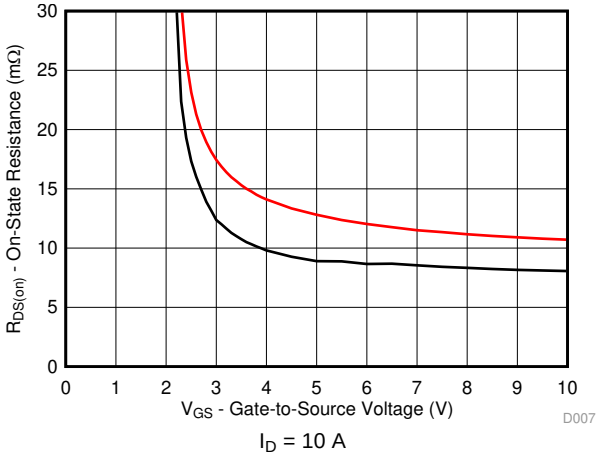

Figure 7. On-State Resistance vs Gate-to-Source Voltage

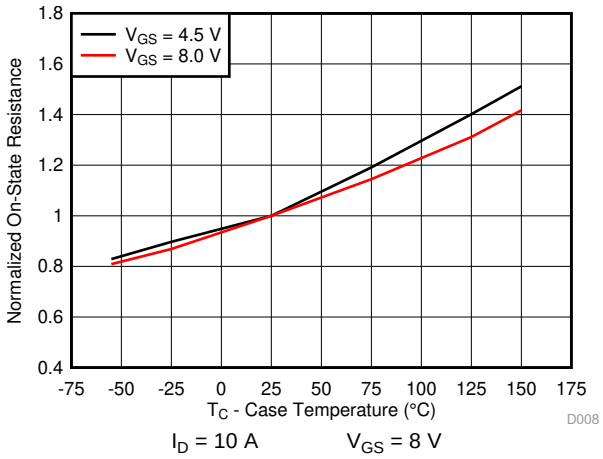

Figure 8. Normalized On-State Resistance vs Temperature

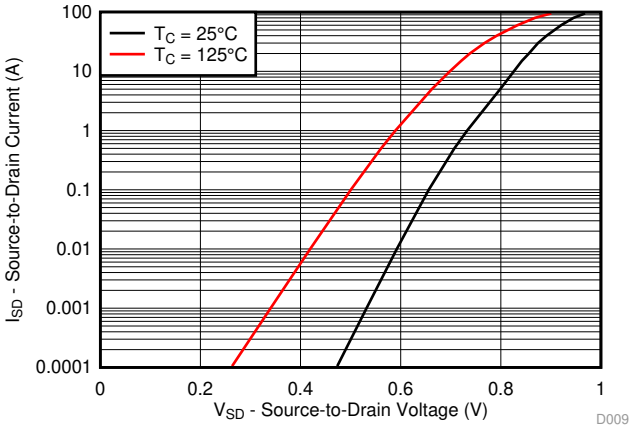

Figure 9. Typical Diode Forward Voltage

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Typical MOSFET Characteristics (continued)

T_A = 25°C unless otherwise stated

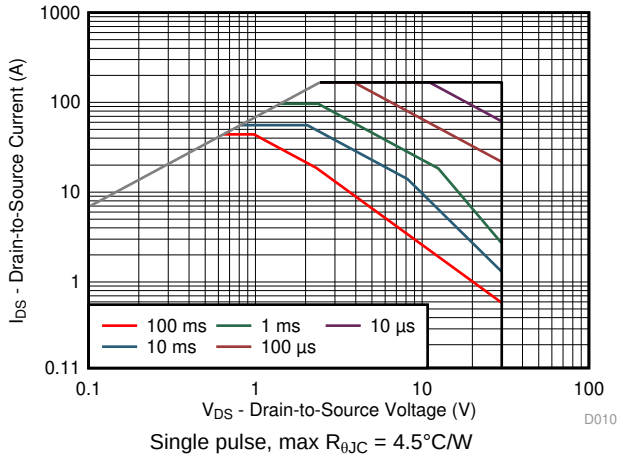

Figure 10. Maximum Safe Operating Area

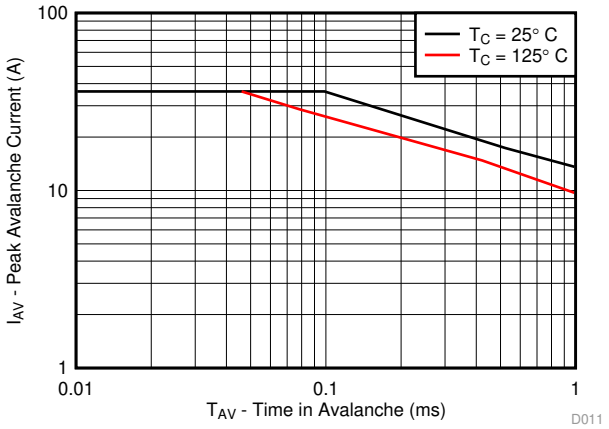

Figure 11. Single Pulse Unclamped Inductive Switching

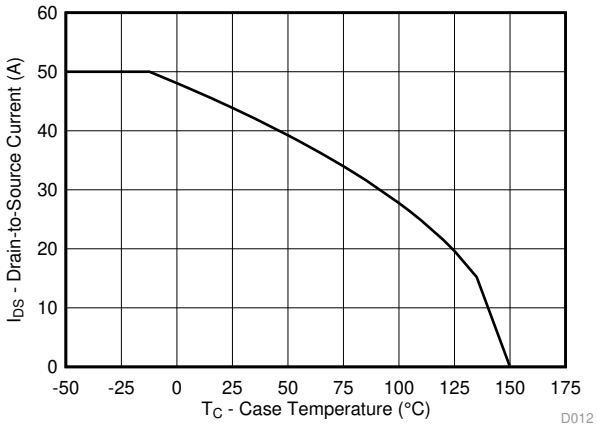

Figure 12. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6.2 商标

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6.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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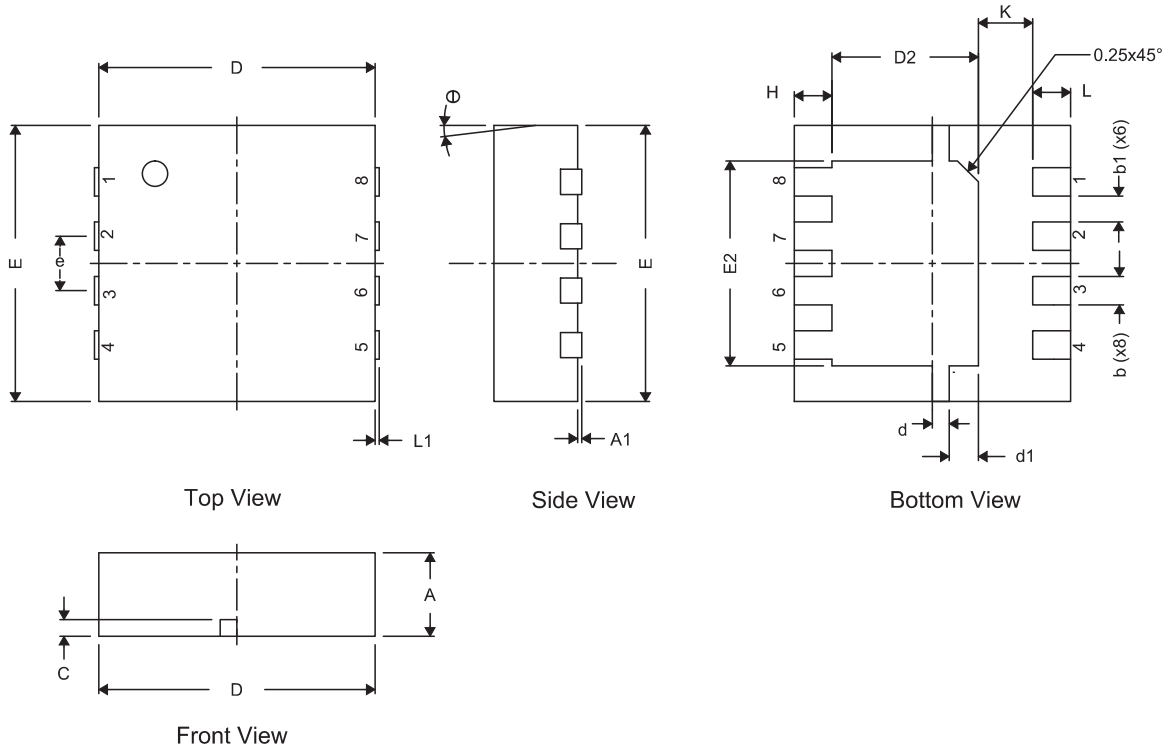
7 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

7.1 Q3 封装尺寸



DIM	毫米			英寸		
	最小值	标称值	最大值	最小值	标称值	最大值
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
b1		0.310（标称值）			0.012（标称值）	
c	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D2	1.650	1.750	1.800	0.065	0.069	0.071
d	0.150	0.200	0.250	0.006	0.008	0.010
d1	0.300	0.350	0.400	0.012	0.014	0.016
E	3.200	3.300	3.400	0.126	0.130	0.134
E2	2.350	2.450	2.550	0.093	0.096	0.100
e		0.650 典型值			0.026 典型值	
H	0.35	0.450	0.550	0.014	0.018	0.022
K		0.650 典型值			0.026 典型值	
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	0	—	0	0	—	0
θ	0	—	0	0	—	0

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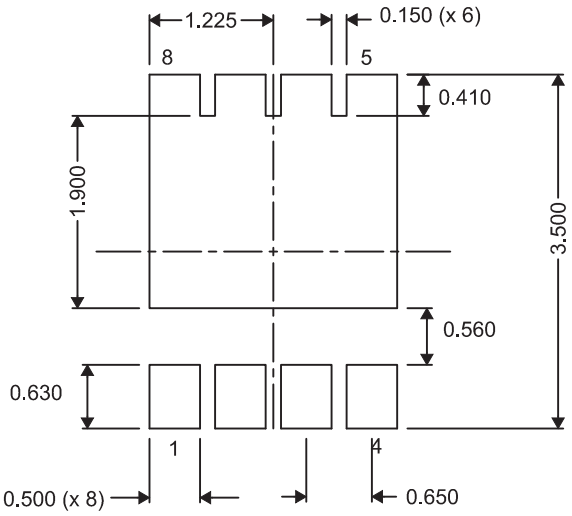
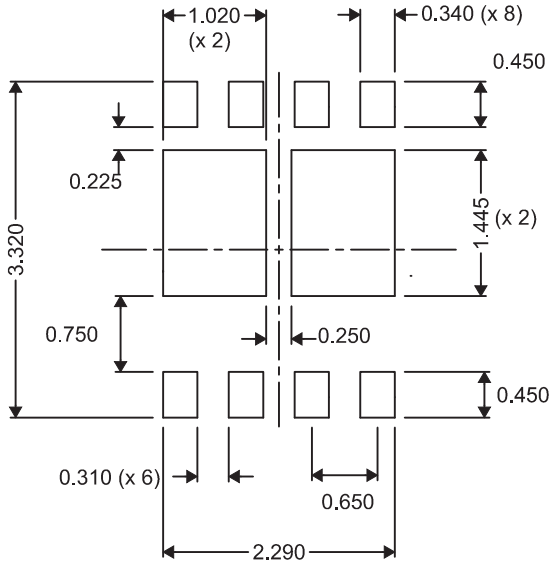
7.2 建议 PCB 布局



要获得与印刷电路板 (PCB) 设计相关的建议电路布局布线，请参阅《应用说明》SLPA005 - *通过 PCB 布局布线技巧来减少振铃*。

7.3 建议模版开孔



全部尺寸单位为 mm，除非另外注明。

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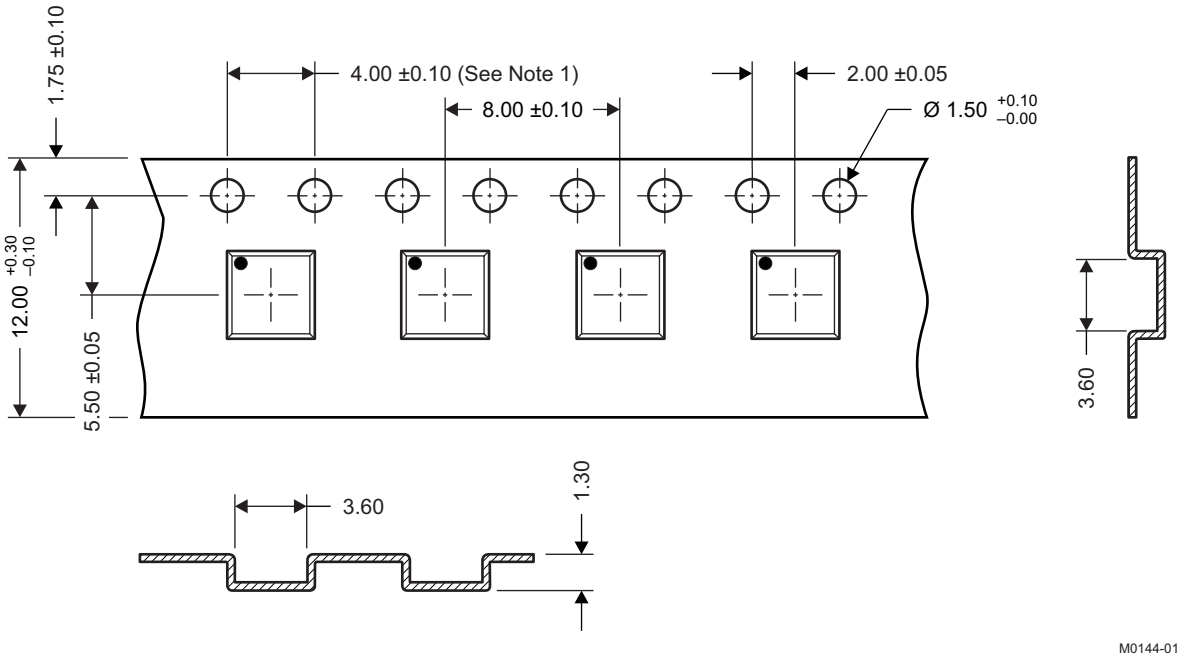
7.4 Q3 卷带信息



注：

1. 10 链轮孔距累积容差为 ±0.2
2. 每 100mm 长度的翘曲不能超过 1mm，在 250mm 长度上不累积
3. 材料：黑色抗静电聚苯乙烯
4. 全部尺寸单位为 mm（除非另外注明）。
5. 厚度：0.30 ± 0.05mm
6. MSL1 260°C（红外 (IR) 和传导）无铅回流焊兼容

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD17308Q3	Active	Production	VSON-CLIP (DQG) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17308
CSD17308Q3.B	Active	Production	VSON-CLIP (DQG) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17308
CSD17308Q3T	Active	Production	VSON-CLIP (DQG) | 8	250 | SMALL T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17308
CSD17308Q3T.B	Active	Production	VSON-CLIP (DQG) | 8	250 | SMALL T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD17308

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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