N 沟道 NexFET™ 功率 MOSFET

1 特性

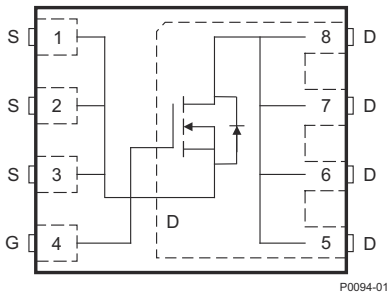
- 超低 Q_g 和 Q_{gd}
- 低热阻
- 具有雪崩能力
- SON 5mm × 6mm 塑料封装

2 应用

- 网络、电信和计算系统中的负载点同步降压转换器
- 针对控制 FET 应用进行了优化

3 说明

NexFET™ 功率 MOSFET 旨在更大限度地降低功率转换应用中的损耗。



顶视图

产品概要

V_{DS}	漏源极电压	25	V
Q_g	栅极电荷，总数(4.5V)	6.7	nC
Q_{gd}	栅极电荷（栅漏极）	1.9	nC
$r_{DS(接通)}$	漏源导通电阻	V_{GS} = 4.5V 5.4	mΩ
		V_{GS} = 10V 3.6	mΩ
$V_{GS(th)}$	阈值电压	1.8	V

订购信息

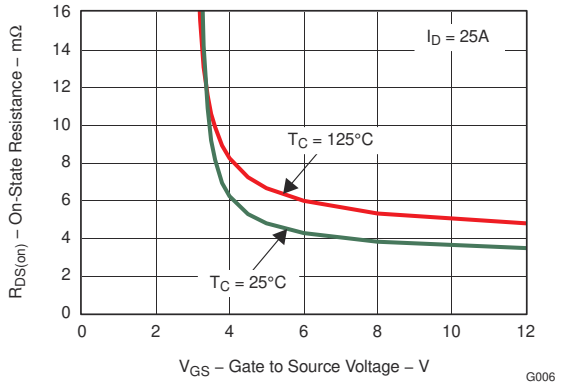
器件	封装	介质	数量	出货
CSD16408Q5	SON 5mm × 6mm 塑料封装	13 英寸 (33cm)卷带	2500	卷带

绝对最大额定值

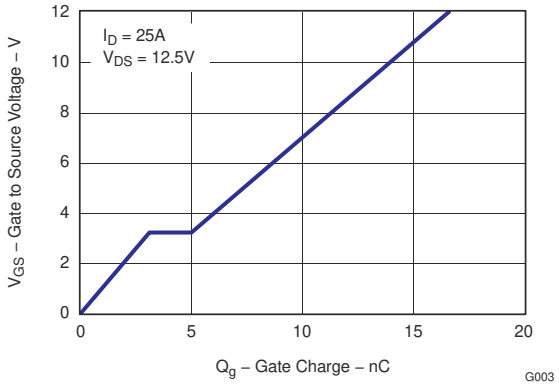
T_A = 25°C 时测得，除非另外注明		值	单位
V_{DS}	漏源极电压	25	V
V_{GS}	栅源电压	–12 至 16	V
I_D	持续漏极电流，T_C = 25°C	113	A
	持续漏极电流(1)	22	A
I_{DM}	脉冲漏极电流，T_A = 25°C(2)	141	A
P_D	功率耗散(1)	3.1	W
T_J，T_{STG}	运行结温和储存温度范围	–55 至 150	°C
E_{AS}	雪崩能量，单一脉冲 I_D = 23A，L = 0.1mH，R_G = 25Ω	126	mJ

(1) 典型 $R_{\theta JA}$ = 41°C/W（在 0.06 英寸 (1.52mm) 厚的 FR4 PCB 上安装 1 平方英寸 (6.45cm^2)、2oz、0.071mm 厚的铜焊盘时）。

(2) 脉冲持续时间 ≤ 300µs，占空比 ≤ 2%



$R_{DS(on)}$ 与 V_{GS} 间的关系



栅极电荷

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (September 2010) to Revision B (October 2023)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1

Changes from Revision * (October 2009) to Revision A (September 2010)	Page
• 删除了特性列表中的环境要点	1

5 Electrical Characteristics

T_A = 25°C unless otherwise stated

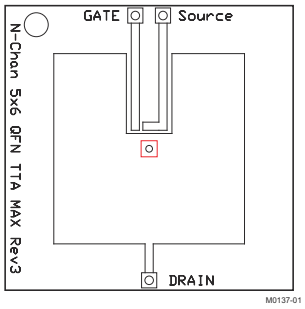
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 µA	25			V
I_{DSS}	Drain-to-source leakage	V_{GS} = 0 V, V_{DS} = 20 V			1	µA
I_{GSS}	Gate-to-source leakage	V_{DS} = 0 V, V_{GS} = –12 V to 16 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1.4	1.8	2.1	V
$r_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 4.5 V, I_D = 25 A		5.4	6.8	mΩ
		V_{GS} = 10 V, I_D = 25 A		3.6	4.5	mΩ
g_{fs}	Transconductance	V_{DS} = 15 V, I_D = 25 A		60		S
Dynamic Characteristics						
C_{ISS}	Input capacitance	V_{GS} = 0 V, V_{DS} = 12.5 V , f = 1 MHz		990	1300	pF
C_{OSS}	Output capacitance			760	1000	pF
C_{RSS}	Reverse transfer capacitance			75	100	pF
R_g	Series gate resistance			0.8	1.6	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 12.5 V, I_D = 25 A		6.7	8.9	nC
Q_{gd}	Gate charge, gate-to-drain			1.9		nC
Q_{gs}	Gate charge, gate-to-source			3.1		nC
$Q_{g(th)}$	Gate charge at Vth			1.8		nC
Q_{OSS}	Output charge	V_{DS} = 13 V, V_{GS} = 0 V		15.7		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 12.5 V, V_{GS} = 4.5 V, I_D = 20 A, R_G = 2 Ω		11.3		ns
t_r	Rise time			25		ns
$t_{d(off)}$	Turnoff delay time			11		ns
t_f	Fall time			10.8		ns
Diode Characteristics						
V_{SD}	Diode forward voltage	I_S = 25 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse recovery charge	V_{DD} = 13 V, I_F = 2 5A, di/dt = 300 A/µs		17		nC
t_{rr}	Reverse recovery time	V_{DD} = 13 V, I_F = 25 A, di/dt = 300 A/µs		21		ns

6 Thermal Characteristics

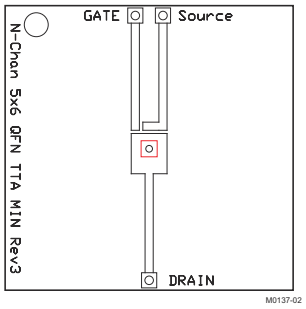
T_A = 25°C unless otherwise stated

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case(1)			1.9	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient(1) (2)			51	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 51°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on minimum pad area of 2-oz. (0.071-mm thick) Cu.

7 Typical MOSFET Characteristics

T_A = 25°C unless otherwise stated

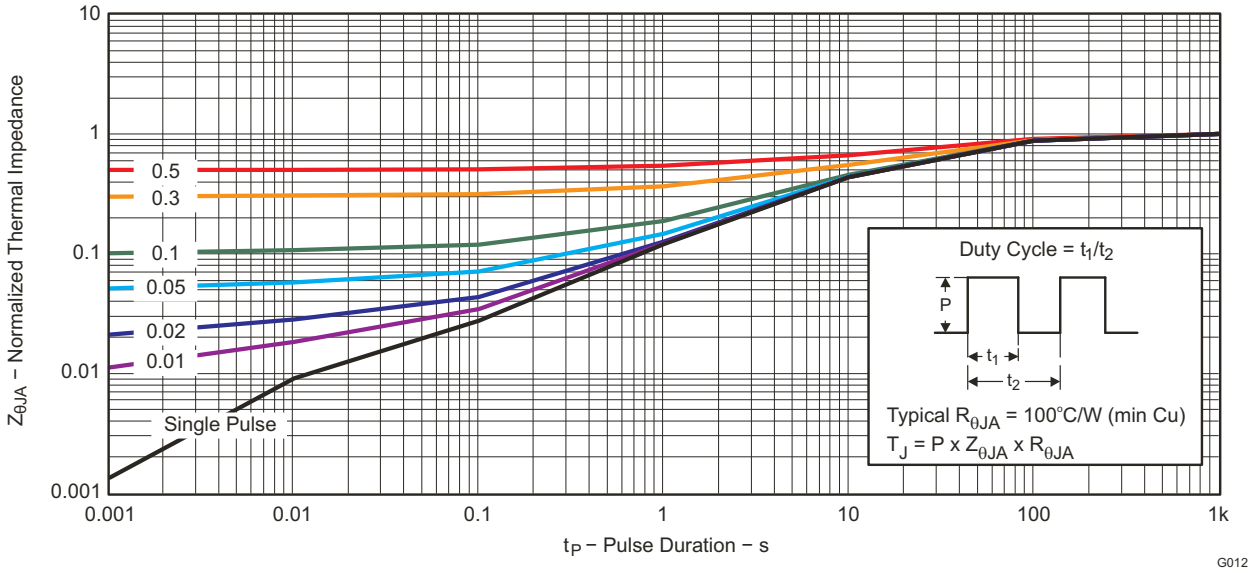


图 7-1. Transient Thermal Impedance

7 Typical MOSFET Characteristics

T_A = 25°C unless otherwise stated

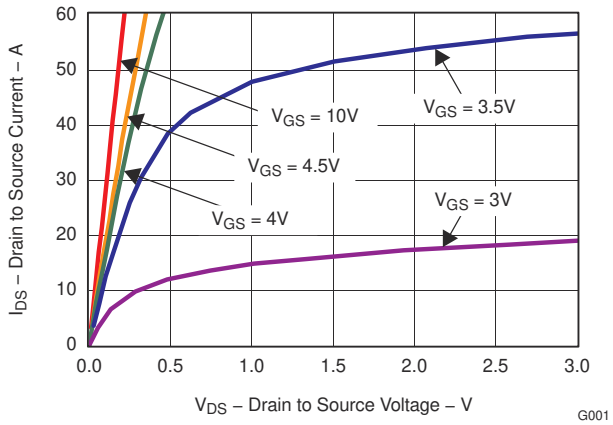


图 7-2. Saturation Characteristics

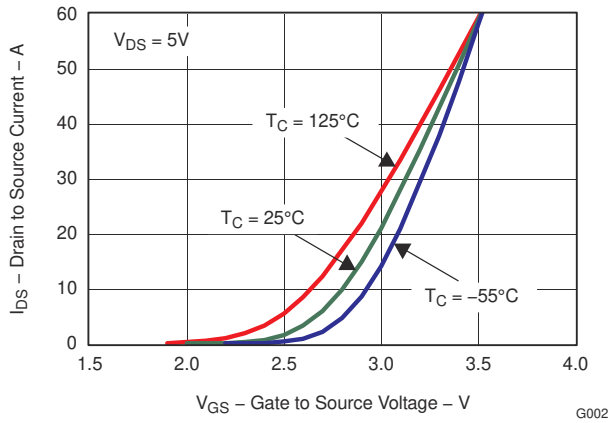


图 7-3. Transfer Characteristics

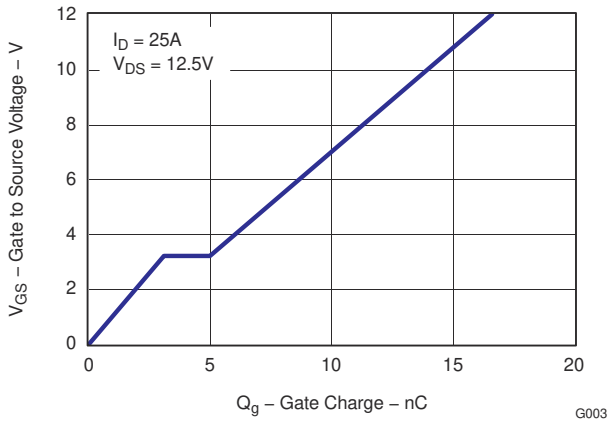


图 7-4. Gate Charge

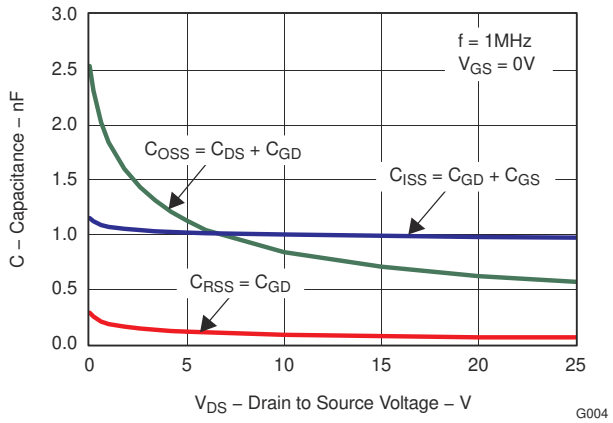


图 7-5. Capacitance

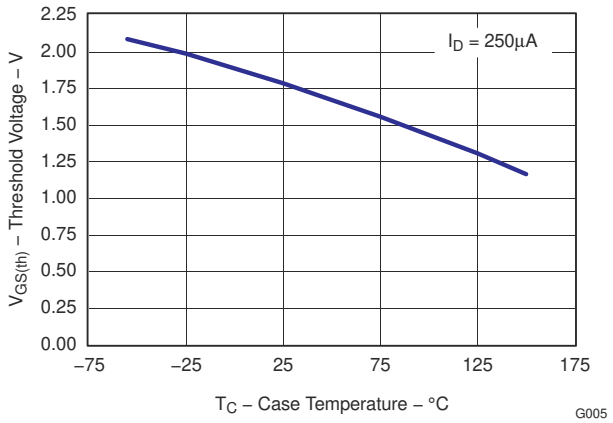


图 7-6. Threshold Voltage vs. Temperature

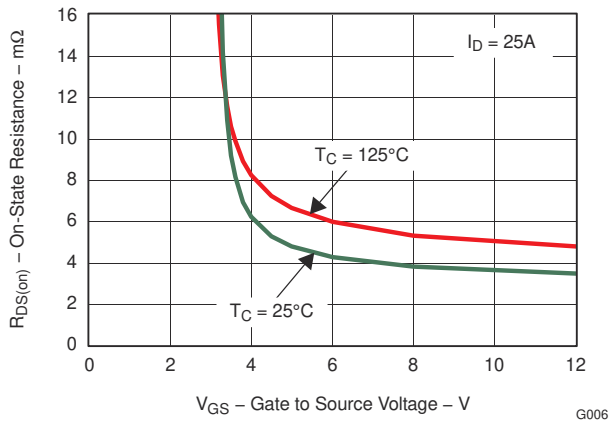


图 7-7. On-State Resistance vs. Gate-to-Source Voltage

7 Typical MOSFET Characteristics (continued)

T_A = 25°C unless otherwise stated

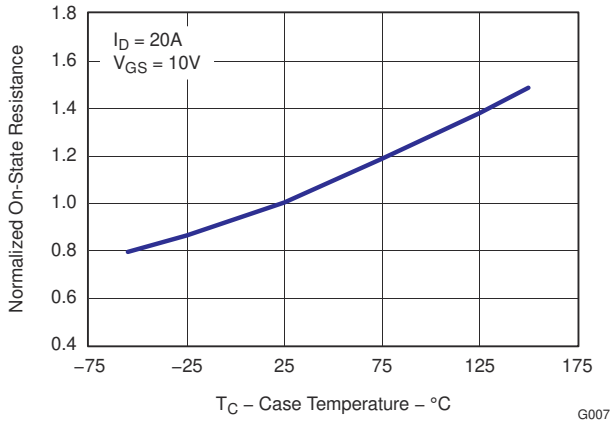


图 7-8. Normalized On-State Resistance vs. Temperature

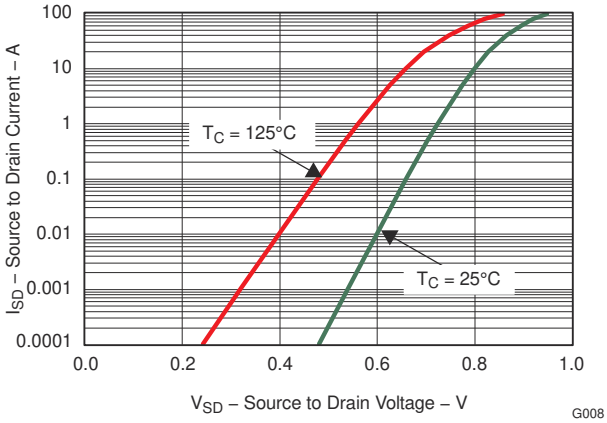


图 7-9. Typical Diode Forward Voltage

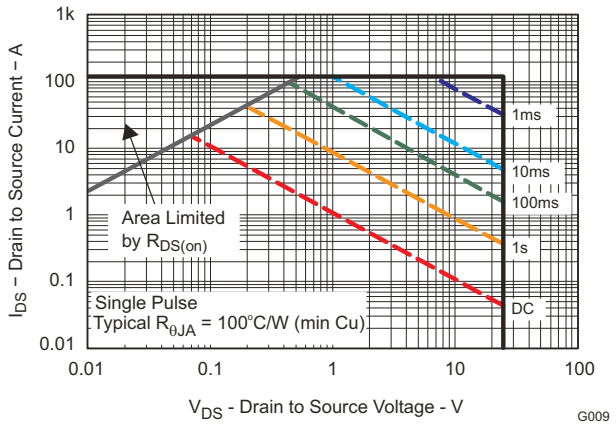


图 7-10. Maximum Safe Operating Area

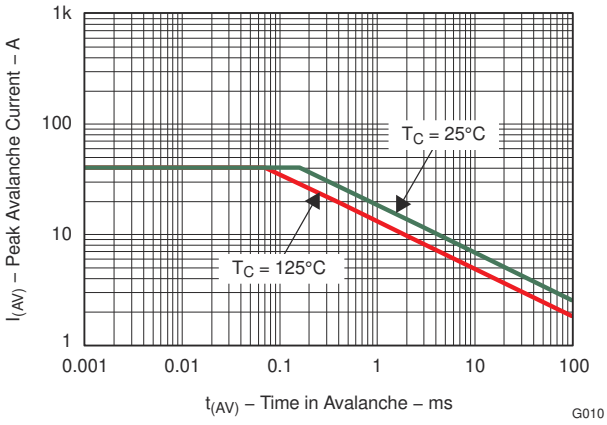


图 7-11. Single-Pulse Unclamped Inductive Switching

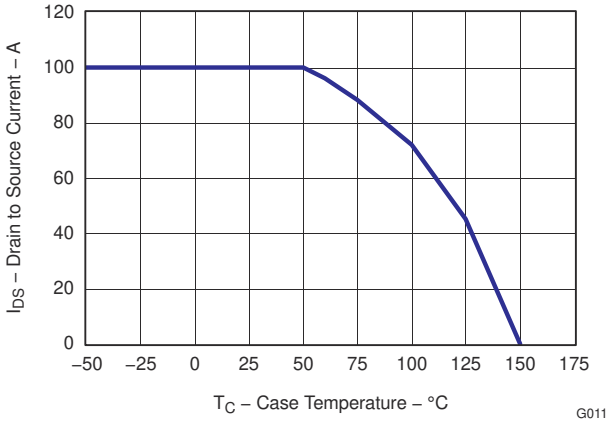


图 7-12. Maximum Drain Current vs. Temperature

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD16408Q5	Active	Production	VSON-CLIP (DQH) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16408
CSD16408Q5.B	Active	Production	VSON-CLIP (DQH) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16408

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。 严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265