CSD16342Q5A 25V N 沟道 NexFET™ 功率 MOSFET

1 特性

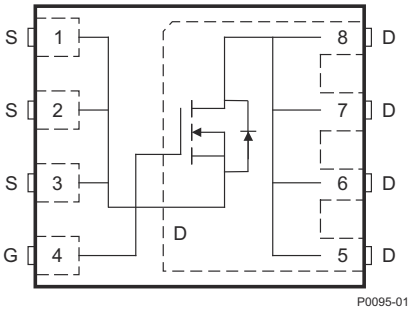
- 针对 5V 栅极驱动进行了优化
- V_{GS} = 2.5V 时的额定电阻
- 超低 Qg 和 Qgd
- 低热阻
- 具有雪崩能力
- 无铅引脚镀层
- 符合 RoHS
- 无卤素
- SON 5mm x 6mm 塑料封装

2 应用

- 用于组网、电信和计算系统应用的负载点同步降压转换器
- 针对控制或同步 FET 应用进行了优化

3 说明

NexFET™ 功率 MOSFET 旨在更大限度地减少功率转换中的损耗，并针对 5V 栅极驱动应用进行了优化。



顶视图

产品概要

V_{DS}	漏源极电压	25		V
Q_g	栅极电荷总量 (4.5V)	6.8		nC
Q_{gd}	栅漏栅极电荷	1.2		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 2.5V	6.1	mΩ
		V_{GS} = 4.5V	4.3	mΩ
		V_{GS} = 8V	3.8	mΩ
V_{th}	阈值电压	0.85		V

订购信息

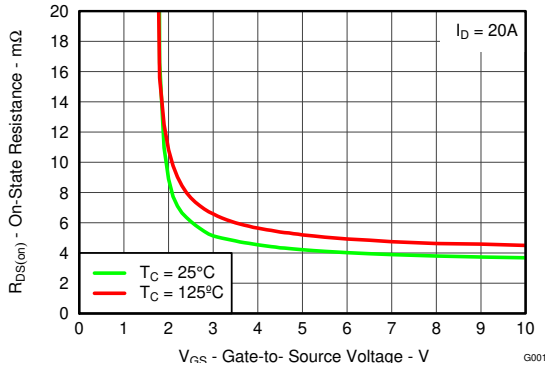
器件	封装	介质	数量	运输
CSD16342Q5A	SON 5 × 6 塑料封装	13 英寸卷带	2500	卷带包装

绝对最大额定值

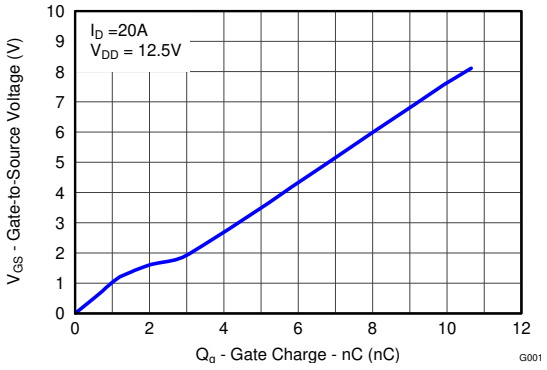
T_A = 25°C 时测得，除非另有说明		值	单位
V_{DS}	漏源极电压	25	V
V_{GS}	栅源电压	+10/-8	V
I_D	持续漏极电流，T_C = 25°C	100	A
	持续漏极电流(1)	21	A
I_{DM}	脉冲漏极电流，T_A = 25°C(2)	131	A
P_D	功率耗散(1)	3	W
T_J，T_{STG}	运行结温和储存温度范围	-55 至 150	°C
E_{AS}	雪崩能量，单脉冲 I_D = 40A，L = 0.1mH，R_G = 25Ω	80	mJ

(1) 0.060 英寸厚 FR4 PCB 上采用 1 平方英寸、2 盎司铜焊盘时的 $R_{\theta JA}$ 典型值为 40°C/W。

(2) 脉冲宽度 ≤ 300 μs，占空比 ≤2%



$R_{DS(ON)}$与 V_{GS} 间的关系



栅极电荷

4 规格

4.1 电气特性

（T_A = 25°C 时测得，除非另有说明）

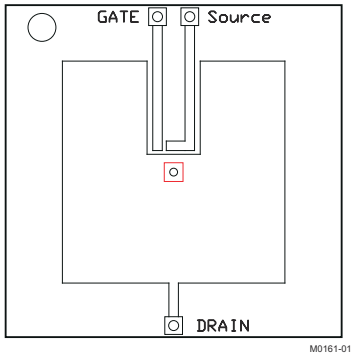
参数		测试条件	最小值	典型值	最大值	单位
静态特性						
BV_{DSS}	漏源极电压	V_{GS} = 0V，I_{DS} = 250 μA	25			V
I_{DSS}	漏源漏电流	V_{GS} = 0V，V_{DS} = 20V			1	μA
I_{GSS}	栅源漏电流	V_{DS} = 0V，V_{GS} = +10/-8V			100	nA
$V_{GS(th)}$	栅源阈值电压	V_{DS} = $V_{GS}I_{DS}$ = 250 μA	0.6	0.85	1.1	V
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 2.5V，I_{DS} = 20A		6.1	7.8	mΩ
		V_{GS} = 4.5V，I_{DS} = 20A		4.3	5.5	mΩ
		V_{GS} = 8V，I_{DS} = 20A		3.8	4.7	mΩ
g_{fs}	跨导	V_{DS} = 15V，I_{DS} = 20A		91		S
动态特性						
C_{ISS}	输入电容	V_{GS} = 0V，V_{DS} = 12.5V，f = 1MHz		1050	1350	pF
C_{OSS}	输出电容			730	950	pF
C_{RSS}	反向传输电容			53	69	pF
R_g	串联栅极电阻			1.5	3	Ω
Q_g	栅极电荷总量 (4.5V)	V_{DS} = 12.5V，I_D = 20A		6.8	7.1	nC
Q_{gd}	栅漏栅极电荷			0.9		nC
Q_{gs}	栅源栅极电荷			1.9		nC
Qg(th)	Vth 下的栅极电荷			1.2		nC
Q_{OSS}	输出电荷	V_{DS} = 13V，V_{GS} = 0V		13.7		nC
$t_{d(on)}$	导通延时时间	V_{DS} = 12.5V，V_{GS} = 4.5V，I_D = 20A，R_G = 2Ω		5.2		ns
t_r	上升时间			16.6		ns
$t_{d(off)}$	关断延迟时间			13.4		ns
t_f	下降时间			3.1		ns
二极管特性						
V_{SD}	二极管正向电压	I_S = 20A，，V_{GS} = 0V		0.8	1	V
Q_{rr}	反向恢复电荷	V_{DD} = 13V，I_F = 20A，di/dt = 300A/μs		14.5		nC
t_{rr}	反向恢复时间			20		ns

4.2 热特性

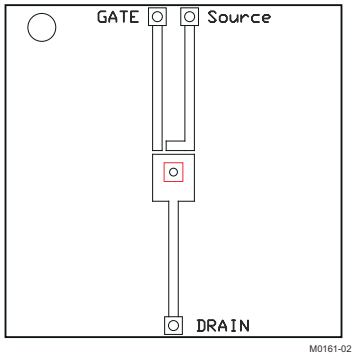
（T_A = 25°C 时测得，除非另有说明）

参数		最小值	典型值	最大值	单位
$R_{\theta JC}$	结至外壳热阻(1)			1.2	°C/W
$R_{\theta JA}$	结至环境热阻(1) (2)			50	°C/W

(1) $R_{\theta JC}$ 是在器件安装在 1.5 英寸 × 1.5 英寸 (3.81cm × 3.81cm)、厚度为 0.06 英寸 (1.52mm) 的 FR4 PCB 上的 1 英寸 ^{2} (6.45cm^2)、2 盎司（厚度为 0.071mm）的覆铜焊盘上测得的典型值。$R_{\theta JC}$ 由设计指定，而 $R_{\theta JA}$ 由用户的电路板设计确定。
(2) 器件安装在具有 1 英寸 ^{2} (6.45cm^2)、2 盎司（厚度为 0.071mm）的覆铜焊盘的 FR4 材料上。



$R_{\theta JA}$ 最大值 = 50°C/W，安装在 1 平方英寸、2 盎司铜焊盘上



$R_{\theta JA}$ 最大值 = 123°C/W，安装在最小面积的 2 盎司铜焊盘上

5 典型 MOSFET 特性

（T_A = 25°C 时测得，除非另有说明）

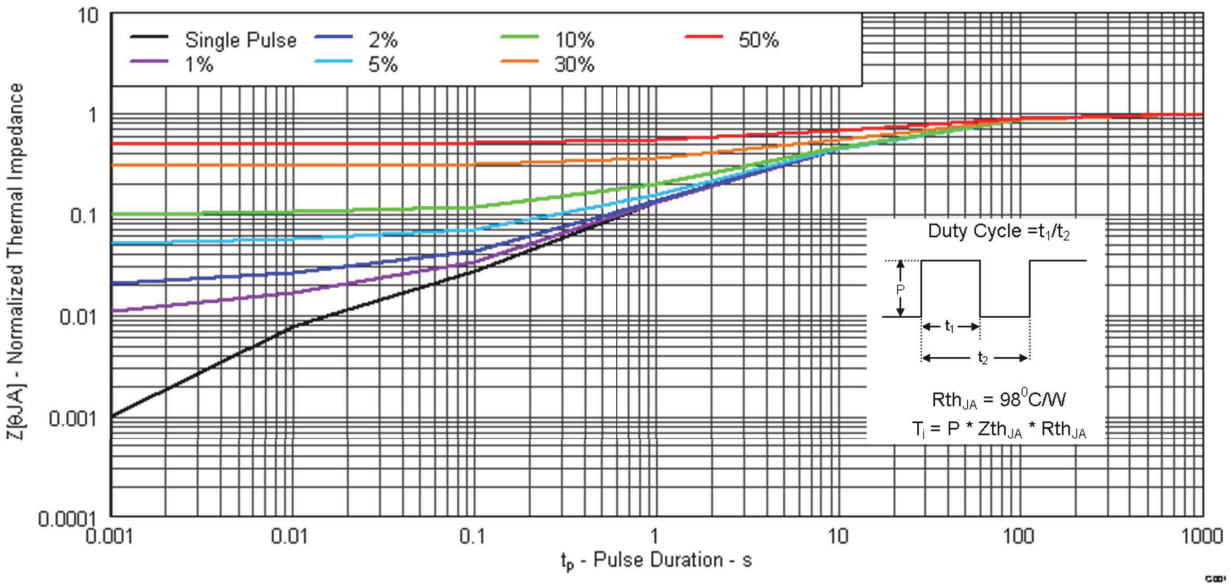


图 5-1. 瞬态热阻抗

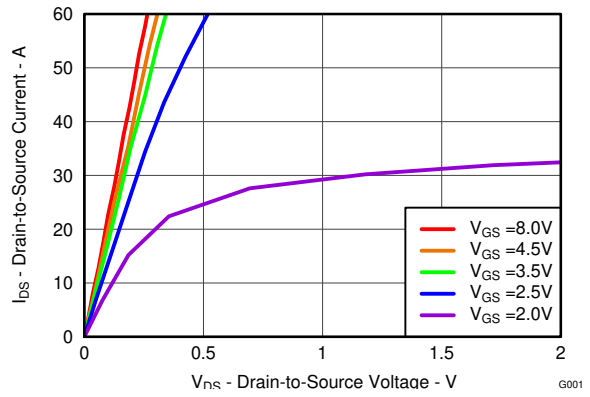


图 5-2. 饱和特性

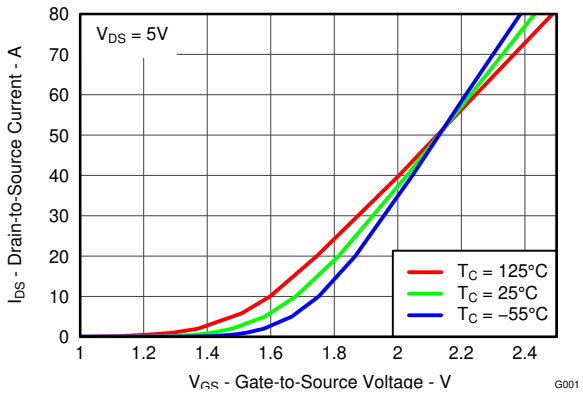


图 5-3. 传输特性

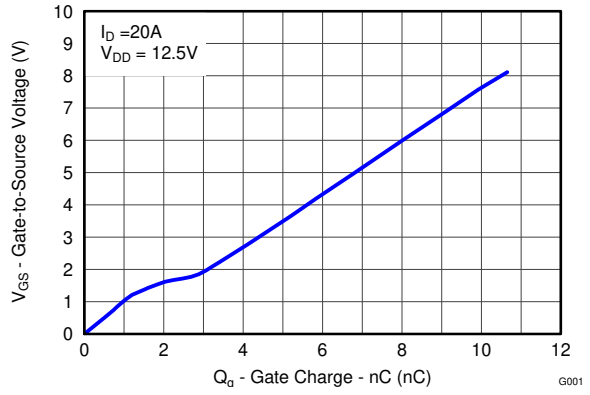


图 5-4. 栅极电荷

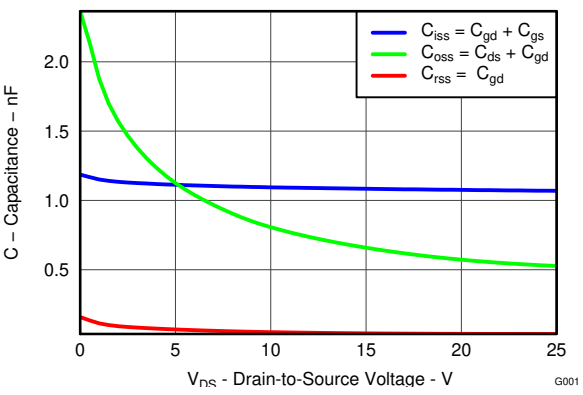


图 5-5. 电容

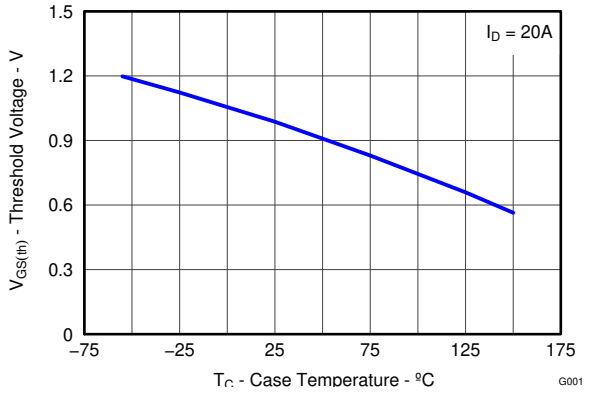


图 5-6. 阈值电压与温度间的关系

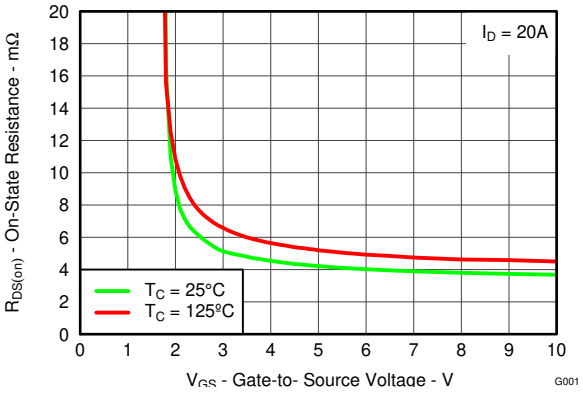


图 5-7. 导通电阻与栅极电压间的关系

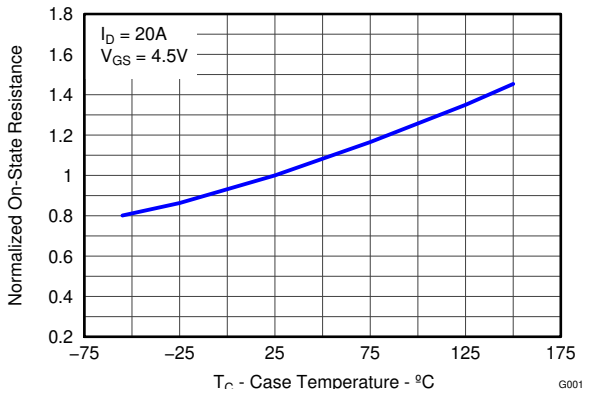


图 5-8. 标准化导通电阻与温度间的关系

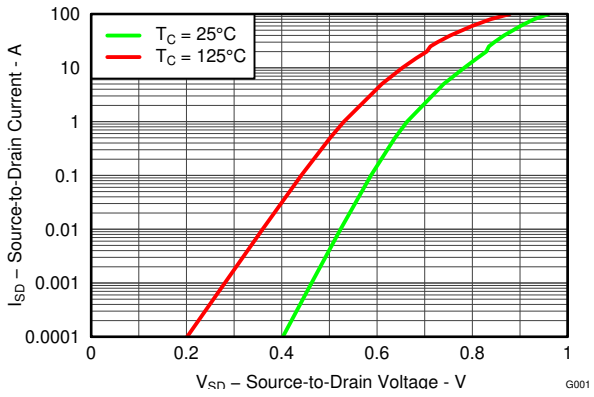


图 5-9. 典型二极管正向电压

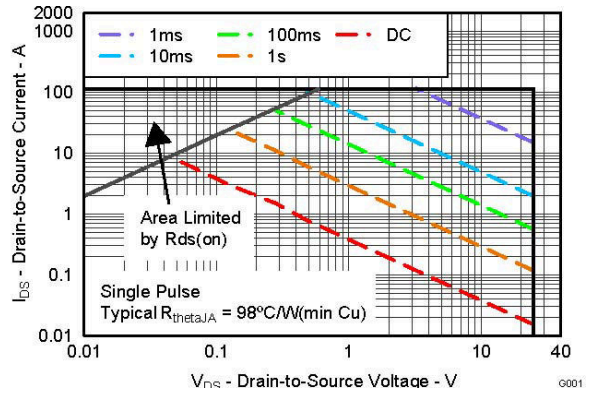


图 5-10. 最大安全工作区

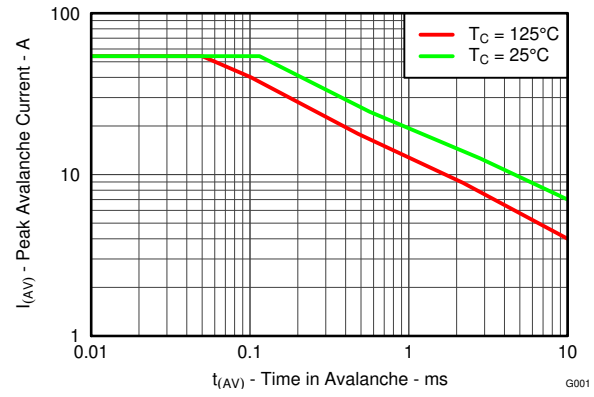


图 5-11. 单脉冲非钳位电感式开关

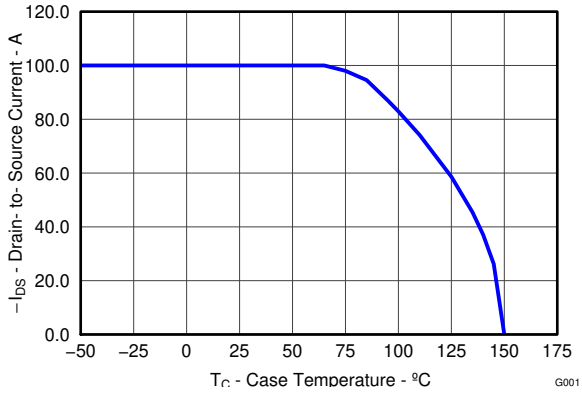


图 5-12. 最大漏极电流与温度间的关系

6 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (January 2025) to Revision C (May 2025)	Page
• 将文档标题从 CSD16342Q5A 40V N 通道 NexFET™ 功率 MOSFET 更新为 CSD16342Q5A 25V N 通道 NexFET™ 功率 MOSFET	1

Changes from Revision A (March 2012) to Revision B (January 2025)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1

Changes from Revision * (February 2012) to Revision A (March 2012)	Page
• 将器件状态从“产品预发布”更改为“量产数据”	1

7 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD16342Q5A	Active	Production	VSONP (DQJ) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16342
CSD16342Q5A.B	Active	Production	VSONP (DQJ) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16342

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

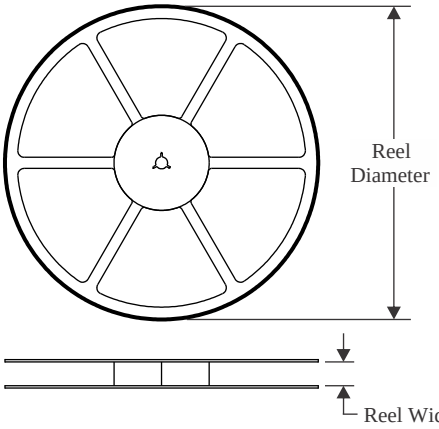
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

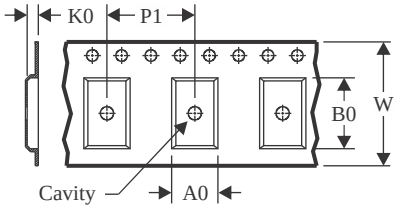
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

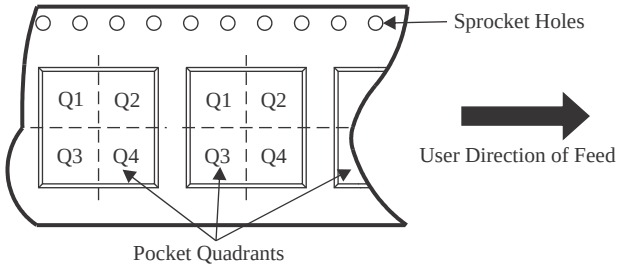


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

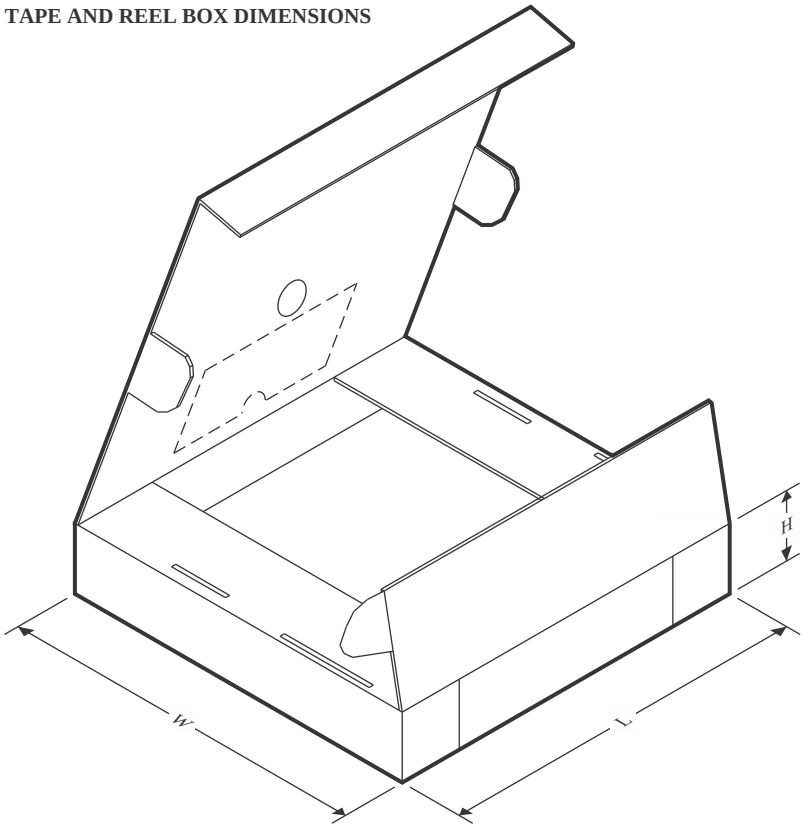
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

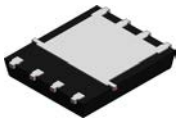
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD16342Q5A	VSONP	DQJ	8	2500	330.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD16342Q5A	VSONP	DQJ	8	2500	340.0	340.0	38.0

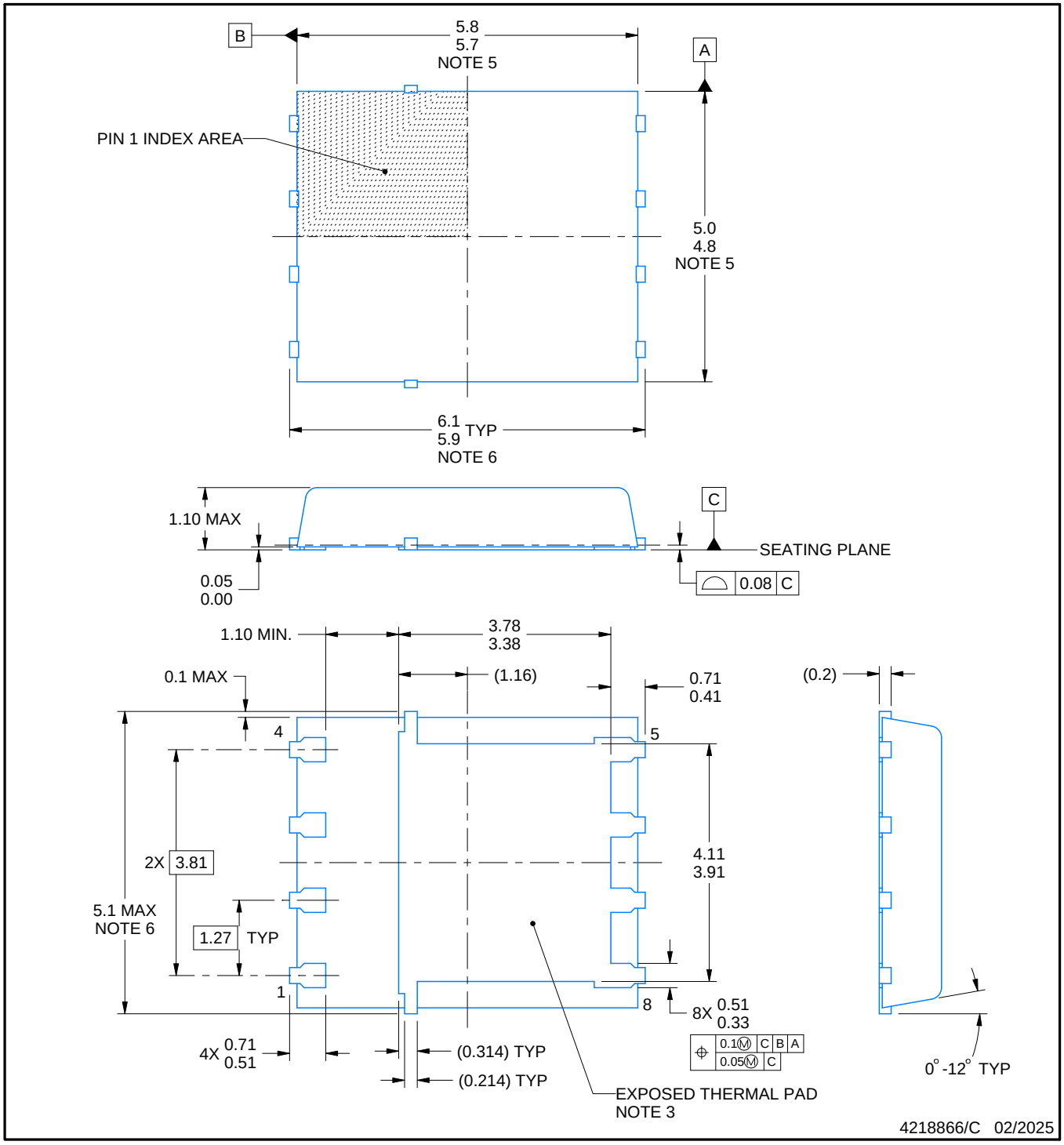


PACKAGE OUTLINE

DQJ0008A

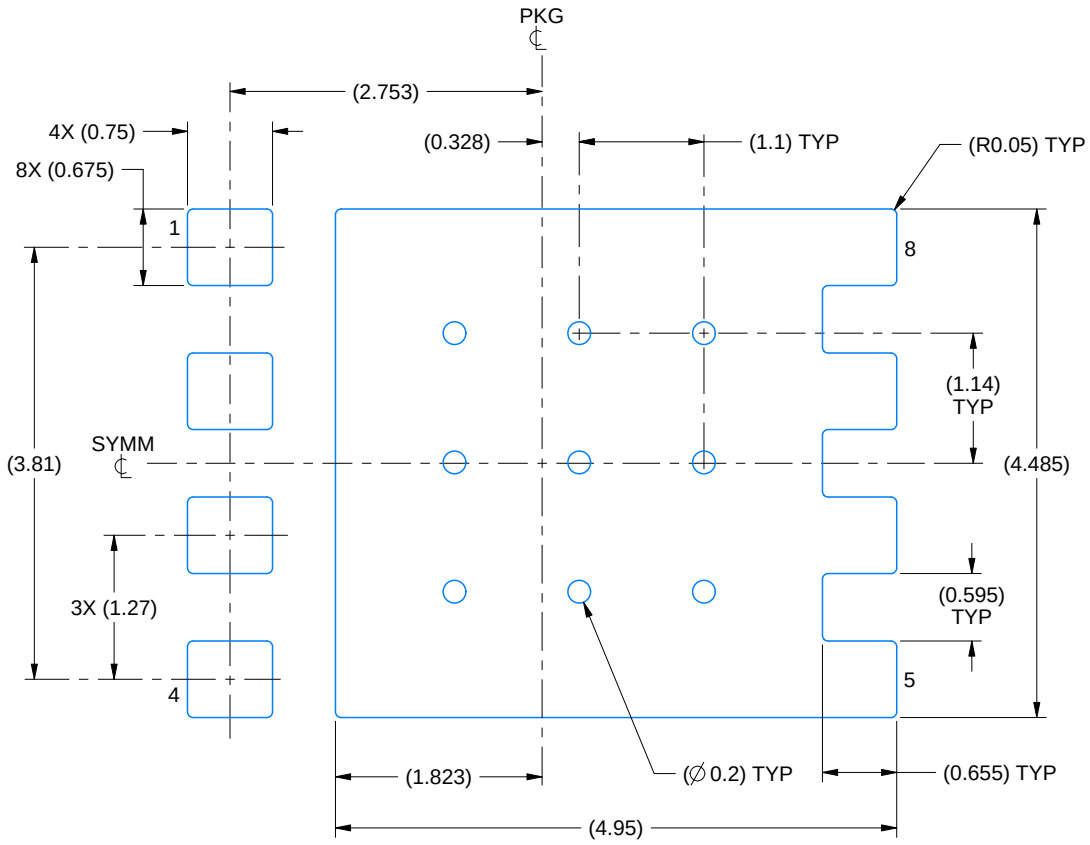
VSONP - 1.1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

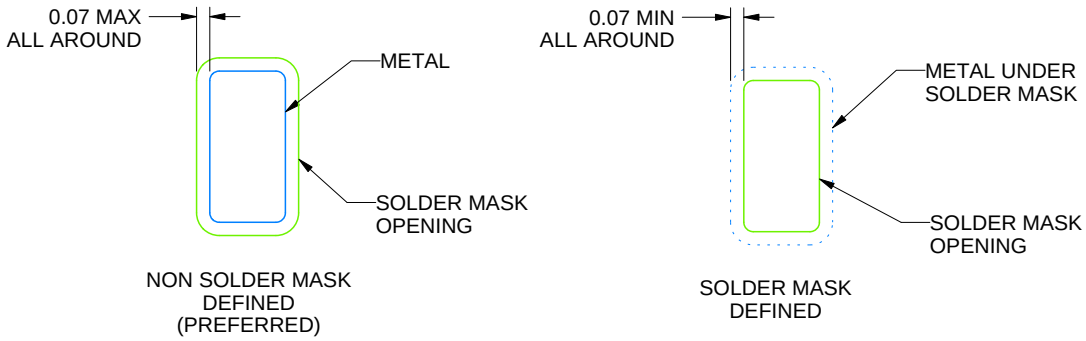


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Metalized features are supplier options and may not be on the package.
5. These dimensions do not include mold flash protrusions or gate burrs.
6. These dimensions include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE: 15X

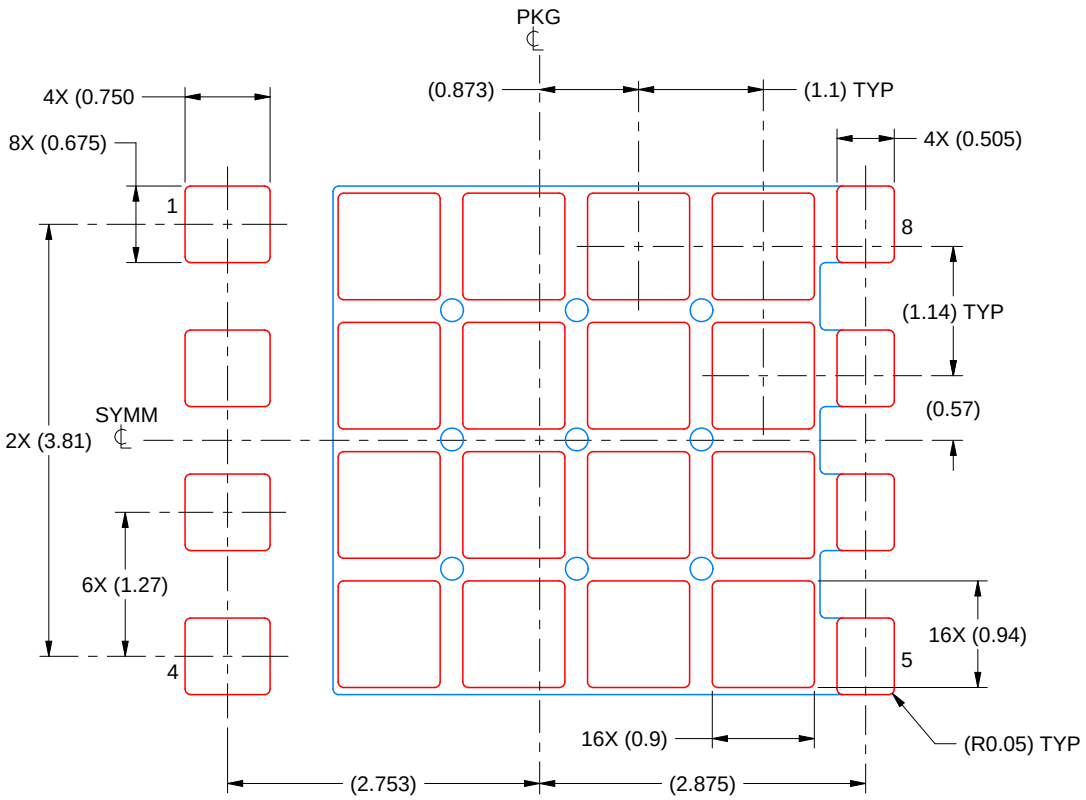


SOLDER MASK DETAILS

4218866/C 02/2025

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD:
70% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 15X

4218866/C 02/2025

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

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