TEXAS INSTRUMENTS
CSD16325Q5
ZHCSTJ9D – AUGUST 2009 – REVISED OCTOBER 2023

N 通道 NexFet 功率 MOSFET

1 特性

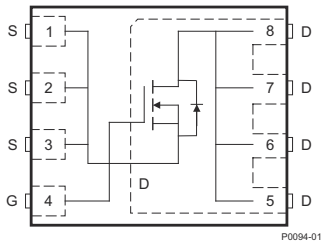
- 针对 5V 栅极驱动进行了优化
- 超低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩级
- 无铅引脚镀层
- 符合 RoHS 标准
- 无卤素
- 5mm × 6mm SON 塑料封装

2 应用

- 网络、电信和计算系统中的负载点同步降压转换器
- 已针对同步场效应晶体管 (FET) 应用进行优化

3 说明

NexFET™ 功率 MOSFET 旨在更大限度地减少功率转换应用中的损耗，并针对 5V 栅极驱动应用进行了优化。



顶视图

产品概要

V_{DS}	漏源电压	25		V
Q_g	栅极电荷总量 (4.5V)	18		nC
Q_{gd}	栅漏栅极电荷	3.5		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS}=3V	2.1	mΩ
		V_{GS} = 4.5V	1.7	mΩ
		V_{GS} = 8V	1.5	mΩ
$V_{GS(th)}$	阈值电压	1.1		V

订购信息

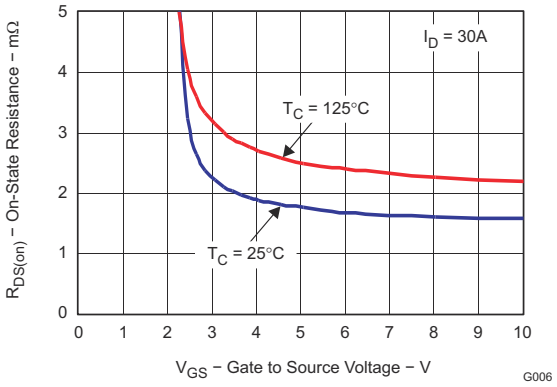
器件	封装	介质	数量	出货
CSD16325Q5	5mm × 6mm SON 塑料封装	13 英寸卷带	2500	卷带包装

绝对最大额定值

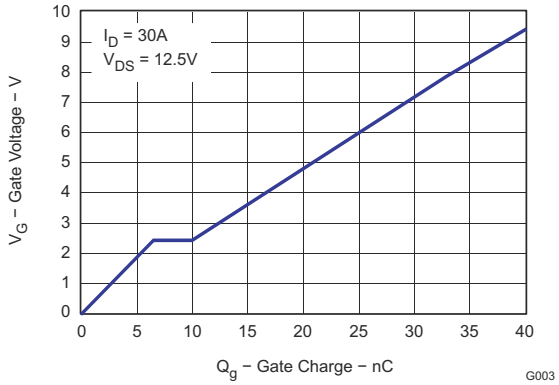
T_A = 25°C 时测得，除非另有说明		值	单位
V_{DS}	漏源电压	25	V
V_{GS}	栅源电压	+10 / – 8	V
I_D	持续漏极电流，T_C=25°C 时测得	100	A)
	持续漏极电流(1)	33	A
I_{DM}	脉冲漏极电流，T_A = 25°C(2)	200	A
P_D	功率耗散(1)	3.1	W
T_J，T_{STG}	运行结温和储存温度范围	-55 至 150	°C
E_{AS}	雪崩能量，单一脉冲 I_D = 100A，L = 0.1mH，R_G = 25Ω	500	mJ

(1) 典型 $R_{\theta JA}$ = 38°C/W（在 0.06 英寸 (1.52mm) 厚的 FR4 PCB 上安装 1 平方英寸 (6.45cm²)、2oz、0.071mm 厚的铜焊盘时）。

(2) 脉冲持续时间 ≤ 300 µs，占空比 ≤ 2%



$R_{DS(on)}$ 与 V_{GS} 之间的关系



栅极电荷

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Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (April 2010) to Revision D (October 2023)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1

Changes from Revision B (April 2010) to Revision C (April 2010)	Page
• Changed $R_{DS(on)}$, V_{GS} = 3 V in the Electrical Characteristics table From: 2.7 to 2.9 in the max column	3

4 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0 V, I_D = 250 μA	25			V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0 V, V_{DS} = 20 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0 V, V_{GS} = +10/ – 8 V			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	0.9	1.1	1.4	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 3 V, I_D = 30 A		2.1	2.9	mΩ
		V_{GS} = 4.5 V, I_D = 30 A		1.7	2.2	mΩ
		V_{GS} = 8 V, I_D = 30 A		1.5	2	mΩ
g_{fs}	Transconductance	V_{DS} = 15 V, I_D = 30 A		159		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 12.5 V, f = 1 MHz		3070	4000	pF
C_{oss}	Output Capacitance			2190	2850	pF
C_{rss}	Reverse Transfer Capacitance			120	150	pF
R_G	Series Gate Resistance			1.6	3.2	Ω
Q_g	Gate Charge Total (4.5 V)	V_{DS} = 12.5 V, I_{DS} = 30 A		18	25	nC
Q_{gd}	Gate Charge – Gate to Drain			3.5		nC
Q_{gs}	Gate Charge – Gate to Source			6.6		nC
$Q_{g(th)}$	Gate Charge at Vth			3.3		nC
Q_{oss}	Output Charge	V_{DS} = 13 V, V_{GS} = 0 V		43		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 12.5 V, V_{GS} = 4.5 V, I_{DS} = 30 A, R_G =2 Ω		10.5		ns
t_r	Rise Time			16		ns
$t_{d(off)}$	Turn Off Delay Time			32		ns
t_f	Fall Time			12		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_{DS} = 30 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DD} = 10 V, I_F = 30 A, di/dt = 300 A/μs		63		nC
t_{rr}	Reverse Recovery Time	V_{DD} = 10 V, I_F = 30 A, di/dt = 300 A/μs		47		ns

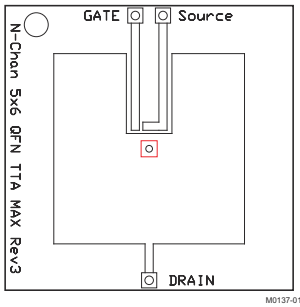
5 Thermal Characteristics

(T_A = 25°C unless otherwise stated)

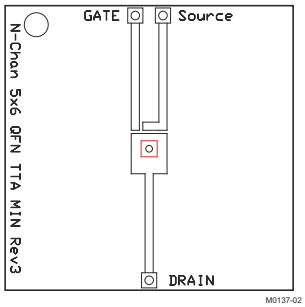
PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case(1)			1	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient(1) (2)			50	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.

(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 50°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 126°C/W when mounted on minimum pad area of 2-oz. (0.071-mm thick) Cu.

6 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

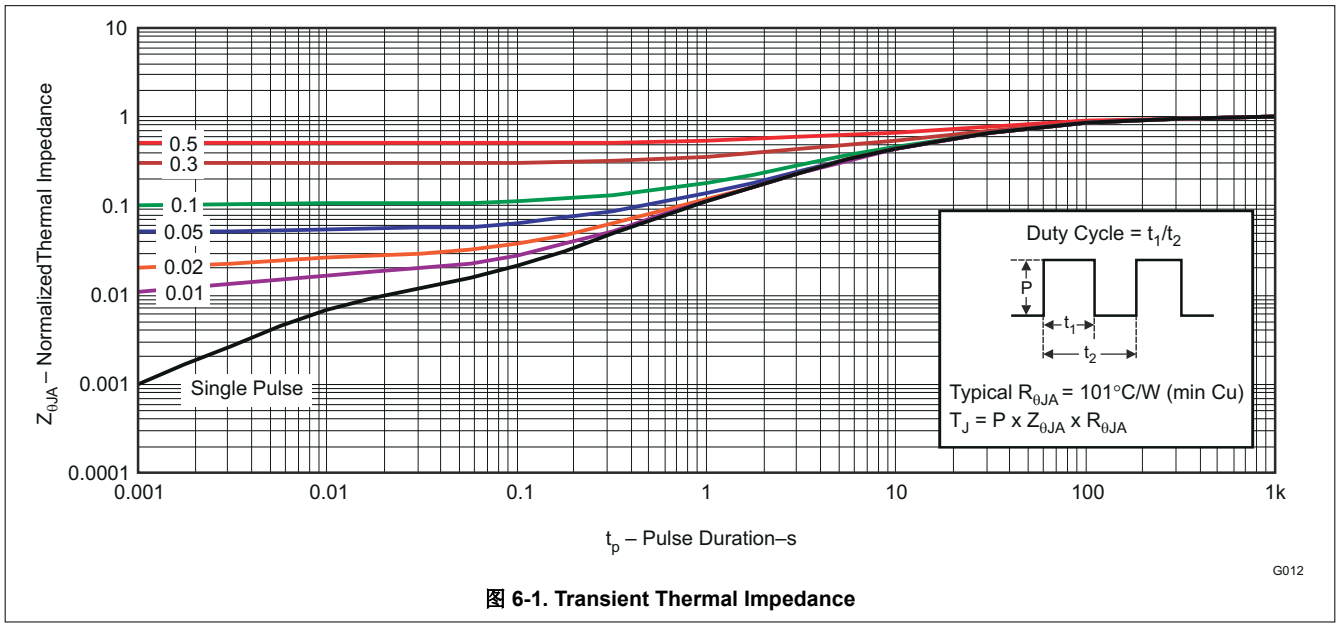


图 6-1. Transient Thermal Impedance

6 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

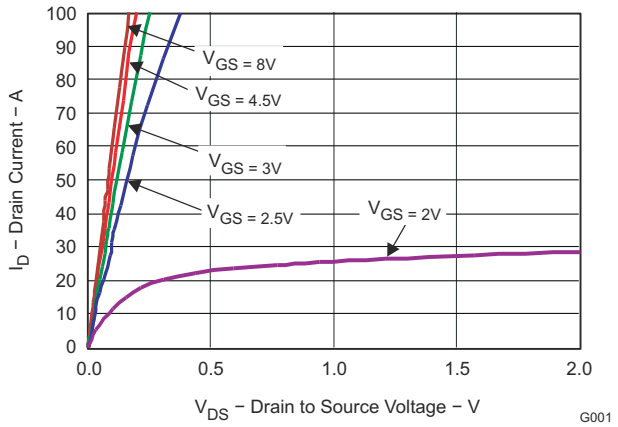


图 6-2. Saturation Characteristics

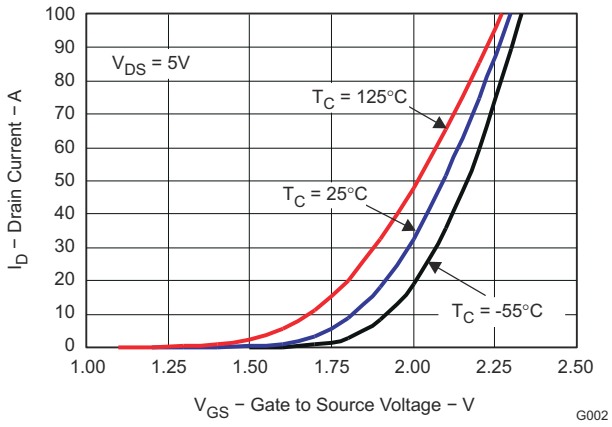


图 6-3. Transfer Characteristics

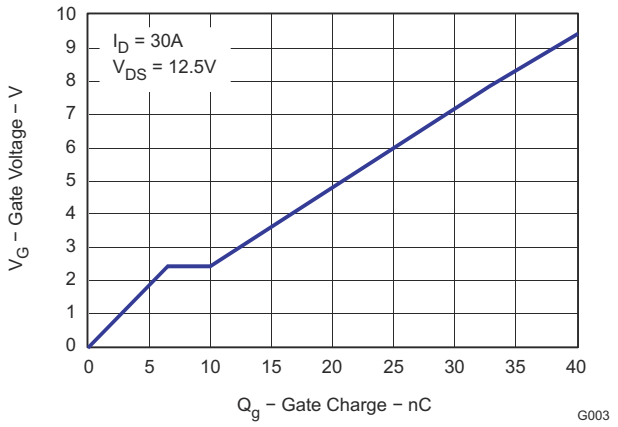


图 6-4. Gate Charge

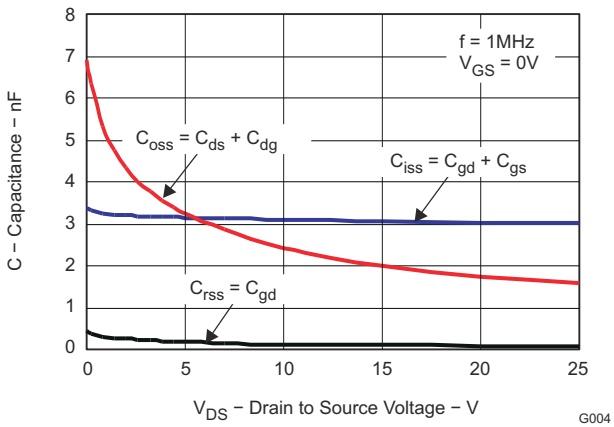


图 6-5. Capacitance

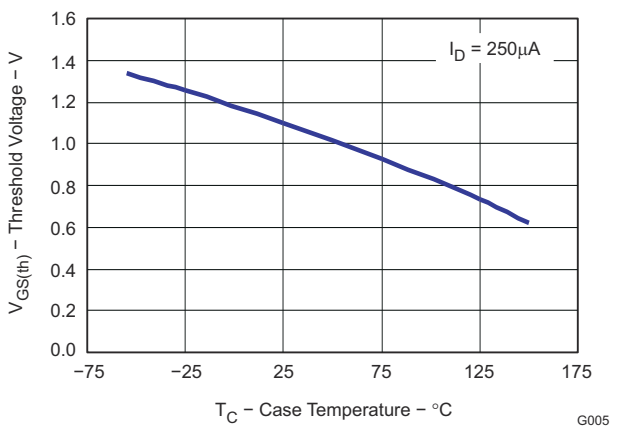


图 6-6. Threshold Voltage vs. Temperature

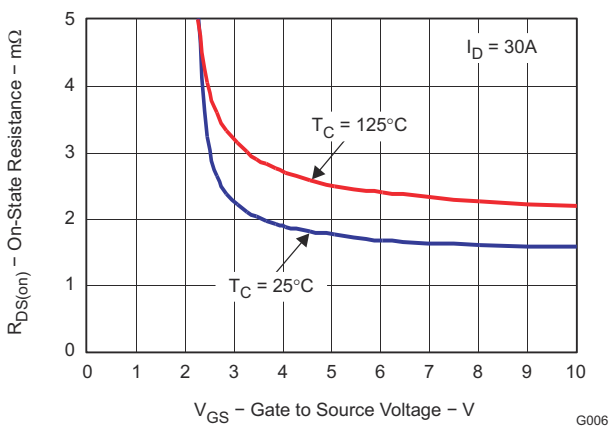


图 6-7. On-State Resistance vs. Gate to Source Voltage

6 Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

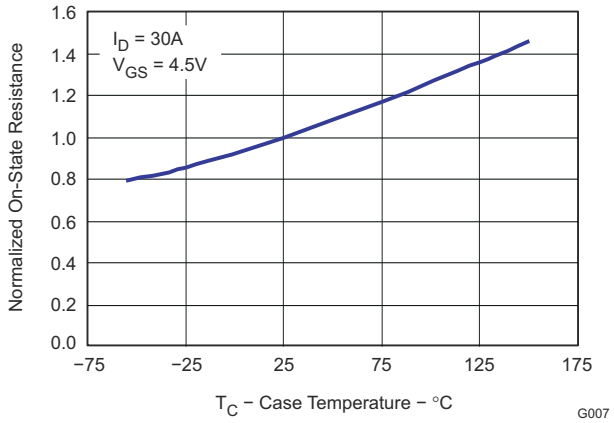


图 6-8. Normalized On-State Resistance vs. Temperature

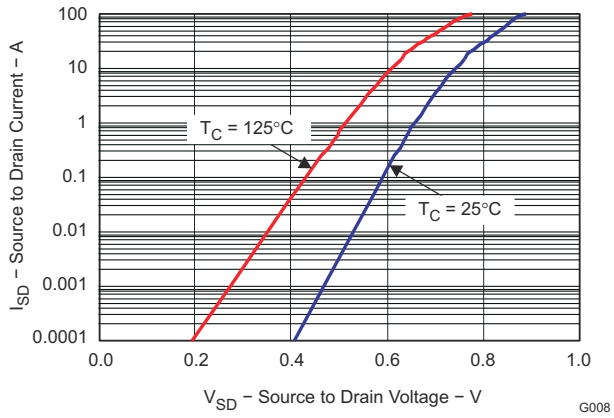


图 6-9. Typical Diode Forward Voltage

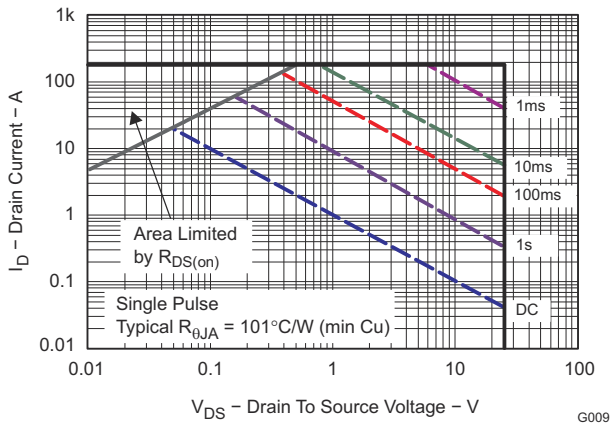


图 6-10. Maximum Safe Operating Area

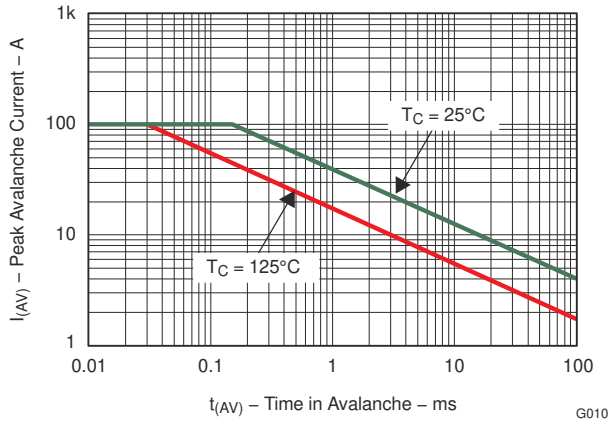


图 6-11. Single Pulse Unclamped Inductive Switching

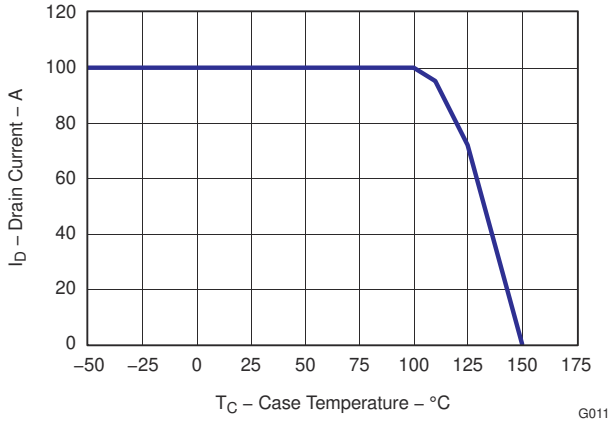


图 6-12. Maximum Drain Current vs. Temperature

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD16325Q5	Active	Production	VSON-CLIP (DQH) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16325
CSD16325Q5.B	Active	Production	VSON-CLIP (DQH) | 8	2500 | LARGE T&R	ROHS Exempt	SN	Level-1-260C-UNLIM	-55 to 150	CSD16325

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

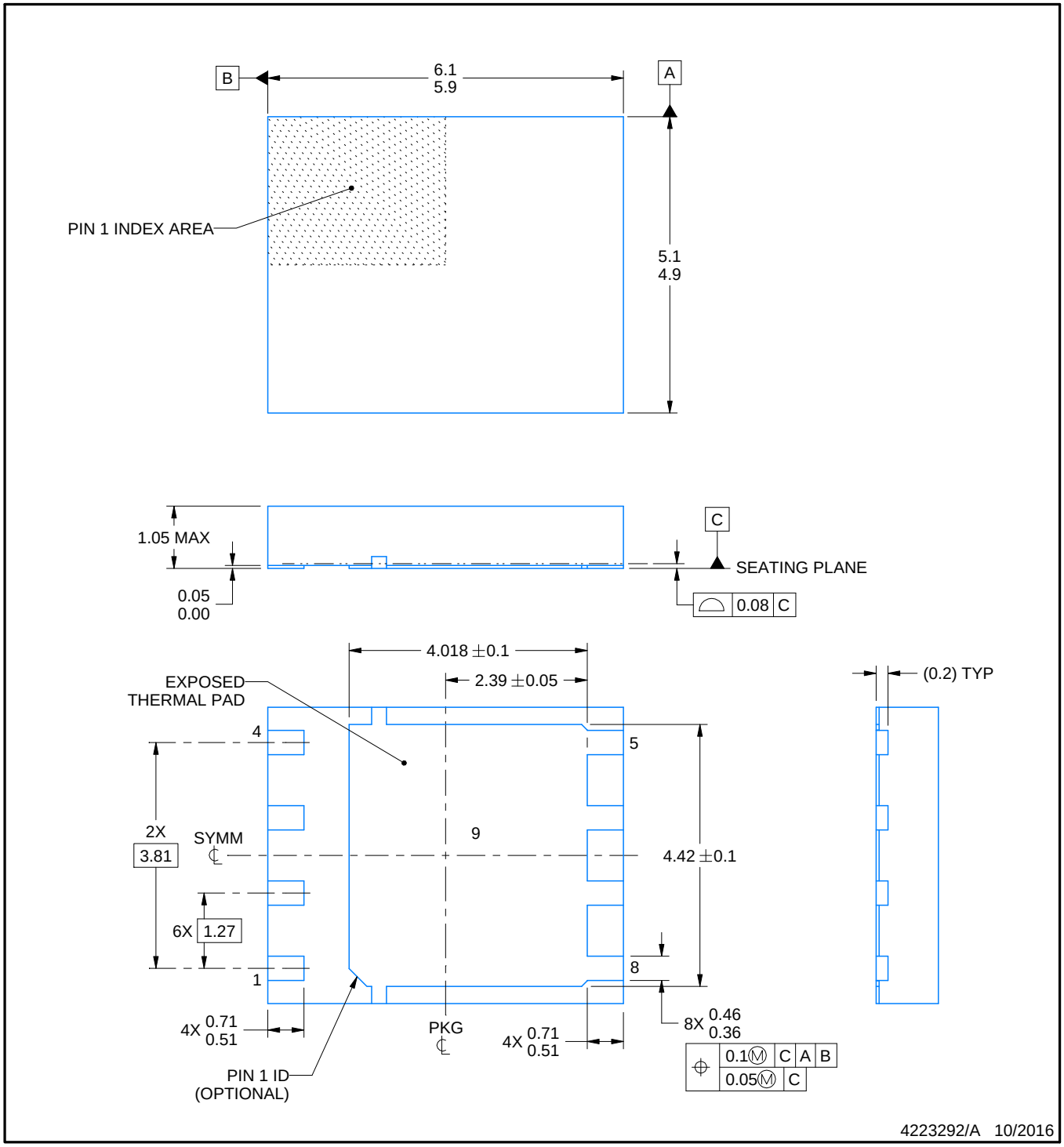
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

DQH0008A

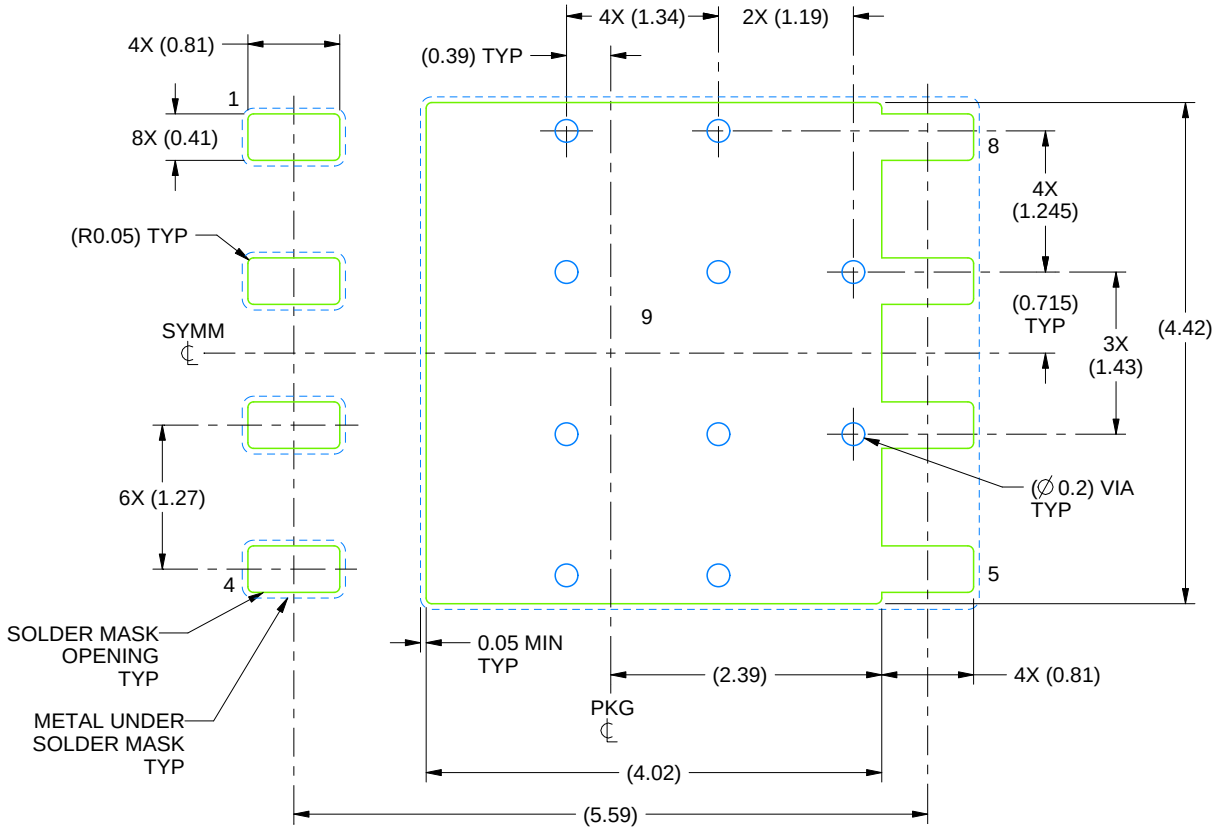
VSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:15X

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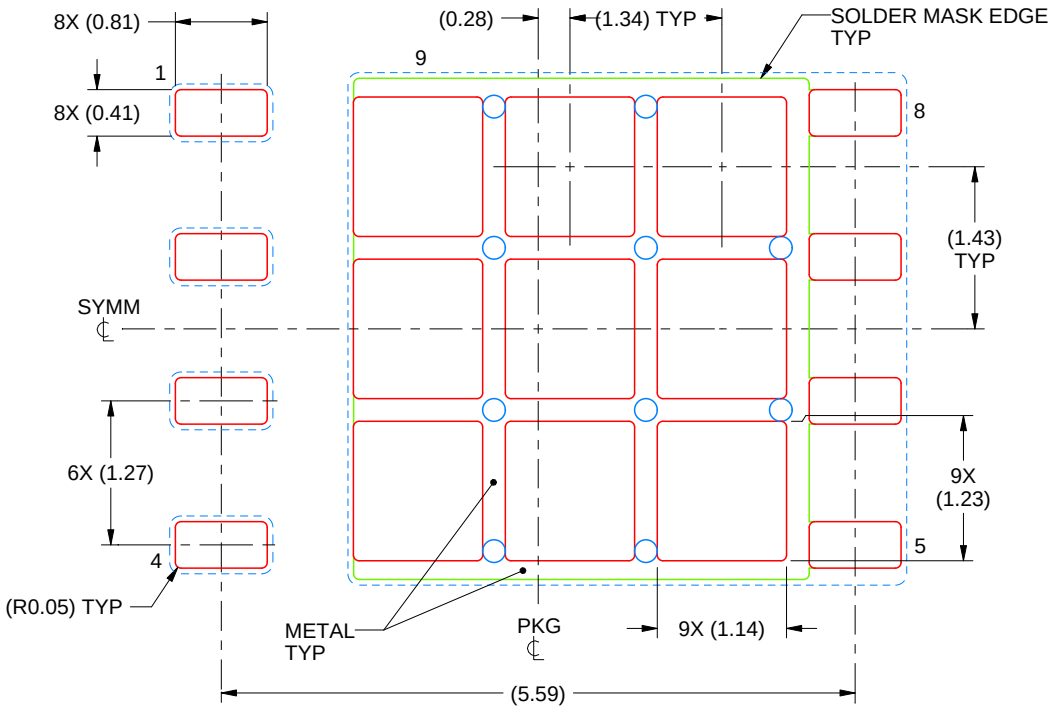
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

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