

CSD13302W 12V N 通道 NexFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET)

1 特性

- 超低导通电阻
- 低 Q_g 和 Q_{gd}
- 1mm x 1mm 小尺寸封装
- 低高度（高度为 0.62mm）
- 无铅
- 符合 RoHS 环保标准
- 无卤素

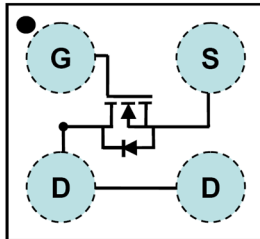
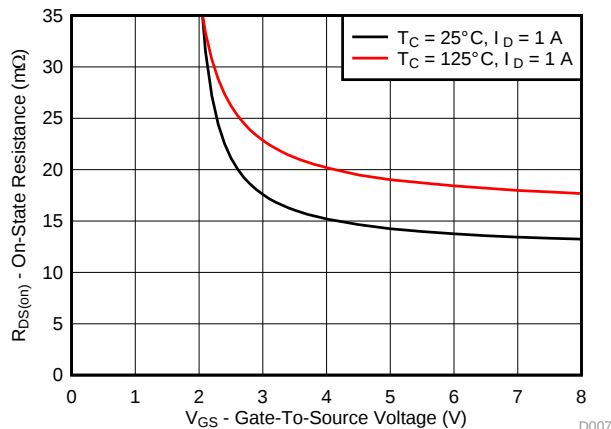
2 应用范围

- 电池管理
- 负载开关
- 电池保护

3 说明

这款 14.6mΩ、12V N 通道器件设计用于在超薄且具有出色散热特性的 1mm × 1mm 小外形封装内提供最低的导通电阻和栅极电荷。

顶视图

 $R_{DS(on)}$ 与 V_{GS} 间的关系

D007

产品概要

$T_A = 25^\circ\text{C}$		典型值	单位
V_{DS}	漏源电压	12	V
Q_g	栅极电荷总量 (4.5V)	6.0	nC
Q_{gd}	栅极电荷 (栅极到漏极)	2.1	nC
$R_{DS(on)}$	漏源导通电阻	$V_{GS} = 2.5\text{V}$	21.2 mΩ
		$V_{GS} = 4.5\text{V}$	14.6 mΩ
$V_{GS(th)}$	阈值电压	1.0	V

订购信息⁽¹⁾

器件	数量	介质	封装	出货
CSD13302W	3000	7 英寸卷带	1.0mm × 1.0mm 晶圆级封装	卷带封装
CSD13302WT	250	7 英寸卷带		

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

最大绝对额定值

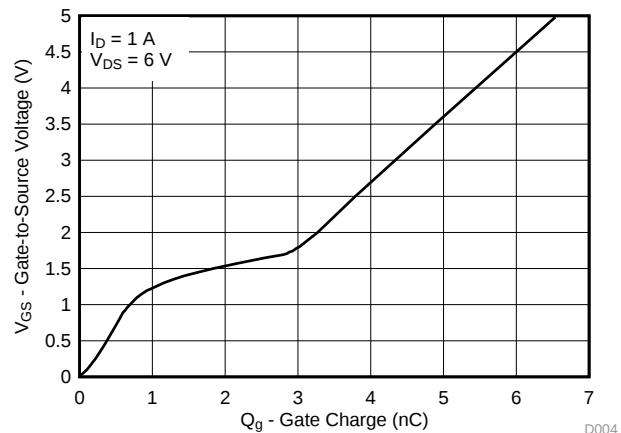
$T_A = 25^\circ\text{C}$		值	单位
V_{DS}	漏源电压	12	V
V_{GS}	栅源电压	±10	V
I_D	持续漏极电流 ⁽¹⁾	1.6	A
I_{DM}	脉冲漏极电流 ⁽²⁾	29	A
P_D	功耗 ⁽³⁾	1.8	W
T_J, T_{stg}	运行结温和 储存温度范围	-55 至 150	°C

(1) 器件在 105°C 温度下运行

(2) $R_{\theta JA} = 170^\circ\text{C/W}$ （覆铜面积最小时的典型值），脉宽 ≤ 100μs，占空比 ≤ 1%

(3) $R_{\theta JA} = 70^\circ\text{C/W}$ （覆铜面积最大时的典型值）

栅极电荷



D004



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4 修订历史记录

日期	修订版本	注释
2015 年 3 月	*	最初发布。

5 Specifications

5.1 Electrical Characteristics

 $(T_A = 25^{\circ}\text{C})$

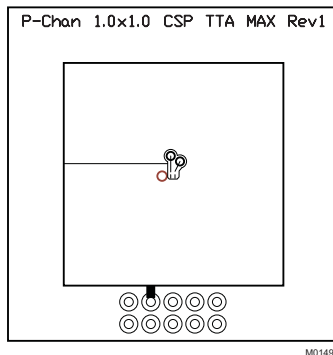
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-Source Voltage	V _{GS} = 0 , I _D = 250 μA	12			V
I _{DSS}	Drain-to-Source Leakage Current	V _{GS} = 0 V, V _{DS} = 9.6 V			1	μA
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = 10 V			100	nA
V _{GS(th)}	Gate-to-Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	0.7	1.0	1.3	V
R _{DS(on)}	Drain-to-Source On-Resistance	V _{GS} = 2.5 V, I _D = 1 A		21.2	25.8	mΩ
		V _{GS} = 4.5 V, I _D = 1 A		14.6	17.1	
g _{fs}	Transconductance	V _{DS} = 1.2 V, I _D = 1 A		10		S
DYNAMIC CHARACTERISTICS						
C _{ISS}	Input Capacitance	V _{GS} = 0 V, V _{DS} = 6 V, f = 1 MHz		663	862	pF
C _{OSS}	Output Capacitance			211	274	pF
C _{RSS}	Reverse Transfer Capacitance			151	196	pF
R _g	Series Gate Resistance			3.6	7.2	Ω
Q _g	Gate Charge Total (4.5 V)	V _{DS} = 6 V, I _D = 1 A		6.0	7.8	nC
Q _{gd}	Gate Charge Gate-to-Drain			2.1		nC
Q _{gs}	Gate Charge Gate-to-Source			0.7		nC
Q _{g(th)}	Gate Charge at V _{th}			0.7		nC
Q _{OSS}	Output Charge	V _{DS} = 6 V, V _{GS} = 0 V		1.3		nC
t _{d(on)}	Turn On Delay Time	V _{DS} = 6 V, V _{GS} = 4.5 V, I _D = 1 A R _G = 0 Ω		6		ns
t _r	Rise Time			7		ns
t _{d(off)}	Turn Off Delay Time			17		ns
t _f	Fall Time			7		ns
DIODE CHARACTERISTICS						
V _{SD}	Diode Forward Voltage	I _S = 1 A, V _{GS} = 0 V		0.7	1.0	V
Q _{rr}	Reverse Recovery Charge	V _{DS} = 6 V, I _S = 1 A, di/dt = 200 A/μs		11.6		nC
t _{rr}	Reverse Recovery Time			19.6		ns

5.2 Thermal Information

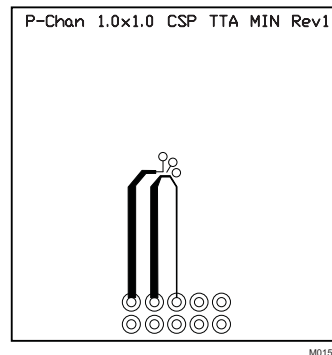
 $(T_A = 25^{\circ}\text{C}$ unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ⁽¹⁾		275		$^{\circ}\text{C}/\text{W}$
	Junction-to-Ambient Thermal Resistance ⁽²⁾		70		

(1) Device mounted on FR4 material with minimum Cu mounting area.

(2) Device mounted on FR4 material with 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu.


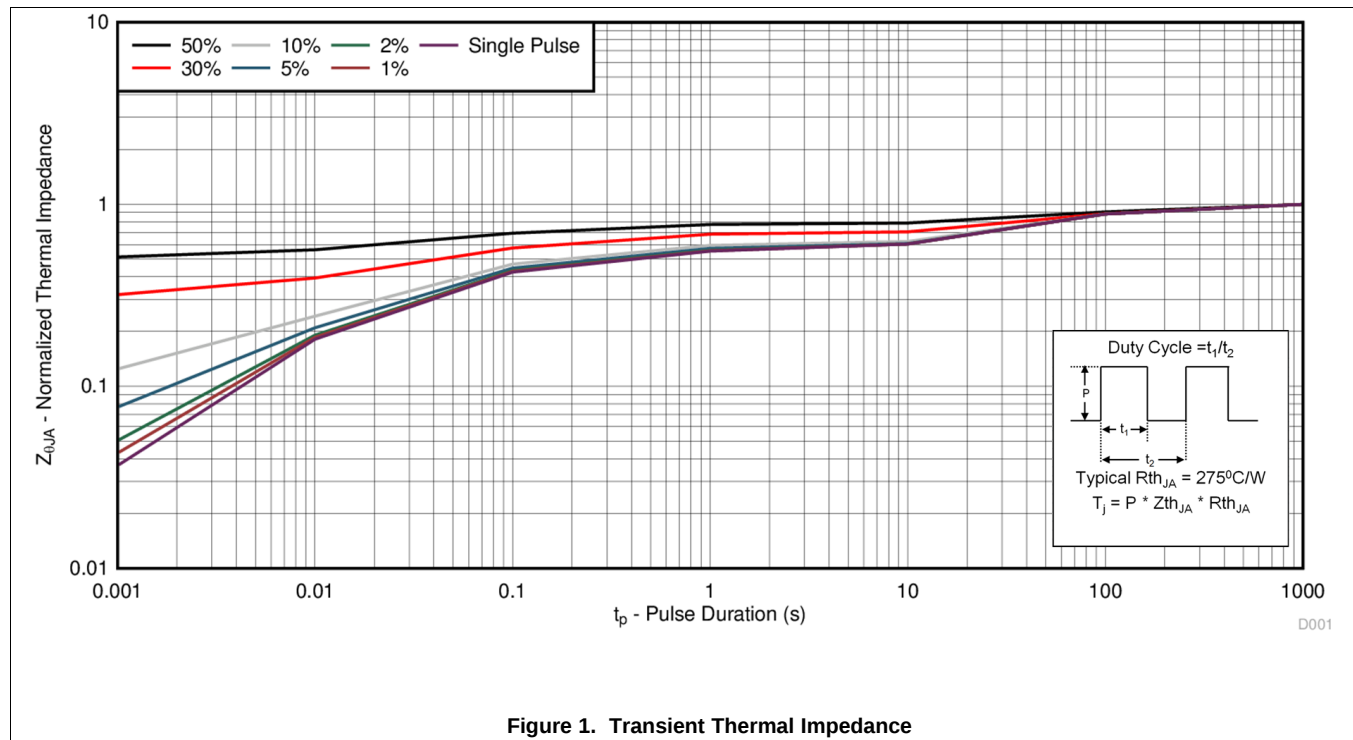
Typical $R_{\theta JA} = 70^{\circ}\text{C}/\text{W}$
when mounted on
1 inch² of 2 oz. Cu.



Typical $R_{\theta JA} = 275^{\circ}\text{C}/\text{W}$
when
mounted on minimum
pad area of 2 oz. Cu.

5.3 Typical MOSFET Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)



Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

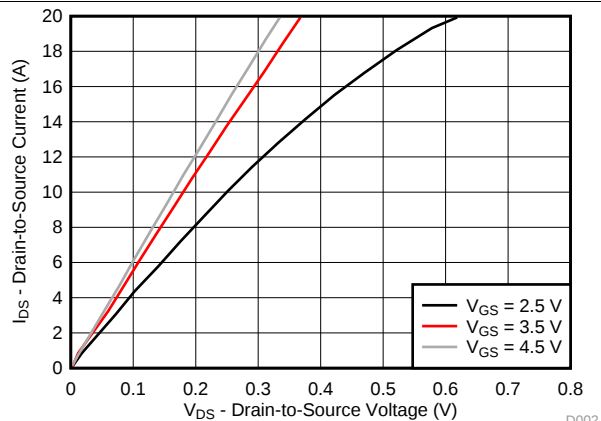


Figure 2. Saturation Characteristics

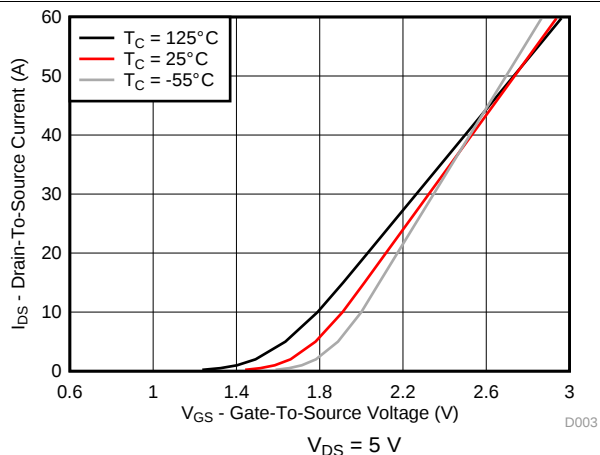


Figure 3. Transfer Characteristics

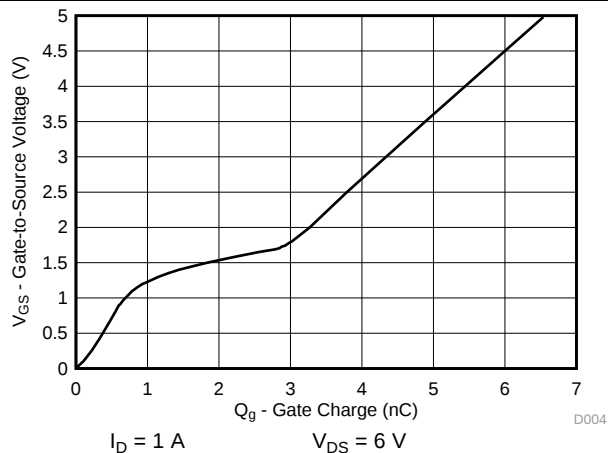


Figure 4. Gate Charge

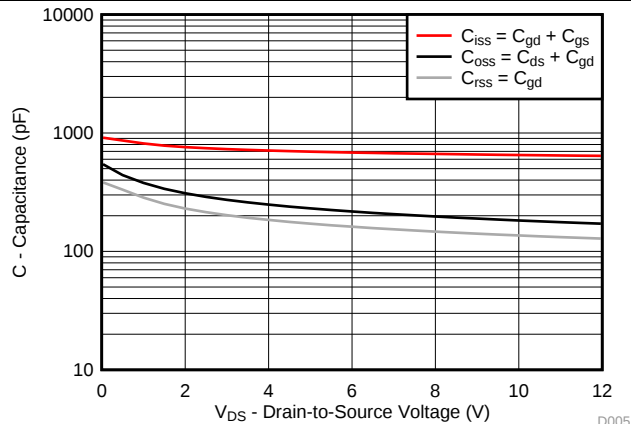


Figure 5. Capacitance

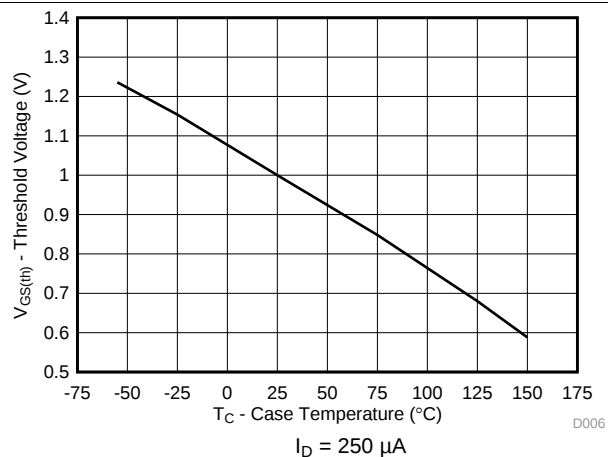


Figure 6. Threshold Voltage vs Temperature

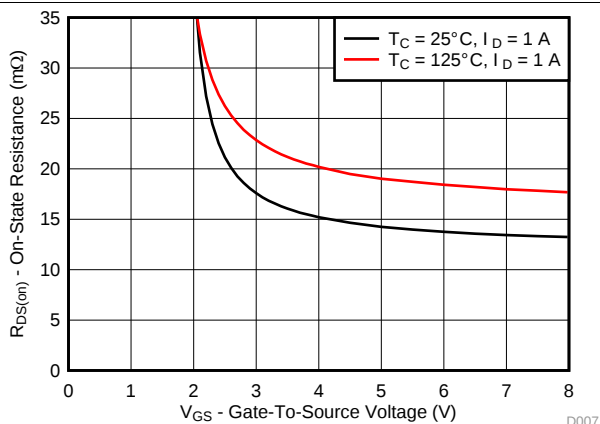


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

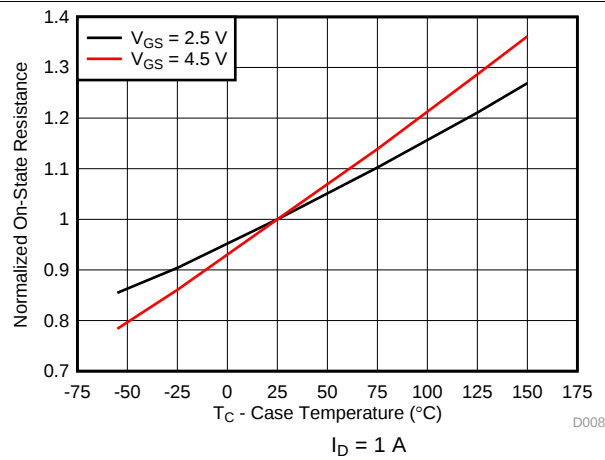


Figure 8. Normalized On-State Resistance vs Temperature

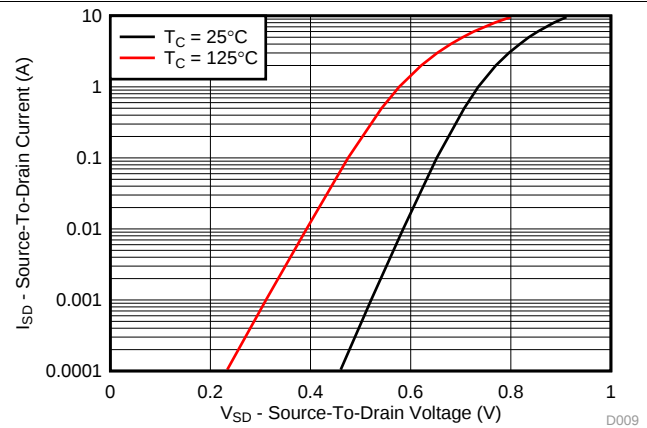


Figure 9. Typical Diode Forward Voltage

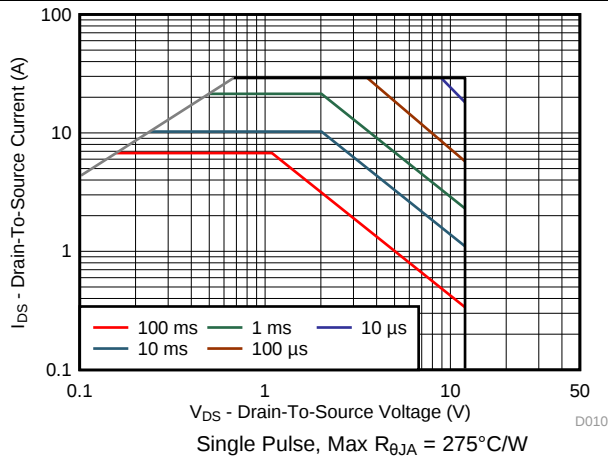


Figure 10. Maximum Safe Operating Area

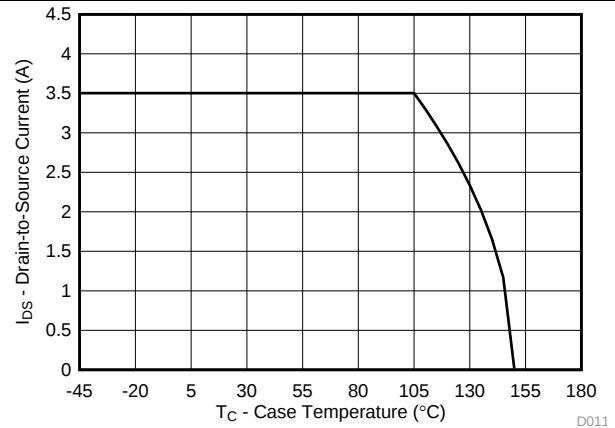


Figure 11. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 商标

NexFET is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

6.2 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.3 术语表

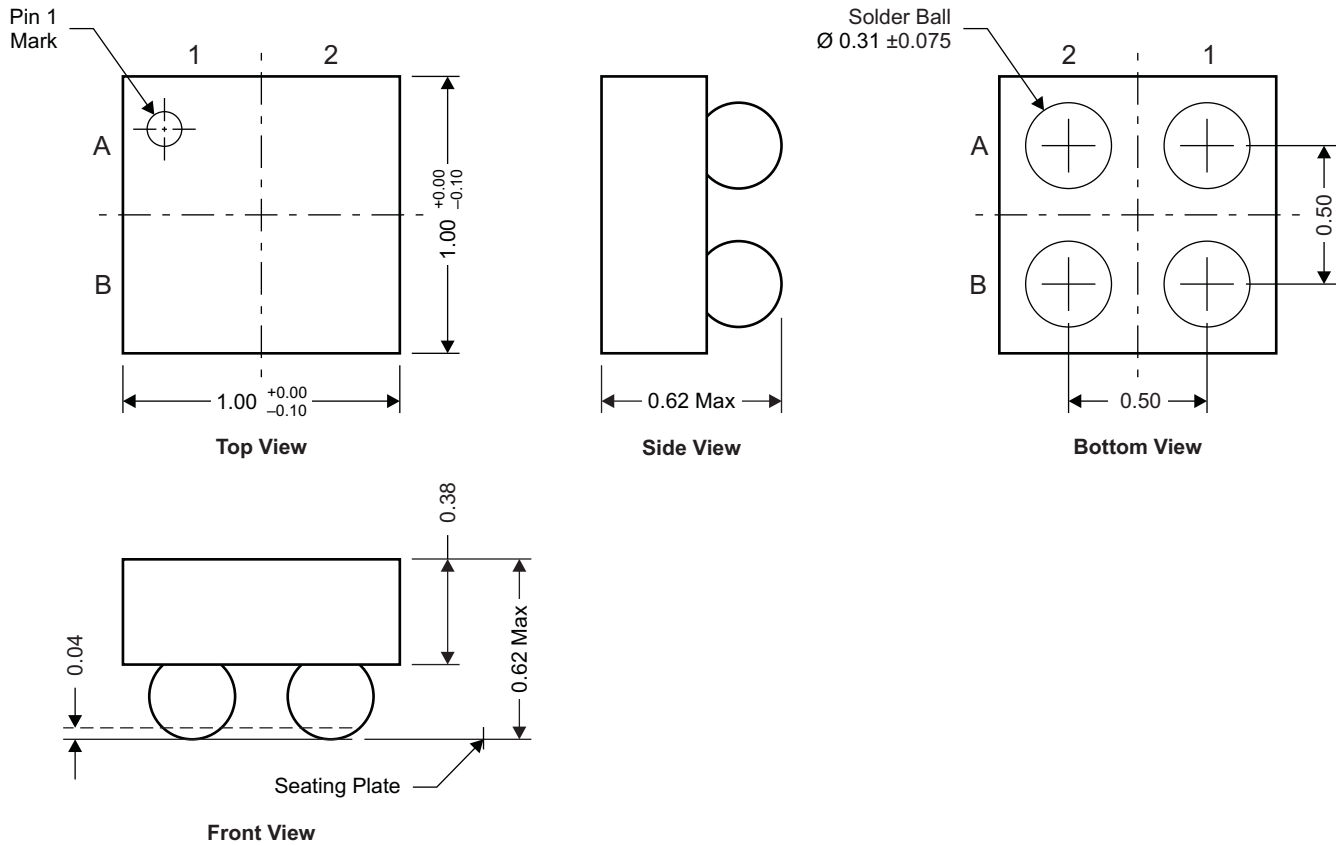
[SLYZ022](#) — TI 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

7 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

7.1 CSD13302W 封装尺寸



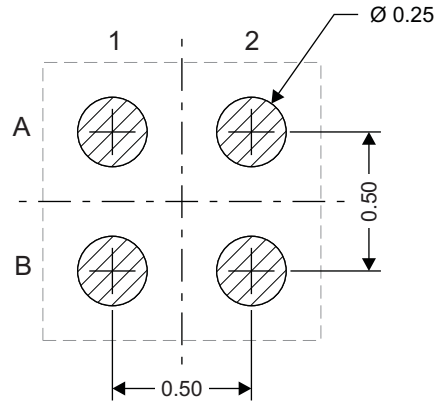
NOTE: 全部尺寸单位为 mm (除非另外注明)

M0151-01

引脚配置表

位置	名称
A2	源极
A1	栅极
B1, B2	漏极

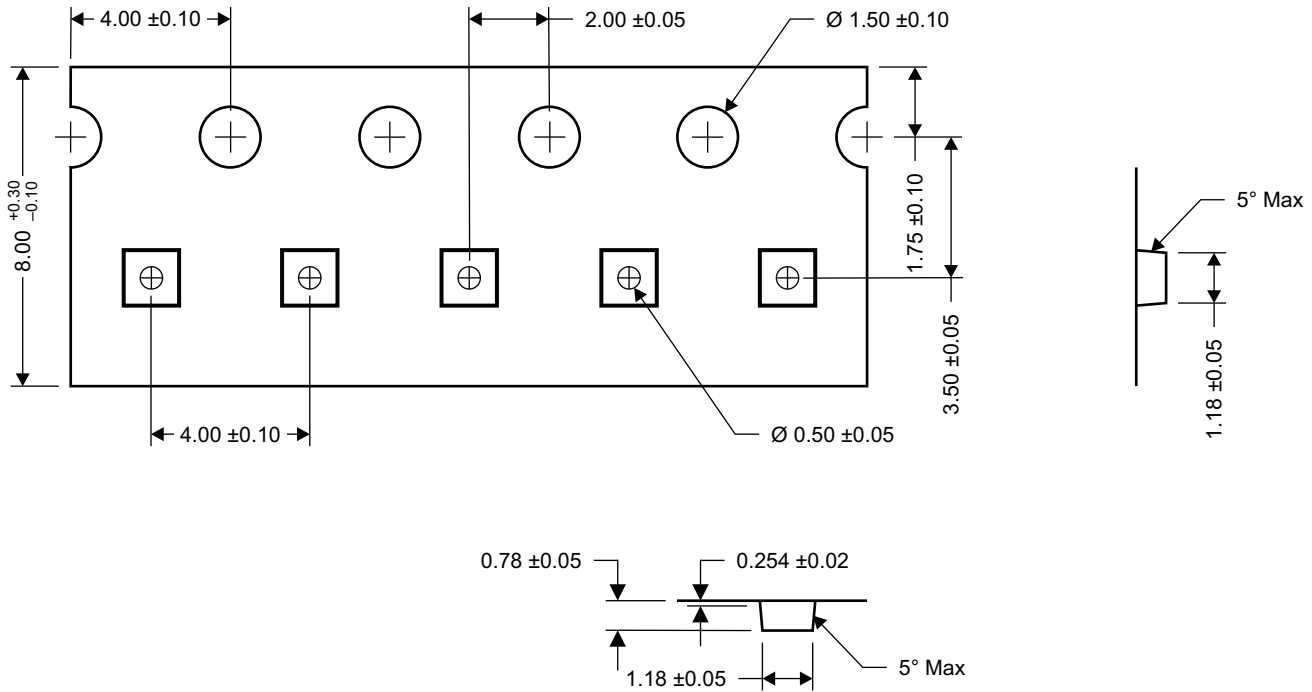
焊盘布局建议



M0152-01

NOTE: 全部尺寸单位为 mm (除非另外注明)

7.2 卷带信息



M0153-01

NOTE: 全部尺寸单位为 mm (除非另外注明)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD13302W	Active	Production	DSBGA (YZB) 4	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 150	302
CSD13302W.B	Active	Production	DSBGA (YZB) 4	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 150	302
CSD13302WT	Active	Production	DSBGA (YZB) 4	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 150	302
CSD13302WT.B	Active	Production	DSBGA (YZB) 4	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-55 to 150	302

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

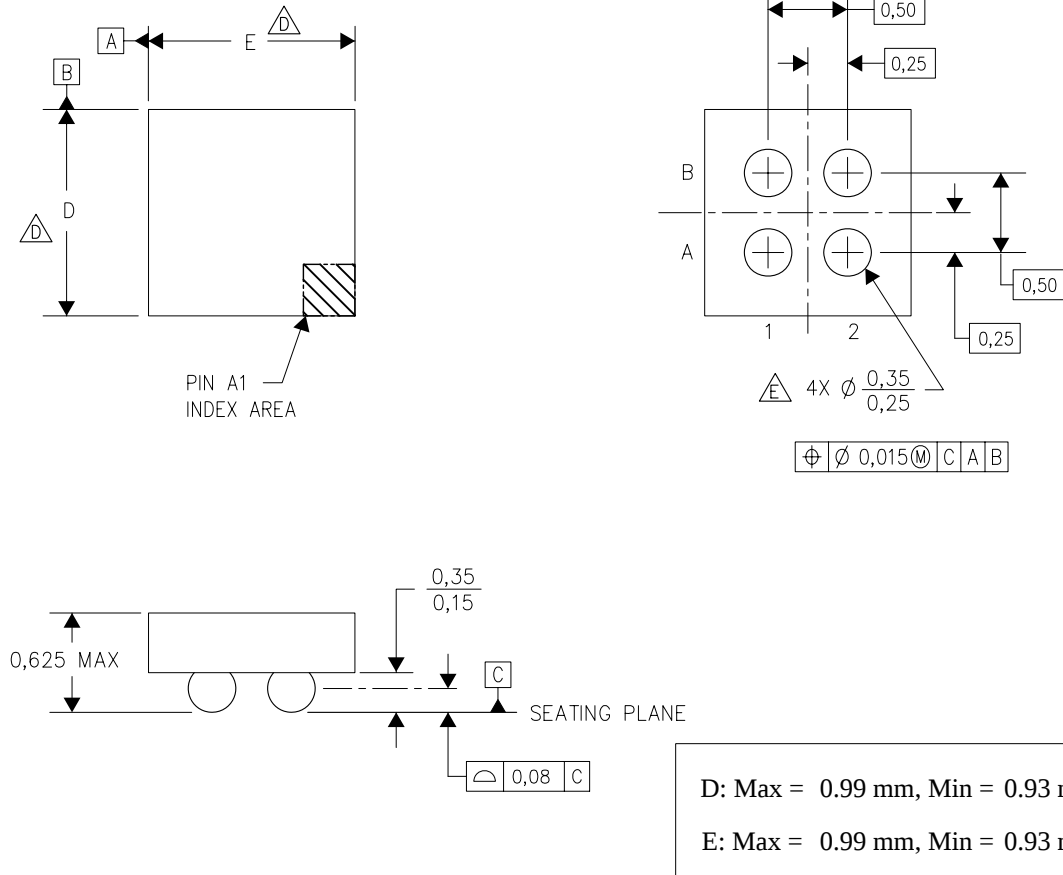
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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YZB (S-XBGA-N4)

DIE-SIZE BALL GRID ARRAY



4205055/D 07/08

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - $\triangle D$. Devices in YZB package can have dimension D ranging from 0.94 to 1.65 mm and dimension E ranging from 0.94 to 1.65 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
 - E. Reference Product Data Sheet for array population.
2 x 2 matrix pattern is shown for illustration only.
 - F. This package contains lead-free balls.
Refer to YEB (Drawing #4204178) for tin-lead (SnPb) balls.

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