CDCS504-Q1 时钟缓冲器和时钟乘法器

1 特性

- 符合汽车应用 标准
- 具有下列结果的 AEC-Q100 测试指南：
  - 器件温度 2 级：–40°C 至 105°C 的环境运行温度范围
  - 器件人体放电模式 (HBM) 静电放电 (ESD) 分类等级 H2
  - 器件组件充电模式 (CDM) ESD 分类等级 C3B
- 属于易用型时钟发生器器件系列的一部分
- 具有可选输出频率的时钟乘法器
- 可使用一个外部控制引脚来选择 x1 或者 x4 的频率倍乘
- 通过控制引脚进行输出禁用
- 单一 3.3V 器件电源
- 宽温度范围：-40°C 至 105°C
- 节省空间的 8 引脚薄型小外形尺寸 (TSSOP) 封装
- 使用 CDCS504-Q1 并借助 WEBENCH® 电源设计器创建定制设计方案

2 应用

汽车 应用 （需要时钟倍乘）

3 说明

CDCS504-Q1 器件是一款带有可选频率倍乘的 LVCMOS 输入时钟缓冲器。

CDCS504-Q1 具有输出使能引脚。

此器件在输入上接受一个 3.3V LVCMOS 信号。

这个输入信号由一个锁相环路 (PLL) 处理，此环路的输出频率或者与输入频率相等或者被乘以因子 4。

这样一来，该器件可生成介于 2MHz 和 108MHz 之间的输出频率。

独立的控制引脚可用于启用或者禁用输出。CDCS504-Q1 器件在 3.3V 环境下工作。

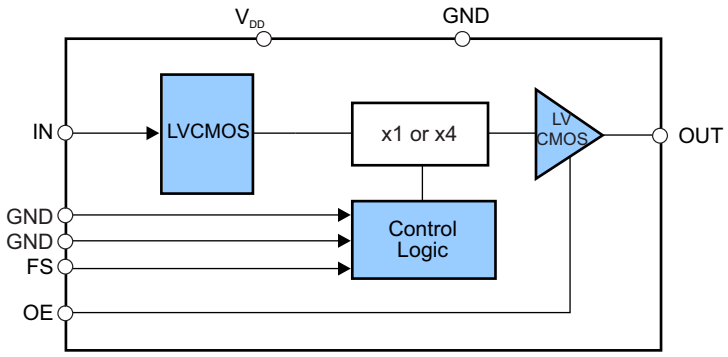
其特征在于运行温度范围介于 -40°C 至 105°C 之间，并采用 8 引脚 TSSOP 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
CDCS504-Q1	TSSOP (8)	3.00mm x 4.40mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

框图



目录

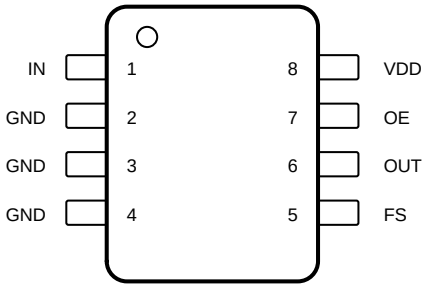
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	注释
2017 年 4 月	*	初始发行版。

5 Pin Configuration and Functions

PW Package
8-Pin TSSOP
Top View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
FS	5	I	Frequency multiplication selection, internal pullup
GND	2, 3, 4	Ground	Ground
IN	1	I	LVCMOS clock input
OE	7	I	Output enable, internal pullup
OUT	6	O	LVCMOS clock output
VDD	8	Power	3.3-V power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	–0.5	4.6	V
V_{IN}	Input voltage	–0.5	4.6	V
V_{out}	Output voltage	–0.5	4.6	V
I_{IN}	Input current ($V_I < 0$, $V_I > V_{DD}$)		20	mA
I_{out}	Continuous output current		50	mA
T_J	Maximum junction temperature		125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±1500	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		3		3.6	V
f_{IN}	Input frequency	FS = 0	2		27	MHz
		FS = 1	2		27	
V_{IL}	Low-level input voltage LVCMOS				0.3 × V_{DD}	V
V_{IH}	High-level input voltage LVCMOS		0.7 × V_{DD}			V
V_I	Input voltage threshold LVCMOS			0.5 × V_{DD}		V
C_L	Output load test LVCMOS				15	pF
I_{OH}/I_{OL}	Output current				±12	mA
T_A	Operating free-air temperature		–40		105	°C

6.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)(1)

THERMAL METRIC(2)				CDCS504-Q1 PW (TSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance			179.9	°C/W
		High K	Thermal Airflow (CFM) 0	149	
			Thermal Airflow (CFM) 150	142	
			Thermal Airflow (CFM) 250	138	
			Thermal Airflow (CFM) 500	132	
		Low K	Thermal Airflow (CFM) 0	230	
			Thermal Airflow (CFM) 150	185	
			Thermal Airflow (CFM) 250	170	
			Thermal Airflow (CFM) 500	150	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance			64.9	°C/W
		High K		65	
		Low K		69	
$R_{\theta JB}$	Junction-to-board thermal resistance			108.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter			9	°C/W
ψ_{JB}	Junction-to-board characterization parameter			107	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance			n/a	°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).
(2) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics – Device Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Device supply current	f_{in} = 3.072 MHz; FS = 1		24		mA
f_{OUT}	Output frequency	FS = 0	2		27	MHz
		FS = 1	8		108	
I_{IH}	LVCMOS input current	$V_I = V_{DD}$; V_{DD} = 3.6 V			10	µA
I_{IL}	LVCMOS input current	V_I = 0 V; V_{DD} = 3.6 V			–10	µA
V_{OH}	LVCMOS high-level output voltage	I_{OH} = -–0.1 mA	2.9			V
		I_{OH} = -–8 mA	2.4			
		I_{OH} = -–12 mA	2.2			

Electrical Characteristics – Device Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	LVCMOS low-level output voltage	I_{OL} = 0.1 mA			0.1	V
		I_{OL} = 8 mA			0.5	
		I_{OL} = 12 mA			0.8	
I_{OZ}	High-impedance-state output current	OE = Low	–2		2	µA
$t_{JIT(C-C)}$	Cycle to cycle jitter(1)	f_{out} = 11.264 MHz; FS = 1, 10000 Cycles		144		ps
t_r	Rise time(1)	20%–80%		0.65		ns
t_f	Fall time(1)	20%–80%		0.55		ns
O_{dc}	Output duty cycle(2)		45%		55%	

(1) Measured with Test Load, see Figure 4.
(2) Not production tested.

6.6 Typical Characteristics

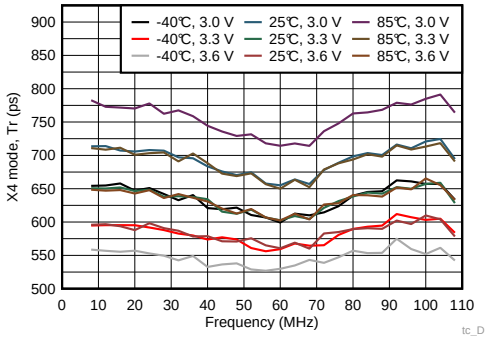


Figure 1. Typical Tr vs Output Frequency, VDD, Temperature in X4 Mode

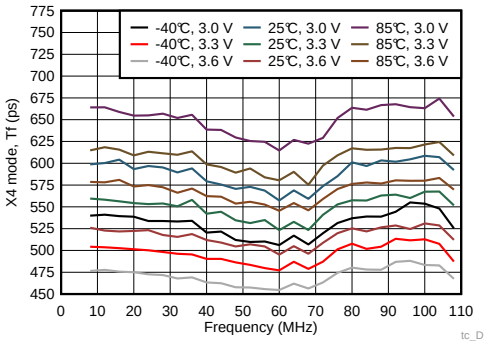
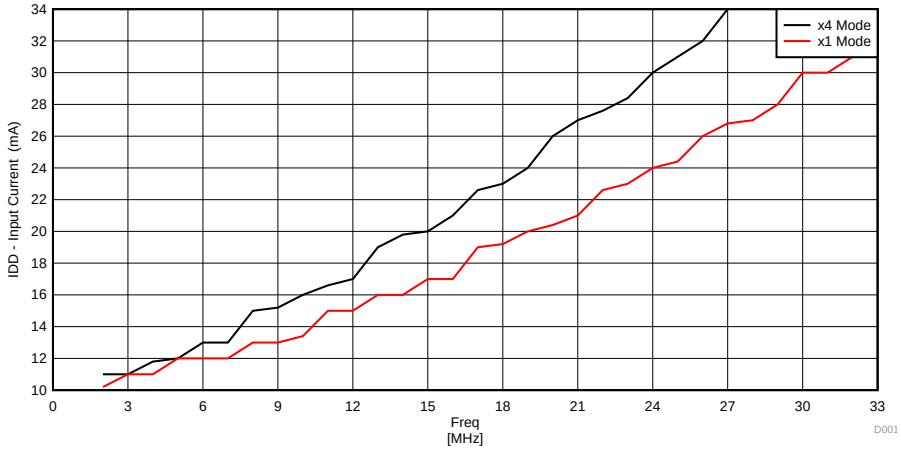


Figure 2. Typical Tf vs Output Frequency, VDD, Temperature in X4 Mode



V_{CC} = 3.3 V, output loaded with test load

Figure 3. I_{DD} vs Input Frequency

7 Parameter Measurement Information

7.1 Measurement Circuits

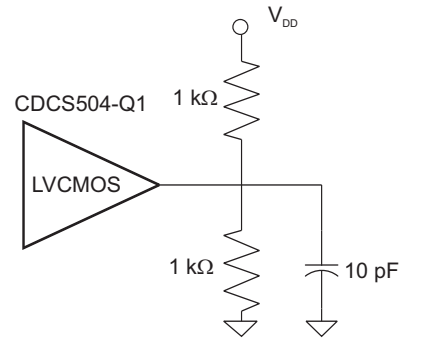


Figure 4. Test Load

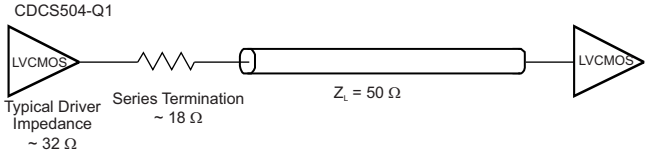


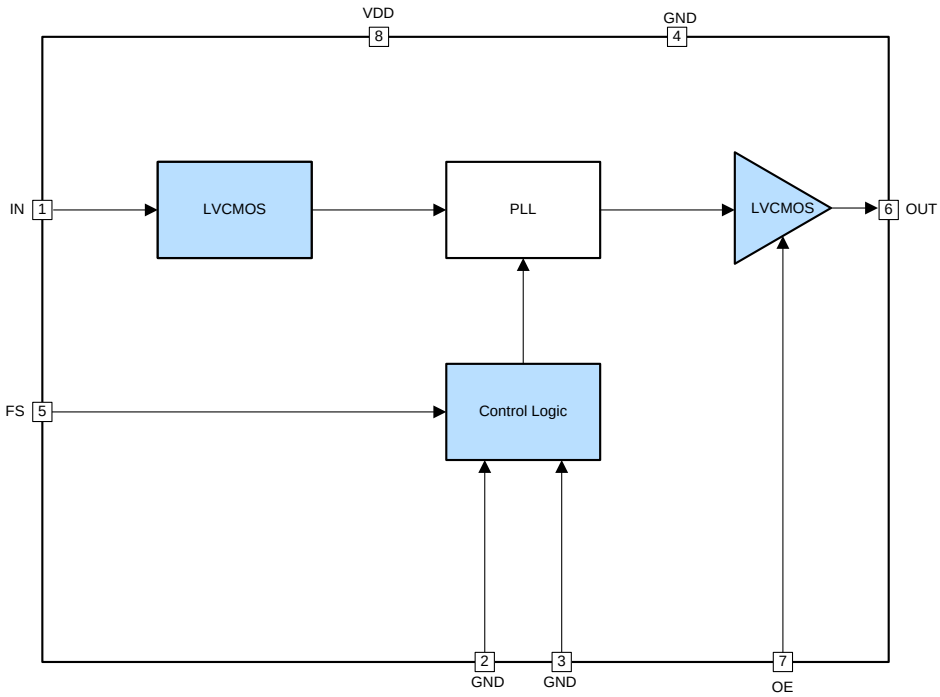
Figure 5. Load for 50-Ω Board Environment

8 Detailed Description

8.1 Overview

The CDCS504-Q1 is a LVCMOS clock buffer (x1 mode) or quadrupler (x4 mode). It integrates an internal PLL and generates a LVCMOS clock frequency range from 2 MHz to 108 MHz.

8.2 Functional Block Diagram



8.3 Feature Description

The CDCS504-Q1 is qualified for automotive applications with AEC-Q100 test, which could support wide temperature range from –40°C to 105°C. The device is easy to use, only need single 3.3-V power supply. The output enable or disable mode, along with frequency multiplication, could be controlled by external controls pins.

8.4 Device Functional Modes

When pin 7 OE is in low, the CDCS504-Q1 outputs 3-state. When pin 7 OE is set in high, the device would output clocks, output frequency depends on pin 5 FS status. FS = high enables frequency ×4 mode. FS= low makes output frequency equal to input frequency. If no input clock is provided, it is recommended to set OE=low in order to avoid random clock pulses from the internal PLL at the outputs.

Table 1. Function Table

OE	FS	f_{OUT}/f_{IN}	f_{OUT} at f_{in} = 27 MHz
0	x	x	3-state
1	0	1	27 MHz
1	1	4	108 MHz

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The CDCS504-Q1 is a clock buffer or multiplier for automotive amplifiers and infotainment. It is fit for the TAS6424-Q1, a four-channel, class-D, digital-input audio-amplifier, when the applications are without available MCLK. See Figure 6 for more details.

9.2 Typical Application

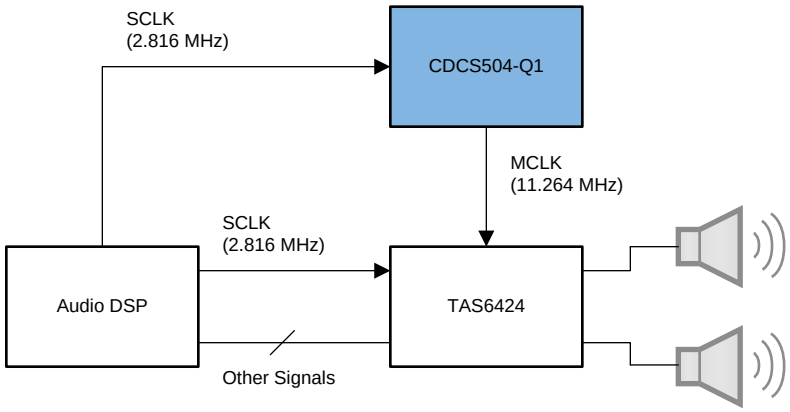


Figure 6. Clock for Automotive Amplifiers

9.2.1 Design Requirements

The CDCS504-Q1 is supplied with a single-power 3.3 V. The device supports minimum input frequency to 2 MHz. For maximum input frequency, it is 32 MHz in ×1 mode, and 27 MHz in ×4 mode. The input clock is LVCMOS type and should satisfy requirements in the *Recommended Operating Conditions*.

9.2.2 Detailed Design Procedure

In some applications, the clock input for CDCS504-Q1 is not always presented. In case there is an unexpected clock output without clock input, TI recommends setting OE pin to low. When it gets clock input ready, set OE pin to high to get expected clock output. If the other application presents continuous clock input for CDCS504-Q1, the OE pin could be floated, internal pullup brings output enable, or an external pullup circuits could be used fixedly.

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the CDCS504-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

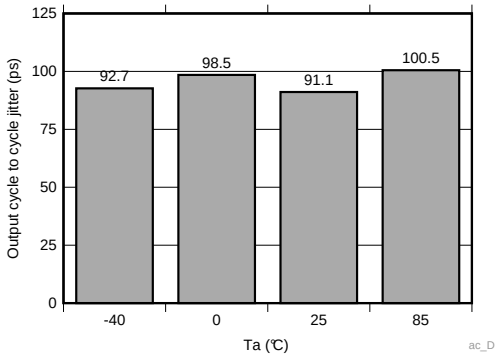
Typical Application (continued)

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

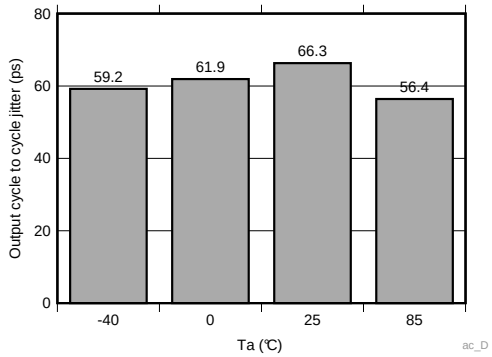
Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.3 Application Curves



X1 mode, 8-MHz input, 8-MHz output, VDD = 3.3 V

Figure 7. Typical Cycle-to-Cycle Jitter vs Temperature



X4 mode, 27.5-MHz input, 110-MHz output, VDD = 3.3 V

Figure 8. Typical Cycle-to-Cycle Jitter vs Temperature

10 Power Supply Recommendations

The CDCS504-Q1 requires a 3.3-V supply.

11 Layout

11.1 Layout Guidelines

The CDCS504-Q1 only has typical 20-mA supply current, so there is no thermal design challenge. A 0.01-µF capacitor may be placed close to VDD pin as a bypass capacitor.

11.2 Layout Example

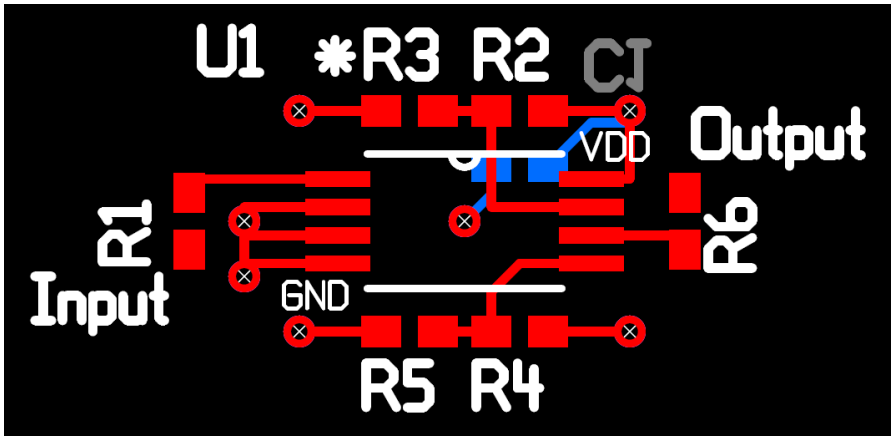


Figure 9. Layout Example

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

12.1.1.1 使用 WEBENCH® 工具定制设计方案

请单击此处，借助 WEBENCH® 电源设计器并使用 CDCS504-Q1 器件创建定制设计方案。

1. 在开始阶段键入输出电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化关键设计参数，如效率、封装和成本。
3. 将生成的设计与德州仪器 (TI) 的其他解决方案进行比较。

WEBENCH Power Designer 提供一份定制原理图以及罗列实时价格和组件可用性的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案导出至常用 CAD 格式
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com/WEBENCH。

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商标

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDCS504TPWRQ1	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	CS504Q
CDCS504TPWRQ1.B	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	CS504Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

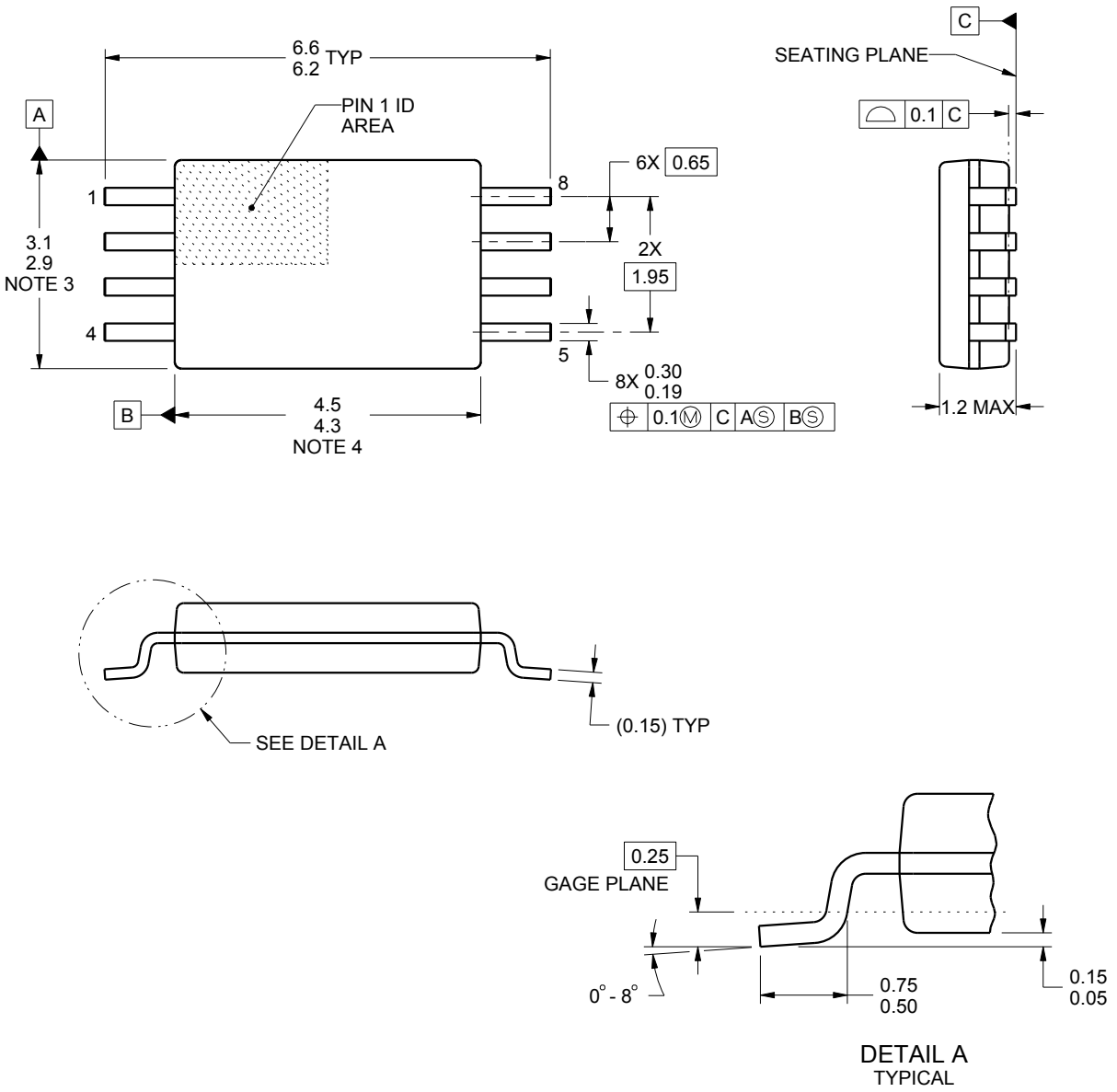
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

PW0008A

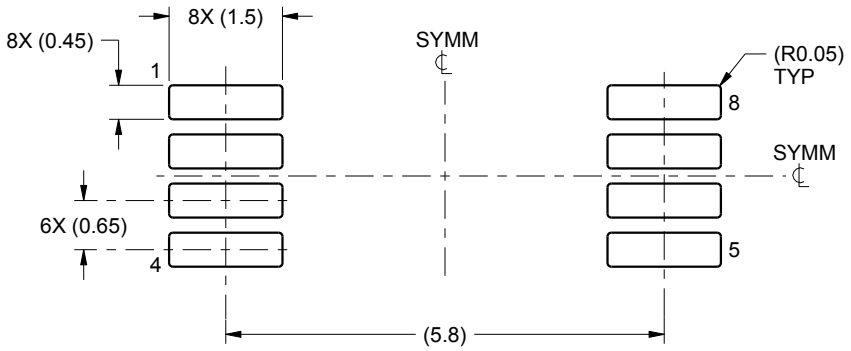
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

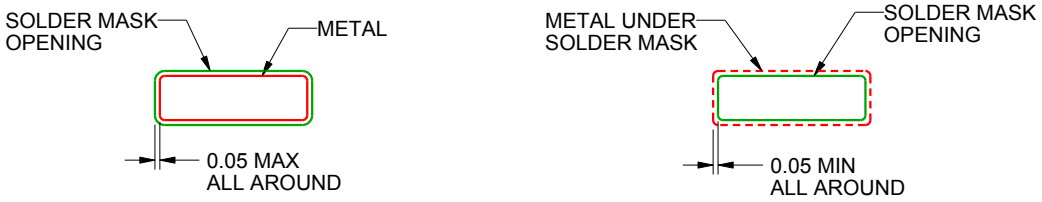


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

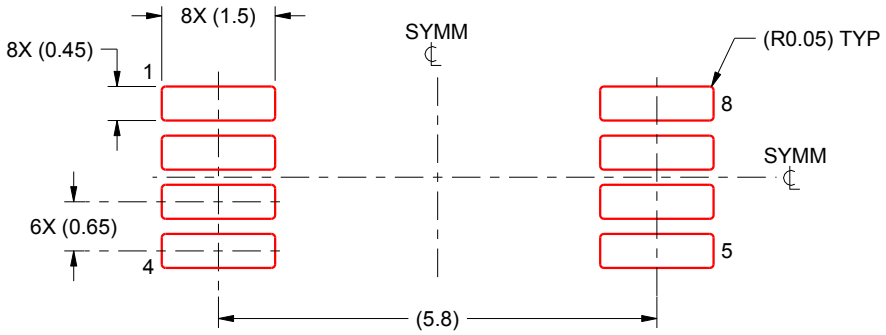


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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