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4 Pin Configuration and Functions

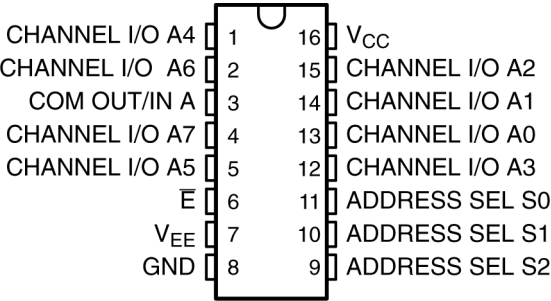


图 4-1. PW, D Package, 16-Pin TSSOP, SOIC (Top View)

表 4-1. Function Table

INPUTS				ON CHANNEL(S)
E	S ₂	S ₁	S ₀	
L	L	L	L	A0
L	L	L	H	A1
L	L	H	L	A2
L	L	H	H	A3
L	H	L	L	A4
L	H	L	H	A5
L	H	H	L	A6
L	H	H	H	A7
H	X	X	X	None

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

			MIN	MAX	UNIT
$V_{CC} - V_{EE}$ (see ⁽²⁾)	Supply voltage range		-0.5	10.5	V
V_{CC}	Supply voltage range		-0.5	7	V
V_{EE}	Supply voltage range		+0.5	-7	V
I_{IK} ($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$)	Input clamp current			±20	mA
I_{OK} ($V_O < V_{EE} - 0.5V$ or $V_O > V_{CC} + 0.5V$)	Output clamp current			±20	mA
($V_I > V_{EE} - 0.5V$ or $V_I < V_{CC} + 0.5V$)	Switch current			±25	mA
	Continuous current through V_{CC} or GND			±50	mA
I_{EE}	V_{EE} current			-20	mA
$R_{\theta JA}$	Package thermal impedance	D package		91.6	°C/W
		PW package		116.5	°C/W
T_J	Maximum junction temperature			150	°C
Lead temperature (during soldering):		At distance 1/16 ± 1/32 inch (1,59 ± 0,79 mm) from case for 10 s max		300	°C
T_{stg}	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to GND unless otherwise specified.

5.2 Recommended Operating Conditions

(see ⁽¹⁾)

			MIN	MAX	UNIT
V_{CC}	Supply voltage (see ⁽²⁾)		2	6	V
	Supply voltage, $V_{CC} - V_{EE}$ (see 图 5-1)		2	10	V
V_{EE}	Supply voltage, (see ⁽²⁾ and 图 5-2)		0	-6	V
V_{IH}	High-level input voltage	$V_{CC} = 2V$	1.5		V
		$V_{CC} = 4.5V$	3.15		
		$V_{CC} = 6V$	4.2		
V_{IL}	Low-level input voltage	$V_{CC} = 2V$		0.5	V
		$V_{CC} = 4.5V$		1.35	
		$V_{CC} = 6V$		1.8	
V_I	Input control voltage		0	V_{CC}	V
V_{IS}	Analog switch I/O voltage		V_{EE}	V_{CC}	V
t_t	Input transition (rise and fall) time	$V_{CC} = 2V$	0	1000	ns
		$V_{CC} = 4.5V$	0	500	
		$V_{CC} = 6V$	0	400	
T_A	Operating free-air temperature		-40	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

- (2) In certain applications, the external load resistor current may include both V_{CC} and signal-line components. To avoid drawing V_{CC} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.6V (calculated from r_{on} values shown in electrical characteristics table). No V_{CC} current flows through R_L if the switch current flows into the COM OUT/IN A terminal.

5.3 Recommended Operating Area as a Function of Supply Voltages

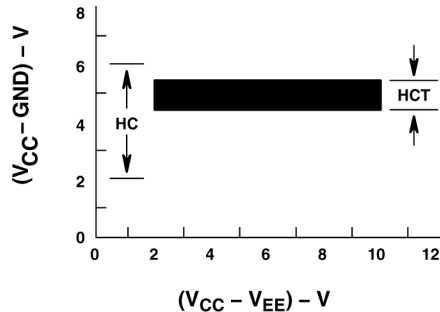


图 5-1. $(V_{CC} - V_{EE}) - V$

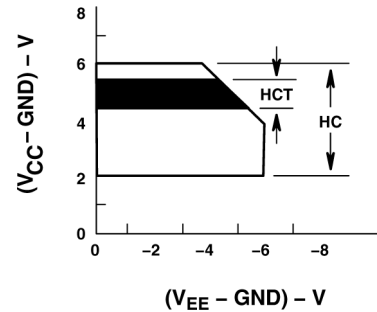


图 5-2. $(V_{EE} - GND) - V$

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{EE}	V _{CC}	T _A = 25 °C			T _A = -40 °C TO 125°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
r _{on}	I _O = 1 mA, V _I = V _{IH} or V _{IL} , See 图 5-3	V _{IS} = V _{CC} or V _{EE}	0V	4.5V		70	160		240	Ω
			0V	6V		60	140		210	
			-4.5 V	4.5V		40	120		180	
		V _{IS} = V _{CC} to V _{EE}	0V	4.5V		90	180		270	
			0V	6V		80	160		240	
			-4.5 V	4.5V		45	130		195	
Δ r _{on}	Between any two channels	0V	4.5V		10				Ω	
		0V	6V		8.5					
		-4.5 V	4.5V		5					
I _{Iz}	For switch OFF: When V _{IS} = V _{CC} , V _{OS} = V _{EE} ; When V _{IS} = V _{EE} , V _{OS} = V _{CC} For switch ON: All applicable combinations of V _{IS} and V _{OS} voltage levels, V _I = V _{IH} or V _{IL}	0V	6V			±0.2		±2	μ A	
		-5V	5V			±0.4		±4		
I _{IL}	V _I = V _{CC} or GND		0V	6V			±0.1		±1	μ A
I _{CC}	I _O = 0, V _I = V _{CC} or GND	When V _{IS} = V _{EE} , V _{OS} = V _{CC}	0V	6V			12		160	μ A
		When V _{IS} = V _{CC} , V _{OS} = V _{EE}	-5V	5V			32		320	

5.5 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see 图 6-5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V _{EE}	V _{CC}	T _A = 25°C			T _A = -40 °C TO 125°C		UNI T
						MIN	TYP	MAX	MIN	MA X	
t _{pd}	IN	OUT	C _L = 15pF		5V			4			ns
			C _L = 50pF	0V	2V			60		90	ns
					4.5V			12		18	
					6V			10		15	
				-4.5 V	4.5V			8		12	
t _{en}	ADDRESS SEL or $\bar{E}$	OUT	C _L = 15pF		5V			19			ns
			C _L = 50pF	0V	2V			325		490	
					4.5V			45		68	
					6V			38		57	
				-4.5 V	4.5V			32		48	
t _{dis}	ADDRESS SEL or $\bar{E}$	OUT	C _L = 15pF		5V			27			ns
			C _L = 50pF	0V	2V			250		400	
					4.5V			50		68	
					6V			44		57	
				-4.5 V	4.5V			44		55	
C _I	Control		C _L = 50pF					10		10	pF

5.6 Operating Characteristics

V_{CC} = 5V, T_A = 25°C, Input t_r, t_f = 6 ns

PARAMETER		TYP	UNIT
C _{pd}	Power dissipation capacitance (see (1))	50	pF

(1) C_{pd} is used to determine the dynamic power consumption, per package.

- $P_D = C_{pd} V_{CC}^2 f_I + \sum (C_L + C_S) V_{CC}^2 f_O$
- f_O = output frequency
- f_I = input frequency
- C_L = output load capacitance
- C_S = switch capacitance
- V_{CC} = supply voltage

5.7 Analog Channel Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{EE}	V _{CC}	MIN	TYP	MA X	UNI T
C _I	Switch input capacitance					5		pF
C _{COM}	Common output capacitance					25		pF
f _{max}	Minimum switch frequency response at -3 dB	See 图 6-1 and 图 5-4, and (1) and (2)	-2.25V	2.25V		145		MHz
			-4.5V	4.5V		180		

5.7 Analog Channel Characteristics (续)

 $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V_{EE}	V_{CC}	MIN	TYP	MAX	UNIT
THD	Sine-wave distortion	See 图 6-2	-2.25V	2.25V	0.03	5		%
			-4.5V	4.5V	0.01	8		
O_{ISO}	Switch OFF signal feed through	See 图 6-4 and 图 5-5, and (2) and (3)	-2.25V	2.25V	-73			dB
			-4.5V	4.5V	-75			

(1) Adjust input voltage to obtain 0 dBm at V_{OS} for $f_{IN} = 1\text{MHz}$.

(2) V_{IS} is centered at $(V_{CC} - V_{EE})/2$.

(3) Adjust input for 0 dBm.

5.8 Typical Characteristics

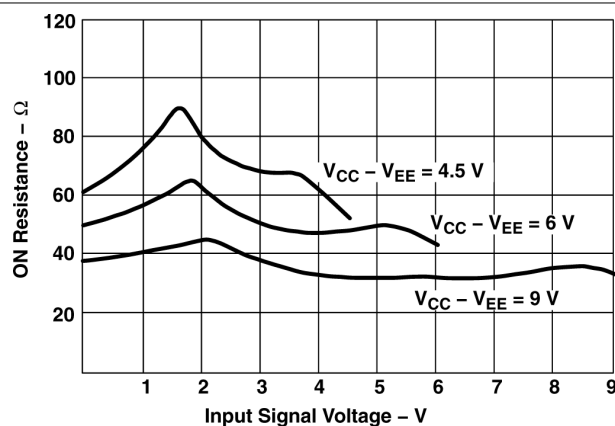


图 5-3. Typical on Resistance vs Input Signal Voltage

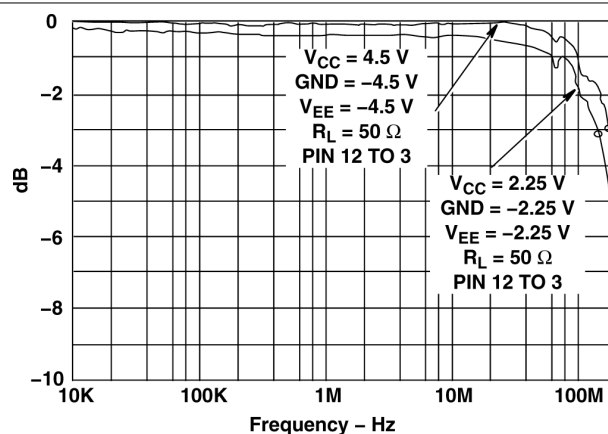


图 5-4. Channel on Bandwidth

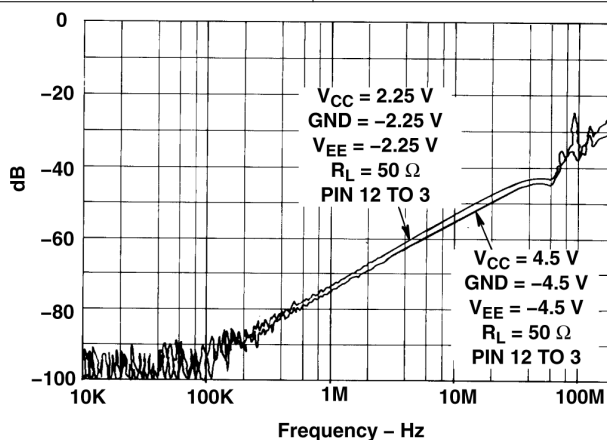


图 5-5. Channel off Feed-through

6 Parameter Measurement Information

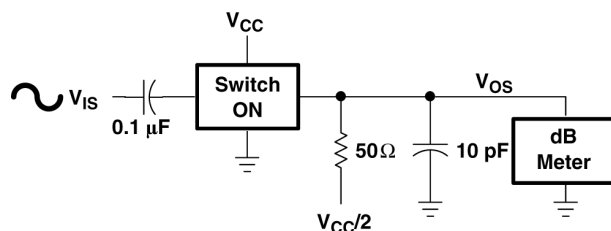


图 6-1. Frequency-Response Test Circuit

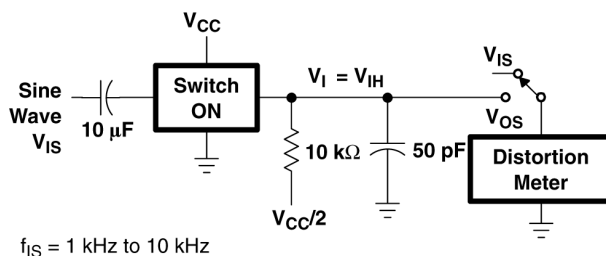


图 6-2. Sine-Wave Distortion Test Circuit

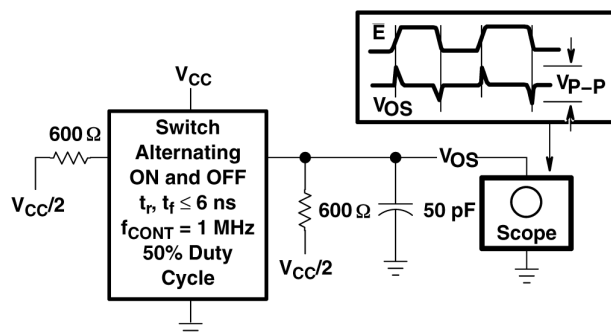


图 6-3. Control to Switch Feed-through Noise Test Circuit

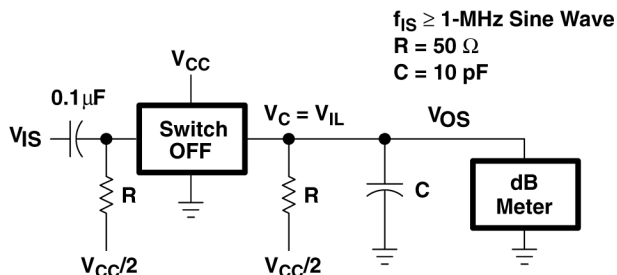
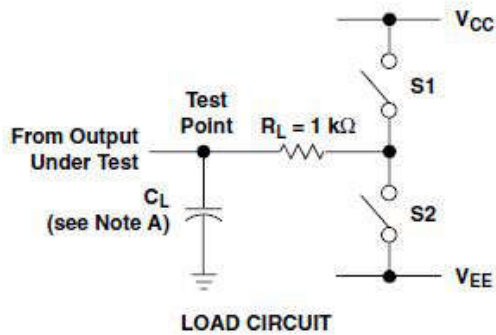
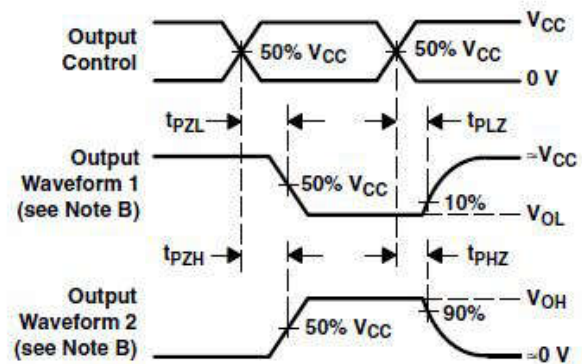
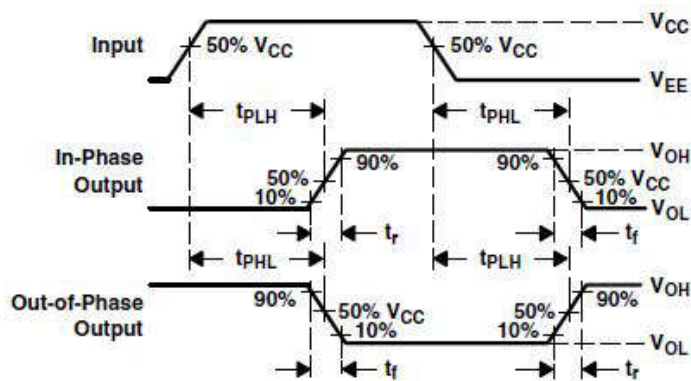


图 6-4. Switch off Signal Feed-through Test Circuit



PARAMETER		S1	S2
t_{en}	t_{pZH}	Open	Closed
	t_{pZL}	Closed	Open
t_{dis}	t_{pHZ}	Open	Closed
	t_{pLZ}	Closed	Open
t_{pd}		Open	Open



- A. C_L includes probe and test-fixture capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{MHz}$, $Z_O = 50\ \Omega$, $t_r = 6\text{ ns}$, $t_f = 6\text{ ns}$.
- D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
- E. The outputs are measured one at a time with one input transition per measurement.
- F. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- G. t_{PZL} and t_{PZH} are the same as t_{en} .
- H. t_{PLH} and t_{PHL} are the same as t_{pd} .

图 6-5. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Functional Block Diagram

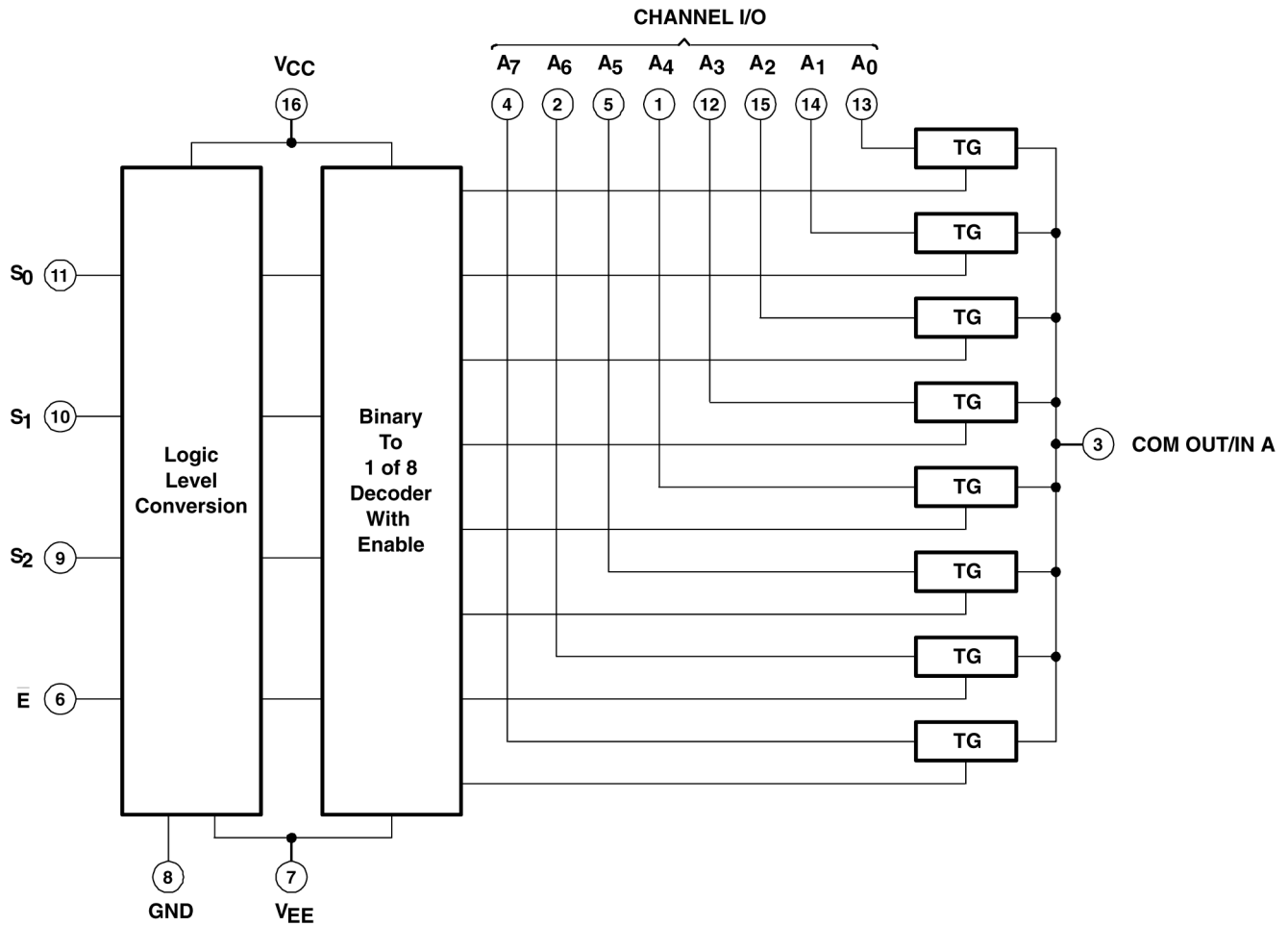


图 7-1. Logic Diagram (Positive Logic)

7.2 Device Functional Modes

表 7-1. Function Table

INPUTS				ON CHANNEL(S)
E	S ₂	S ₁	S ₀	
L	L	L	L	A0
L	L	L	H	A1
L	L	H	L	A2
L	L	H	H	A3
L	H	L	L	A4
L	H	L	H	A5
L	H	H	L	A6
L	H	H	H	A7
H	X	X	X	None

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

8.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (April 2008) to Revision B (April 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• 将 M (SOIC , 16) 更改为 D (SOIC , 16) ，以准确反映封装图.....	1
• Changed the package thermal impedance for the D package from: 73°C/W to: 91.6°C/W	3
• Changed the package thermal impedance for the PW package from: 108°C/W to: 116.5°C/W	3
• Changed I _{CC} MAX from: 8 μA to: 12 μA when V _{IS} = V _{EE} , V _{OS} = V _{CC} at a TA = 25°C	4
• Changed I _{CC} MAX from: 16 μA to: 32 μA when V _{IS} = V _{CC} , V _{OS} = V _{EE} at a TA = 25°C	4
• Changed t _{en} MAX from: 225ns to: 325ns when C _L = 50pF at a TA = 25°C and from: 340ns to: 490ns when C _L = 50pF at a TA = -40°C to 125°C.....	5
• Changed t _{dis} TYP from: 19ns to: 27ns when C _L = 15pF at a TA = 25°C.....	5
• Changed t _{dis} MAX from: 225ns to: 250ns when C _L = 50pF, V _{EE} = 0V, and V _{CC} = 2V at a TA = 25°C, and from: 340ns to: 400ns at a TA = -40°C to 125°C.....	5
• Changed t _{dis} MAX from: 45ns to: 50ns when C _L = 50pF, V _{EE} = 0V, and V _{CC} = 4.5V at a TA = 25°C.....	5
• Changed t _{dis} MAX from: 38ns to: 44ns when C _L = 50pF, V _{EE} = 0V, and V _{CC} = 6V at a TA = 25°C.....	5
• Changed t _{dis} MAX from: 32ns to: 44ns when C _L = 50pF, V _{EE} = -4.5V, and V _{CC} = 4.5V at a TA = 25°C, and from: 48ns to: 55ns at a TA = -40°C to 125°C.....	5
• Removed the TBD E or ADDRESS SEL to switch feed-through noise parameter.....	5

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74HC4051QM96G4Q1	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-40 to 125	HC4051Q
CD74HC4051QM96Q1	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4051Q
CD74HC4051QM96Q1.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4051Q
CD74HC4051QPWRG4Q1	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-40 to 125	HJ4051Q
CD74HC4051QPWRQ1	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HJ4051Q
CD74HC4051QPWRQ1.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HJ4051Q

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

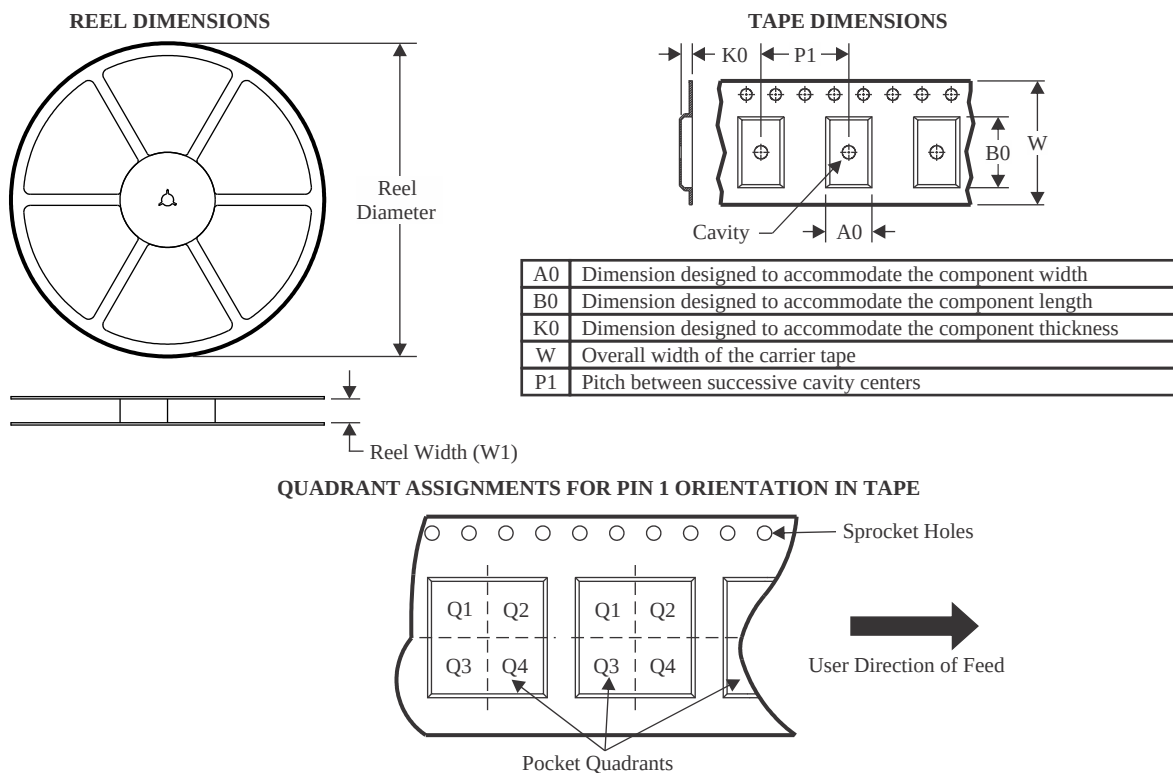
OTHER QUALIFIED VERSIONS OF CD74HC4051-Q1 :

- Catalog : [CD74HC4051](#)
- Enhanced Product : [CD74HC4051-EP](#)
- Military : [CD54HC4051](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

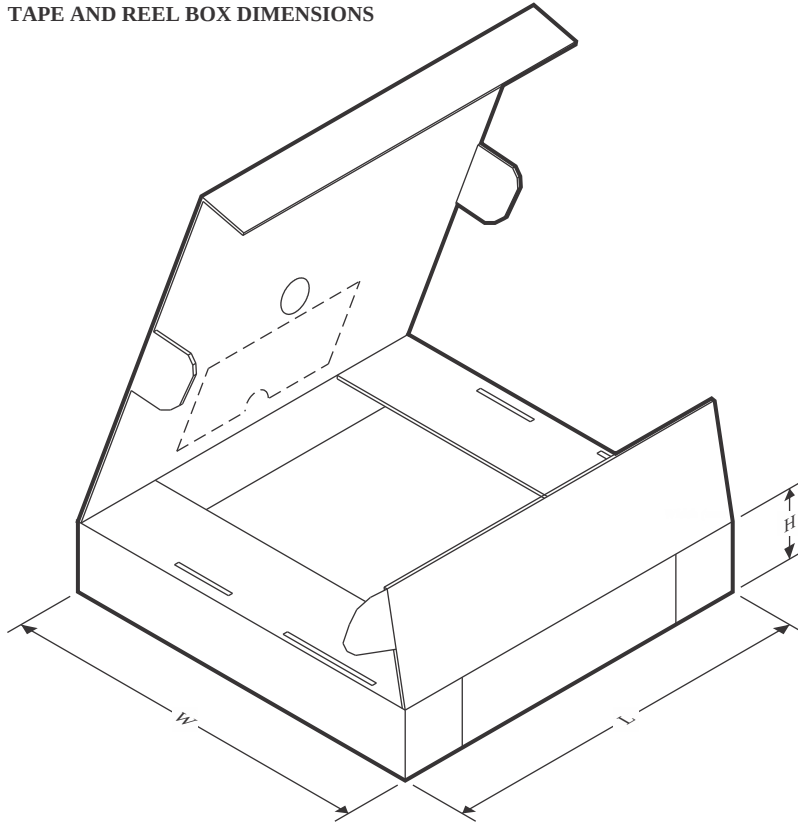
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4051QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4051QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

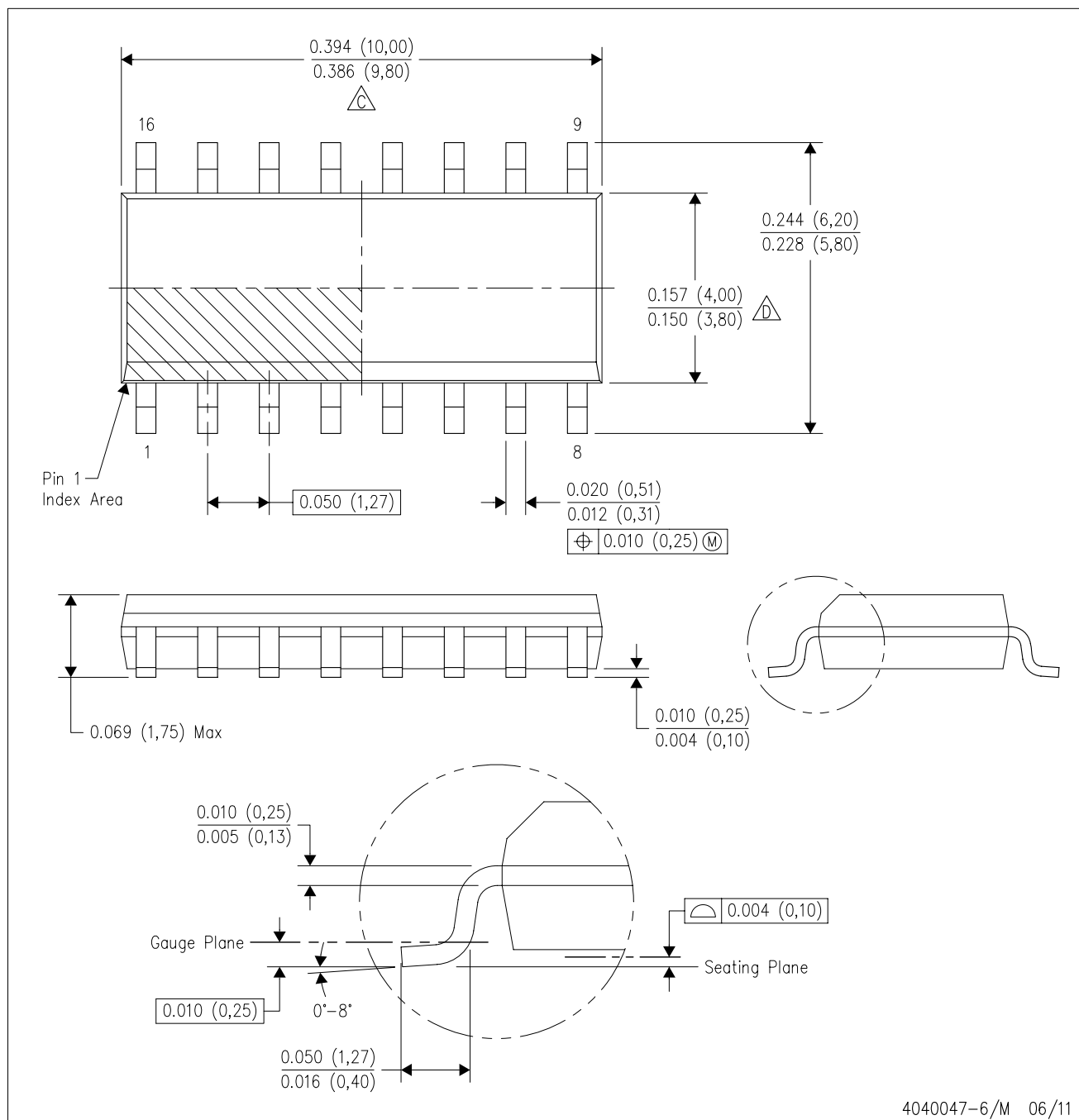


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4051QPWRQ1	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HC4051QPWRQ1	TSSOP	PW	16	2000	353.0	353.0	32.0

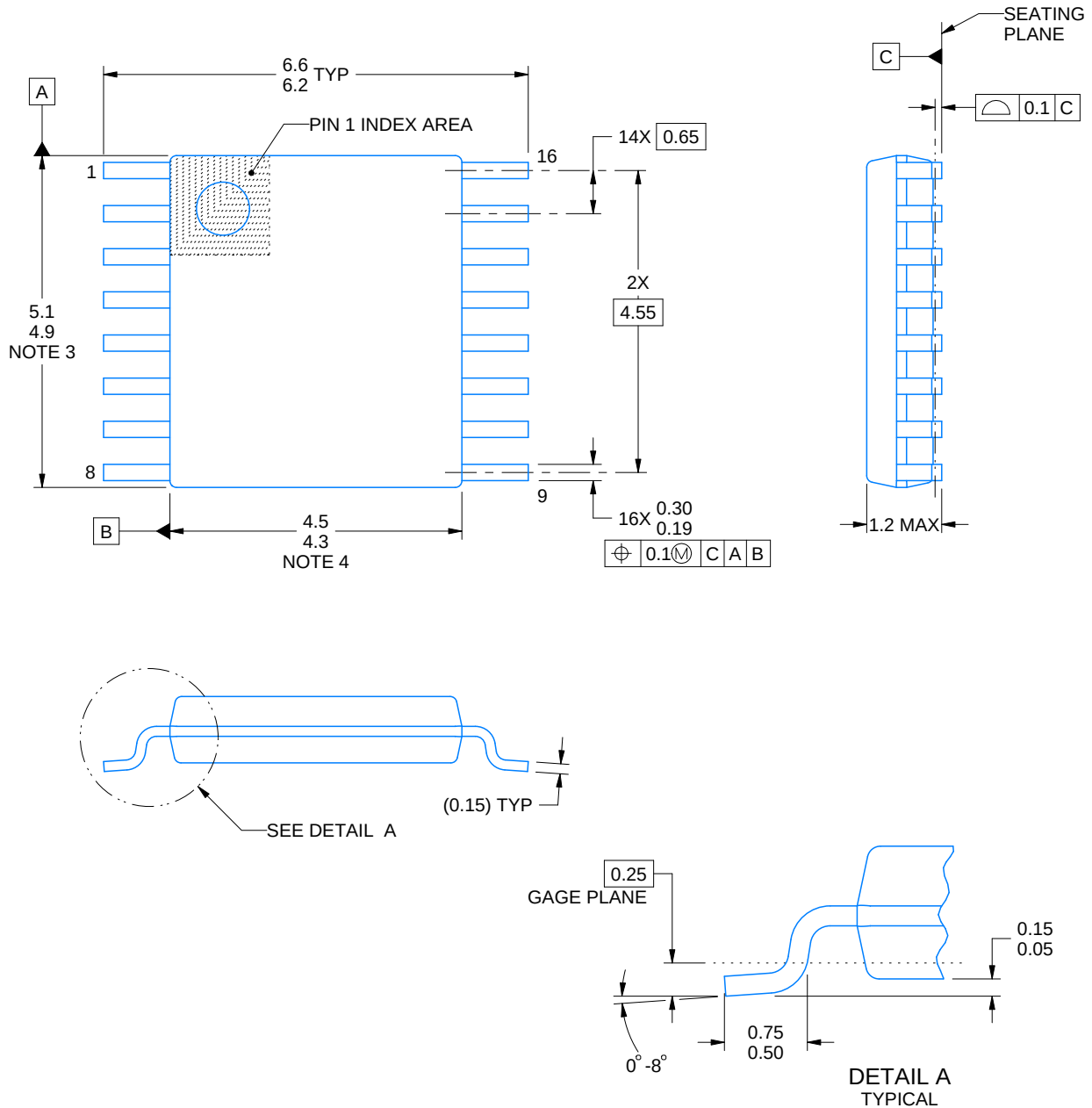
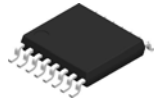
D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.



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NOTES:

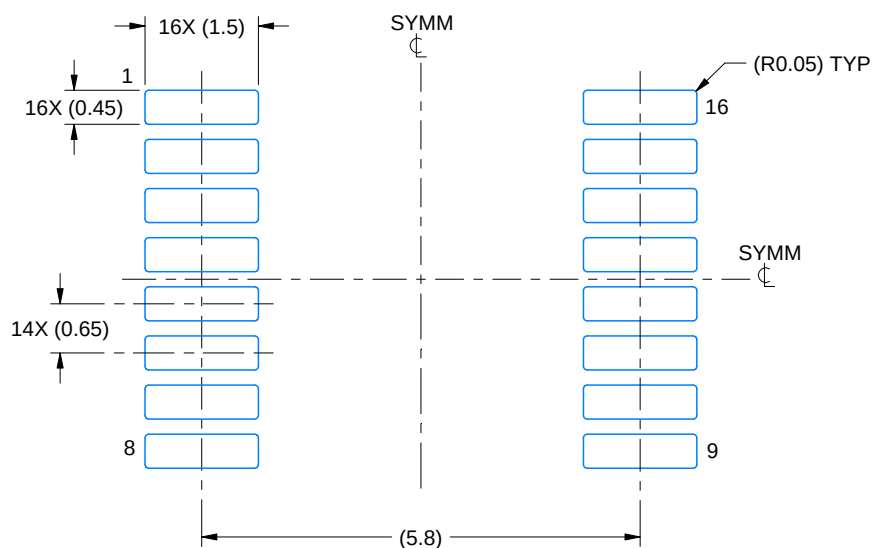
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

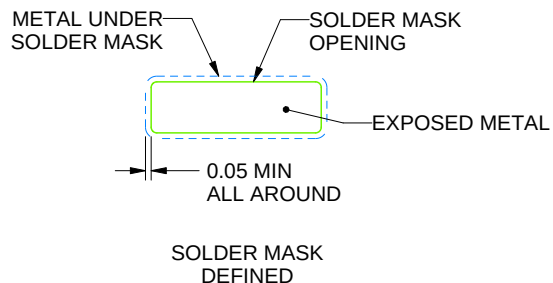
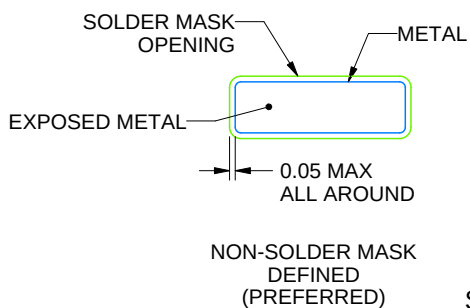
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

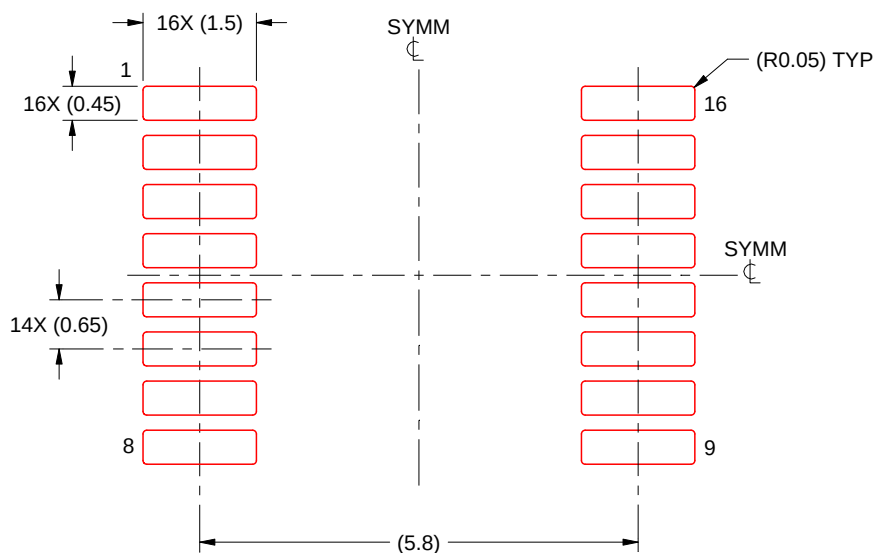
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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