

## 高速 CMOS 逻辑六路缓冲器/线路驱动器，三态同相和反相

### 1 特性

- 缓冲输入
- 高电流总线驱动器输出
- 传播延迟典型值  $t_{PLH}$ 、 $t_{PHL} = 8\text{ns}$   
 $V_{CC} = 5\text{V}$ 、 $C_L = 15\text{pF}$  且  $T_A = 25^\circ\text{C}$  时
- 扇出 (在温度范围内)
  - 标准输出：10 个 LSTTL 负载
  - 总线驱动器输出：15 个 LSTTL 负载
- 宽工作温度范围： $-55^\circ\text{C}$  至  $+125^\circ\text{C}$
- 平衡的传播延迟及转换时间
- 与 LSTTL 逻辑 IC 相比，可显著降低功耗
- HC 类型
  - 工作电压为 2V 至 6V
  - 高抗噪性：当  $V_{CC} = 5\text{V}$  时， $N_{IL} = 30\%$ ， $N_{IH} = V_{CC}$  的 30%
- HCT 类型
  - 工作电压为 4.5V 至 5.5V
  - 直接 LSTTL 输入逻辑兼容性，  
 $V_{IL} = 0.8\text{V}$  (最大值)， $V_{IH} = 2\text{V}$  (最小值)
  - CMOS 输入兼容性，当电压为  $V_{OL}$ 、 $V_{OH}$  时， $I_I \leq 1\mu\text{A}$

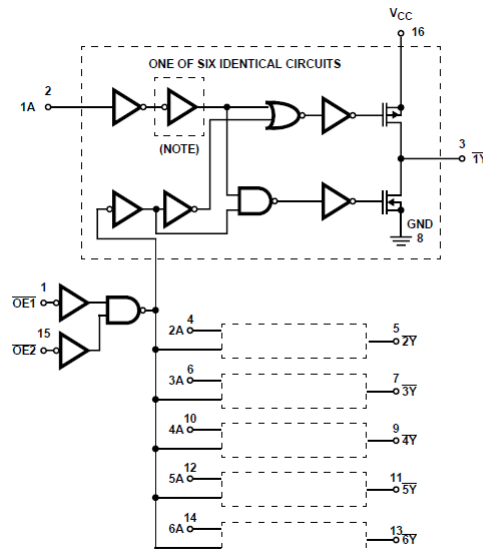
### 器件信息

| 器件型号       | 封装 <sup>(1)</sup> | 封装尺寸 (标称值)       |
|------------|-------------------|------------------|
| CD54HC365  | J (CerDIP, 16)    | 19.56mm × 6.92mm |
| CD54HC366  | J (CerDIP, 16)    | 19.56mm × 6.92mm |
| CD54HCT365 | J (CerDIP, 16)    | 19.56mm × 6.92mm |
| CD74HC365  | N (PDIP, 16)      | 19.30mm × 6.35mm |
|            | D (SOIC, 16)      | 9.90mm × 3.90mm  |
|            | D (SOIC, 16)      | 9.90mm × 3.90mm  |
|            | D (SOIC, 16)      | 9.90mm × 3.90mm  |
| CD74HC366  | N (PDIP, 16)      | 19.30mm × 6.35mm |
|            | D (SOIC, 16)      | 9.90mm × 3.90mm  |
|            | D (SOIC, 16)      | 9.90mm × 3.90mm  |
| CD74HCT365 | N (PDIP, 16)      | 19.30mm × 6.35mm |
|            | D (SOIC, 16)      | 9.90mm × 3.90mm  |
|            | D (SOIC, 16)      | 9.90mm × 3.90mm  |
|            | D (SOIC, 16)      | 9.90mm × 3.90mm  |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

### 2 说明

HC365、HCT365 和 HC366 硅栅 CMOS 三态缓冲器是通用型高速同相和反相缓冲器。



HC/HCT365 和 HC366 的逻辑图 (HC/HCT365 的输出是所示输出的补充，即 1Y、2Y 等)

A. HC/HCT 365 中不包含逆变器。



## Table of Contents

|                                                   |          |                                                                  |           |
|---------------------------------------------------|----------|------------------------------------------------------------------|-----------|
| <b>1 特性</b> .....                                 | <b>1</b> | 7.2 Functional Block Diagram.....                                | <b>8</b>  |
| <b>2 说明</b> .....                                 | <b>1</b> | 7.3 Device Functional Modes.....                                 | <b>8</b>  |
| <b>3 Revision History</b> .....                   | <b>2</b> | <b>8 Power Supply Recommendations</b> .....                      | <b>9</b>  |
| <b>4 Pin Configuration and Functions</b> .....    | <b>3</b> | <b>9 Layout</b> .....                                            | <b>9</b>  |
| <b>5 Specifications</b> .....                     | <b>4</b> | 9.1 Layout Guidelines.....                                       | <b>9</b>  |
| 5.1 Absolute Maximum Ratings <sup>(1)</sup> ..... | <b>4</b> | <b>10 Device and Documentation Support</b> .....                 | <b>10</b> |
| 5.2 Operating Conditions.....                     | <b>4</b> | 10.1 接收文档更新通知.....                                               | <b>10</b> |
| 5.3 Thermal Information.....                      | <b>4</b> | 10.2 支持资源.....                                                   | <b>10</b> |
| 5.4 Electrical Characteristics.....               | <b>5</b> | 10.3 Trademarks.....                                             | <b>10</b> |
| 5.5 HCT Input Loading Table.....                  | <b>6</b> | 10.4 Electrostatic Discharge Caution.....                        | <b>10</b> |
| 5.6 Switching Characteristics.....                | <b>6</b> | 10.5 术语表.....                                                    | <b>10</b> |
| <b>6 Parameter Measurement Information</b> .....  | <b>7</b> | <b>11 Mechanical, Packaging, and Orderable Information</b> ..... | <b>10</b> |
| <b>7 Detailed Description</b> .....               | <b>8</b> |                                                                  |           |
| 7.1 Overview.....                                 | <b>8</b> |                                                                  |           |

## 3 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision C (October 2003) to Revision D (July 2022) | Page     |
|------------------------------------------------------------------|----------|
| • 更新了整个文档中的编号、格式、表格、图和交叉参考，以反映现代数据表标准.....                       | <b>1</b> |

## 4 Pin Configuration and Functions

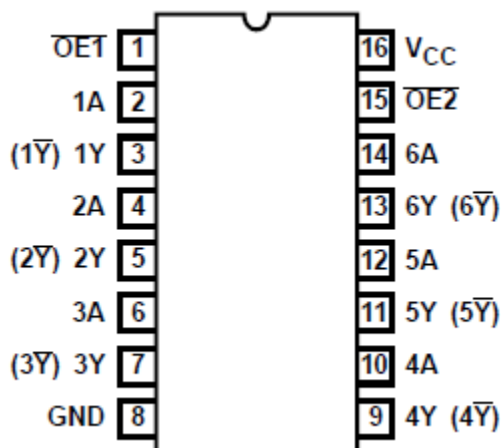


图 4-1. CD54HC365, CD54HCT365, CD54HC366 (CERDIP) CD74HC365, CD74HCT365, CD74HC366 (PDIP, SOIC) Top View

表 4-1. Pin Functions

| PIN |      | TYPE <sup>(1)</sup> | DESCRIPTION                 |
|-----|------|---------------------|-----------------------------|
| NO. | NAME |                     |                             |
| 1   | OE1  | I                   | Output Enable 1, Active Low |
| 2   | 1A   | I                   | 1A Input                    |
| 3   | 1Y   | O                   | 1Y Output                   |
| 4   | 2A   | I                   | 2A Input                    |
| 5   | 2Y   | O                   | 2Y Output                   |
| 6   | 3A   | I                   | 3A Input                    |
| 7   | 3Y   | O                   | 3Y Output                   |
| 8   | GND  | —                   | Ground Pin                  |
| 9   | 4Y   | O                   | 4Y Output                   |
| 10  | 4A   | I                   | 4A Input                    |
| 11  | 5Y   | O                   | 5Y Output                   |
| 12  | 5A   | I                   | 5A Input                    |
| 13  | 6Y   | O                   | 6Y Output                   |
| 14  | 6A   | I                   | 6A Input                    |
| 15  | OE2  | I                   | Output Enable 2, Active Low |
| 16  | VCC  | —                   | Power Pin                   |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

## 5 Specifications

### 5.1 Absolute Maximum Ratings<sup>(1)</sup>

|                  |                                                               |                                                                         | MIN  | MAX | UNIT |
|------------------|---------------------------------------------------------------|-------------------------------------------------------------------------|------|-----|------|
| V <sub>CC</sub>  | DC supply voltage                                             |                                                                         | -0.5 | 7   | V    |
| I <sub>IK</sub>  | DC input diode current                                        | For V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V |      | ±20 | mA   |
| I <sub>OK</sub>  | DC output diode current                                       | For V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V |      | ±20 | mA   |
| I <sub>O</sub>   | DC drain current, per output                                  | For -0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V                   |      | ±35 | mA   |
| I <sub>O</sub>   | DC output source or sink current per output pin               | For V <sub>O</sub> > -0.5 V or V <sub>O</sub> < V <sub>CC</sub> + 0.5 V |      | ±25 | mA   |
| I <sub>CC</sub>  | DC V <sub>CC</sub> or ground current                          |                                                                         |      | ±50 | mA   |
| T <sub>J</sub>   | Maximum junction temperature                                  |                                                                         |      | 150 | °C   |
| T <sub>stg</sub> | Maximum storage temperature range                             |                                                                         | -65  | 150 | °C   |
|                  | Maximum lead temperature (soldering 10s)SOIC - lead tips only |                                                                         |      | 300 | °C   |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 5.2 Operating Conditions

|                                 |                            |           | MIN | MAX             | UNIT |
|---------------------------------|----------------------------|-----------|-----|-----------------|------|
| V <sub>CC</sub>                 | Supply voltage range       | HC Types  | 2   | 6               | V    |
|                                 |                            | HCT Types | 4.5 | 5.5             | V    |
| V <sub>I</sub> , V <sub>O</sub> | DC input or output voltage |           | 0   | V <sub>CC</sub> | V    |
|                                 | Input rise and fall time   | 2 V       |     | 1000            | ns   |
|                                 |                            | 4.5 V     |     | 500             |      |
|                                 |                            | 6 V       |     | 400             |      |
| T <sub>A</sub>                  | Temperature range          |           | -55 | 125             | °C   |

### 5.3 Thermal Information

| THERMAL METRIC   |                                                       | N (PDIP) | D (SOIC) | UNIT |
|------------------|-------------------------------------------------------|----------|----------|------|
|                  |                                                       | 16 PINS  | 16 PINS  |      |
| R <sub>θJA</sub> | Junction-to-ambient thermal resistance <sup>(1)</sup> | 67       | 73       | °C/W |

- (1) The package thermal impedance is calculated in accordance with JESD 51 - 7

## 5.4 Electrical Characteristics

| PARAMETER                                |                                                                     | TEST CONDITIONS                    |                                         | V <sub>CC</sub><br>(V) | 25°C       |     |     | – 40°C to<br>85°C |     | – 55°C to<br>125°C |     | UNIT |
|------------------------------------------|---------------------------------------------------------------------|------------------------------------|-----------------------------------------|------------------------|------------|-----|-----|-------------------|-----|--------------------|-----|------|
|                                          |                                                                     | V <sub>I</sub> (V)                 | I <sub>O</sub> (mA)                     |                        | MIN        | TYP | MAX | MIN               | MAX | MIN                | MAX |      |
| HC TYPES                                 |                                                                     |                                    |                                         |                        |            |     |     |                   |     |                    |     |      |
| V <sub>IH</sub> High level input voltage |                                                                     |                                    |                                         | 2                      | 1.5        |     |     | 1.5               |     | 1.5                |     | V    |
|                                          |                                                                     |                                    |                                         | 4.5                    | 3.15       |     |     | 3.15              |     | 3.15               |     |      |
|                                          |                                                                     |                                    |                                         | 6                      | 4.2        |     |     | 4.2               |     | 4.2                |     |      |
| V <sub>IL</sub> Low level input voltage  |                                                                     |                                    |                                         | 2                      | 0.5        |     |     | 0.5               |     | 0.5                |     | V    |
|                                          |                                                                     |                                    |                                         | 4.5                    | 1.35       |     |     | 1.35              |     | 1.35               |     |      |
|                                          |                                                                     |                                    |                                         | 6                      | 1.8        |     |     | 1.8               |     | 1.8                |     |      |
| V <sub>OH</sub>                          | High level output voltage CMOS loads                                | V <sub>IH</sub> or V <sub>IL</sub> | -0.02                                   | 2                      | 1.9        |     |     | 1.9               |     | 1.9                |     | V    |
|                                          |                                                                     |                                    | -0.02                                   | 4.5                    | 4.4        |     |     | 4.4               |     | 4.4                |     |      |
|                                          |                                                                     |                                    | -0.02                                   | 6                      | 5.9        |     |     | 5.9               |     | 5.9                |     |      |
|                                          | High level output voltage TTL loads                                 |                                    | -6                                      | 4.5                    | 3.98       |     |     | 3.84              |     | 3.7                |     |      |
|                                          |                                                                     |                                    | -7.8                                    | 6                      | 5.48       |     |     | 5.34              |     | 5.2                |     |      |
| V <sub>OL</sub>                          | Low level output voltage CMOS loads                                 | V <sub>IH</sub> or V <sub>IL</sub> | 0.02                                    | 2                      | 0.1        |     |     | 0.1               |     | 0.1                |     | V    |
|                                          |                                                                     |                                    | 0.02                                    | 4.5                    | 0.1        |     |     | 0.1               |     | 0.1                |     |      |
|                                          |                                                                     |                                    | 0.02                                    | 6                      | 0.1        |     |     | 0.1               |     | 0.1                |     |      |
|                                          | Low level output voltage TTL loads                                  | V <sub>IH</sub> or V <sub>IL</sub> | 6                                       | 4.5                    | 0.26       |     |     | 0.33              |     | 0.4                |     |      |
|                                          |                                                                     |                                    | 7.8                                     | 6                      | 0.26       |     |     | 0.33              |     | 0.4                |     |      |
| I <sub>I</sub>                           | Input leakage current                                               | V <sub>CC</sub> or GND             |                                         | 6                      | ±0.1       |     |     | ±1                |     | ±1                 |     | μ A  |
| I <sub>CC</sub>                          | Quiescent device current                                            | V <sub>CC</sub> or GND             | 0                                       | 6                      | 8          |     |     | 80                |     | 160                |     | μ A  |
| I <sub>OZ</sub>                          | Three-state leakage current                                         | V <sub>IH</sub> or V <sub>IL</sub> | V <sub>O</sub> = V <sub>CC</sub> or GND | 6                      | ±0.5       |     |     | ±5                |     | ±10                |     | μ A  |
| HCT TYPES                                |                                                                     |                                    |                                         |                        |            |     |     |                   |     |                    |     |      |
| V <sub>IH</sub> High level input voltage |                                                                     |                                    |                                         | 4.5 to 5.5             | 2          |     |     | 2                 |     | 2                  |     | V    |
| V <sub>IL</sub> Low level input voltage  |                                                                     |                                    |                                         | 4.5 to 5.5             | 0.8        |     |     | 0.8               |     | 0.8                |     | V    |
| V <sub>OH</sub>                          | High level output voltage CMOS loads                                | V <sub>IH</sub> or V <sub>IL</sub> | -0.02                                   | 4.5                    | 4.4        |     |     | 4.4               |     | 4.4                |     | V    |
|                                          | High level output voltage TTL loads                                 |                                    | -4                                      | 4.5                    | 3.98       |     |     | 3.84              |     | 3.7                |     |      |
| V <sub>OL</sub>                          | Low level output voltage CMOS loads                                 | V <sub>IH</sub> or V <sub>IL</sub> | 0.02                                    | 4.5                    | 0.1        |     |     | 0.1               |     | 0.1                |     | V    |
|                                          | Low level output voltage TTL loads                                  |                                    | 4                                       | 4.5                    | 0.26       |     |     | 0.33              |     | 0.4                |     |      |
| I <sub>I</sub>                           | Input leakage current                                               | V <sub>CC</sub> or GND             | 0                                       | 5.5                    | ±0.1       |     |     | ±1                |     | ±1                 |     | μ A  |
| I <sub>CC</sub>                          | Quiescent device current                                            | V <sub>CC</sub> or GND             | 0                                       | 5.5                    | 8          |     |     | 80                |     | 160                |     | μ A  |
| Δ I <sub>CC</sub>                        | Additional supply current per input pin: 1 Unit Load <sup>(1)</sup> | V <sub>CC</sub> - 2.1              |                                         | 4.5 to 5.5             | 100    360 |     |     | 450               |     | 490                |     | μ A  |
| I <sub>OZ</sub>                          | Three-state leakage current                                         | V <sub>IL</sub> or V <sub>IH</sub> | V <sub>O</sub> = V <sub>CC</sub> or GND | 5.5                    | ±0.5       |     |     | ±5                |     | ±10                |     | μ A  |

(1) For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4 V, V<sub>CC</sub> = 5.5 V) specification is 1.8 mA

## 5.5 HCT Input Loading Table

| Input            | Unit Loads <sup>(1)</sup> |
|------------------|---------------------------|
| $\overline{OE}1$ | 0.6                       |
| All others       | 0.55                      |

(1) Unit Load is  $\Delta I_{CC}$  limit specified in 节 5.4, e.g., 360  $\mu A$  max at 25°C.

## 5.6 Switching Characteristics

$t_r, t_f = 6$  ns

| PARAMETER                           |                                                              | TEST CONDITIONS        | V <sub>CC</sub> (V) | 25°C |     | 40°C to 85°C | 55°C to 125°C | UNIT |
|-------------------------------------|--------------------------------------------------------------|------------------------|---------------------|------|-----|--------------|---------------|------|
|                                     |                                                              |                        |                     | TYP  | MAX | MAX          | MAX           |      |
| HC TYPES                            |                                                              |                        |                     |      |     |              |               |      |
| t <sub>PLH</sub> , t <sub>PHL</sub> | Propagation delay, data to outputs<br>HC/HCT 365             | C <sub>L</sub> = 50 pF | 2                   | 105  | 130 | 160          | ns            |      |
|                                     |                                                              |                        | 4.5                 | 21   | 26  | 32           | ns            |      |
|                                     |                                                              |                        | 6                   | 18   | 22  | 27           | ns            |      |
|                                     |                                                              | C <sub>L</sub> = 15 pF | 5                   | 8    |     |              | ns            |      |
| t <sub>PLH</sub> , t <sub>PHL</sub> | Propagation delay, data to outputs<br>HC 366                 | C <sub>L</sub> = 50 pF | 2                   | 110  | 140 | 165          | ns            |      |
|                                     |                                                              |                        | 4.5                 | 22   | 28  | 33           | ns            |      |
|                                     |                                                              |                        | 6                   | 19   | 24  | 28           | ns            |      |
|                                     |                                                              | C <sub>L</sub> = 15 pF | 5                   | 9    |     |              | ns            |      |
| t <sub>PLH</sub> , t <sub>PHL</sub> | Propagation delay time, output enable and disable to outputs | C <sub>L</sub> = 50 pF | 2                   | 150  | 190 | 225          | ns            |      |
|                                     |                                                              |                        | 4.5                 | 30   | 38  | 45           | ns            |      |
|                                     |                                                              |                        | 6                   | 26   | 33  | 38           | ns            |      |
|                                     |                                                              | C <sub>L</sub> = 15 pF | 5                   | 12   |     |              | ns            |      |
| t <sub>TLH</sub> , t <sub>THL</sub> | Output transition time                                       | C <sub>L</sub> = 50 pF | 2                   | 60   | 75  | 90           | ns            |      |
|                                     |                                                              |                        | 4.5                 | 12   | 15  | 18           | ns            |      |
|                                     |                                                              |                        | 6                   | 10   | 13  | 15           | ns            |      |
| C <sub>I</sub>                      | Input capacitance                                            |                        |                     | 10   | 10  | 10           | pF            |      |
| C <sub>O</sub>                      | Three-state ouput capacitance                                |                        |                     | 20   | 20  | 20           | pF            |      |
| C <sub>PD</sub>                     | Power dissipation capacitance <sup>(1)</sup><br>(2)          |                        | 5                   | 40   |     |              | pF            |      |
| HCT TYPES                           |                                                              |                        |                     |      |     |              |               |      |
| t <sub>PLH</sub> , t <sub>PHL</sub> | Propagation delay, data to outputs<br>HC/HCT 365             | C <sub>L</sub> = 50 pF | 4.5                 | 25   | 31  | 38           | ns            |      |
|                                     |                                                              |                        |                     |      |     |              | ns            |      |
|                                     |                                                              | C <sub>L</sub> = 15 pF | 5                   | 9    |     |              | ns            |      |
|                                     |                                                              |                        |                     |      |     |              | ns            |      |
| t <sub>PLH</sub> , t <sub>PHL</sub> | Propagation delay, data to outputs<br>HC 366                 | C <sub>L</sub> = 50 pF | 4.5                 | 27   | 34  | 41           | ns            |      |
|                                     |                                                              | C <sub>L</sub> = 15 pF | 5                   | 11   |     |              | ns            |      |
| t <sub>PLH</sub> , t <sub>PHL</sub> | Propagation delay time, output enable and disable to ouputs  | C <sub>L</sub> = 50 pF | 4.5                 | 35   | 44  | 53           | ns            |      |
|                                     |                                                              | C <sub>L</sub> = 15 pF | 5                   | 14   |     |              | ns            |      |
| t <sub>TLH</sub> , t <sub>THL</sub> | Output transition time                                       | C <sub>L</sub> = 50 pF | 4.5                 | 12   | 15  | 18           | ns            |      |
| C <sub>IN</sub>                     | Input capacitance                                            |                        |                     | 10   | 10  | 10           | pF            |      |
| C <sub>O</sub>                      | Three-stage capacitance                                      |                        |                     | 20   | 20  | 20           | pF            |      |
| C <sub>PD</sub>                     | Power dissipation capacitance <sup>(1)</sup><br>(2)          |                        | 5                   | 42   |     |              | pF            |      |

(1)  $C_{PD}$  is used to determine the dynamic power consumption, per buffer.

(2)  $P_D = V_{CC}^2 f_i (C_{PD} + C_I)$  where  $f_i$  = input frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.

## 6 Parameter Measurement Information

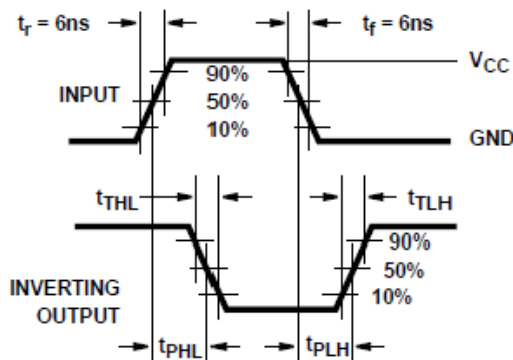


图 6-1. HC Transition Times and Propagation Delay Times, Combination Logic

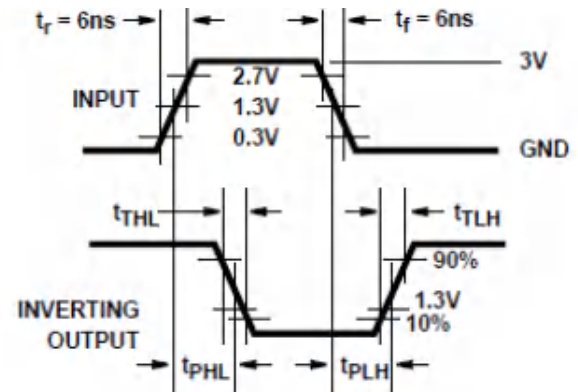


图 6-2. HCT Transition Times and Propagation Delay Times, Combination Logic

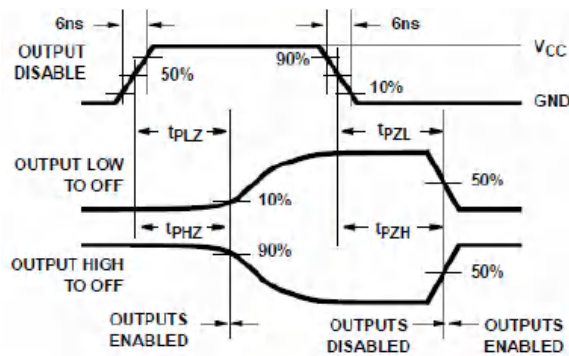


图 6-3. HC Three-State Propagation Delay Waveform

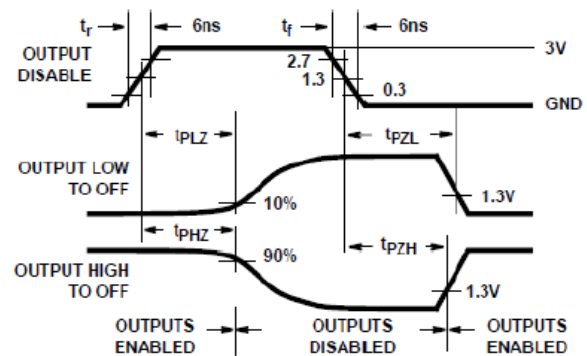
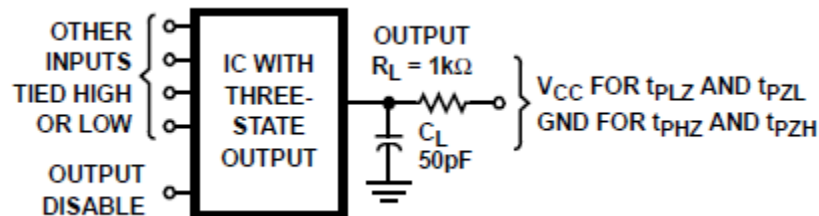


图 6-4. HCT Three-State Propagation Delay Waveform



- A. Open drain waveforms  $t_{PLZ}$  and  $t_{PZL}$  are the same as those for three-state shown on the left. The test circuit is output  $R_L = 1\text{ k}\Omega$  to  $V_{CC}$ ,  $C_L = 50\text{ pF}$ .

图 6-5. HC and HCT Three-State Propagation Delay Test Circuit

## 7 Detailed Description

### 7.1 Overview

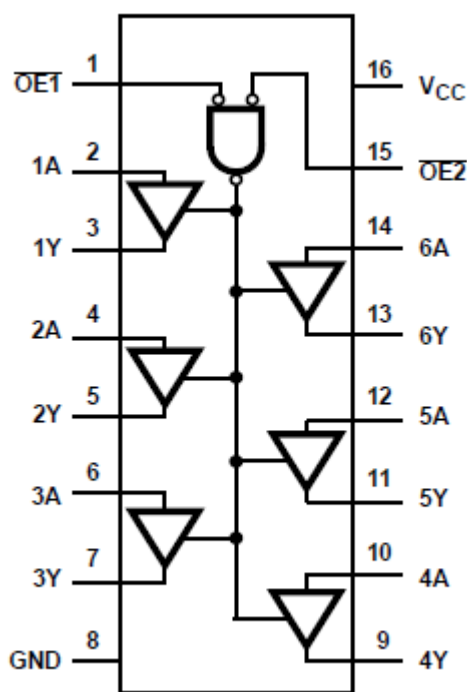
The ' HC365, ' HCT365, and ' HC366 silicon gate CMOS three-state buffers are general purpose high-speed non-inverting and inverting buffers. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. Both circuits are capable of driving up to 15 low power Schottky inputs.

The ' HC365 and ' HCT365 are non-inverting buffers, whereas the ' HC366 is an inverting buffer. These devices have two three-state control inputs ( $\overline{OE1}$  and  $\overline{OE2}$ ) which are NORed together to control all six gates.

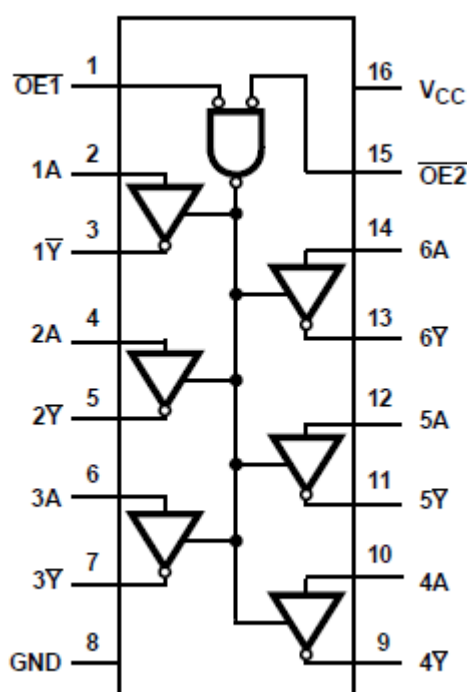
The ' HCT365 logic families are speed, function and pin compatible with the standard LS logic family.

### 7.2 Functional Block Diagram

#### Functional Diagrams



HC365, HCT365



HC366

### 7.3 Device Functional Modes

表 7-1. Function Table

| INPUTS <sup>(1)</sup> |      |   | OUTPUTS (Y) <sup>(2)</sup> |         |
|-----------------------|------|---|----------------------------|---------|
| OE 1                  | OE 2 | A | HC/HCT 365                 | HCT 366 |
| L                     | L    | L | L                          | H       |
| L                     | L    | H | H                          | L       |
| X                     | H    | X | Z                          | Z       |
| H                     | X    | X | Z                          | Z       |

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

(2) H = Driving High, L = Driving Low, Z = High Impedance State

## 8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 9 Layout

### 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 10.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 10.2 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

### 10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)            |
|-------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|--------------------------------|
| <a href="#">CD54HC365F3A</a>  | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8500101EA<br>CD54HC365F3A      |
| CD54HC365F3A.A                | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8500101EA<br>CD54HC365F3A      |
| <a href="#">CD54HC366F3A</a>  | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8682801EA<br>CD54HC366F3A |
| CD54HC366F3A.A                | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8682801EA<br>CD54HC366F3A |
| <a href="#">CD54HCT365F3A</a> | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD54HCT365F3A                  |
| CD54HCT365F3A.A               | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD54HCT365F3A                  |
| <a href="#">CD74HC365E</a>    | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HC365E                     |
| CD74HC365E.A                  | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HC365E                     |
| <a href="#">CD74HC365M</a>    | Obsolete      | Production           | SOIC (D)   16  | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | HC365M                         |
| <a href="#">CD74HC365M96</a>  | Active        | Production           | SOIC (D)   16  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HC365M                         |
| CD74HC365M96.A                | Active        | Production           | SOIC (D)   16  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HC365M                         |
| <a href="#">CD74HC365MT</a>   | Obsolete      | Production           | SOIC (D)   16  | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | HC365M                         |
| <a href="#">CD74HC366E</a>    | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HC366E                     |
| CD74HC366E.A                  | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HC366E                     |
| <a href="#">CD74HC366M</a>    | Obsolete      | Production           | SOIC (D)   16  | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | HC366M                         |
| <a href="#">CD74HC366M96</a>  | Active        | Production           | SOIC (D)   16  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HC366M                         |
| CD74HC366M96.A                | Active        | Production           | SOIC (D)   16  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HC366M                         |
| <a href="#">CD74HCT365E</a>   | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HCT365E                    |
| CD74HCT365E.A                 | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD74HCT365E                    |
| <a href="#">CD74HCT365M</a>   | Obsolete      | Production           | SOIC (D)   16  | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | HCT365M                        |
| <a href="#">CD74HCT365M96</a> | Active        | Production           | SOIC (D)   16  | 2500   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -55 to 125   | HCT365M                        |
| CD74HCT365M96.A               | Active        | Production           | SOIC (D)   16  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | HCT365M                        |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

**(2) Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

**(3) RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54HC365, CD54HC366, CD54HCT365, CD74HC365, CD74HC366, CD74HCT365 :**

- Catalog : [CD74HC365](#), [CD74HC366](#), [CD74HCT365](#)
- Automotive : [CD74HC366-Q1](#), [CD74HC366-Q1](#)
- Military : [CD54HC365](#), [CD54HC366](#), [CD54HCT365](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HC365M96  | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| CD74HC366M96  | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| CD74HCT365M96 | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

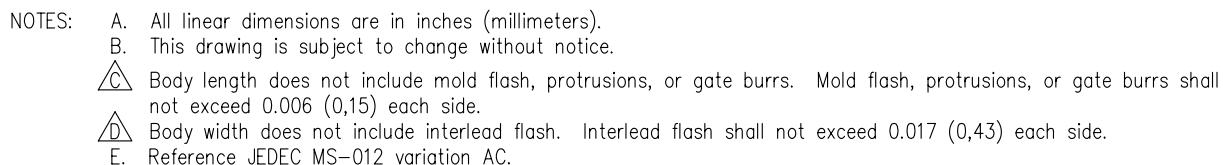
| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HC365M96  | SOIC         | D               | 16   | 2500 | 353.0       | 353.0      | 32.0        |
| CD74HC366M96  | SOIC         | D               | 16   | 2500 | 353.0       | 353.0      | 32.0        |
| CD74HCT365M96 | SOIC         | D               | 16   | 2500 | 356.0       | 356.0      | 35.0        |

## TUBE



\*All dimensions are nominal

| Device        | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD74HC365E    | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC365E    | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC365E.A  | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC365E.A  | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC366E    | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC366E    | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC366E.A  | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HC366E.A  | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT365E   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT365E   | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT365E.A | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD74HCT365E.A | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |



J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

## 重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
版权所有 © 2025，德州仪器 (TI) 公司