TEXAS INSTRUMENTS

CD54/74AC280, CD54/74ACT280

Data sheet acquired from Harris Semiconductor
SCHS250A

August 1998 - Revised May 2000

9-Bit Odd/Even Parity Generator/Checker

Features

- **Buffered Inputs**
- **Typical Propagation Delay**
  - **10ns at V_{CC} = 5V, T_A = 25°C, C_L = 50pF**
- **Exceeds 2kV ESD Protection per MIL-STD-883, Method 3015**
- **SCR-Latchup-Resistant CMOS Process and Circuit Design**
- **Speed of Bipolar FAST™/AS/S with Significantly Reduced Power Consumption**
- **Balanced Propagation Delays**
- **AC Types Feature 1.5V to 5.5V Operation and Balanced Noise Immunity at 30% of the Supply**
- **±24mA Output Drive Current**
  - **Fanout to 15 FAST™ ICs**
  - **Drives 50Ω Transmission Lines**

Description

The ’AC280 and ’ACT280 are 9-bit odd/even parity generator/checkers that utilize Advanced CMOS Logic technology. Both even and odd parity outputs are available for checking or generating parity for words up to nine bits long. Even parity is indicated (∑E output is HIGH) when an even number of data inputs is HIGH. Odd parity is indicated (∑O output is HIGH) when an odd number of data inputs is HIGH. Parity checking for words larger than nine bits can be accomplished by tying the ∑E output to any input of an additional ’AC280, ’ACT280 parity checker.

Ordering Information

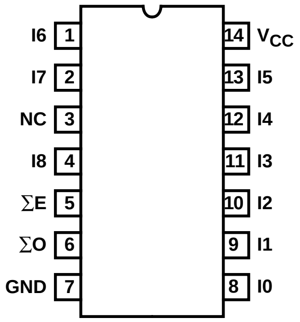
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54AC280F3A	-55 to 125	14 Ld CERDIP
CD74AC280E	0 to 70°C, -40 to 85, -55 to 125	14 Ld PDIP
CD74AC280M	0 to 70°C, -40 to 85, -55 to 125	14 Ld SOIC
CD54ACT280F3A	-55 to 125	14 Ld CERDIP
CD74ACT280E	0 to 70°C, -40 to 85, -55 to 125	14 Ld PDIP
CD74ACT280M	0 to 70°C, -40 to 85, -55 to 125	14 Ld SOIC

NOTES:

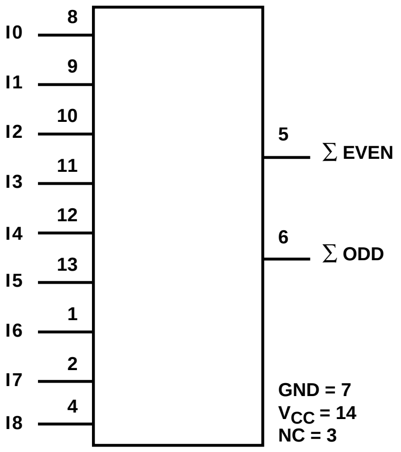
1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.

Pinout

CD54AC280, CD54ACT280
(CERDIP)
CD74AC280, CD74ACT280
(PDIP, SOIC)
TOP VIEW



Functional Diagram



Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . -0.5V to 6V
DC Input Diode Current, I_{IK}
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ . . . . ±20mA
DC Output Diode Current, I_{OK}
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ . . . . ±50mA
DC Output Source or Sink Current per Output Pin, I_O
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ . . . . ±50mA
DC V_{CC} or Ground Current, I_{CC} or I_{GND} (Note 3) . . . . ±100mA

Thermal Information

Thermal Resistance (Typical, Note 5) θ_{JA} ($^oC/W$)
PDIP Package . . . . ___
SOIC Package . . . . ___
Maximum Junction Temperature (Plastic Package) . . . . 150^{o}C
Maximum Storage Temperature Range . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . 300^{o}C

Operating Conditions

Temperature Range, T_A . . . . -55^{o}C to 125^{o}C
Supply Voltage Range, V_{CC} (Note 4)
AC Types. . . . . .1.5V to 5.5V
ACT Types . . . . .4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . 0V to V_{CC}
Input Rise and Fall Slew Rate, dt/dv
AC Types, 1.5V to 3V . . . . 50ns (Max)
AC Types, 3.6V to 5.5V. . . . . 20ns (Max)
ACT Types, 4.5V to 5.5V. . . . . 10ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

3. For up to 4 outputs per device, add ±25mA for each additional output.
4. Unless otherwise specified, all voltages are referenced to ground.
5. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25^{o}C		-40^{o}C TO 85^{o}C		-55^{o}C TO 125^{o}C		UNITS
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
AC TYPES											
High Level Input Voltage	V_{IH}	-	-	1.5	1.2	-	1.2	-	1.2	-	V
				3	2.1	-	2.1	-	2.1	-	V
				5.5	3.85	-	3.85	-	3.85	-	V
Low Level Input Voltage	V_{IL}	-	-	1.5	-	0.3	-	0.3	-	0.3	V
				3	-	0.9	-	0.9	-	0.9	V
				5.5	-	1.65	-	1.65	-	1.65	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	-	1.4	-	1.4	-	V
			-0.05	3	2.9	-	2.9	-	2.9	-	V
			-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-4	3	2.58	-	2.48	-	2.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Note 6, 7)	5.5	-	-	3.85	-	-	-	V
			-50 (Note 6, 7)	5.5	-	-	-	-	3.85	-	V

DC Electrical Specifications **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	0.05	1.5	-	0.1	-	0.1	-	0.1	V
			0.05	3	-	0.1	-	0.1	-	0.1	V
			0.05	4.5	-	0.1	-	0.1	-	0.1	V
			12	3	-	0.36	-	0.44	-	0.5	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 6, 7)	5.5	-	-	-	1.65	-	-	V
			50 (Note 6, 7)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	I_I	V_{CC} or GND	-	5.5	-	±0.1	-	±1	-	±1	µA
Quiescent Supply Current MSI	I_{CC}	V_{CC} or GND	0	5.5	-	8	-	80	-	160	µA
ACT TYPES											
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Note 6, 7)	5.5	-	-	3.85	-	-	-	V
			-50 (Note 6, 7)	5.5	-	-	-	-	3.85	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	0.05	4.5	-	0.1	-	0.1	-	0.1	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 6, 7)	5.5	-	-	-	1.65	-	-	V
			50 (Note 6, 7)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	I_I	V_{CC} or GND	-	5.5	-	±0.1	-	±1	-	±1	µA
Quiescent Supply Current MSI	I_{CC}	V_{CC} or GND	0	5.5	-	8	-	80	-	160	µA
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI_{CC}	V_{CC} -2.1	-	4.5 to 5.5	-	2.4	-	2.8	-	3	mA

NOTES:

6. Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
7. Test verifies a minimum 50Ω transmission-line-drive capability at 85°C, 75Ω at 125°C.

ACT Input Load Table

INPUT	UNIT LOAD
All	1.43

NOTE: Unit load is ΔI_{CC} limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

Switching Specifications Input t_r, t_f = 3ns, C_L = 50pF (Worst Case)

PARAMETER	SYMBOL	V_{CC} (V)	-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
AC TYPES									
Propagation Delay, Any Input to ΣO	t_{PLH}, t_{PHL}	1.5	-	-	239	-	-	263	ns
		3.3 (Note 9)	7.5	-	26	7.3	-	29	ns
		5 (Note 10)	5.4	-	19.1	5.3	-	21	ns
Propagation Delay, Any Input to ΣE	t_{PLH}, t_{PHL}	1.5	-	-	227	-	-	250	ns
		3.3	7.2	-	25	7	-	28	ns
		5	5.2	-	18.2	5	-	20	ns
Input Capacitance	C_I	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	C_{PD} (Note 11)	-	-	115	-	-	115	-	pF
ACT TYPES									
Propagation Delay, Any Input to ΣO	t_{PLH}, t_{PHL}	5 (Note 10)	5.6	-	19.6	5.4	-	21.6	ns
Propagation Delay, Any Input to ΣE	t_{PLH}, t_{PHL}	5	5.6	-	19.6	5.4	-	21.6	ns
Input Capacitance	C_I	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	C_{PD} (Note 11)	-	-	115	-	-	115	-	pF

NOTES:

8. Limits tested 100%
9. 3.3V Min is at 3.6V, Max is at 3V.
10. 5V Min is at 5.5V, Max is at 4.5V.
11. C_{PD} is used to determine the dynamic power consumption per package.
    AC: $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
    ACT: $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

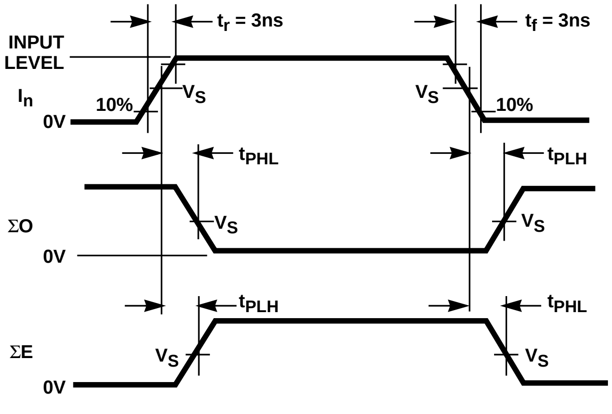
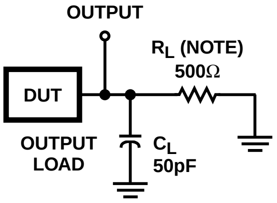


FIGURE 1.



NOTE: For AC Series Only: When V_{CC} = 1.5V, R_L = 1kΩ.

	AC	ACT
Input Level	V_{CC}	3V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

FIGURE 2. PROPAGATION DELAY TIMES

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD54AC280F3A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54AC280F3A
CD54AC280F3A.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54AC280F3A
CD54ACT280F3A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54ACT280F3A
CD54ACT280F3A.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54ACT280F3A
CD74AC280E	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74AC280E
CD74AC280E.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74AC280E
CD74AC280M	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	AC280M
CD74AC280M96	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC280M
CD74AC280M96.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC280M
CD74AC280M96G4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC280M
CD74ACT280E	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74ACT280E
CD74ACT280E.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74ACT280E
CD74ACT280M	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	ACT280M
CD74ACT280M96	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT280M
CD74ACT280M96.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT280M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF CD54AC280, CD54ACT280, CD74AC280, CD74ACT280 :

- Catalog : CD74AC280, CD74ACT280

- Military : CD54AC280, CD54ACT280

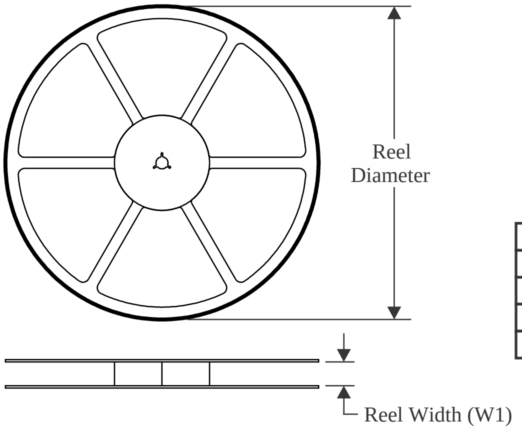
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

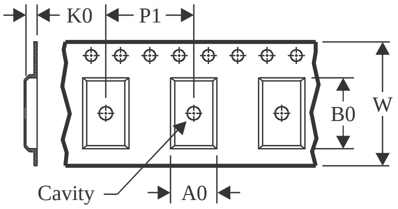
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

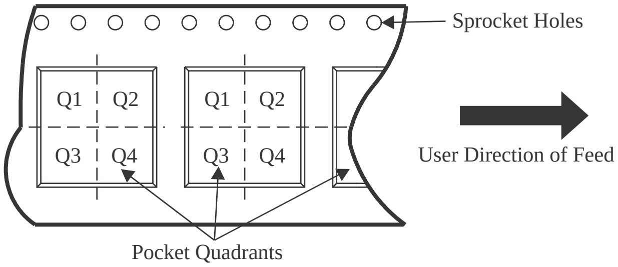


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

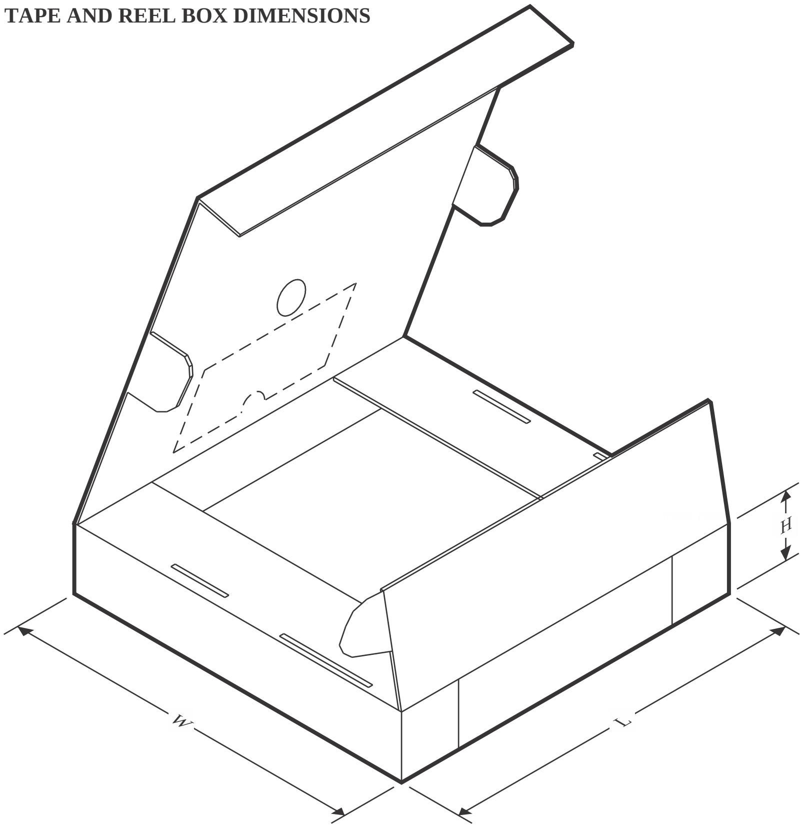
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC280M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74ACT280M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

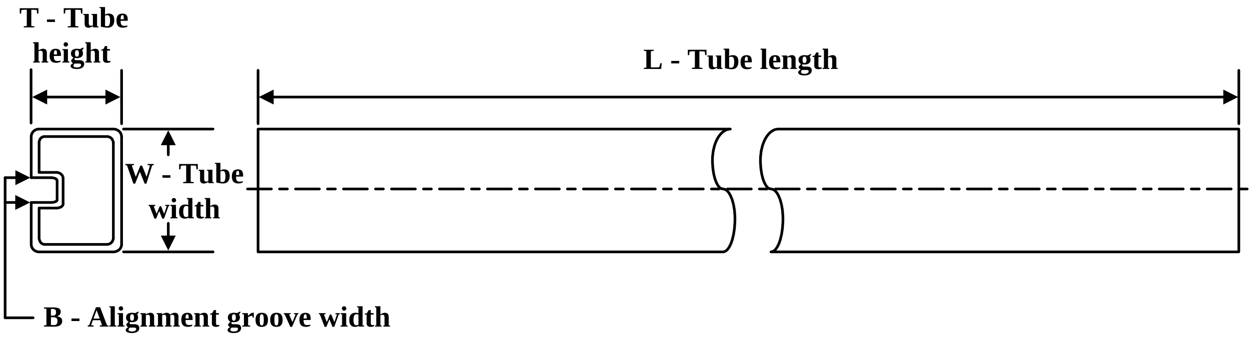
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

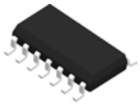
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC280M96	SOIC	D	14	2500	356.0	356.0	35.0
CD74ACT280M96	SOIC	D	14	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74AC280E	N	PDIP	14	25	506	13.97	11230	4.32
CD74AC280E	N	PDIP	14	25	506	13.97	11230	4.32
CD74AC280E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74AC280E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74ACT280E	N	PDIP	14	25	506	13.97	11230	4.32
CD74ACT280E	N	PDIP	14	25	506	13.97	11230	4.32
CD74ACT280E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74ACT280E.A	N	PDIP	14	25	506	13.97	11230	4.32

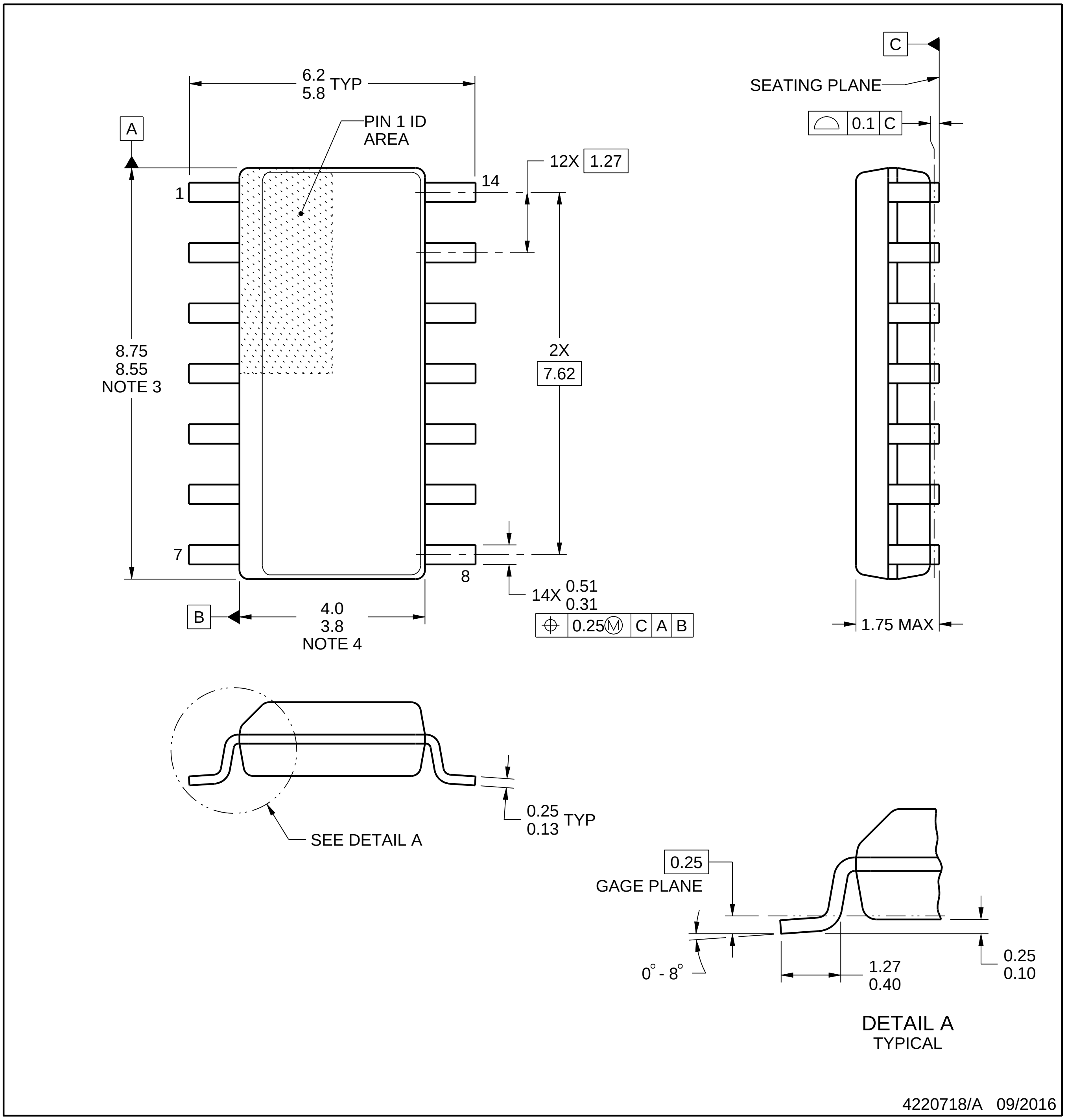


PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

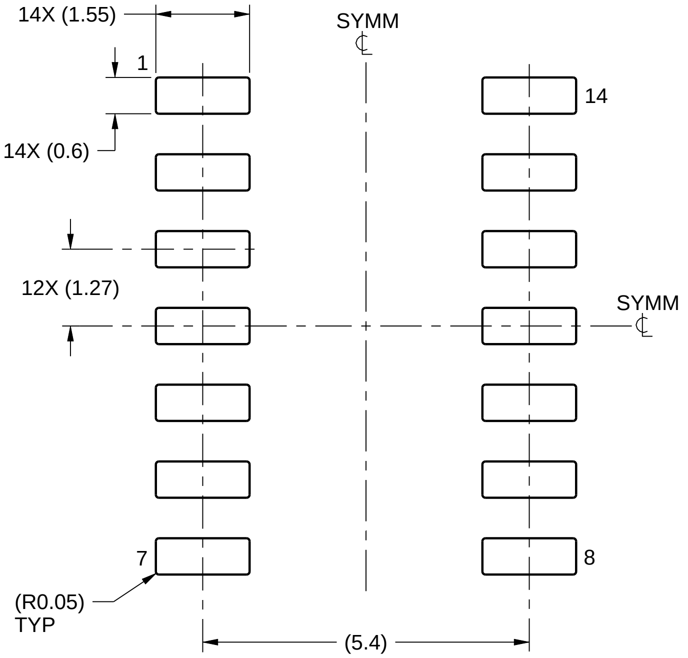
SMALL OUTLINE INTEGRATED CIRCUIT



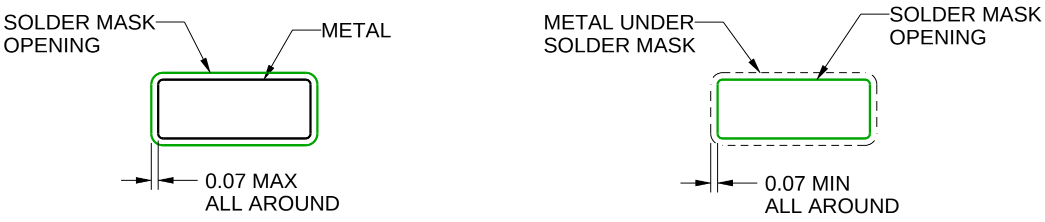
4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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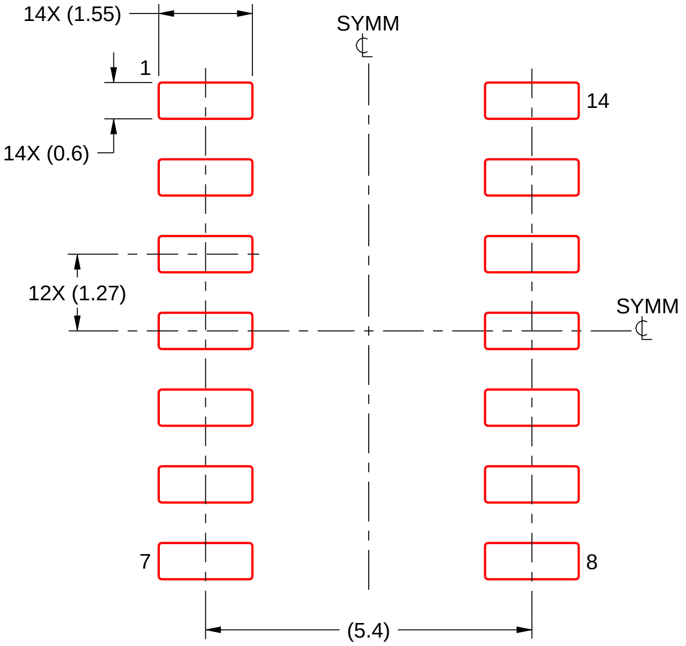
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

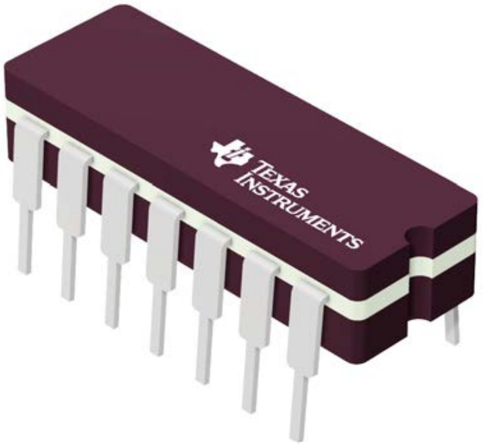
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

J 14

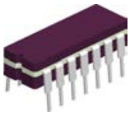
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

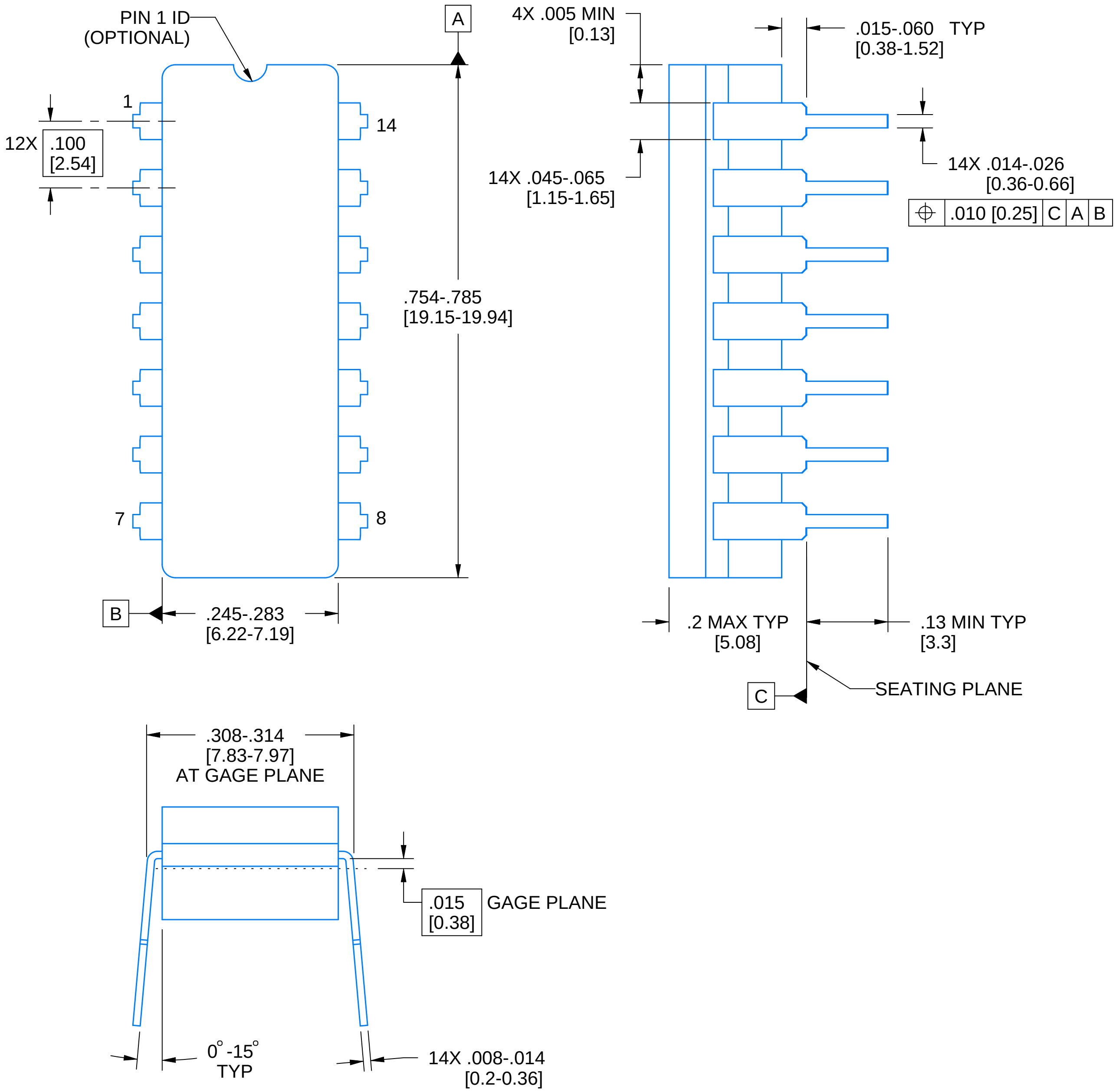
J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE

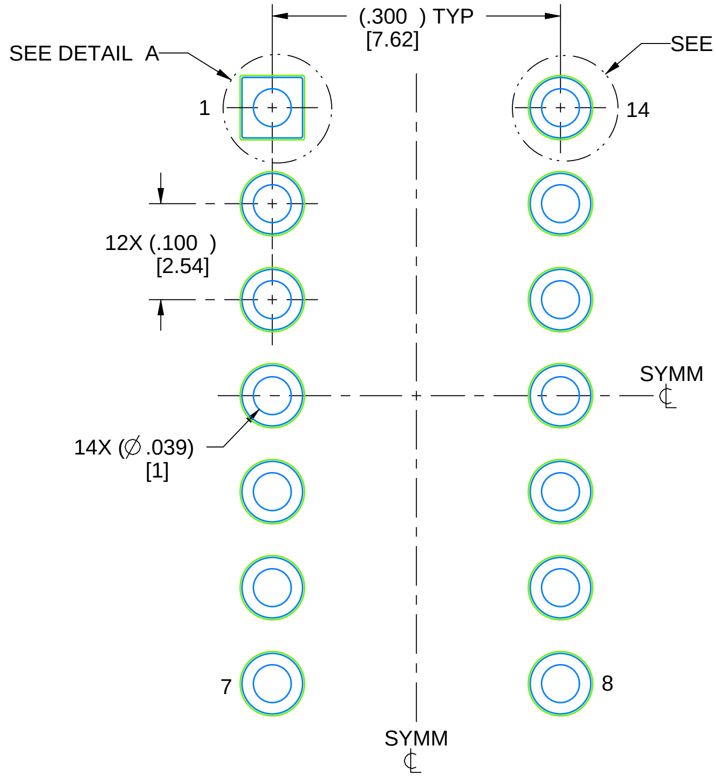


4214771/A 05/2017

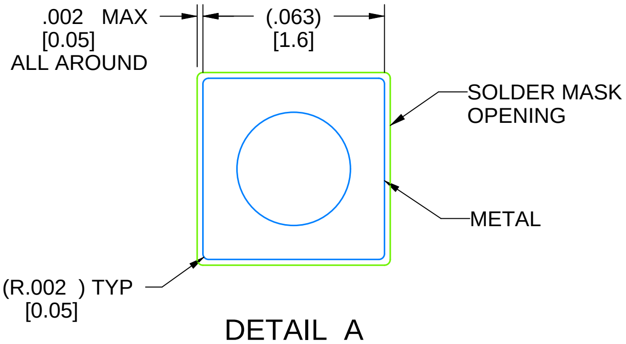
NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

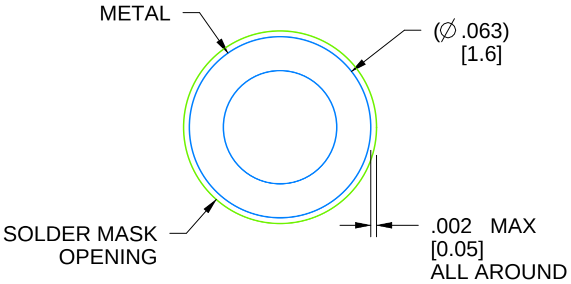
TEXAS INSTRUMENTS



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



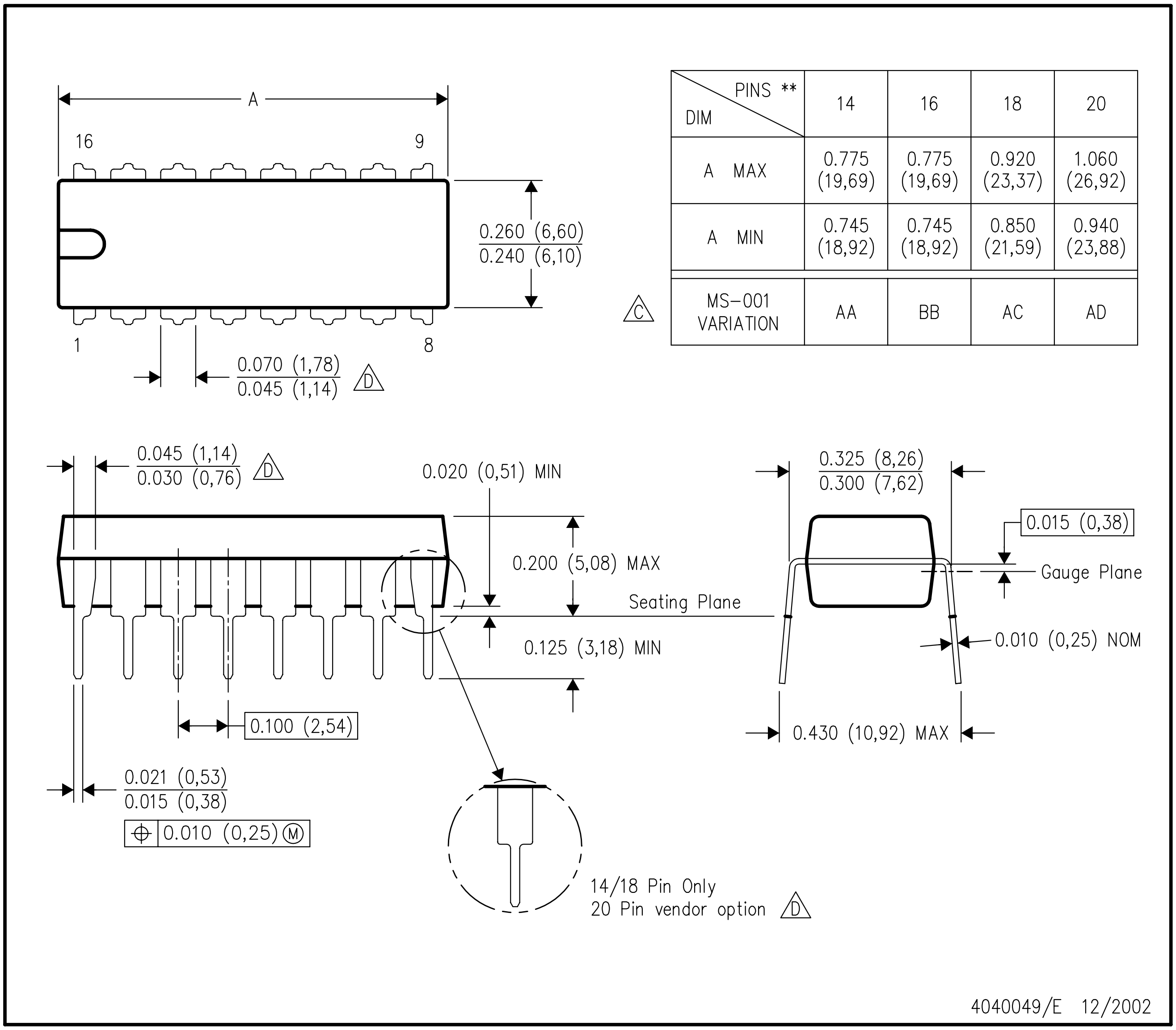
DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

N (R-PDIP-T**) PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

4040049/E 12/2002

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- D The 20 pin end lead shoulder width is a vendor option, either half or full width.

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