

CD74AC251 具有三态输出的 8 输入多路复用器

1 特性

- 缓冲输入
- 典型传播延迟
 - $V_{CC} = 5V$ 、 $T_A = 25^\circ C$ 且 $C_L = 50pF$ 时为 6ns
- ESD 保护超过 2kV (根据 MIL-STD-883 方法 3015)
- 防 SCR 闩锁 CMOS 工艺和电路设计
- 具有双极 FAST™/AS/S 的速度，同时功耗显著降低
- 平衡传播延迟
- 交流类型的工作电压范围为 1.5V 至 5.5V，并在电源电压的 30% 时具有平衡的抗噪性能
- $\pm 24mA$ 输出驱动电流
 - 扇出到 15 个 FAST™ IC
 - 驱动 50 Ω 传输线

2 说明

CD74AC251 8 输入多路复用器采用 Harris 高级 CMOS 逻辑技术。该多路复用器具有真实 (Y) 和补码 ($\bar{Y}$) 输出以及输出使能 ($\overline{OE}$) 输入。OE 必须为低逻辑电平，才能启用此器件。当 $\overline{OE}$ 输入为高电平时，两个输出均处于高阻抗状态。启用后，数据选择输入上的地址信息决定了将哪个数据输入路由到 Y 和 $\bar{Y}$ 输出。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾	本体尺寸 ⁽³⁾
CD74AC251	D (SOIC , 16)	9.9mm × 6mm	9.9mm × 3.9mm

- (1) 有关更多信息，请参阅节 10。
 (2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。
 (3) 本体尺寸 (长 × 宽) 为标称值，不包括引脚。

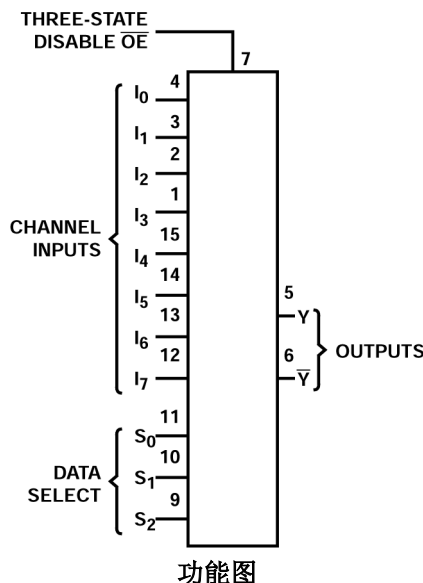


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3 Pin Configuration and Functions

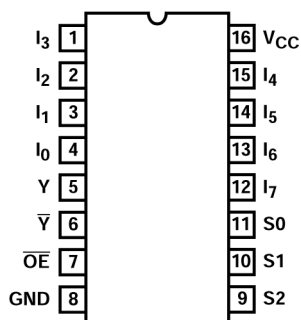


图 3-1. CD74AC251 D Package, 16-Pin SOIC (Top View)

PIN		TYPE ¹	DESCRIPTION
NAME	NO.		
I ₃	1	I	Input 3
I ₂	2	I	Input 2
I ₁	3	I	Input 1
I ₀	4	I	Input 0
Y	5	I	Output
$\bar{Y}$	6	I	Inverted Output
$\overline{OE}$	7	O	Output Enable
GND	8	G	Ground
S2	9	O	Input Select 2
S1	10	O	Input Select 1
S0	11	O	Input Select 0
I ₇	12	O	Input 7
I ₆	13	O	Input 6
I ₅	14	O	Input 5
I ₄	15	O	Input 4
V _{CC}	16	P	Positive Supply

1. Signal Types: I = Input, O = Output, I/O = Input or Output.

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	-0.5	6	V
I _{IK}	Input diode current	(V _I < -0.5V or V _I > V _{CC} + 0.5V)		±20 mA
I _{OK}	Output diode current	(V _I < -0.5V or V _I > V _{CC} + 0.5V)		±50 mA
I _O	Output source or sink current per output pin	V _O < -0.5V or V _O > V _{CC} + 0.5V		±50 mA
	V _{CC} or ground current, ICC or IGND ⁽²⁾			±100 mA
T _J	Maximum junction temperature (plastic package)			150 °C
T _{stg}	Storage temperature	-65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) For up to 4 outputs per device, add ±25mA for each additional output.

4.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC} ⁽¹⁾	Supply voltage	1.5	1.5	
V _I , V _O	Input or output voltage	0	V _{CC}	V
dt/dv	Input rise and fall slew rate			
	AC types, 1.5V to 3V		50	ns
	AC types, 3.6V to 5.5V		20	ns
T _A	Temperature range	-55	125	°C

(1) Unless otherwise specified, all voltages are referenced to ground.

4.3 Thermal Information

THERMAL METRIC		CD74AC251	UNIT
		D (SOIC)	
		16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance ⁽¹⁾	119.9	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

4.4 Electrical Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS		V _{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNIT
		V _I (V)	I _O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
V _{IH}	High level input voltage	-	-	1.5	1.2	-	1.2	-	1.2	-	V
				3	2.1	-	2.1	-	2.1	-	V
				5.5	3.85	-	3.85	-	3.85	-	V
V _{IL}	Low level input voltage	-	-	1.5	-	0.3	-	0.3	-	0.3	V
				3	-	0.9	-	0.9	-	0.9	V
				5.5	-	1.65	-	1.65	-	1.65	V

SYMBOL	PARAMETER	TEST CONDITIONS		V _{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNIT
		V _I (V)	I _O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH}	High level output voltage	V _{IH} or V _{IL}	-0.05	1.5	1.4	-	1.4	-	1.4	-	V
			-0.05	3	2.9	-	2.9	-	2.9	-	V
			-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-4	3	2.58	-	2.48	-	2.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 ^{(1), (2)}	5.5	-	-	3.85	-	-	-	V
			-50 ^{(1), (2)}	5.5	-	-	-	-	3.85	-	V
V _{OL}	Low level output voltage	V _{IH} or V _{IL}	0.05	1.5	-	0.1	-	0.1	-	0.1	V
			0.05	3	-	0.1	-	0.1	-	0.1	V
			0.05	4.5	-	0.1	-	0.1	-	0.1	V
			12	3	-	0.36	-	0.44	-	0.5	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 ^{(1), (2)}	5.5	-	-	-	1.65	-	-	V
			50 ^{(1), (2)}	5.5	-	-	-	-	-	1.65	V
I _I	Input leakage current	V _{CC} or GND	-	5.5	-	±0.1	-	±1	-	±1	μA
I _{OZ}	Three-state leakage current	V _{IH} or V _{IL} V _O = V _{CC} or GND	-	5.5	-	±0.5	-	±5	-	±10	μA
I _{CC}	Quiescent supply current MSI	V _{CC} or GND	0	5.5	-	8	-	80	-	160	μA

- (1) Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
- (2) Test verifies a minimum 50 Ω transmission-line-drive capability at 85°C, 75 Ω at 125°C.

表 4-1. ACT Input Load Table

INPUT	UNIT LOAD
S0, S1, S3	1
OE	1
I ₀ - I ₇	1

备注

Unit load is Δ I_{CC} limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

4.5 Switching Characteristics

Input t_r, t_f = 3ns, C_L = 50pF (Worst Case)

SYMBOL	PARAMETER	V _{CC} (V)	-40°C TO 85°C			-55°C TO 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH} , t _{PHL}	Propagation delay, data to Y output	1.5	-	-	153	-	-	169	ns
		3.3 ⁽¹⁾	4.9	-	17.2	4.7	-	18.9	ns
		5 ⁽²⁾	3.5	-	12.3	3.4	-	13.5	ns
t _{PLH} , t _{PHL}	Propagation delay, data to $\bar{Y}$ output	1.5	-	-	169	-	-	186	ns
		3.3	5.4	-	19	5.2	-	20.9	ns
		5	3.8	-	13.5	3.7	-	14.9	ns

Input $t_r, t_f = 3\text{ns}$, $C_L = 50\text{pF}$ (Worst Case)

SYMBOL	PARAMETER	V_{CC} (V)	-40°C TO 85°C			-55°C TO 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}, t_{PHL}	Propagation delay, select to Y output	1.5	-	-	207	-	-	228	ns
		3.3	6.6	-	23.2	6.4	-	25.5	ns
		5	4.7	-	16.5	4.6	-	18.2	ns
t_{PLH}, t_{PHL}	Propagation Delay, Select to $\bar{Y}$ Output	1.5	-	-	223	-	-	245	ns
		3.3	7.1	-	24.9	6.9	-	27.4	ns
		5	5.1	-	17.8	4.9	-	19.6	ns
$t_{PZH}, t_{PZL}, t_{PHZ}, t_{PLZ}$	Propagation delay, output enable and output disable to output	1.5	-	-	155	-	-	169	ns
		3.3	5.2	-	18.7	5.1	-	20.3	ns
		5	3.5	-	12.3	3.4	-	13.5	ns
C_O	Three-state output capacitance	-	-	-	15	-	-	15	pF
C_I	Input capacitance	-	-	-	10	-	-	10	pF
C_{PD} (3)	Power dissipation capacitance	-	-	120	-	-	120	-	pF

(1) 3.3V Min is at 3.6V, Max is at 3V.

(2) 5V Min is at 5.5V, Max is at 4.5V.

(3) C_{PD} is used to determine the dynamic power consumption per device.

备注

$$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$$
 where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

5 Parameter Measurement Information

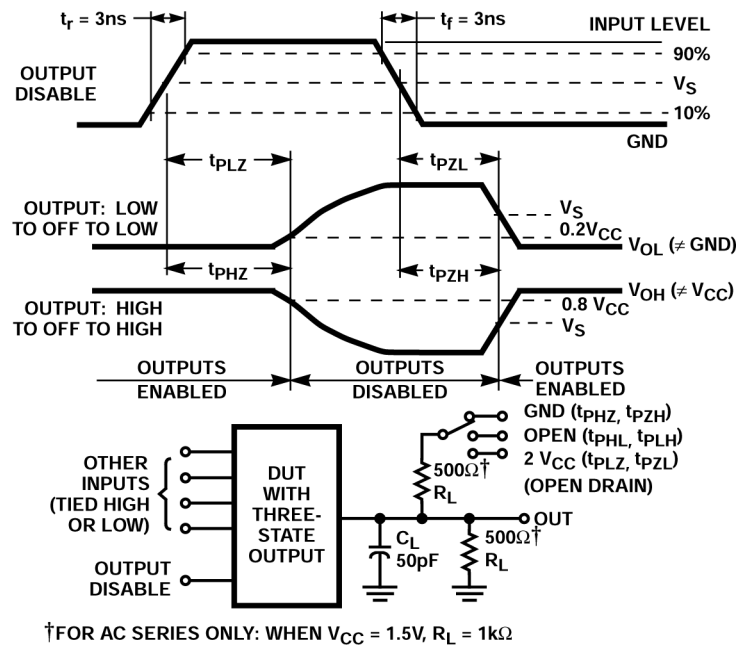


图 5-1. Three-state Propagation Delay Waveforms and Test Circuit

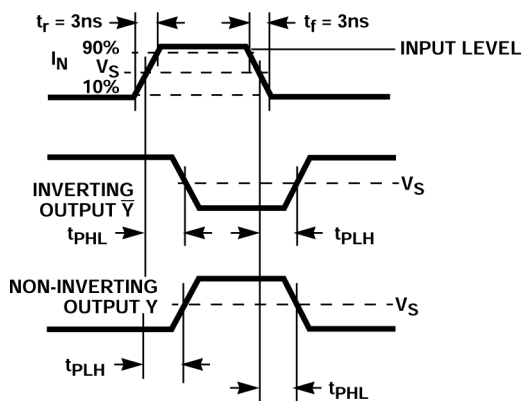
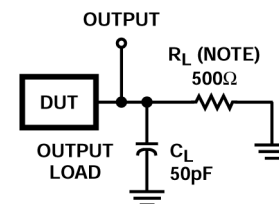


图 5-2. Propagation Delay Times



A. For AC Series Only: When $V_{CC} = 1.5V$, $R_L = 1k\Omega$.

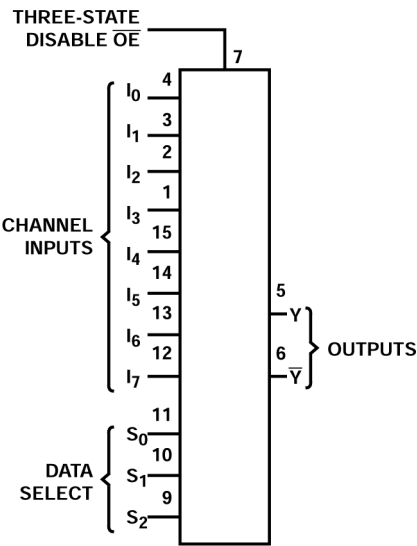
图 5-3. Propagation Delay Times

	CD74AC
Input Level	V_{CC}
Input Switching Voltage, V_S	$0.5 V_{CC}$
Output Switching Voltage, V_S	$0.5 V_{CC}$

† FOR AC SERIES ONLY: WHEN $V_{CC} = 1.5V$, $R_L = 1k\Omega$

6 Detailed Description

6.1 Functional Block Diagram



6.2 Device Functional Modes

表 6-1. Truth Table

INPUTS			OUTPUTS	
SELECT			Y	Y̅
S2	S1	S0		
X	X	X	Z	Z
L	L	L	I ₀	I̅ ₀
L	L	H	I ₁	I̅ ₁
L	H	L	I ₂	I̅ ₂
L	H	H	I ₃	I̅ ₃
H	L	L	I ₄	I̅ ₄
H	L	H	I ₅	I̅ ₅
H	H	L	I ₆	I̅ ₆
H	H	H	I ₇	I̅ ₇

7 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [节 4.2](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μf is recommended; if there are multiple V_{CC} pins, then 0.01 μf or 0.022 μf is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μf and a 1 μf are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Layout Diagram specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is most convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support (Analog)

8.1.1 Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CD74AC251	Click here	Click here	Click here	Click here	Click here

8.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](#) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

8.4 Trademarks

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8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (August 1998) to Revision A (August 2024)	Page
• 删除了数据表通篇对于 CD74ACT251 的引用.....	1
• 添加了封装信息表、引脚功能表、ESD 等级表、热性能信息表、器件功能模式、“应用和实施”部分、器件和文档支持部分以及机械、封装和可订购信息部分.....	1
• Added R _{θJA} value: D = 119.9, all values in °C/W.....	4

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74AC251M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC251M
CD74AC251M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC251M

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC251M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

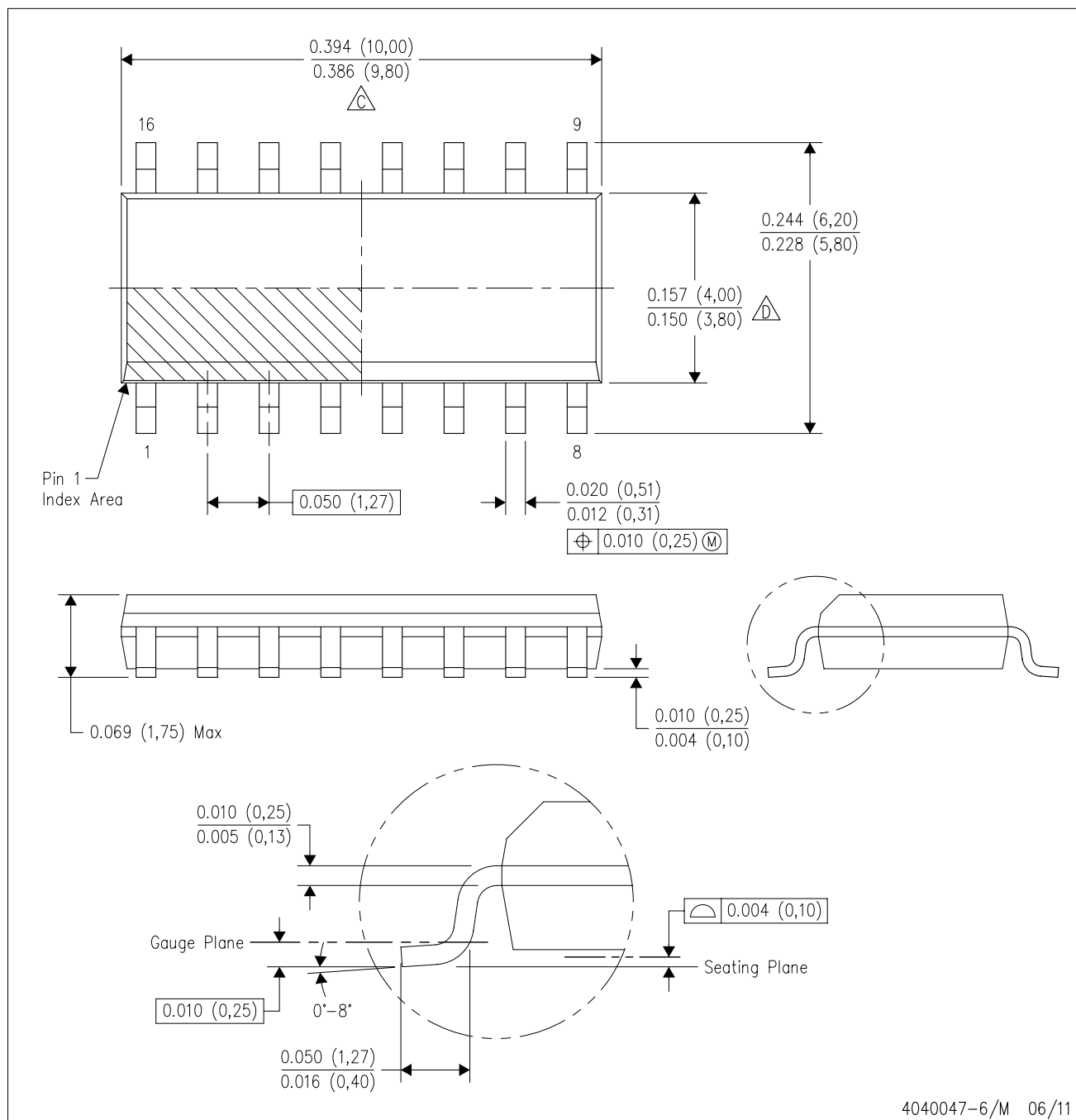


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC251M96	SOIC	D	16	2500	353.0	353.0	32.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

重要通知和免责声明

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邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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