

CD74AC175 具有清零功能的四路 D 类触发器

1 特性

- 交流类型的工作电压范围为 1.5V 至 5.5V，并在电源电压的 30% 时具有平衡的抗噪性能
- 缓冲输入
- 包含四个具有双轨输出的触发器
- 双极 F、AS 和 S 的速度，同时功耗显著降低
- 平衡传播延迟
- $\pm 24mA$ 输出驱动电流
 - 扇出至 15 个 F 器件
- 防 SCR 闩锁 CMOS 工艺和电路设计
- ESD 保护超过 2kV (根据 MIL-STD-883 方法 3015)

2 应用

- 缓冲器/存储寄存器
- 移位寄存器
- 图形发生器

3 说明

这些正边沿触发式 D 类触发器具有直接清零 (\overline{CLR}) 输入。CD74AC175 器具有来自每个触发器的互补输出。

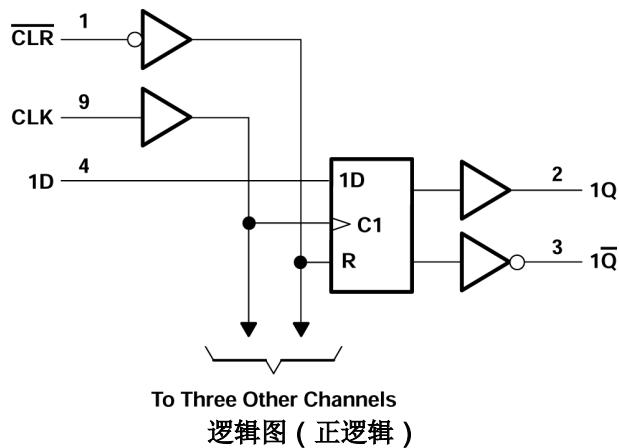
封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾	本体尺寸 ⁽³⁾
CD74AC175	D (SOIC , 16)	9.9mm x 6mm	9.9mm x 3.9mm

(1) 如需了解更多信息，请参阅 [机械、封装和可订购信息](#)。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。

(3) 本体尺寸 (长 × 宽) 为标称值，不包括引脚。



本资源的原文使用英文撰写。为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。为确认准确性，请务必访问 ti.com 参考最新的英文版本 (控制文档)。

Table of Contents

1 特性	1	7 Detailed Description	9
2 应用	1	7.1 Overview.....	9
3 说明	1	7.2 Functional Block Diagram.....	9
4 Pin Configurations and Functions	3	7.3 Device Functional Modes.....	9
5 Specifications	4	8 Application and Implementation	10
5.1 Absolute Maximum Ratings.....	4	8.1 Power Supply Recommendations.....	10
5.2 ESD Ratings.....	4	8.2 Layout.....	10
5.3 Recommended Operating Conditions.....	4	9 Device and Documentation Support	11
5.4 Thermal Information.....	4	9.1 Documentation Support (Analog).....	11
5.5 Electrical Characteristics.....	5	9.2 接收文档更新通知.....	11
5.6 Timing Requirements, $V_{CC} = 1.5V$	5	9.3 支持资源.....	11
5.7 Timing Requirements, $V_{CC} = 3.3V \pm 0.3V$	5	9.4 Trademarks.....	11
5.8 Timing Requirements, $V_{CC} = 5V \pm 0.5V$	6	9.5 静电放电警告.....	11
5.9 Switching Characteristics, $V_{CC} = 1.5V$	6	9.6 术语表.....	11
5.10 Switching Characteristics, $V_{CC} = 3.3V \pm 0.3V$	6	10 Revision History	11
5.11 Switching Characteristics, $V_{CC} = 5V \pm 0.5V$	7	11 Mechanical, Packaging, and Orderable Information	11
5.12 Operating Characteristics.....	7		
6 Parameter Measurement Information	8		

4 Pin Configurations and Functions

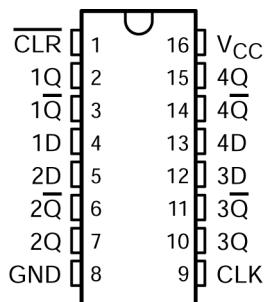


图 4-1. D Package, 16-PIN SCOIC (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	CLR	I	Clear Pin
2	1Q	O	1Q Output
3	1Q̄	O	1Q̄ Output
4	1D	I	1D Input
5	2D	I	2D Input
6	2Q	O	2Q Output
7	2Q̄	O	2Q̄ Output
8	GND	—	Ground Pin
9	CLK	I	Clock Input
10	3Q	O	3Q Output
11	3Q̄	O	3Q̄ Output
12	3D	I	3D Input
13	4D	I	4D Input
14	4Q	O	4Q Output
15	4Q̄	O	4Q̄ Output
16	Vcc	—	Power Pin

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		- 0.5	6	V
I _{IK}	Input clamp current	(V _I < 0 V or V _I > V _{CC}) ⁽²⁾		±20	mA
I _{OK}	Output clamp current	(V _O < 0 V or V _O > V _{CC}) ⁽²⁾		±50	mA
I _O	Continuous output current	(V _O > 0 V or V _O < V _{CC})		±50	mA
	Continuous current through V _{CC} or GND			±200	mA
T _{stg}	Storage temperature range		- 65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		T _A = 25°C		- 55°C to 125°C		- 40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	1.5	5.5	1.5	5.5	1.5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 1.5V	1.2	1.2	1.2	1.2	1.2	V
		V _{CC} = 3V	2.1	2.1	2.1	2.1	2.1	
		V _{CC} = 5.5V	3.85	3.85	3.85	3.85	3.85	
V _{IL}	Low-level input voltage	V _{CC} = 1.5V	0.3	0.3	0.3	0.3	0.3	V
		V _{CC} = 3V	0.9	0.9	0.9	0.9	0.9	
		V _{CC} = 5.5V	1.65	1.65	1.65	1.65	1.65	
V _I	Input voltage	0	V _{CC}	0	V _{CC}	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 4.5V to 5.5V		- 24	- 24	- 24	- 24	mA
I _{OL}	Low-level output current	V _{CC} = 4.5V to 5.5V		24	24	24	24	mA
Δ t / Δ v	Input transition rise or fall rate	V _{CC} = 1.5V to 3V	50	50	50	50	50	ns/V
		V _{CC} = 3.6V to 5.5V	20	20	20	20	20	

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾	D (SOIC)		UNIT
	16 PINS		
R _{θJA}	Junction-to-ambient thermal resistance		106.6 °C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)). The package thermal impedance is calculated in accordance with JESD 51-7.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ C$		$-55^\circ C \text{ to } 125^\circ C$		$-40^\circ C \text{ to } 85^\circ C$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -50 \mu A$	1.5V	1.4	1.4		1.4		V
			3V	2.9	2.9		2.9		
			4.5V	4.4	4.4		4.4		
		$I_{OH} = -4mA$	3V	2.58	2.4		2.48		
		$I_{OH} = -24mA$	4.5V		3.85				
		$I_{OH} = -50mA^{(1)}$	5.5V				3.85		
V_{OL}	$V_I = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 50 \mu A$	1.5V		0.1	0.1	0.1		V
			3V		0.1	0.1	0.1		
			4.5V		0.1	0.1	0.1		
		$I_{OL} = 12mA$	3V		0.36	0.5	0.44		
		$I_{OL} = 24mA$	4.5V		0.36	0.5	0.44		
		$I_{OL} = 50mA^{(1)}$	5.5V			1.65			
I_I	$V_I = V_{CC} \text{ or GND}$		5.5 V		± 0.1	± 1	± 1	μA	
	I_{CC}		$V_I = V_{CC} \text{ or GND}, I_O = 0$	5.5 V		8	160	80	μA
	C_i				10	10	10	10	pF

- (1) Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50- Ω transmission-line drive capability at 85°C and 75- Ω transmission-line drive capability at 125°C.

表 5-1. Act Input Load Table

INPUT	UNIT LOAD
Data	0.58
CLR	0.67
CLK	0.92

5.6 Timing Requirements, $V_{CC} = 1.5V$

over recommended operating free-air temperature range, $V_{CC} = 1.5V$ (unless otherwise noted)

			$-55^\circ C \text{ to } 125^\circ C$		$-40^\circ C \text{ to } 85^\circ C$		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			8		114	MHz
t_w	Pulse duration	CLR low	50		44		ns
		CLK high or low	63		55		
t_{su}	Setup time before CLK \uparrow	Data	2		2		ns
t_h	Hold time, data after CLK \uparrow		2		2		ns
t_{rec}	Recovery time, before CLK \uparrow	CLR \uparrow	1		1		ns

5.7 Timing Requirements, $V_{CC} = 3.3V \pm 0.3V$

over recommended operating free-air temperature range, $V_{CC} = 3.3V \pm 0.3V$ (unless otherwise noted)

			$-55^\circ C \text{ to } 125^\circ C$		$-40^\circ C \text{ to } 85^\circ C$		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			71		81	MHz

over recommended operating free-air temperature range, $V_{CC} = 3.3V \pm 0.3V$ (unless otherwise noted)

		$-55^{\circ}C \text{ to } 125^{\circ}C$		$-40^{\circ}C \text{ to } 85^{\circ}C$		UNIT
		MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLR low	5.6	4.9		ns
		CLK high or low	7	6.1		
t_{su}	Setup time before CLK \uparrow	Data	2	2		ns
t_h	Hold time, data after CLK \uparrow		2	2		ns
t_{rec}	Recovery time, before CLK \uparrow	CLR \uparrow	1	1		ns

5.8 Timing Requirements, $V_{CC} = 5V \pm 0.5V$

over recommended operating free-air temperature range, $V_{CC} = 5V \pm 0.5V$ (unless otherwise noted)

		$-55^{\circ}C \text{ to } 125^{\circ}C$		$-40^{\circ}C \text{ to } 85^{\circ}C$		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		100		114	MHz
t_w	Pulse duration	CLR low	4	3.5		ns
		CLK high or low	5	4.4		
t_{su}	Setup time before CLK \uparrow	Data	2	2		ns
t_h	Hold time, data after CLK \uparrow		2	2		ns
t_{rec}	Recovery time, before CLK \uparrow	CLR \uparrow	1	1		ns

5.9 Switching Characteristics, $V_{CC} = 1.5V$

over recommended operating free-air temperature range, $V_{CC} = 1.5V$, $C_L = 50pF$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$-55^{\circ}C \text{ to } 125^{\circ}C$		$-40^{\circ}C \text{ to } 85^{\circ}C$		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			8		9		MHz
t_{PLH}	CLK	Any Q		153		139	ns
t_{PHL}				153		139	
t_{PLH}	CLR	Any Q		153		139	ns
t_{PHL}				153		139	

5.10 Switching Characteristics, $V_{CC} = 3.3V \pm 0.3V$

over recommended operating free-air temperature range, $V_{CC} = 3.3V \pm 0.3V$, $C_L = 50pF$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$-55^{\circ}C \text{ to } 125^{\circ}C$		$-40^{\circ}C \text{ to } 85^{\circ}C$		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			71		81		MHz
t_{PLH}	CLK	Any Q	4.3	17.1	4.4	15.5	ns
t_{PHL}			4.3	17.1	4.4	15.5	
t_{PLH}	CLR	Any Q	4.3	17.1	4.4	15.5	ns
t_{PHL}			4.3	17.1	4.4	15.5	

5.11 Switching Characteristics, $V_{CC} = 5V \pm 0.5V$

over recommended operating free-air temperature range, $V_{CC} = 5V \pm 0.5V$, $C_L = 50pF$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

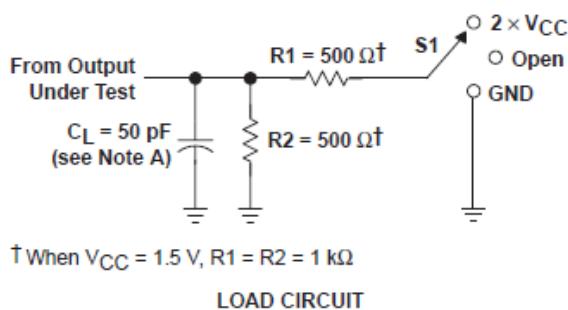
PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			100		114		MHz
t_{PLH}	CLK	Any Q	3.1	12.2	3.2	11.1	ns
t_{PHL}			3.1	12.2	3.2	11.1	
t_{PLH}	\overline{CLR}	Any Q	3.1	12.2	3.2	11.1	ns
t_{PHL}			3.1	12.2	3.2	11.1	

5.12 Operating Characteristics

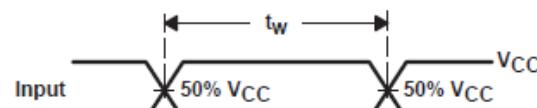
$V_{CC} = 5 V$, $T_A = 25^\circ C$

PARAMETER	TYP	UNIT
C_{pd} Power dissipation capacitance	55	pF

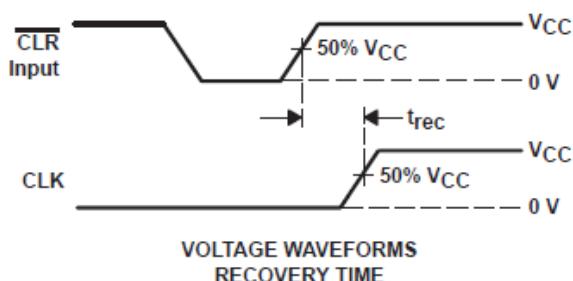
6 Parameter Measurement Information



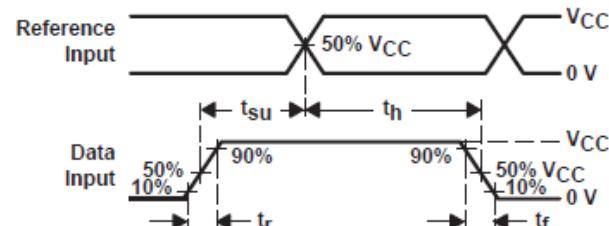
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



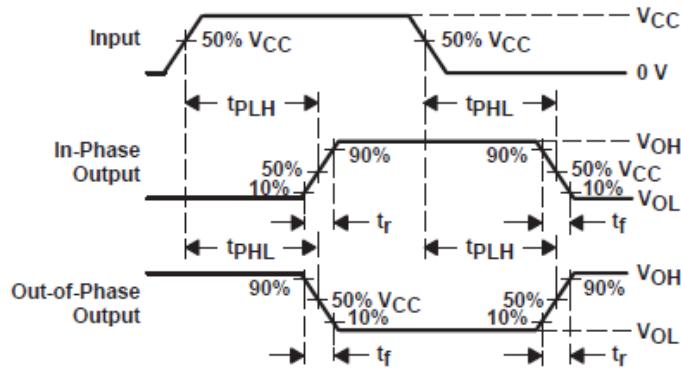
VOLTAGE WAVEFORMS
PULSE DURATION



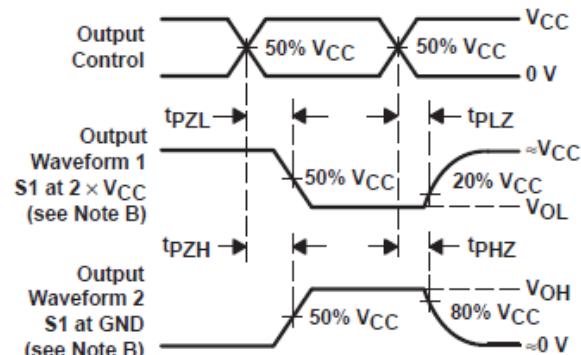
VOLTAGE WAVEFORMS
RECOVERY TIME



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$. Phase relationships between waveforms are arbitrary.
 - D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
 - E. The outputs are measured one at a time, with one input transition per measurement.
 - F. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - G. t_{PZL} and t_{PZH} are the same as t_{en} .
 - H. t_{PLZ} and t_{PHZ} are the same as t_{dis} .

图 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

Information at the data (D) inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

7.2 Functional Block Diagram

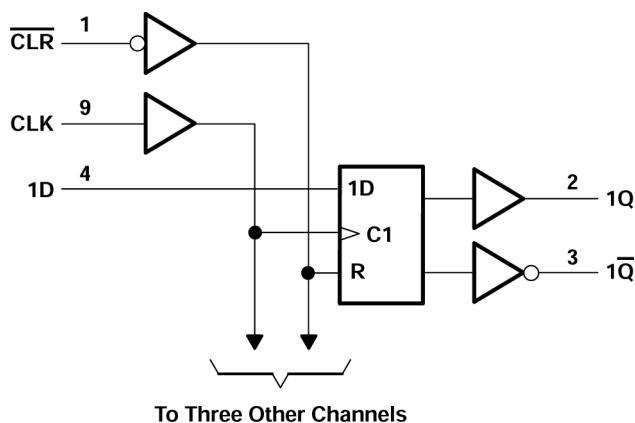


图 7-1. Logic Diagram (Positive Logic)

7.3 Device Functional Modes

表 7-1. Function Table (Each Flip-flop)

INPUTS			OUTPUTS	
CLR	CLK	D	Q	\bar{Q}
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	\bar{Q}_0

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in [#5.3](#).

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends 0.1 μF and if there are multiple V_{CC} terminals, then TI recommends .01 μF or .022 μF for each power terminal. It is okay to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.2 Layout

8.2.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. It is generally okay to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This does not disable the input section of the IOs so they cannot float when disabled.

9 Device and Documentation Support

9.1 Documentation Support (Analog)

9.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CD74AC175	Click here				

9.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](#) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

[TI E2E™ 中文支持论坛](#)是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的[使用条款](#)。

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表

本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (April 2003) to Revision A (April 2024)	Page
• 添加了应用部分、封装信息表、引脚功能表、ESD 等级表、热性能信息表、器件功能模式、应用和实施部分、器件和文档支持部分以及机械、封装和可订购信息部分.....	1
• Updated thermal values for R ^θ JA: D = 73 to 106.6, all values in °C/W	4

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74AC175M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	AC175M
CD74AC175M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC175M
CD74AC175M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC175M

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

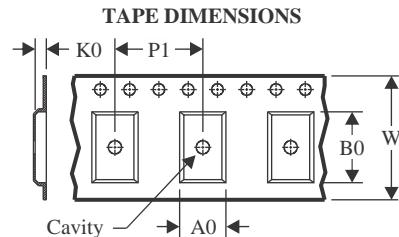
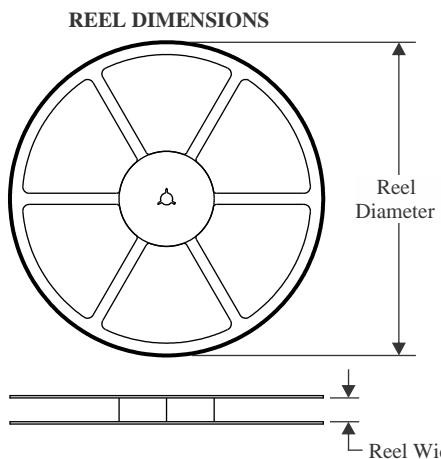
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

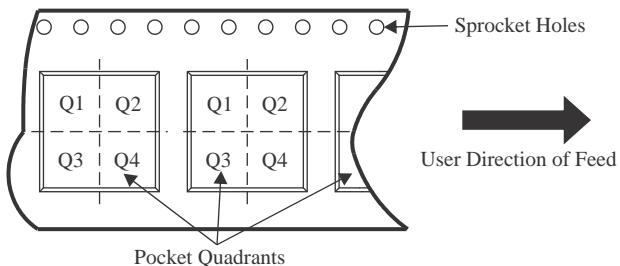
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

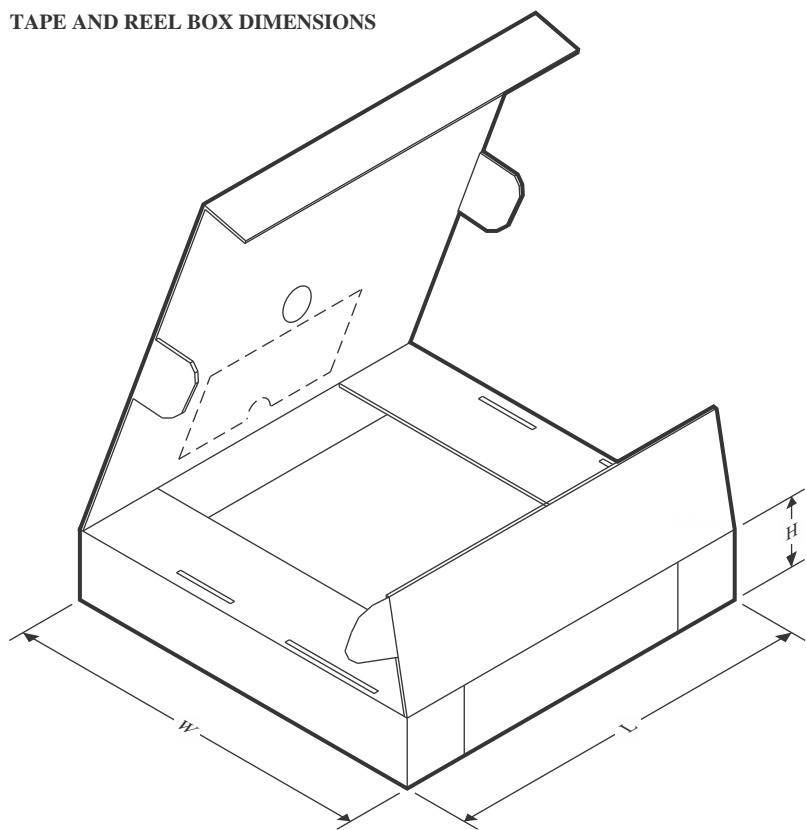
TAPE AND REEL INFORMATION

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC175M96	SOIC	D	16	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
CD74AC175M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74AC175M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

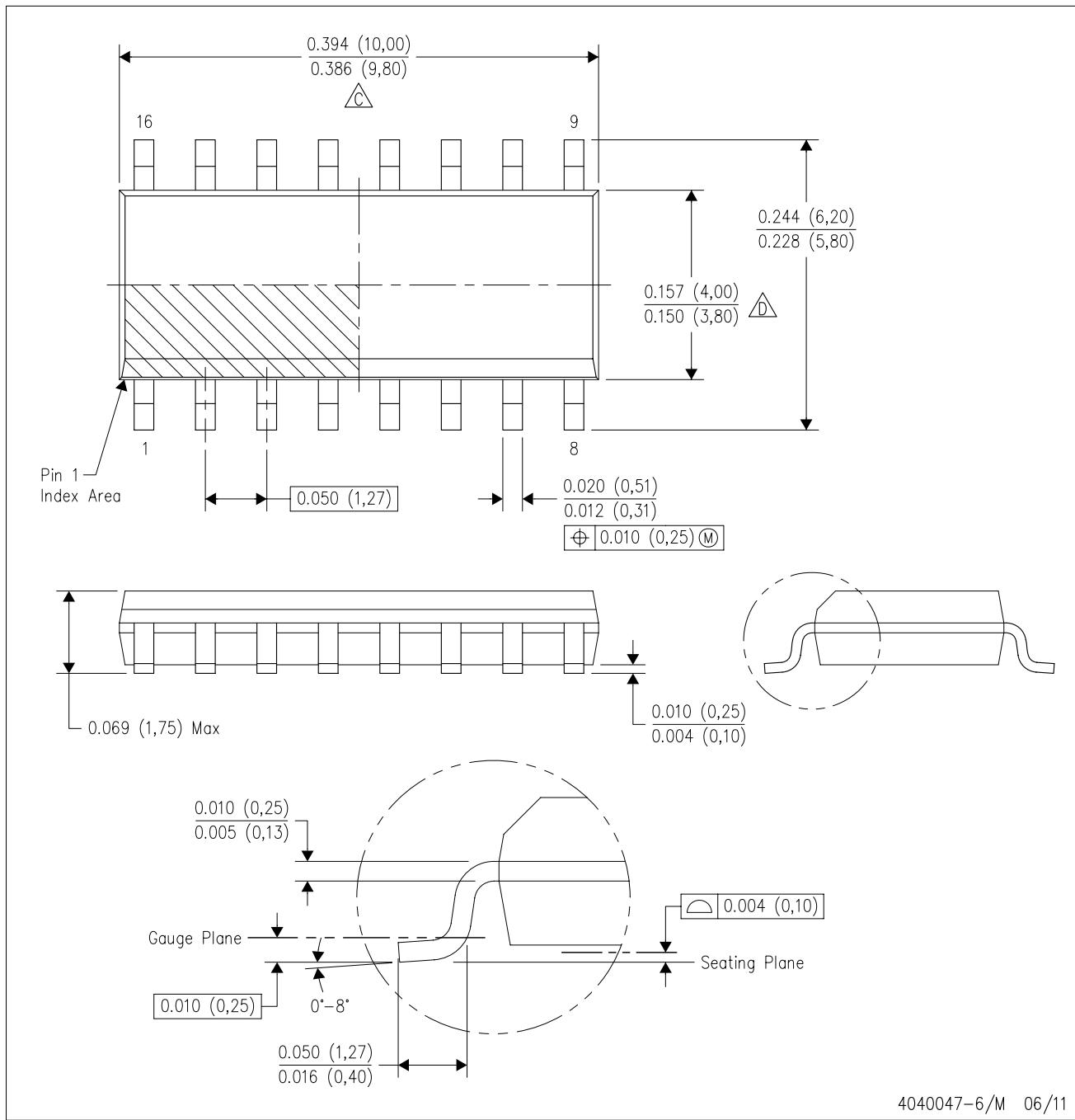
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC175M96	SOIC	D	16	2500	340.5	336.1	32.0
CD74AC175M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74AC175M96	SOIC	D	16	2500	353.0	353.0	32.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

4040047-6/M 06/11

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

版权所有 © 2025 , 德州仪器 (TI) 公司