TEXAS INSTRUMENTS
CD54HC4051, CD74HC4051, CD54HCT4051, CD74HCT4051, CD54HC4052, CD74HC4052, CD54HCT4052, CD74HCT4052, CD54HC4053, CD74HC4053, CD54HCT4053, CD74HCT4053
ZHCSJS2N – NOVEMBER 1997 – REVISED APRIL 2024

CDx4HC405x、CD4HCT405x 高速 CMOS 逻辑模拟多路复用器和多路信号分离器

1 特性

- 符合汽车应用要求
- 宽模拟输入电压范围：±5V（最大值）
- 低导通电阻：
  - 70Ω（典型值）(V_{CC} – V_{EE} = 4.5V)
  - 40Ω（典型值）(V_{CC} – V_{EE} = 9V)
- 低开关间串扰
- 快速开关和传播速度
- 先断后合开关
- 宽工作温度范围：
  –40°C 至 +125°C
- 工作控制电压：4.5V 至 5.5V
- 开关电压：0V 至 10V
- 直接 LSTTL 输入逻辑兼容性
  V_{IL} = 0.8V（最大值），V_{IH} = 2V（最小值）
- CMOS 输入兼容性
  在 V_{OL}、V_{OH} 下 $I_I \leq 1\mu A$

2 应用

- 数字射频
- 信号门控
- 工厂自动化
- 电视
- 电器
- 可编程逻辑电路
- 传感器

3 说明

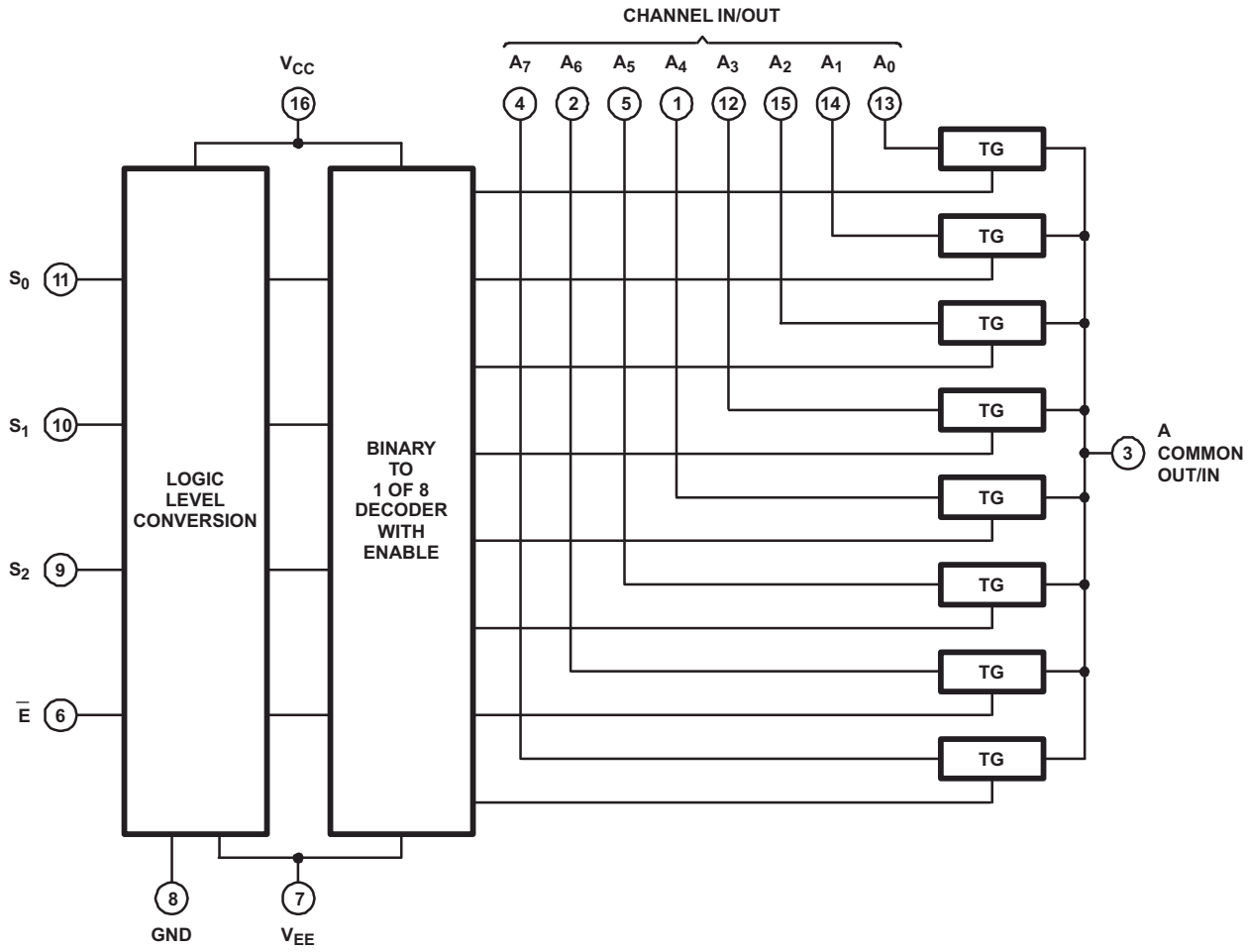
CDx4HC405x 和 CDx4HCT405x 器件是数字控制的模拟开关，它使用硅栅 CMOS 技术并借助标准 CMOS 集成电路的低功耗特性来实现与 LSTTL 接近的运行速度。

该模拟多路复用器和多路信号分离器可控制模拟电压，该电压可能会在整个电源电压范围内变化（例如，V_{CC} 变为 V_{EE}）。它是双向开关，可将任何模拟输入用作输出，反之亦然。该开关具有低导通电阻和低关断泄漏。此外，该器件还具有使能控制，当处于高电平时将禁用所有开关，将其置于关断状态。

器件信息

器件型号	T_A	封装(1)	封装尺寸(2)
CD54HCx405x	-55°C 至 125°C	J（CDIP、16）	19.56mm × 6.92mm
CD74HCx405x		N（PDIP，16）	19.30mm × 6.35mm
		D（SOIC，16）	9.9mm × 3.9mm
		NS（SOP，16）	10.3mm × 5.3mm
		PW（TSSOP，16）	5mm × 4.4mm

(1) 有关更多信息，请参阅节 11。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



HCT4051 的功能方框图

Table of Contents

4 Pin Configuration and Functions

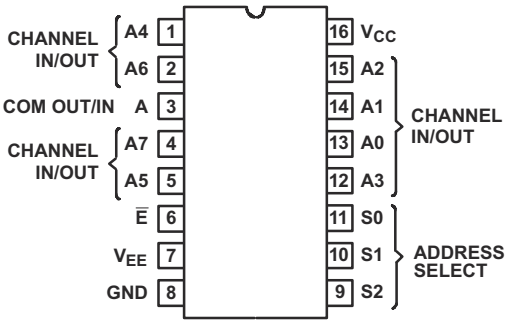


图 4-1. CDx4HCx4051 J, N, D, NS, PW Packages 16-Pin CDIP, PDIP, SOIC, SO, TSSOP (Top View)

表 4-1. Pin Functions for CDxHCx4051B

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
CH A4 IN/OUT	1	I/O	Channel 4 in/out
CH A6 IN/OUT	2	I/O	Channel 6 in/out
COM OUT/IN	3	I/O	Common out/in
CH A7 IN/OUT	4	I/O	Channel 7 in/out
CH A5 IN/OUT	5	I/O	Channel 5 in/out
!E	6	I	Enable Channels (Active Low)
V_{EE}	7	—	Negative power input
GND	8	—	Ground
S2	9	I	Channel select 2
S1	10	I	Channel select 1
S0	11	I	Channel select 0
CH A3 IN/OUT	12	I/O	Channel 3 in/out
CH A0 IN/OUT	13	I/O	Channel 0 in/out
CH A1 IN/OUT	14	I/O	Channel 1 in/out
CH A2 IN/OUT	15	I/O	Channel 2 in/out
V_{CC}	16	—	Positive power input

(1) I = input, O = output

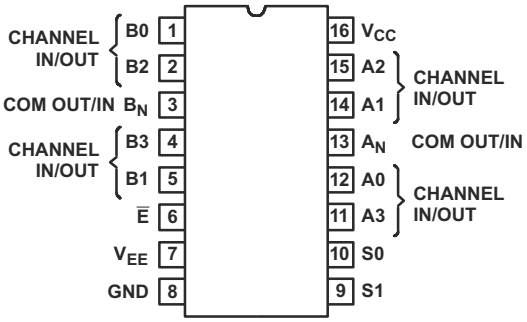


图 4-2. CDx4HCx4052 J, N, D, NS, PW Packages 16-Pin CDIP, PDIP, SOIC, SO, TSSOP (Top View)

表 4-2. Pin Functions for CDx4HCx4052B

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
CH B0 IN/OUT	1	I/O	Channel B0 in/out
CH B2 IN/OUT	2	I/O	Channel B2 in/out
COM B OUT/IN	3	I/O	B common out/in
CH B3 IN/OUT	4	I/O	Channel B3 in/out
CH B1 IN/OUT	5	I/O	Channel B1 in/out
!E	6	I	Enable channels (Active Low)
V_{EE}	7	—	Negative power input
GND	8	—	Ground
S1	9	I	Channel select 1
S0	10	I	Channel select 0
CH A3 IN/OUT	11	I/O	Channel A3 in/out
CH A0 IN/OUT	12	I/O	Channel A0 in/out
COM A IN/OUT	13	I/O	A common out/in
CH A1 IN/OUT	14	I/O	Channel A1 in/out
CH A2 IN/OUT	15	I/O	Channel A2 in/out
V_{CC}	16	—	Positive power input

(1) I = input, O = output

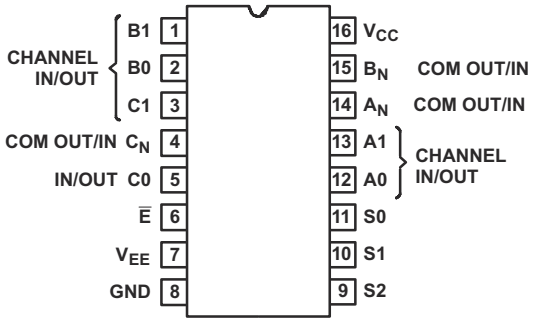


图 4-3. CDx4HCx4053 J, N, D, NS, PW Packages 16-Pin CDIP, PDIP, SOIC, SO, TSSOP (Top View)

表 4-3. Pin Functions CDx4HCx4053B

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
B1IN/OUT	1	I/O	B channel Y in/out
B0 IN/OUT	2	I/O	B channel X in/out
C1 IN/OUT	3	I/O	C channel Y in/out
COM C OUT/IN	4	I/O	C common out/in
C0 IN/OUT	5	I/O	C channel X in/out
!E	6	I	Enable channels (Active Low)
V_{EE}	7	—	Negative power input
GND	8	—	Ground
S2	9	I	Channel select 2
S1	10	I	Channel select 1
S0	11	I	Channel select 0
A0 IN/OUT	12	I/O	A channel X in/out
A1 IN/OUT	13	I/O	A channel Y in/out
COM A OUT/IN	14	I/O	A common out/in
COM B OUT/IN	15	I/O	B common out/in
V_{CC}	16	—	Positive power input

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC} – V_{EE}	DC Supply voltage		-0.5	10.5	V
V_{CC}			– 0.5	7	V
V_{EE}			0.5	-7	V
I_{IK}	DC input diode current	V_I < – 0.5V or V_I > V_{CC} + 0.5V	– 20	20	mA
I_{OK}	DC switch diode current	V_I < V_{EE} – 0.5V or V_I > V_{CC} + 0.5V	– 20	20	mA
	DC switch current(2)	V_I < V_{EE} – 0.5V or V_I > V_{CC} + 0.5V	-25	25	mA
I_{CC}	DC V_{CC} or ground current		– 50	50	mA
I_{EE}	DC V_{EE} current		– 20		mA
V_{SEL} or V_{EN}	Logic control input pin voltage ($\overline{EN}$, Ax, SELx)		– 0.5	30	V
T_{JMAX}	Maximum junction temperature			150	°C
T_{LMAX}	Maximum lead temperature	Soldering 10 s		300	°C
T_{stg}	Storage temperature		– 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Thermal Information

THERMAL METRIC[1]		CD74HC4051			UNIT
		N (PDIP)	NS (SO)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	77.3	99.3	116.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.2	59.6	51.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.6	65.7	73.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	33.7	21.5	4.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	52.1	65.1	73.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage range (T_A = full package temperature range)[2]	CD54 and 74HC types	2		6	V
		CD54 and 74HCT types	4.5		5.5	
$V_{CC} - V_{EE}$	Supply voltage range (T_A = full package temperature range)	CD54 and 74HC types, CD54 and 74HCT types	2		10	V
V_{EE}	Supply voltage range (T_A = full package temperature range)[3]	CD54 and 74HC types, CD54 and 74HCT types	0		–6	V
V_I	DC input control voltage		0		V_{CC}	V
V_{IS}	Analog switch I/O voltage		V_{EE}		V_{CC}	V
T_A	Ambient temperature		–55		125	°C
t_r , t_f	Input rise and fall times	2V	0		1000	ns
		4.5V	0		500	
		6V	0		400	

(1) For maximum reliability, nominal operating conditions must be selected so that operation is always within the ranges specified in the *Recommended Operating Conditions* table.
(2) All voltages referenced to GND unless otherwise specified.
(3) In certain applications, the external load resistor current may include both V_{CC} and signal line components. To avoid drawing V_{CC} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.6V (calculated from r_{ON} values shown in *Electrical Characteristics HC* and *Electrical Characteristics HCT* tables). No V_{CC} current will flow through R_L if the switch current flows into terminal 3 on the HC and HCT40511; terminals 3 and 13 on the HC and HCT4052; terminals 4, 14, and 15 on the HC and HCT4053.

5.5 Electrical Characteristics: HC Devices

Over operating free-air temperature range, V_{SUPPLY} = ±5V, and R_L = 100 Ω, (unless otherwise noted)

PARAMETER	TEST CONDITIONS						MIN	TYP	MAX	UNIT
CD74HC405x										
		V_{IS} (V)	V_I (V)	V_{EE} (V)	V_{CC} (V)	T_A				
Input High Voltage, V_{IH}, Min					2	25°C	1.5			V
						–40°C to +85°C	1.5			
						–55°C to +125°C	1.5			
					4.5	25°C	3.15			
						–40°C to +85°C	3.15			
						–55°C to +125°C	3.15			
					6	25°C	4.2			
						–40°C to +85°C	4.2			
						–55°C to +125°C	4.2			
Input Low Voltage, V_{IL}, Max					2	25°C			0.5	V
						–40°C to +85°C			0.5	
						–55°C to +125°C			0.5	
					4.5	25°C			1.35	
						–40°C to +85°C			1.35	
						–55°C to +125°C			1.35	
					6	25°C			1.8	
						–40°C to +85°C			1.8	
						–55°C to +125°C			1.8	

5.5 Electrical Characteristics: HC Devices （续）

Over operating free-air temperature range, V_{SUPPLY} = ±5V, and R_L = 100 Ω, (unless otherwise noted)

PARAMETER	TEST CONDITIONS						MIN	TYP	MAX	UNIT
r_{ON} ON resistance	I_O = 1mA	V_{CC} or V_{EE}	V_{IL} or V_{IH}	0	4.5	25°C		70	160	Ω
						–40°C to +85°C			200	
						–55°C to +125°C			240	
				0	6	25°C		60	140	
						–40°C to +85°C			175	
						–55°C to +125°C			210	
				-4.5	4.5	25°C		40	120	
						–40°C to +85°C			150	
						–55°C to +125°C			180	
		V_{CC} to V_{EE}		0	4.5	25°C		90	180	Ω
						–40°C to +85°C			225	
						–55°C to +125°C			270	
				0	6	25°C		80	160	
						–40°C to +85°C			200	
						–55°C to +125°C			240	
				-4.5	4.5	25°C		45	130	
						–40°C to +85°C			162	
						–55°C to +125°C			195	
Δr_{ON} Maximum ON resistance between any two channels				0	4.5	25°C		10		Ω
				0	6	25°C		8.5		
				-4.5	4.5	25°C		5		

5.5 Electrical Characteristics: HC Devices （续）

Over operating free-air temperature range, V_{SUPPLY} = ±5V, and R_L = 100 Ω, (unless otherwise noted)

PARAMETER	TEST CONDITIONS						MIN	TYP	MAX	UNIT
I_{IZ} Switch ON/OFF leakage current	1 and 2 channels	For switch OFF: When V_{IS} = V_{CC}, V_{OS} = V_{EE}; When V_{IS} = V_{EE}, V_{OS} = V_{CC}, For switch ON: All applicable combinations of V_{IS} and V_{OS} voltage levels	V_{IL} or V_{IH}	0	6	25°C			±0.1	µA
						–55°C to 85°C			±1	
						–55°C to 125°C			±1	
	4053			-5	5	25°C			±0.1	
						–55°C to 85°C			±1	
						–55°C to 125°C			±1	
	4 channels			0	6	25°C			±0.1	
						–55°C to 85°C			±1	
						–55°C to 125°C			±1	
	4052			-5	5	25°C			±0.2	
						–55°C to 85°C			±2	
						–55°C to 125°C			±2	
	8 channels			0	6	25°C			±0.2	
						–55°C to 85°C			±2	
						–55°C to 125°C			±2	
	4051			-5	5	25°C			±0.4	
						–55°C to 85°C			±4	
						–55°C to 125°C			±4	
I_{IL} Control input leakage current			V_{CC} or GND	0	6	25°C			±0.1	µA
						–55°C to 85°C			±1	
						–55°C to 125°C			±1	
Quiescent Device Current, I_{CC} Max	I_O = 0	When V_{IS} = V_{EE}, V_{OS} = V_{CC}	V_{CC} or GND	0	6	25°C			12	µA
						–55°C to 85°C			80	
						–55°C to 125°C			160	
		When V_{IS} = V_{CC}, V_{OS} = V_{EE}		-5	5	25°C			32	
						–55°C to 85°C			160	
						–55°C to 125°C			320	

5.6 Electrical Characteristics: HCT Devices

Over operating free-air temperature range, V_{SUPPLY} = ±5V, and R_L = 100 Ω, (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS					MIN	TYP	MAX	UNIT
CD74HCT405x										
		V_{IS} (V)	**V_I (V)**	**V_{EE} (V)**	**V_{CC} (V)**	**T_A**				
Input High Voltage, V_{IH}, Min					4.5 to 5.5	25°C	2			V
						–40°C to +85°C	2			
						–55°C to +125°C	2			
Input Low Voltage, V_{IL}, Max					4.5 to 5.5	25°C			0.8	V
						–40°C to +85°C			0.8	
						–55°C to +125°C			0.8	
r_{ON} ON resistance	I_O = 1mA	V_{CC} or V_{EE}	V_{IL} or V_{IH}	0	4.5	25°C		70	160	Ω
						–40°C to +85°C			200	
						–55°C to +125°C			240	
				-4.5	4.5	25°C		40	120	
						–40°C to +85°C			150	
						–55°C to +125°C			180	
		V_{CC} to V_{EE}		0	4.5	25°C		90	180	
						–40°C to +85°C			225	
						–55°C to +125°C			270	
				-4.5	4.5	25°C		45	130	Ω
						–40°C to +85°C			162	
						–55°C to +125°C			195	
Δr_{ON} Maximum ON resistance between any two channels				0	4.5	25°C		10		Ω
				-4.5	4.5	25°C		5		

5.6 Electrical Characteristics: HCT Devices（续）

Over operating free-air temperature range, V_{SUPPLY} = ±5V, and R_L = 100 Ω, (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS						MIN	TYP	MAX	UNIT
I_{IZ} Switch ON/OFF leakage current	1 and 2 channels	For switch OFF: When V_{IS} = V_{CC}, V_{OS} = V_{EE}; When V_{IS} = V_{EE}, V_{OS} = V_{CC}, For switch ON: All applicable combinations of V_{IS} and V_{OS} voltage levels	V_{IL} or V_{IH}	0	6	25°C			±0.1	µA
						–55°C to 85°C			±1	
						–55°C to 125°C			±1	
	4053			-5	5	25°C			±0.1	
						–55°C to 85°C			±1	
						–55°C to 125°C			±1	
	4 channels			0	6	25°C			±0.1	
						–55°C to 85°C			±1	
						–55°C to 125°C			±1	
	4052			-5	5	25°C			±0.2	
						–55°C to 85°C			±2	
						–55°C to 125°C			±2	
	8 channels			0	6	25°C			±0.2	
						–55°C to 85°C			±2	
						–55°C to 125°C			±2	
	4051			-5	5	25°C			±0.4	
						–55°C to 85°C			±4	
						–55°C to 125°C			±4	
I_{IL} Control input leakage current			See(1)	0	5.5	25°C			±0.1	µA
						–55°C to 85°C			±1	
						–55°C to 125°C			±1	
Quiescent Device Current, I_{CC} Max	I_O = 0	When V_{IS} = V_{EE}, V_{OS} = V_{CC}	V_{CC} or GND	0	5.5	25°C			12	µA
						–55°C to 85°C			80	
						–55°C to 125°C			160	
		When V_{IS} = V_{CC}, V_{OS} = V_{EE}		-4.5	5.5	25°C			32	
						–55°C to 85°C			160	
						–55°C to 125°C			320	

5.6 Electrical Characteristics: HCT Devices（续）

Over operating free-air temperature range, V_{SUPPLY} = ±5V, and R_L = 100 Ω, (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS						MIN	TYP	MAX	UNIT
Δ I_{CC} Additional quiescent device current per input pin: 1 unit load(2)		Δ ICC	V_{CC} - 2.1		4.5 to 5.5	25°C		100	360	μA
						– 55°C to 85°C			450	
						– 55°C to 125°C			490	

(1) Any voltage between V_{CC} and GND.
(2) For dual-supply systems, theoretical worse-case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

5.7 Switching Characteristics, VCC = 5V

V_{CC} = 5V, T_A = 25°C, input t_r,t_f = 6 ns

Parameter		Test Conditions		C_L (pF)	MIN	NOM	MAX	UNIT
t_{PHL}, t_{PLH}	Supply voltage range (T_A = full package temperature range)	Switch IN to OUT	CDx4HC4051	15		4		ns
			CDx4HCT4051			4		
			CDx4HC4052			4		
			CDx4HCT4052			4		
			CDx4HC4053			4		
			CDx4HCT4053			4		
t_{PHZ}, t_{PLZ}		Switch turn-off (S or E)	CDx4HC4051	15		27		
			CDx4HCT4051			35		
			CDx4HC4052			33		
			CDx4HCT4052			33		
			CDx4HC4053			30		
			CDx4HCT4053			35		
t_{PZH}, t_{PZL}		Switch turn-on (S or E)	CDx4HC4051	15		19		
			CDx4HCT4051			23		
			CDx4HC4052			27		
			CDx4HCT4052			29		
			CDx4HC4053			18		
			CDx4HCT4053			28		
C_{PD} Power dissipation capacitance(1)			CDx4HC4051			50		pF
			CDx4HCT4051			52		
			CDx4HC4052			74		
			CDx4HCT4052			76		
			CDx4HC4053			38		
			CDx4HCT4053			42		

(1) C_{PD} is used to determine the dynamic power consumption, per package. $P_D = C_{PD} v_{CC}{}^2 f_i + \Sigma (C_L + C_S) V_{CC}{}^2 f_O$, f_O= output frequency, f_I = input frequency, C_L = output load capacitance, C_S = switch capacitance, V_{CC} = supply voltage

5.8 Switching Characteristics, CL = 50pF

C_L = 50pF, input t_r, t_f = 6 ns

Parameter		V_{EE} (V)	V_{CC} (V)	Test Conditions		MIN	NOM	MAX	UNIT
t_{PHL}, t_{PLH} Propagation delay, switch in to out		0	2	T_A = 25°C	HC			60	ns
				T_A = –40°C to +85°C	HC			75	
				T_A = –55°C to +125°C	HC			90	
		0	4.5	T_A = 25°C	HC, HCT			12	
				T_A = –40°C to +85°C	HC, HCT			15	
				T_A = –55°C to +125°C	HC, HCT			18	
		0	6	T_A = 25°C	HC			10	
				T_A = –40°C to +85°C	HC			13	
				T_A = –55°C to +125°C	HC			15	
		-4.5	4.5	T_A = 25°C	HC, HCT			8	
				T_A = –40°C to +85°C	HC, HCT			10	
				T_A = –55°C to +125°C	HC, HCT			12	
t_{PHZ}, t_{PLZ} Maximum switch turn OFF delay from S or E to switch output	4051	0	2	T_A = 25°C	HC			250	ns
				T_A = –40°C to +85°C	HC			340	
				T_A = –55°C to +125°C	HC			400	
		0	4.5	T_A = 25°C	HC, HCT			50	
				T_A = –40°C to +85°C	HC, HCT			56	
				T_A = –55°C to +125°C	HC, HCT			68	
		0	6	T_A = 25°C	HC			44	
				T_A = –40°C to +85°C	HC			50	
				T_A = –55°C to +125°C	HC			57	
		-4.5	4.5	T_A = 25°C	HC, HCT			44	
				T_A = –40°C to +85°C	HC, HCT			50	
				T_A = –55°C to +125°C	HC, HCT			55	

5.8 Switching Characteristics, CL = 50pF（续）

C_L = 50pF, input t_r, t_f = 6 ns

Parameter		V_{EE} (V)	V_{CC} (V)	Test Conditions		MIN	NOM	MAX	UNIT
t_{PHZ}, t_{PLZ} Maximum switch turn OFF delay from S or E to switch output	4052	0	2	T_A = 25°C	HC			250	ns
				T_A = –40°C to +85°C	HC			340	
				T_A = –55°C to +125°C	HC			400	
		0	4.5	T_A = 25°C	HC, HCT			50	
				T_A = –40°C to +85°C	HC, HCT			63	
				T_A = –55°C to +125°C	HC, HCT			75	
		0	6	T_A = 25°C	HC			45	
				T_A = –40°C to +85°C	HC			54	
				T_A = –55°C to +125°C	HC			65	
		-4.5	4.5	T_A = 25°C	HC			45	
					HCT			45	
				T_A = –40°C to +85°C	HC			48	
					HCT			50	
				T_A = –55°C to +125°C	HC			57	
					HCT			57	
t_{PHZ}, t_{PLZ} Maximum switch turn OFF delay from S or E to switch output	4053	0	2	T_A = 25°C	HC			250	ns
				T_A = –40°C to +85°C	HC			340	
				T_A = –55°C to +125°C	HC			400	
		0	4.5	T_A = 25°C	HC			45	
					HCT			50	
				T_A = –40°C to +85°C	HC			53	
					HCT			53	
				T_A = –55°C to +125°C	HC			63	
					HCT			66	
		0	6	T_A = 25°C	HC			45	
				T_A = –40°C to +85°C	HC			50	
				T_A = –55°C to +125°C	HC			55	
		-4.5	4.5	T_A = 25°C	HC			45	
					HCT			45	
				T_A = –40°C to +85°C	HC			50	
					HCT			50	
				T_A = –55°C to +125°C	HC			55	
					HCT			55	

5.8 Switching Characteristics, CL = 50pF（续）

C_L = 50pF, input t_r, t_f = 6 ns

Parameter		V_{EE} (V)	V_{CC} (V)	Test Conditions		MIN	NOM	MAX	UNIT
t_{PZL}, t_{PZH} Maximum switch turn ON delay from S or E to switch output	4051	0	2	T_A = 25°C	HC			325	ns
				T_A = –40°C to +85°C	HC			405	
				T_A = –55°C to +125°C	HC			490	
		0	4.5	T_A = 25°C	HC			45	
					HCT			55	
				T_A = –40°C to +85°C	HC			56	
					HCT			69	
				T_A = –55°C to +125°C	HC			68	
					HCT			83	
		0	6	T_A = 25°C	HC			38	
				T_A = –40°C to +85°C	HC			48	
				T_A = –55°C to +125°C	HC			57	
		-4.5	4.5	T_A = 25°C	HC			36	
					HCT			48	
				T_A = –40°C to +85°C	HC			40	
					HCT			55	
				T_A = –55°C to +125°C	HC			48	
					HCT			60	
t_{PZL}, t_{PZH} Maximum switch turn ON delay from S or E to switch output	4052	0	2	T_A = 25°C	HC			325	ns
				T_A = –40°C to +85°C	HC			405	
				T_A = –55°C to +125°C	HC			490	
		0	4.5	T_A = 25°C	HC			65	
					HCT			70	
				T_A = –40°C to +85°C	HC			81	
					HCT			68	
				T_A = –55°C to +125°C	HC			98	
					HCT			105	
		0	6	T_A = 25°C	HC			55	
				T_A = –40°C to +85°C	HC			69	
				T_A = –55°C to +125°C	HC			83	
		-4.5	4.5	T_A = 25°C	HC			46	
					HCT			48	
				T_A = –40°C to +85°C	HC			58	
					HCT			60	
				T_A = –55°C to +125°C	HC			69	
					HCT			72	

5.8 Switching Characteristics, CL = 50pF （续）

C_L = 50pF, input t_r, t_f = 6 ns

Parameter		V_{EE} (V)	V_{CC} (V)	Test Conditions		MIN	NOM	MAX	UNIT
t_{PZL}, t_{PZH} Maximum switch turn ON delay from S or E to switch output	4053	0	2	T_A = 25°C	HC			325	ns
				T_A = –40°C to +85°C	HC			405	
				T_A = –55°C to +125°C	HC			490	
		0	4.5	T_A = 25°C	HC			44	
					HCT			48	
				T_A = –40°C to +85°C	HC			55	
					HCT			60	
				T_A = –55°C to +125°C	HC			66	
					HCT			72	
		0	6	T_A = 25°C	HC			37	
				T_A = –40°C to +85°C	HC			47	
				T_A = –55°C to +125°C	HC			56	
		-4.5	4.5	T_A = 25°C	HC			40	
					HCT			48	
				T_A = –40°C to +85°C	HC			45	
					HCT			55	
				T_A = –55°C to +125°C	HC			47	
					HCT			60	
C_I Input (control) capacitance				T_A = 25°C	HC, HCT			10	pF
				T_A = –40°C to +85°C	HC, HCT			10	
				T_A = –55°C to +125°C	HC, HCT			10	

5.9 Analog Channel Specifications

Typical values at T_A = 25°C

Parameter	Test Conditions	HC, HCT TYPES	V_{EE} (V)	V_{CC} (V)	MIN	NOM	MAX	UNIT
C_I Switch input capacitance		All				5		pF
C_{COM} Common output capacitance		4051				25		pF
		4052				12		
		4053				8		
f_{MAX} Minimum switch frequency response at –3 dB	See note(1) and (2)	4051	-2.25	2.25		145		MHz
		4052	-2.25	2.25		165		
		4053	-2.25	2.25		200		
		4051	-4.5	4.5		180		
		4052	-4.5	4.5		185		
		4053	-4.5	4.5		200		

5.9 Analog Channel Specifications（续）

Typical values at T_A = 25°C

Parameter	Test Conditions	HC, HCT TYPES	V_{EE} (V)	V_{CC} (V)	MIN	NOM	MAX	UNIT
THD Sine-wave distortion		All	-2.25	2.25		0.035		%
		All	-4.5	4.5		0.018		
Switch OFF signal feedthrough	See note(2) and (3)	4051	-2.25	2.25		-73		dB
		4052	-2.25	2.25		-65		
		4053	-2.25	2.25		-64		
		4051	-4.5	4.5		-75		
		4052	-4.5	4.5		-67		
		4053	-4.5	4.5		-66		

(1) Adjust input voltage to obtain 0 dBm at V_{OS} for f_{IN} = 1 MHz.
(2) V_{is} is centered at (V_{CC} - V_{EE}) / 2.
(3) Adjust input for 0 dBm.

5.10 Typical Characteristics

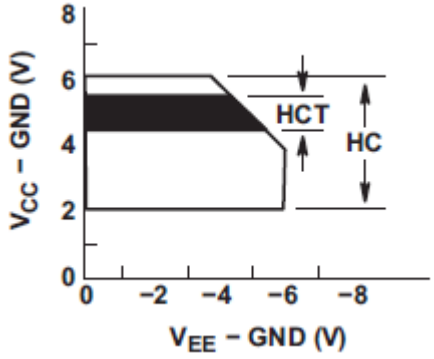


图 5-1. Recommended Operating Area as a Function of (V_{CC} - V_{EE})

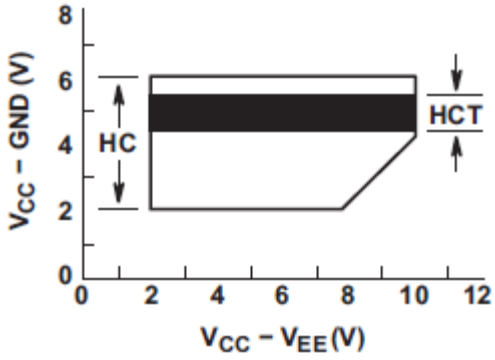


图 5-2. Recommended Operating Area as a Function of (V_{CC} - GND)

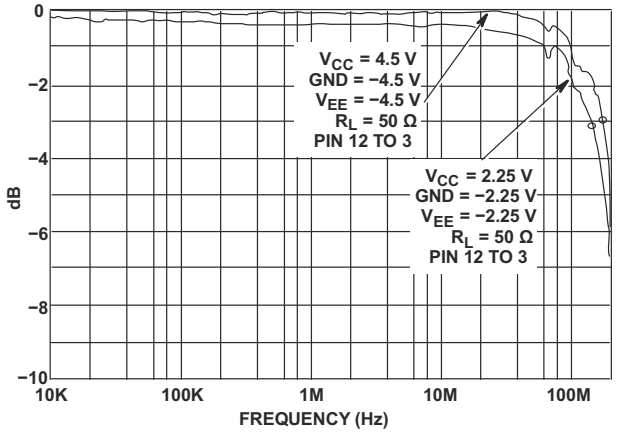


图 5-3. Channel ON Bandwidth (HC and HCT4051)

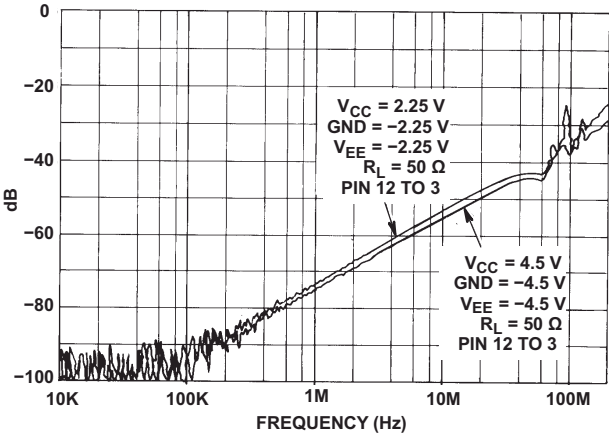


图 5-4. Channel OFF Feedthrough (HC and HCT4051)

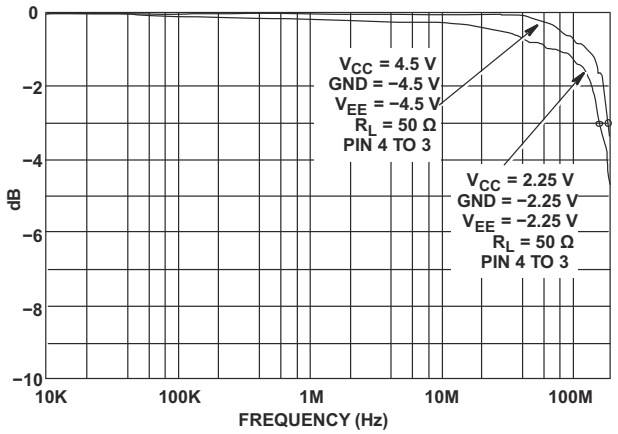


图 5-5. Channel ON Bandwidth (HC and HCT4052)

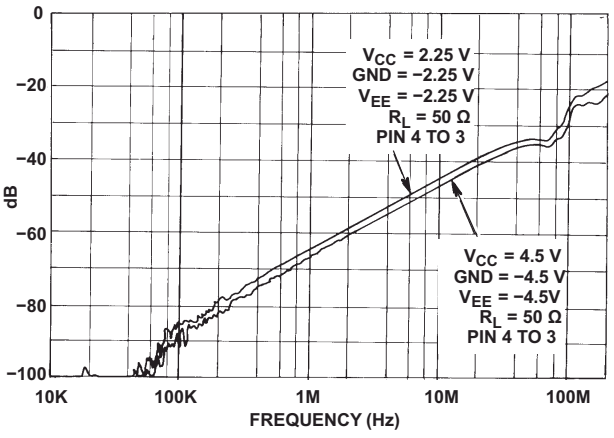


图 5-6. Channel OFF Feedthrough (HC and HCT4052)

5.10 Typical Characteristics (continued)

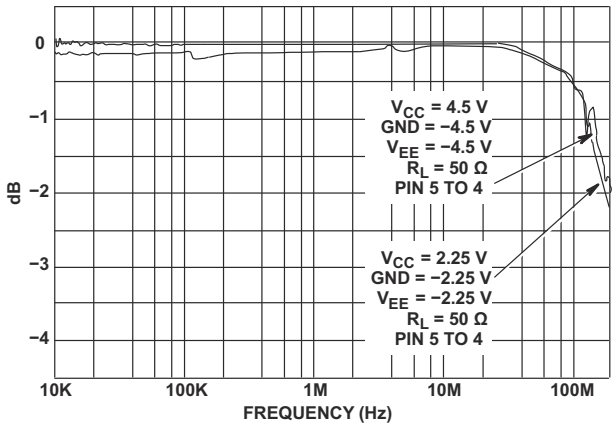


图 5-7. Channel ON Bandwidth (HC and HCT4053)

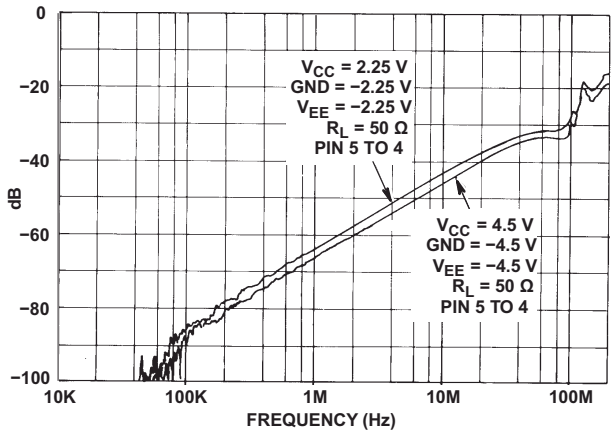
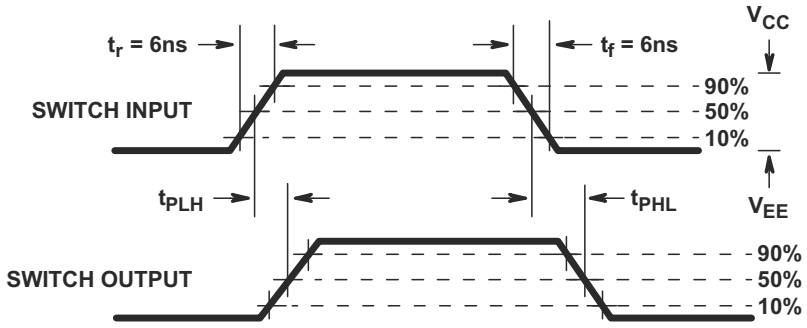
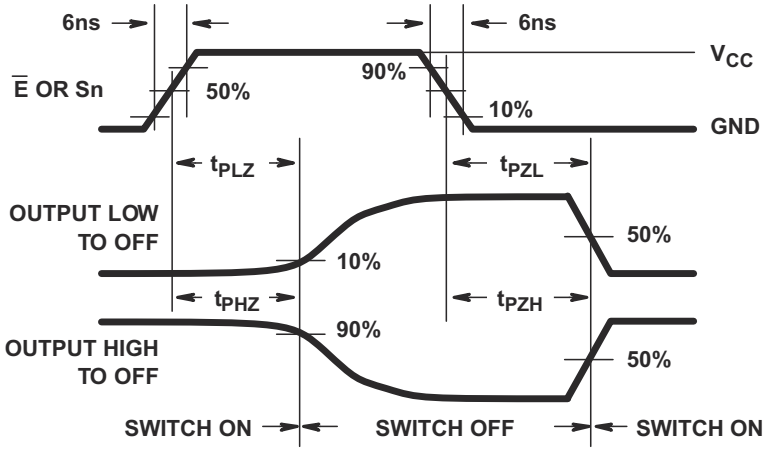


图 5-8. Channel OFF Feedthrough (HC and HCT4053)

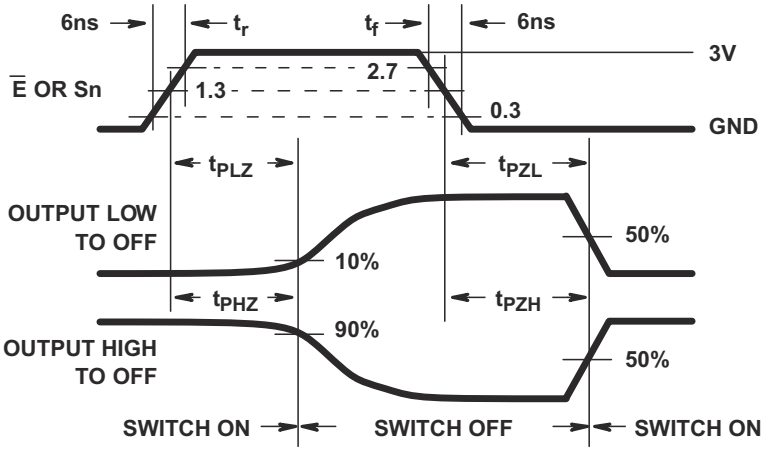
6 Parameter Measurement Information



(FIGURE A)



(FIGURE B) HC TYPES



(FIGURE C) HCT TYPES

图 6-1. Switch Propagation Delay, Turn-On, Turn-Off Times

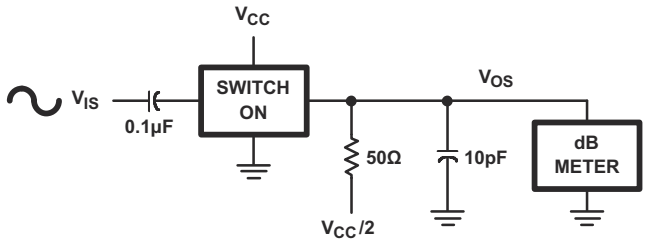
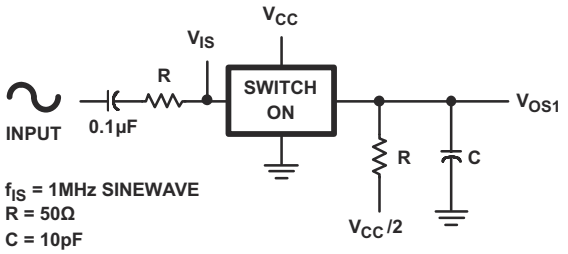


图 6-2. Frequency Response Test Circuit



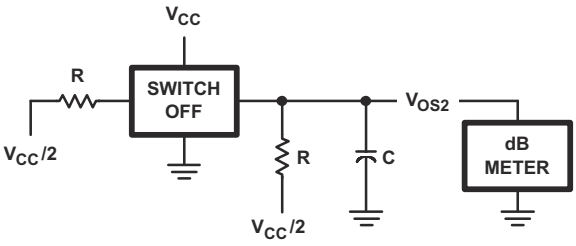


图 6-3. Crosstalk Between Two Switches Test Circuit

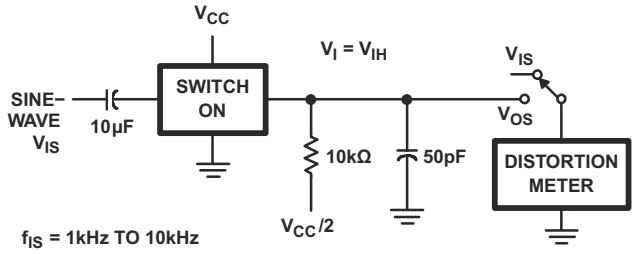


图 6-4. ¼Sine-Wave Distortion Test Circuit

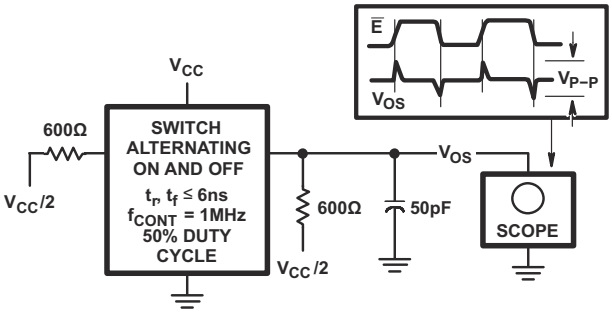


图 6-5. Control to Switch Feedthrough Noise Test Circuit

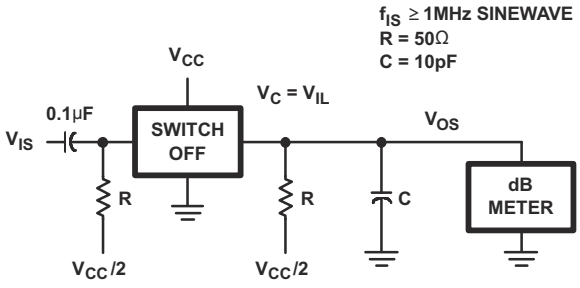


图 6-6. Switch OFF Signal Feedthrough

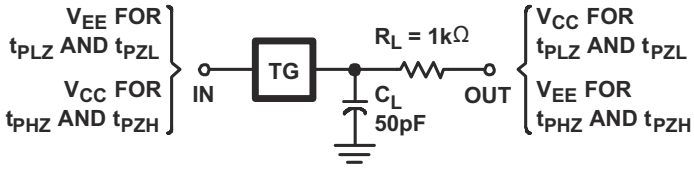


图 6-7. Switch ON/OFF Propagation Delay Test Circuit

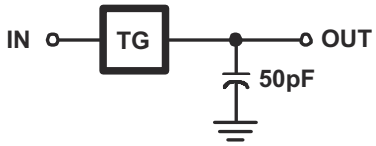


图 6-8. Switch In to Switch Out Propagation Delay Test Circuit

7 Detailed Description

7.1 Overview

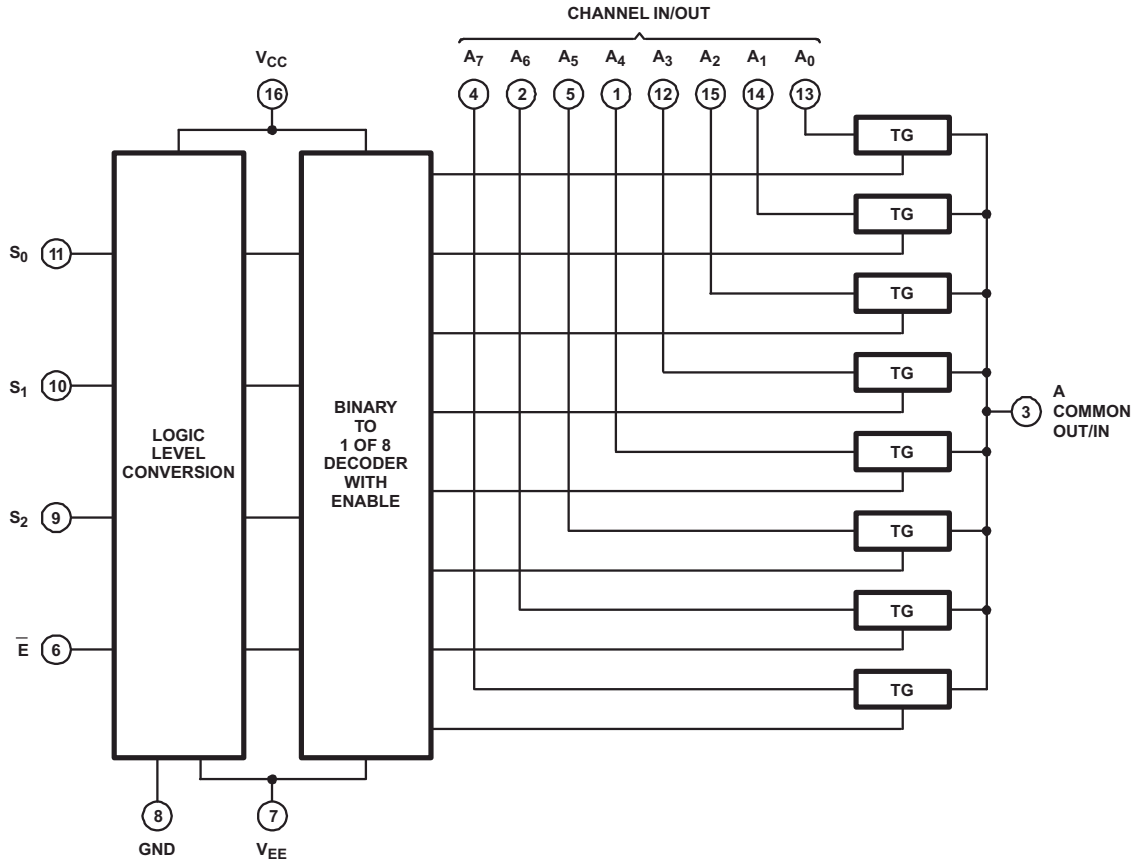
The CDx4HCx4051 devices are a single 8-channel multiplexer having three binary control inputs, S_0, S_1, and S_2 and an $\overline{\text{ENABLE}}$ input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The CDx4HCx4052 devices are a differential 4-channel multiplexer having two binary control inputs, S_0 and S_1, and an $\overline{\text{ENABLE}}$ input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The CDx4HCx4053 devices are a triple 2-channel multiplexer having three separate digital control inputs, S_0, S_1, and S_2 and an $\overline{\text{ENABLE}}$ input. Each control input selects one of a pair of channels that are connected in a single-pole, double-throw configuration.

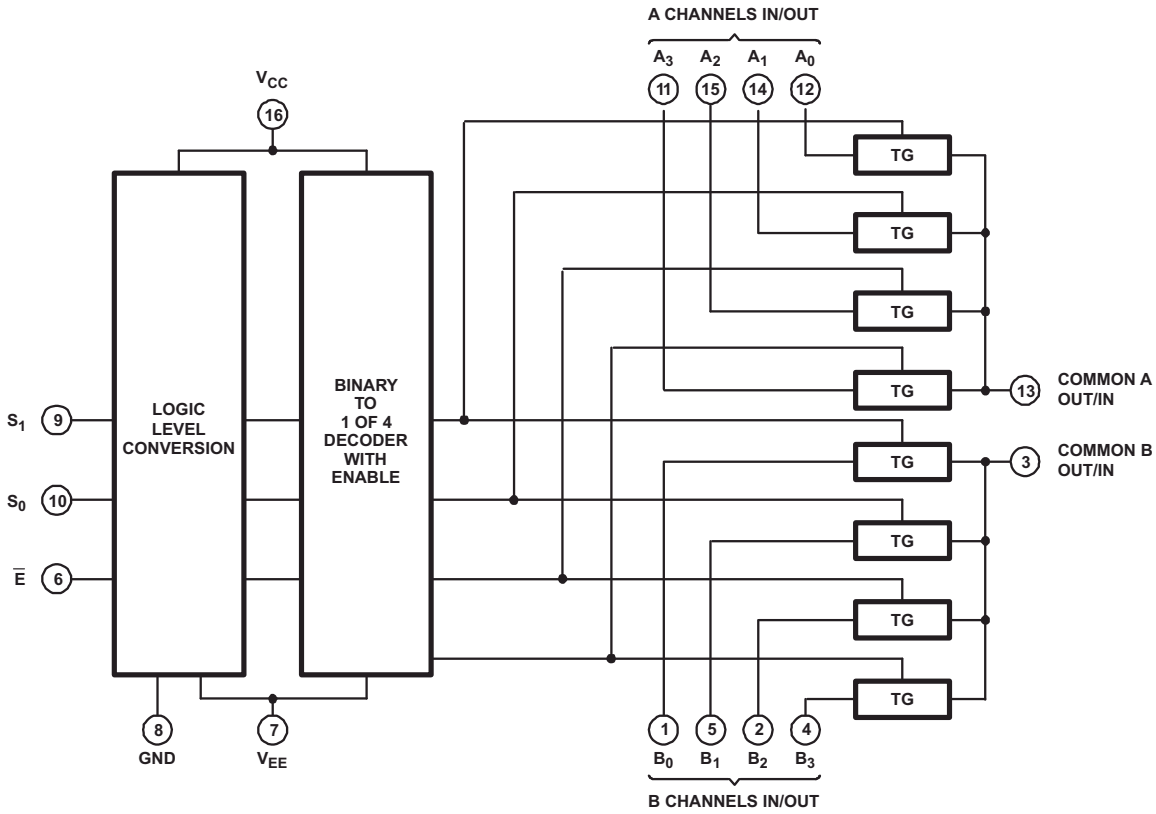
When these devices are used as demultiplexers, the CHANNEL IN/OUT terminals are the outputs and the COMMON OUT/IN terminals are the inputs.

7.2 Functional Block Diagrams



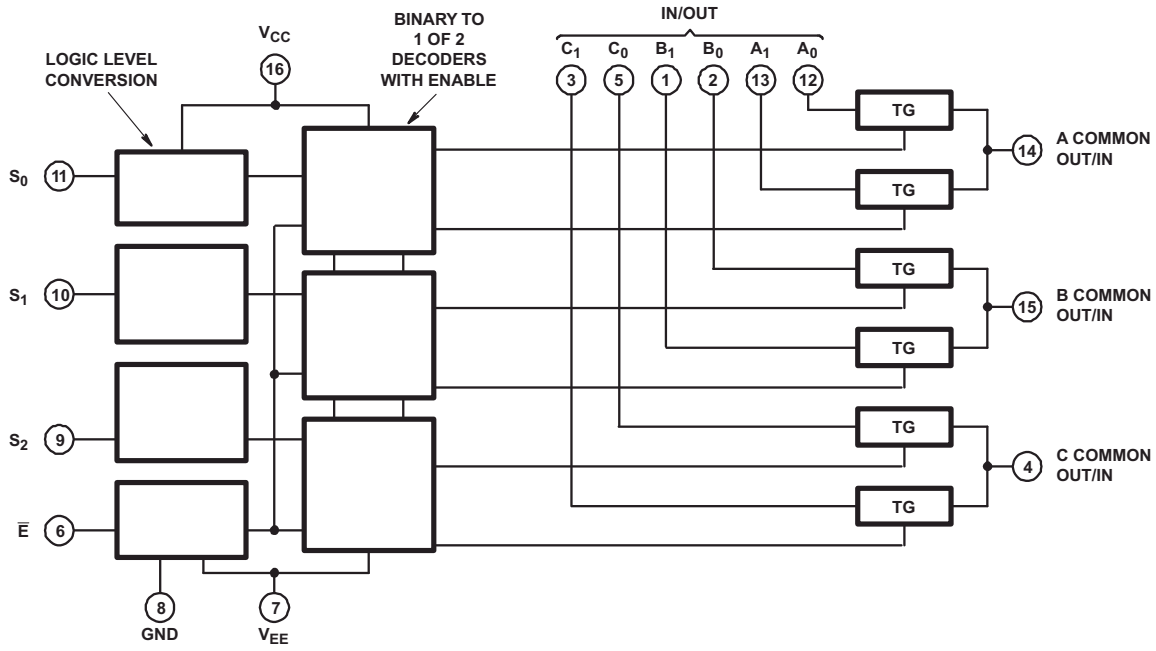
All inputs are protected by standard CMOS protection network.

图 7-1. CDx4HCx4051 Functional Block Diagram



All inputs are protected by standard CMOS protection network.

图 7-2. CDx4HCx4052 Functional Block Diagram



All inputs are protected by standard CMOS protection network.

图 7-3. CDx4HCx4053 Functional Block Diagram

7.3 Feature Description

The CDx4HCx405x line of multiplexers and demultiplexers can accept a wide range of analog signal levels from –5 to +5V. They have low ON resistance, typically 70Ω for V_{CC} – V_{EE} = 4.5V and 40Ω for V_C – V_{EE} = 4.5V, which allows for very little signal loss through the switch.

Binary address decoding on chip makes channel selection easy. When channels are changed, a break-before-make system eliminates channel overlap.

7.4 Device Functional Modes

表 7-1. CD54HC4051, CD74HC4051, CD54HCT4051, CD74HCT4051 Function Table(1)

INPUT STATES				ON CHANNEL
ENABLE	S_2	S_1	S_0	
L	L	L	L	A0
L	L	L	H	A1
L	L	H	L	A2
L	L	H	H	A3
L	H	L	L	A4
L	H	L	H	A5
L	H	H	L	A6
L	H	H	H	A7
H	X	X	X	None

(1) X = Don't care

表 7-2. CD54HC4052, CD74HC4052, CD54HCT4052, CD74HCT4052 Function Table(1)

INPUT STATES			ON CHANNELS
ENABLE	S_1	S_0	
L	L	L	A0, B0
L	L	H	A1, B1
L	H	L	A2, B2
L	H	H	A3, B3
H	X	X	None

(1) X = Don't care

表 7-3. CD54HC4053, CD74HC4053, CD54HCT4053, CD74HCT4053 Function Table(1)

INPUT STATES				ON CHANNELS
ENABLE	S_2	S_1	S_0	
L	L	L	L	C0, B0, A0
L	L	L	H	C0, B0, A1
L	L	H	L	C0, B1, A0
L	L	H	H	C0, B1, A1
L	H	L	L	C1, B0, A0
L	H	L	H	C1, B0, A1
L	H	H	L	C1, B1, A0
L	H	H	H	C1, B1, A1
H	X	X	X	None

(1) X = Don't care

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The CDx4HCx405x line of multiplexers and demultiplexers can be used for a wide variety of applications.

8.2 Typical Application

One application of the CD74HC4051 device is used in conjunction with a microcontroller to poll a keypad. 图 8-1 shows the basic schematic for such a polling system. The microcontroller uses the channel-select pins to cycle through the different channels while reading the input to see if a user is pressing any of the keys. This is a very robust setup that allows for simultaneous key presses with very little power consumption. It also uses very few pins on the microcontroller. The down side of polling is that the microcontroller must frequently scan the keys for a press.

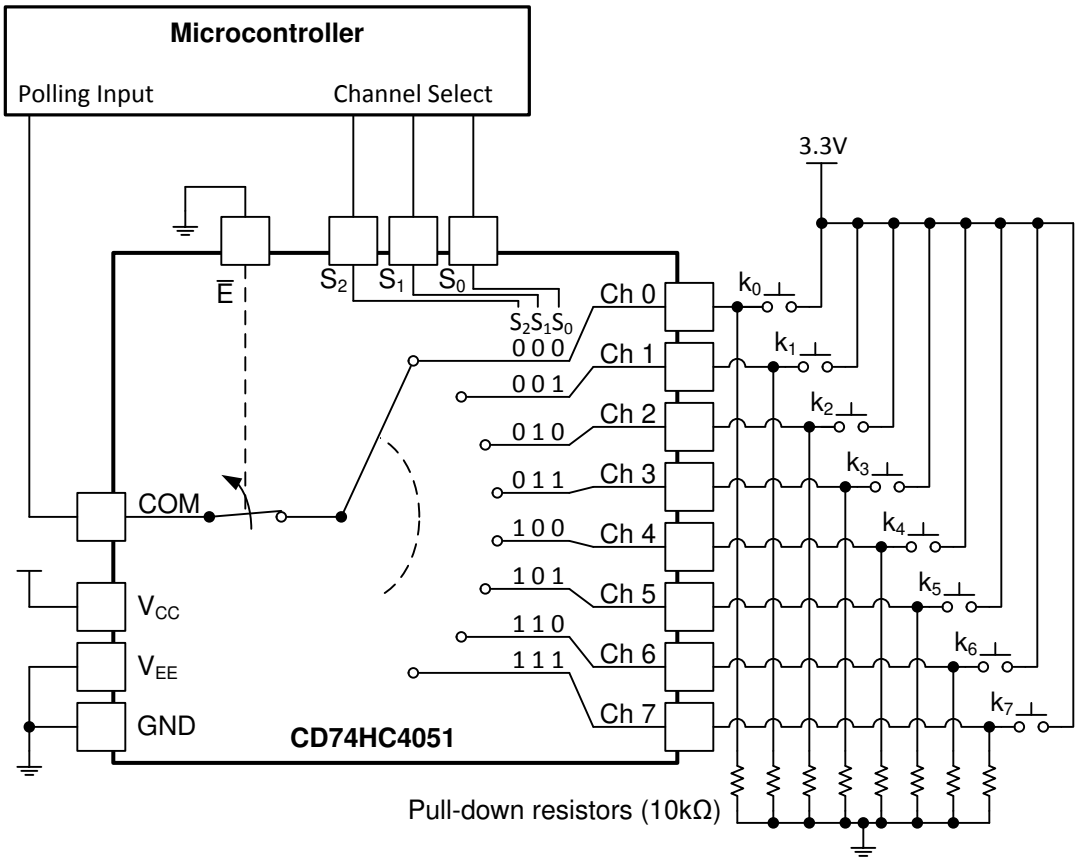


图 8-1. CD74HC4051 Being Used to Help Read Button Presses on a Keypad

8.2.1 Design Requirements

These devices use CMOS technology and have balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions must be considered to prevent ringing.

See 表 8-1 for the input loading details.

表 8-1. HCT Input Loading Table

TYPE	INPUT	UNIT LOADS(1)
4051, 4053	All	0.5
4052	All	0.4

(1) Unit load is ΔI_{CC} limit specified in 节 5, for example, 360mA MAX at 25°C.

8.2.2 Detailed Design Procedure

1. Recommended input conditions:
   - For switch time specifications, see propagation delay times in 节 5.5.
   - Inputs must not be pushed more than 0.5V above V_{DD} or below V_{EE}.
   - For input voltage level specifications for control inputs, see V_{IH} and V_{IL} in 节 5.5.
2. Recommended output conditions:
   - Outputs must not be pulled above V_{DD} or below V_{EE}.
3. Input and output current consideration:
   - The CDx4HCx405x series of parts do not have internal current-drive circuitry, and thus cannot sink or source current. Any current will be passed through the device.

8.2.3 Application Curve

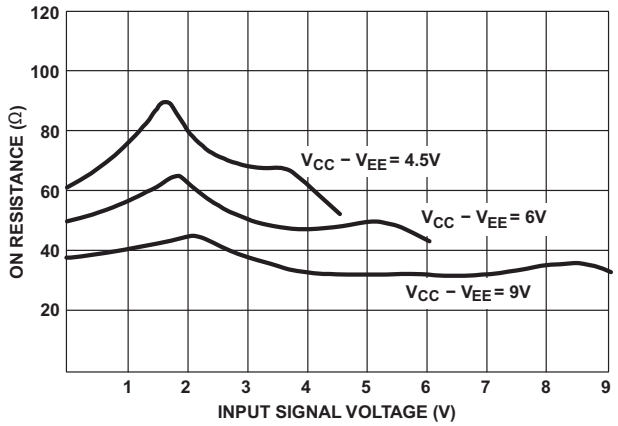


图 8-2. Typical ON Resistance vs Input Signal Voltage

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the 节 5.5.

Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 μF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01 μF or 0.022 μF capacitor is recommended for each V_{CC} because the V_{CC} pins will be tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1μF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 μF and a 1 μF capacitor are commonly used in parallel. For best results, the bypass capacitor or capacitors must be installed as close as possible to the power terminal.

8.4 Layout

8.4.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change in width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This change in width upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace, thus resulting in the reflection. Not all PCB traces can be straight, so they will have to turn corners. 图 8-3 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

8.4.2 Layout Example

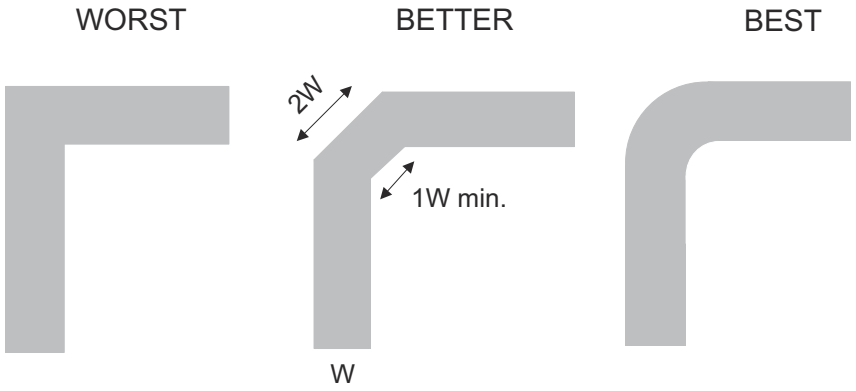


图 8-3. Trace Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs*

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision M (May 2019) to Revision N (April 2024)	Page
• Changed thermal metrics	8
• Changed HC ICC at 25°C single/dual supply	9
• Changed HCT ICC at 25°C single/dual supply	12
• Changed: tPHZ/tPLZ typicals Switch turn-off (S or E)	14
• Changed tPHZ/tPLZ maximum switch turn OFF delay from S or E to switch output for 4051/4052/4053	15
• Changed tPZL/tPZH maximum switch turn ON delay from S or E to switch output for 4051/4053	15

Changes from Revision L (February 2017) to Revision M (May 2019)	Page
• 将*特性* 从 7 Ω（典型值）更改为 70 Ω（典型值）	1

Changes from Revision K (September 2015) to Revision L (February 2017)	Page
• Changed charged device model (CDM) value from: ±1000V to: ±200V	7

- Added *Receiving Notification of Documentation Updates* section.....7

Changes from Revision J (February 2011) to Revision K (September 2015) **Page**

- 向*特性* 列表中添加了“军用免责声明”..... 1
- 删除了*订购信息* 表.....1
- 添加了*器件信息* 表、*引脚功能* 表、*ESD* *等级* 表、*热性能信息* 表、*详细说明* 部分、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分，以及*机械、封装和可订购信息* 部分.....1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8775401EA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8775401EA CD54HC4053F3A
5962-8855601EA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8855601EA CD54HC4052F3A
5962-9065401MEA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9065401MEA CD54HCT4051F3A
CD54HC4051F	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC4051F
CD54HC4051F.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC4051F
CD54HC4051F3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC4051F3A
CD54HC4051F3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC4051F3A
CD54HC4052F	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC4052F
CD54HC4052F.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC4052F
CD54HC4052F3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8855601EA CD54HC4052F3A
CD54HC4052F3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8855601EA CD54HC4052F3A
CD54HC4053F	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC4053F
CD54HC4053F.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC4053F
CD54HC4053F3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8775401EA CD54HC4053F3A
CD54HC4053F3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8775401EA CD54HC4053F3A
CD54HCT4051F3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9065401MEA CD54HCT4051F3A
CD54HCT4051F3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9065401MEA CD54HCT4051F3A
CD74HC4051E	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4051E
CD74HC4051E.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4051E
CD74HC4051EE4	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4051E

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74HC4051M	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HC4051M
CD74HC4051M96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051M
CD74HC4051M96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051M
CD74HC4051M96G3	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HC4051M
CD74HC4051M96G4	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HC4051M
CD74HC4051MT	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HC4051M
CD74HC4051NSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051M
CD74HC4051NSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051M
CD74HC4051NSRE4	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051M
CD74HC4051PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4051
CD74HC4051PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4051
CD74HC4051PWRG4	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-55 to 125	HJ4051
CD74HC4051PWT	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-55 to 125	HJ4051
CD74HC4052E	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4052E
CD74HC4052E.A	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4052E
CD74HC4052M	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HC4052M
CD74HC4052M96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M
CD74HC4052M96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M
CD74HC4052M96G4	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HC4052M
CD74HC4052MT	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HC4052M
CD74HC4052NSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M
CD74HC4052NSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4052M
CD74HC4052PW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-55 to 125	HJ4052
CD74HC4052PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	HJ4052
CD74HC4052PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4052
CD74HC4052PWRG4	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-55 to 125	HJ4052
CD74HC4052PWT	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-55 to 125	HJ4052
CD74HC4053E	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4053E
CD74HC4053E.A	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4053E
CD74HC4053M	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HC4053M
CD74HC4053M96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	HC4053M

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74HC4053M96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4053M
CD74HC4053M96G3	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HC4053M
CD74HC4053M96G4	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HC4053M
CD74HC4053MT	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HC4053M
CD74HC4053NSR	NRND	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4053M
CD74HC4053NSR.A	NRND	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4053M
CD74HC4053PW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-55 to 125	HJ4053
CD74HC4053PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4053
CD74HC4053PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4053
CD74HC4053PWRG4	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-55 to 125	HJ4053
CD74HC4053PWT	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-55 to 125	HJ4053
CD74HCT4051E	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT4051E
CD74HCT4051E.A	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT4051E
CD74HCT4051M	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HCT4051M
CD74HCT4051M96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4051M
CD74HCT4051M96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4051M
CD74HCT4051M96E4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4051M
CD74HCT4051M96G4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4051M
CD74HCT4051MT	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HCT4051M
CD74HCT4052E	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT4052E
CD74HCT4052E.A	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT4052E
CD74HCT4052EE4	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT4052E
CD74HCT4052M	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HCT4052M
CD74HCT4052M96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4052M
CD74HCT4052M96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4052M
CD74HCT4052M96G4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4052M
CD74HCT4052MT	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HCT4052M
CD74HCT4053E	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT4053E
CD74HCT4053E.A	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT4053E
CD74HCT4053M	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HCT4053M
CD74HCT4053M96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4053M

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74HCT4053M96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4053M
CD74HCT4053M96E4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4053M
CD74HCT4053M96G4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4053M
CD74HCT4053MT	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HCT4053M
CD74HCT4053PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HK4053
CD74HCT4053PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HK4053
CD74HCT4053PWT	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-55 to 125	HK4053

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF CD54HC4051, CD54HC4052, CD54HC4053, CD54HCT4051, CD74HC4051, CD74HC4052, CD74HC4053, CD74HCT4051 :

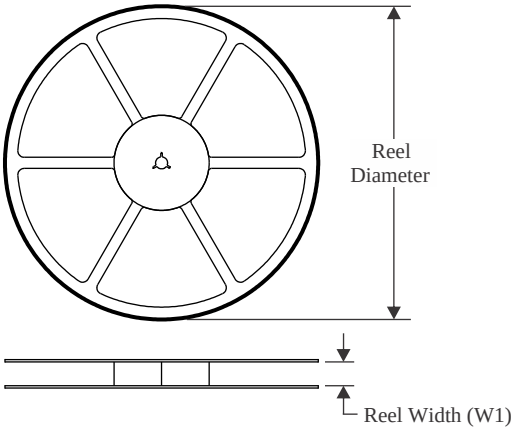
- Catalog : CD74HC4051, CD74HC4052, CD74HC4053, CD74HCT4051
- Automotive : CD74HC4051-Q1, CD74HCT4051-Q1, CD74HC4051-Q1, CD74HCT4051-Q1
- Enhanced Product : CD74HC4051-EP, CD74HC4051-EP
- Military : CD54HC4051, CD54HC4052, CD54HC4053, CD54HCT4051

NOTE: Qualified Version Definitions:

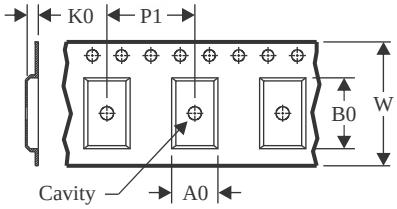
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

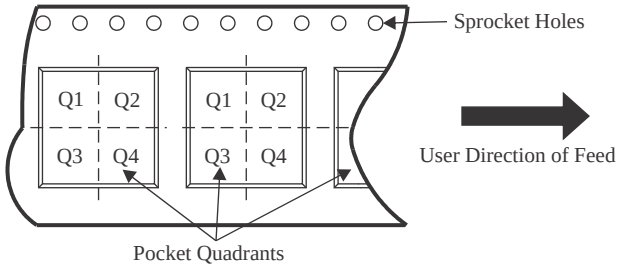


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

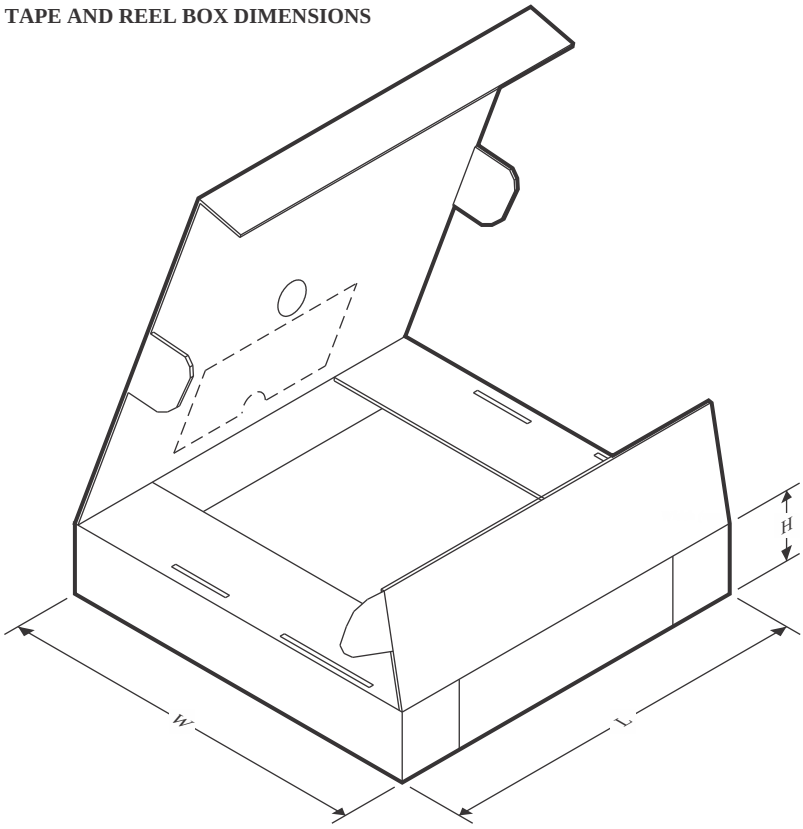


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4051M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4051M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4051NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD74HC4051PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4052M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4052M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4052NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD74HC4052PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4053M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4053M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4053NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD74HC4053PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HCT4051M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT4051M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT4052M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT4052M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HCT4053M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT4053M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT4053PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

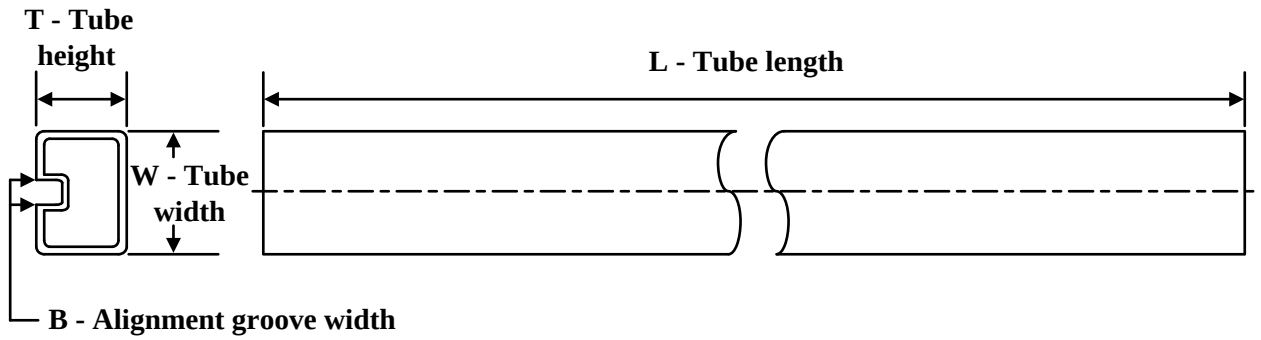


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4051M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HC4051M96	SOIC	D	16	2500	340.5	336.1	32.0
CD74HC4051NSR	SOP	NS	16	2000	353.0	353.0	32.0
CD74HC4051PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
CD74HC4052M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HC4052M96	SOIC	D	16	2500	340.5	336.1	32.0
CD74HC4052NSR	SOP	NS	16	2000	353.0	353.0	32.0
CD74HC4052PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
CD74HC4053M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HC4053M96	SOIC	D	16	2500	340.5	336.1	32.0
CD74HC4053NSR	SOP	NS	16	2000	353.0	353.0	32.0
CD74HC4053PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
CD74HCT4051M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HCT4051M96	SOIC	D	16	2500	340.5	336.1	32.0
CD74HCT4052M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HCT4052M96	SOIC	D	16	2500	340.5	336.1	32.0
CD74HCT4053M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HCT4053M96	SOIC	D	16	2500	340.5	336.1	32.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HCT4053PWR	TSSOP	PW	16	2000	353.0	353.0	32.0

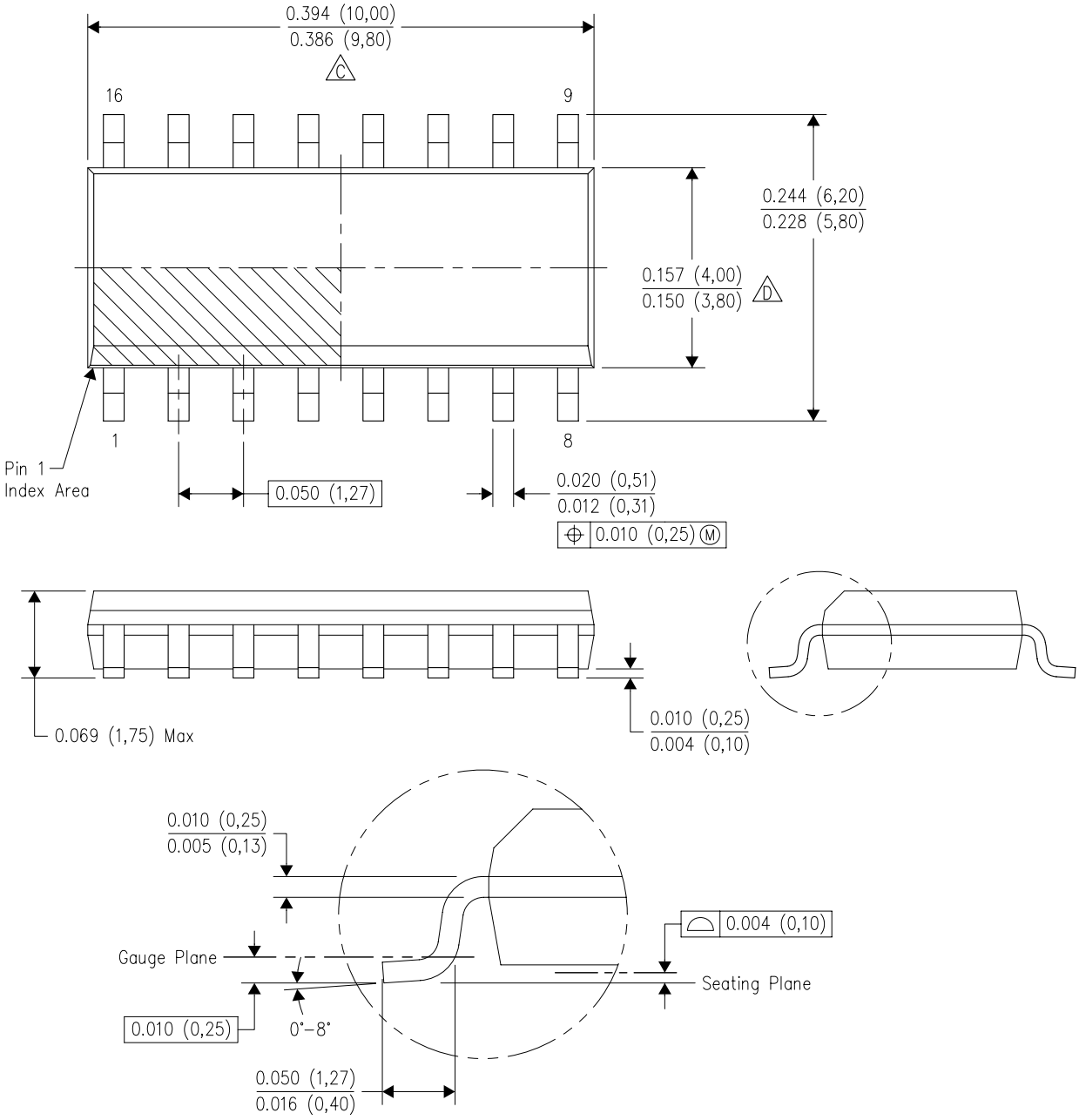
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC4051E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4051E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4051EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4052E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4052E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4052E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4052E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4053E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4053E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4053E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4053E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4051E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4051E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4051E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4051E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4052E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4052E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4052E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4052E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4052EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4052EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4053E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4053E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4053E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4053E.A	N	PDIP	16	25	506	13.97	11230	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

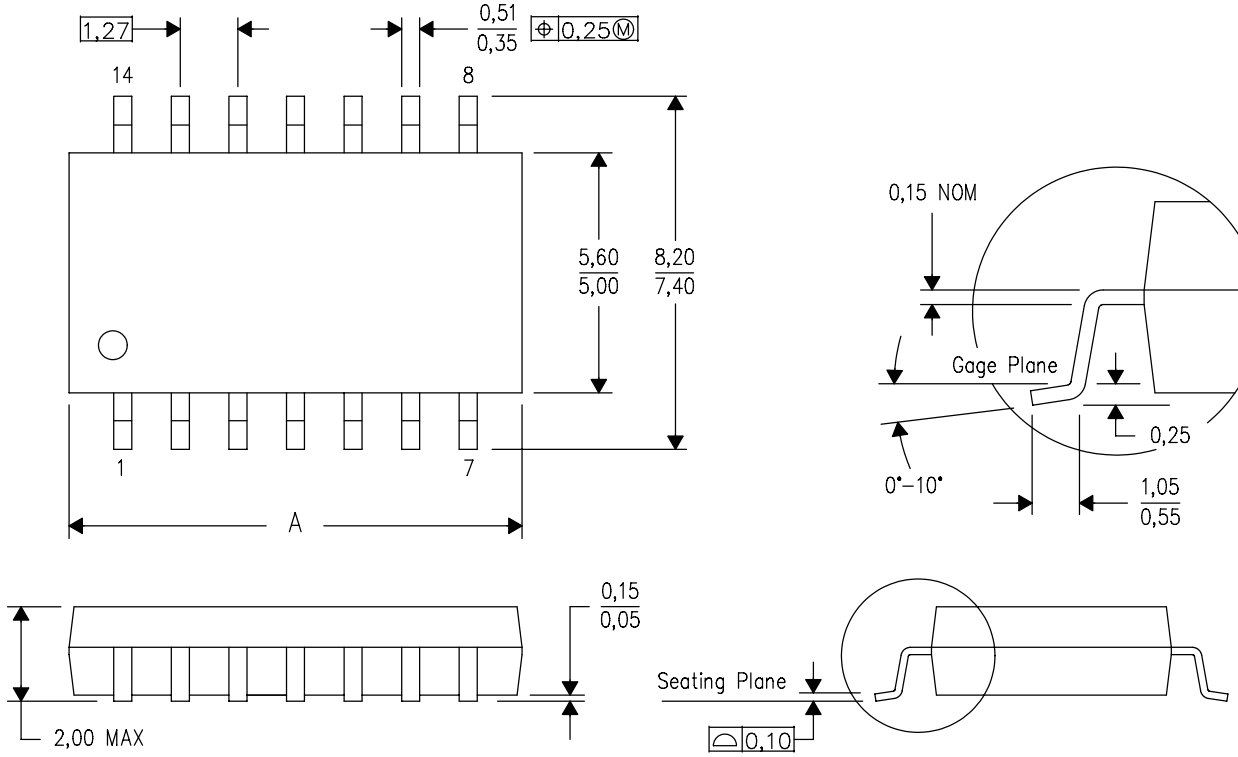


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

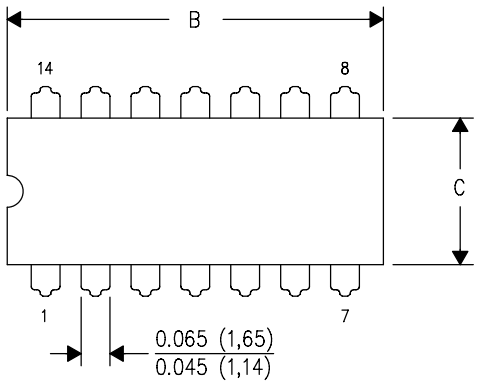
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

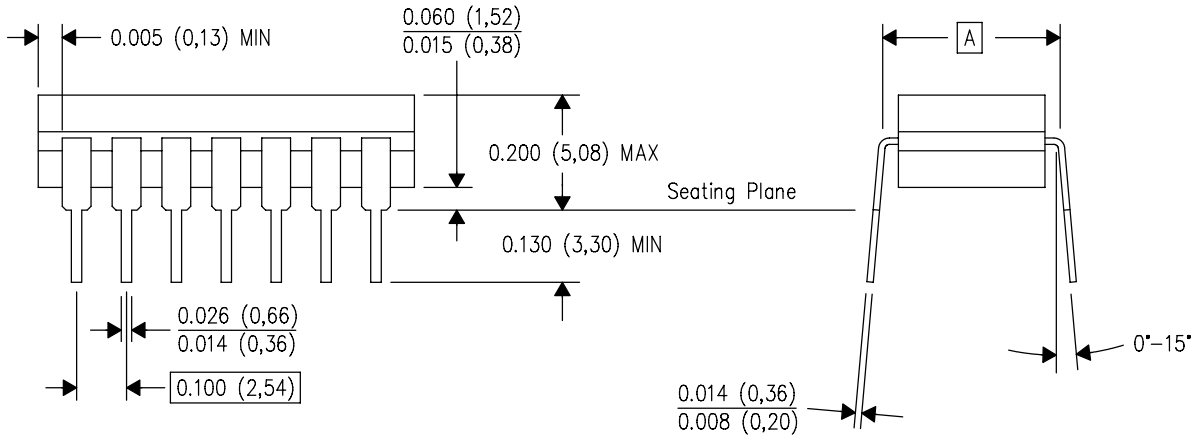
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

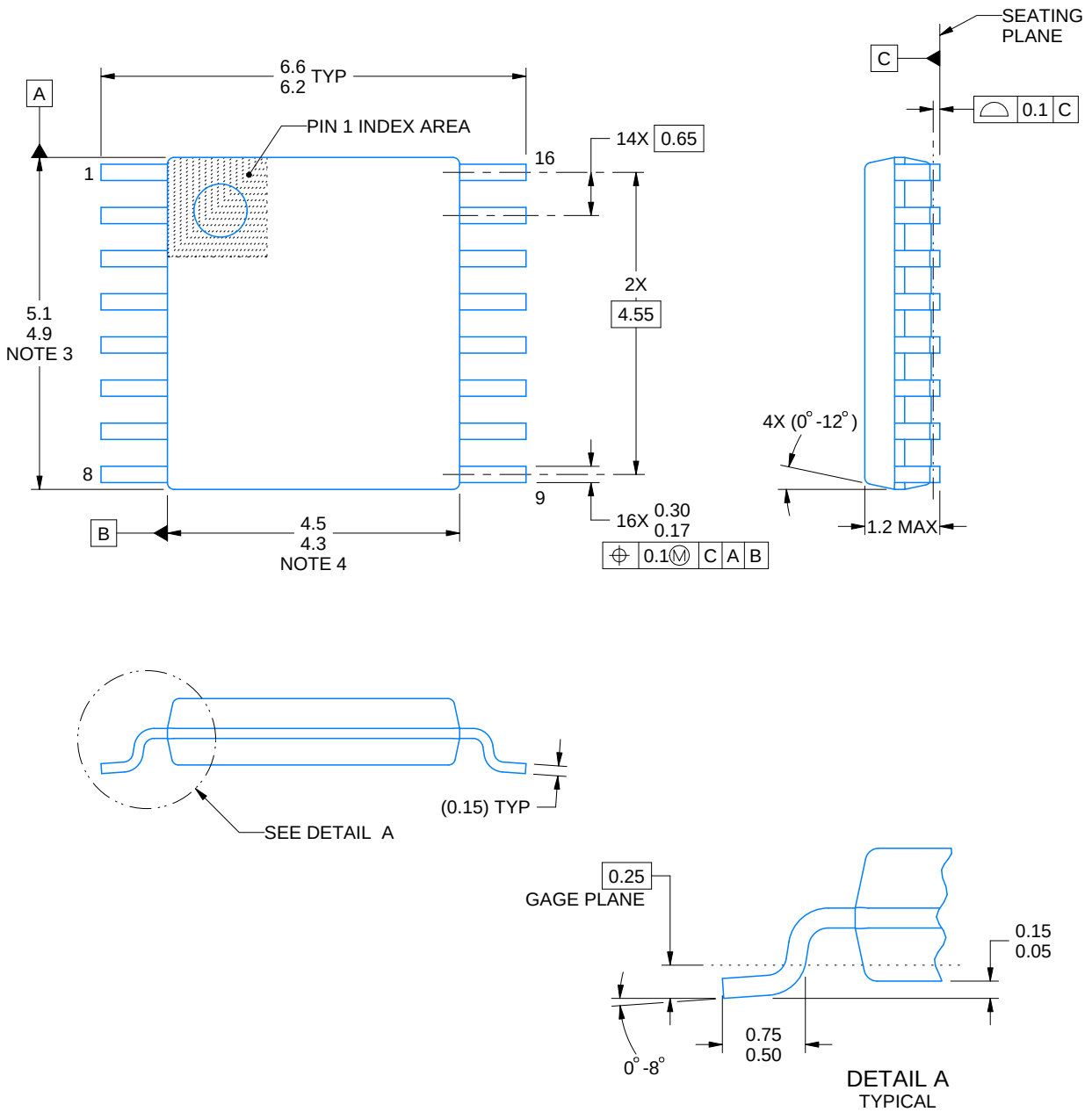
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

PACKAGE OUTLINE

PW0016A

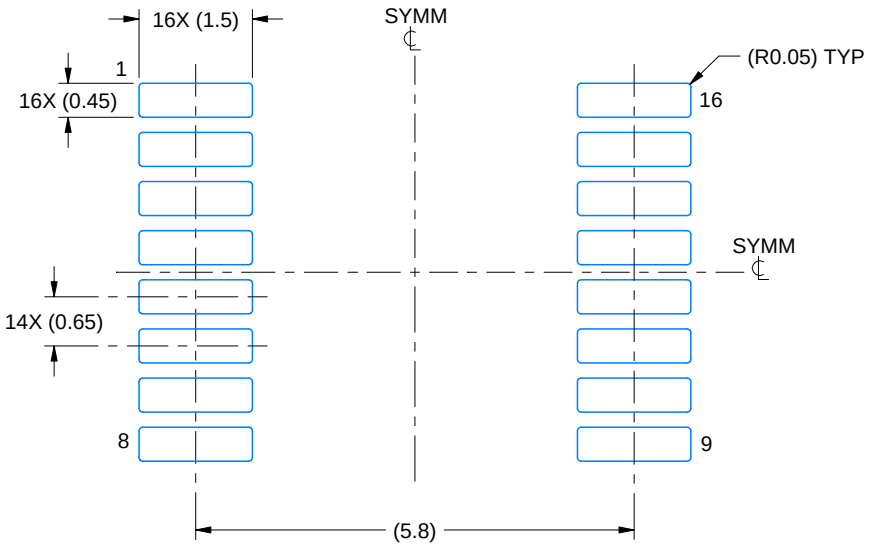
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



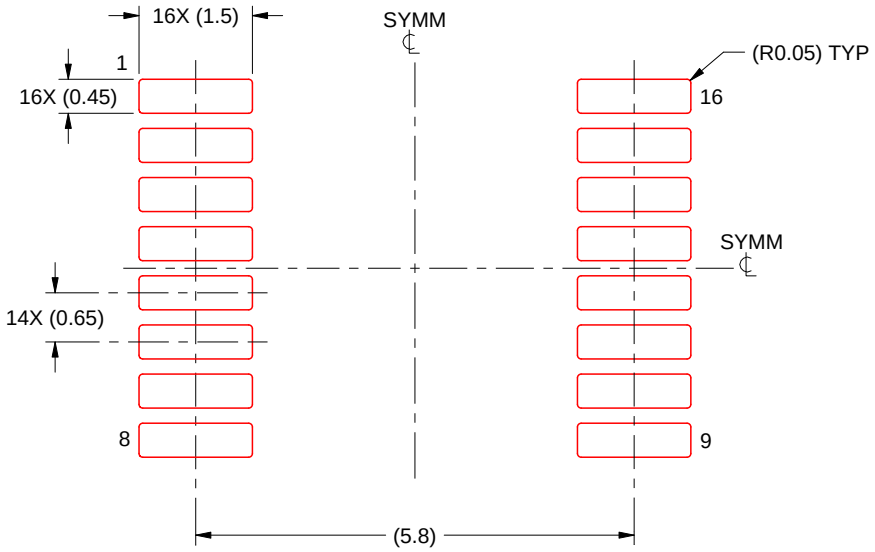
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

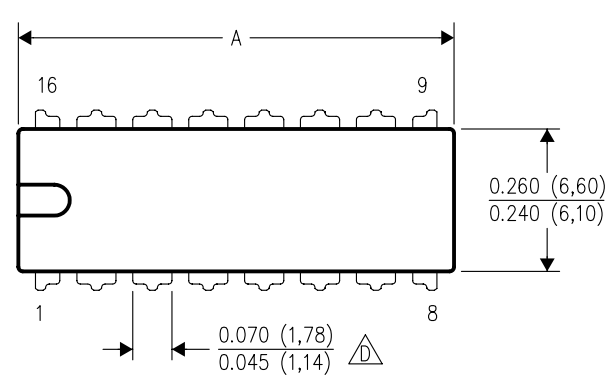
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

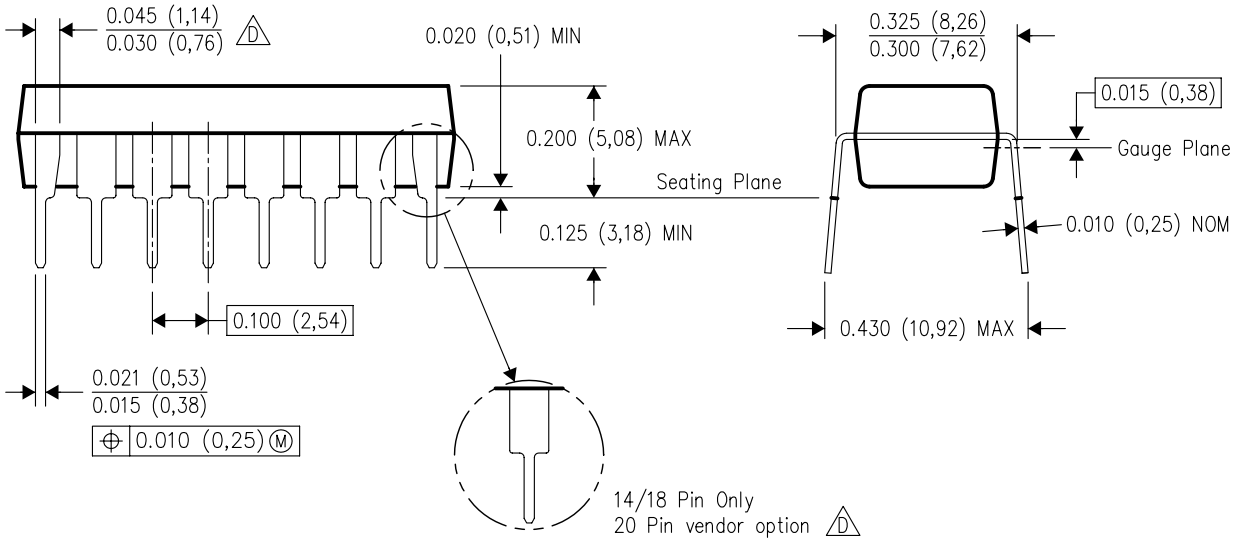
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

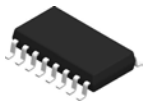


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

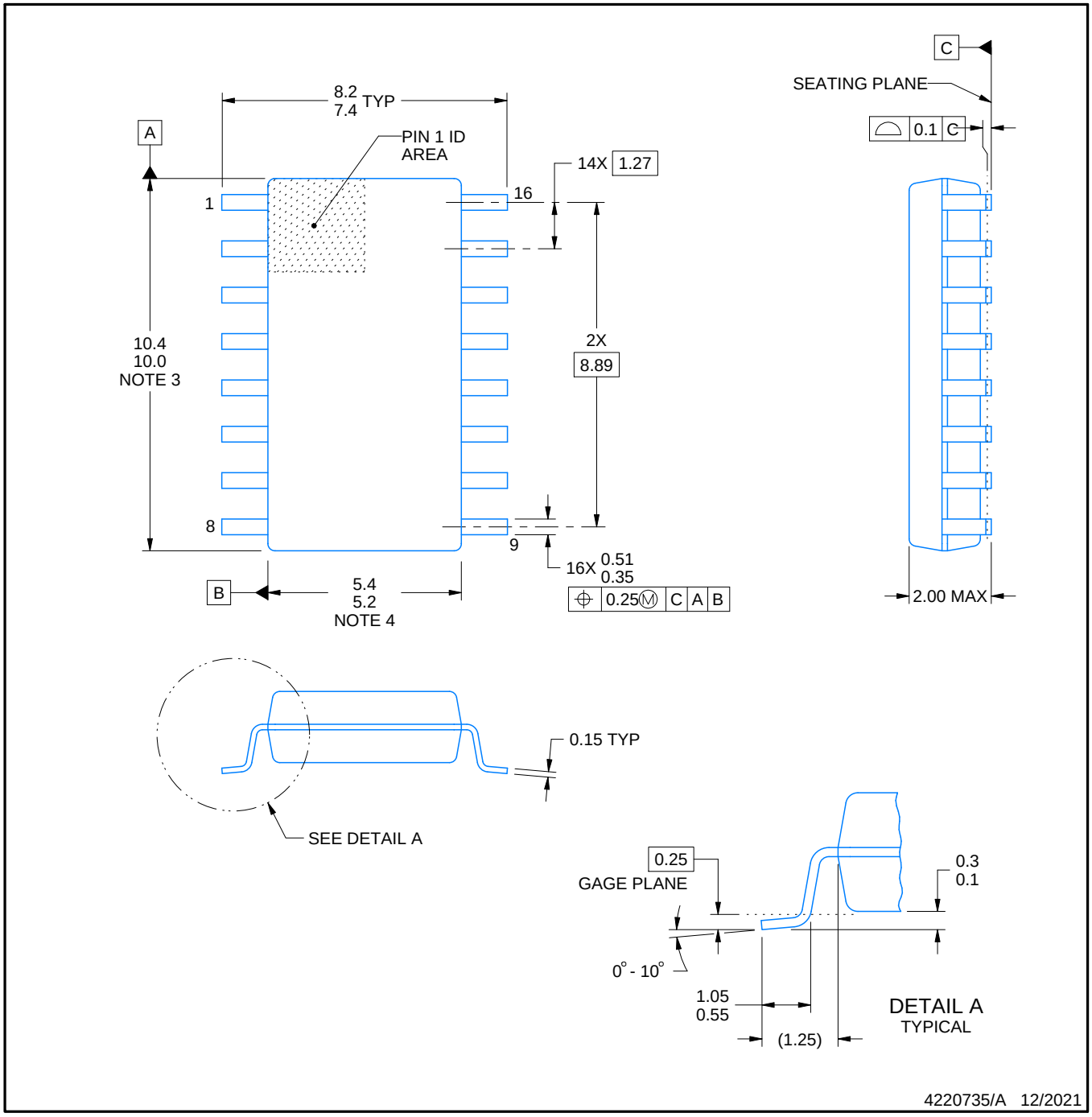


PACKAGE OUTLINE

NS0016A

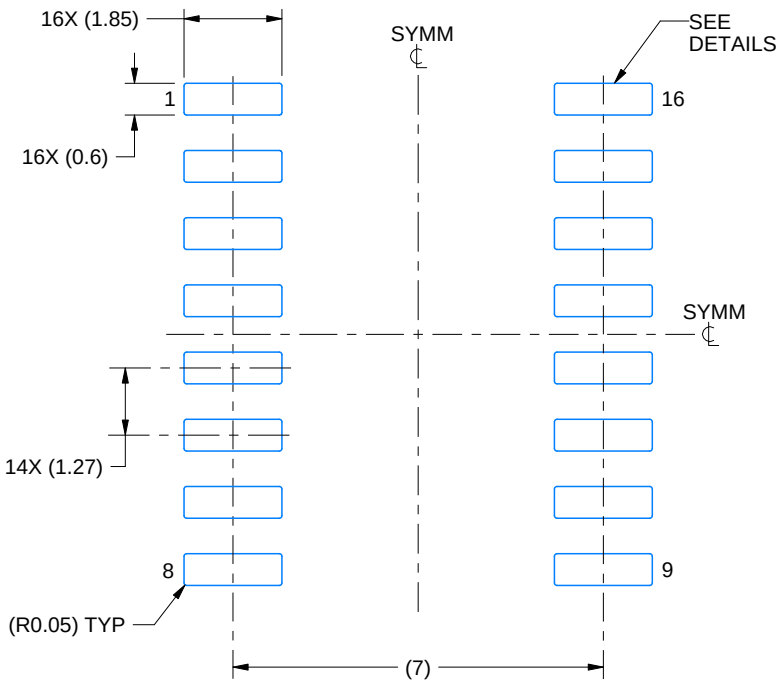
SOP - 2.00 mm max height

SOP

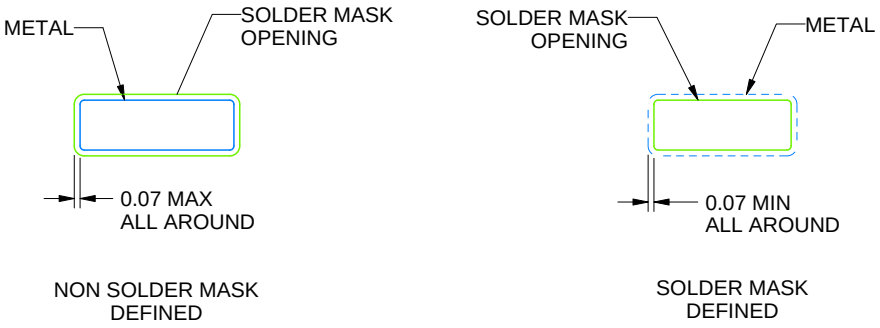


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

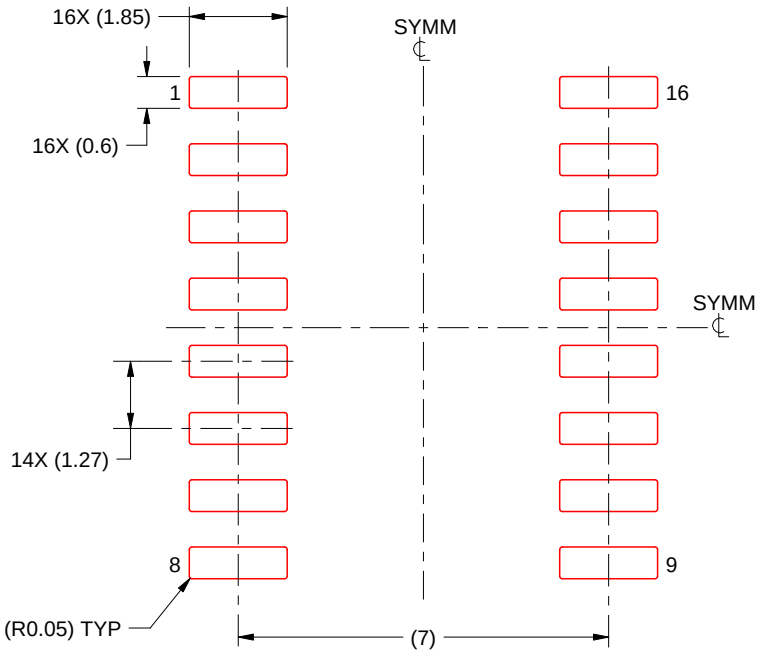
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。 严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265