# CD4051B-Q1 具有逻辑电平转换功能的汽车类 CMOS 单路 8 通道模拟多路复用器或多路信号分离器

## 1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 温度等级 1：–45°C 至 +125°C，$T_A$
- 各种数字和模拟信号电平：
  - 数字：3V 至 20V
  - 模拟：≤ $20V_{P-P}$
- 单电源范围：3V 至 20V（VDD < 3V 时，性能会下降）
- 双电源范围：±3V 至 ±10V
- 在 VDD = 15V 时，输入范围内的低导通电阻为 125Ω（典型值）
- 在 VDD = 15V 时，低通道漏电流为 ±10pA（典型值）
- 低静态功耗：0.2µW（典型值）
- 双向信号路径
- ESD 保护 HBM：3000V，CDM：2000V
- 与业界通用的 4051 引脚兼容

## 2 应用

- 模拟和数字多路复用和多路信号分离
- 模数和数模转换
- 信号门控
- 工厂自动化
- 电视
- 电器
- 消费类音频
- 可编程逻辑电路
- 传感器

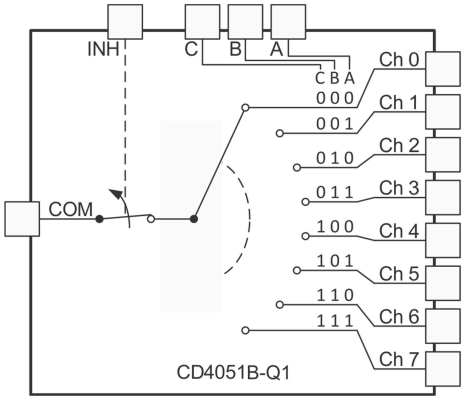
## 3 说明

CD4051B-Q1 模拟多路复用器和多路信号分离器是数字控制的模拟开关，具有低接通阻抗和极低的关断漏电流。这些多路复用器电路在整个 $V_{DD}$ – $V_{SS}$ 和 $V_{DD}$ – $V_{EE}$ 电源电压范围内，消耗的静态功率极低，而不受控制信号的逻辑状态影响。

**封装信息**

| 器件型号 | 封装 (1) | 封装尺寸(2) |
|---|---|---|
| CD4051B-Q1 | D（SOIC，16） | 9.9mm × 6mm |
| | PW（TSSOP，16） | 5mm × 6.4mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。




**CD4051B-Q1 的功能图**

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# 4 Pin Configuration and Functions

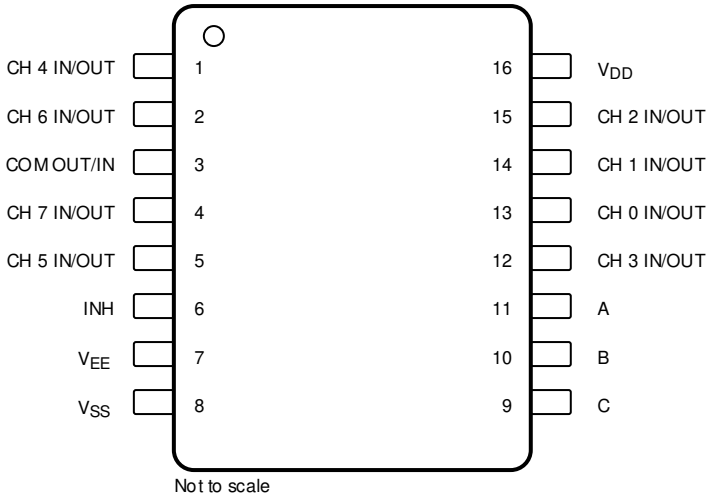



**图 4-1. CD4051B-Q1 D or PW Package, (Top View)**

**表 4-1. Pin Functions CD4051B-Q1**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | CH 4 IN/OUT | I/O | Channel 4 in/out |
| 2 | CH 6 IN/OUT | I/O | Channel 6 in/out |
| 3 | COM OUT/IN | I/O | Common out/in |
| 4 | CH 7 IN/OUT | I/O | Channel 7 in/out |
| 5 | CH 5 IN/OUT | I/O | Channel 5 in/out |
| 6 | INH | I | Disables all channels. See 表 7-1. |
| 7 | $V_{EE}$ | — | Negative power input |
| 8 | $V_{SS}$ | — | Ground |
| 9 | C | I | Channel select C. See 表 7-1. |
| 10 | B | I | Channel select B. See 表 7-1. |
| 11 | A | I | Channel select A. See 表 7-1. |
| 12 | CH 3 IN/OUT | I/O | Channel 3 in/out |
| 13 | CH 0 IN/OUT | I/O | Channel 0 in/out |
| 14 | CH 1 IN/OUT | I/O | Channel 1 in/out |
| 15 | CH 2 IN/OUT | I/O | Channel 2 in/out |
| 16 | $V_{DD}$ | — | Positive power input |

(1) I = input, O = output

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| | Supply Voltage | V+ to V-, Voltages Referenced to $V_{SS}$ Terminal | –0.5 | 20 | V |
| | DC Input Voltage | | –0.5 | $V_{DD}$+0.5 | V |
| | DC Input Current | Any One Input | –10 | 10 | mA |
| $T_{JMAX1}$ | Maximum junction temperature, ceramic package | | | 175 | °C |
| $T_{JMAX2}$ | Maximum junction temperature, plastic package | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±3000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±2000 | |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Temperature Range | –55 | | 125 | °C |

## 5.4 Thermal Information

| THERMAL METRIC(1) | | CD4051B-Q1 | | UNIT |
|---|---|---|---|---|
| | | D (SOIC) | PW (TSSOP) | |
| | | 16 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 86.7 | 116.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 47.3 | 47.2 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 45.3 | 63.0 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 12.1 | 6.4 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 44.9 | 62.1 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 5.5 Electrical Characteristics - CD4051B-Q1

Over operating free-air temperature range, $V_{SUPPLY}$ = ±5 V, and $R_L$ = 100 Ω, (unless otherwise noted)(1)

| PARAMETER | TEST CONDITIONS | | | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| **SIGNAL INPUTS ($V_{IS}$) AND OUTPUTS ($V_{OS}$) - CD4051B-Q1** | | | | | | | | | |
| | **$V_{IS}$ (V)** | **$V_{EE}$ (V)** | **$V_{SS}$ (V)** | **$V_{DD}$ (V)** | **TEMP** | | | | |
| Quiescent Device Current, $I_{DD}$ (Max) | | 0 V | 0 V | 5 V | –55°C | | | 60 | µA |
| | | | | | –40°C | | | 60 | |
| | | | | | 25°C | | 17 | 60 | |
| | | | | | 85°C | | | 150 | |
| | | | | | 125°C | | | 150 | |
| | | 0 V | 0 V | 10 V | –55°C | | | 60 | |
| | | | | | –40°C | | | 60 | |
| | | | | | 25°C | | 18 | 60 | |
| | | | | | 85°C | | | 300 | |
| | | | | | 125°C | | | 300 | |
| | | 0 V | 0 V | 15 V | –55°C | | | 60 | |
| | | | | | –40°C | | | 60 | |
| | | | | | 25°C | | 18 | 60 | |
| | | | | | 85°C | | | 600 | |
| | | | | | 125°C | | | 600 | |
| | | 0 V | 0 V | 20 V | –55°C | | | 100 | |
| | | | | | –40°C | | | 100 | |
| | | | | | 25°C | | 18 | 100 | |
| | | | | | 85°C | | | 3000 | |
| | | | | | 125°C | | | 3000 | |
| Drain to Source ON Resistance $r_{ON}$ (Max)<br>$0 \leqslant V_{IS} \leqslant V_{DD}$ | | 0 V | 0 V | 5 V | –55°C | | | 800 | Ω |
| | | | | | –40°C | | | 850 | |
| | | | | | 25°C | | 470 | 1050 | |
| | | | | | 85°C | | | 1200 | |
| | | | | | 125°C | | | 1300 | |
| | | 0 V | 0 V | 10 V | –55°C | | | 310 | |
| | | | | | –40°C | | | 300 | |
| | | | | | 25°C | | 180 | 400 | |
| | | | | | 85°C | | | 520 | |
| | | | | | 125°C | | | 550 | |
| | | 0 V | 0 | 15 V | –55°C | | | 200 | |
| | | | | | –40°C | | | 210 | |
| | | | | | 25°C | | 125 | 240 | |
| | | | | | 85°C | | | 300 | |
| | | | | | 125°C | | | 300 | |

## 5.5 Electrical Characteristics - CD4051B-Q1（续）

Over operating free-air temperature range, $V_{SUPPLY}$ = ±5 V, and $R_L$ = 100 Ω, (unless otherwise noted)(1)

| PARAMETER | | | TEST CONDITIONS | | | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Change in ON Resistance (Between Any Two Channels), $\Delta R_{ON}$ | | | | 0 V | 0 V | 5 V | 25°C | | 15 | | Ω |
| | | | | 0 V | 0 V | 10 V | | | 10 | | |
| | | | | 0 V | 0 V | 15 V | | | 5 | | |
| OFF Channel Leakage Current: Any Channel OFF (Max) or ALL Channels OFF (COMMON OUT/IN) (Max) | | | | 0 V | 0 V | 18 V | –55°C | | | ±100 | nA |
| | | | | | | | –40°C | | | | |
| | | | | | | | 25°C | | ±0.01 | ±100(2) | |
| | | | | | | | 85°C | | | ±1000(2) | |
| | | | | | | | 125°C | | | | |
| ON Channel Leakage Current: Any Channel ON (Max) or ALL Channels ON (COMMON OUT/IN) (Max) | | | 5 or 0 | –5 V | 0 V | 10.5 V | 85°C | | | ±300 | nA |
| | | | 5 | 0 V | 0 V | 18 V | 85°C | | | ±300 | |
| Capacitance | Input, $C_{IS}$ | | | 0 V | 0 V | 10 V | 25°C | | 5 | | pF |
| | Output, $C_{OS}$ | CD4051-Q1 | | | | | | | 30 | | |
| | Feed through, $C_{IOS}$ | | | | | | | | 0.2 | | |
| Prop Delay | | | $V_{DD}$ | $R_L$ = 200 kΩ | | 5 V | 25°C | | 30 | 60 | ns |
| | | | | $C_L$ = 50 pF | | 10 V | | | 15 | 30 | |
| | | | | $t_r$, $t_f$ = 20 ns | | 15 V | | | 10 | 20 | |

## 5.5 Electrical Characteristics - CD4051B-Q1 （续）

Over operating free-air temperature range, $V_{SUPPLY}$ = ±5 V, and $R_L$ = 100 Ω, (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | | | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| **CONTROL (ADDRESS OR INHIBIT), $V_C$ - CD4051B-Q1** | | | | | | | | | | |
| Input Low Voltage, $V_{IL}$, (Max) | | | | | 5 V | –55°C | | | 0.8 | V |
| | | | | | | –40°C | | | 0.8 | |
| | | | | | | 25°C | | | 0.8 | |
| | | | | | | 85°C | | | 0.8 | |
| | | | | | | 125°C | | | 0.8 | |
| | | | | | 10 V | –55°C | | | 0.8 | |
| | | | | | | –40°C | | | 0.8 | |
| | | | | | | 25°C | | | 0.8 | |
| | | | | | | 85°C | | | 0.8 | |
| | | | | | | 125°C | | | 0.8 | |
| | | | | | 15 V | –55°C | | | 0.8 | |
| | | | | | | –40°C | | | 0.8 | |
| | | | | | | 25°C | | | 0.8 | |
| | | | | | | 85°C | | | 0.8 | |
| | | | | | | 125°C | | | 0.8 | |
| Input High Voltage, $V_{IH}$, (Min) | | | | | 5 V | –55°C | | | 3.5 | V |
| | | | | | | –40°C | | | 3.5 | |
| | | | | | | 25°C | 3.5 | | | |
| | | | | | | 85°C | | | 3.5 | |
| | | | | | | 125°C | | | 3.5 | |
| | | | | | 10 V | –55°C | | | 7 | |
| | | | | | | –40°C | | | 7 | |
| | | | | | | 25°C | 7 | | | |
| | | | | | | 85°C | | | 7 | |
| | | | | | | 125°C | | | 7 | |
| | | | | | 15 V | –55°C | | | 11 | |
| | | | | | | –40°C | | | 11 | |
| | | | | | | 25°C | 11 | | | |
| | | | | | | 85°C | | | 11 | |
| | | | | | | 125°C | | | 11 | |
| Input current, $I_{IN}$ (Max) | | $V_{IN}$ = 0, 18 | | | 18 V | –55°C | | | ±1 | µA |
| | | | | | | –40°C | | | ±1 | |
| | | | | | | 25°C | | ±0.6 | ±1 | |
| | | | | | | 85°C | | | ±1 | |
| | | | | | | 125°C | | | ±1 | |
| Propagation Delay Time | Address-to-Signal OUT (Channels ON or OFF) (See Figure 10, Figure 11, and Figure 15) | $t_r$ , $t_f$ = 20ns, $C_L$ = 50 pF, $R_L$ = 10 kΩ | 0 V | 0 V | 5 V | | | 450 | 720 | ns |
| | | | 0 V | 0 V | 10 V | | | 160 | 320 | |
| | | | 0 V | 0 V | 15 V | | | 120 | 240 | |
| | | | –5 V | 0 V | 5 V | | | 225 | 450 | |

## 5.5 Electrical Characteristics - CD4051B-Q1（续）

Over operating free-air temperature range, $V_{SUPPLY}$ = ±5 V, and $R_L$ = 100 Ω, (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | | | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| Propagation Delay Time | Inhibit-to-Signal OUT (Channel Turning ON) (See Figure 11) | $t_r$ , $t_f$ = 20 ns, $C_L$ = 50 pF, $R_L$ = 1 kΩ | 0 V | 0 V | 5 V | | | 400 | 720 | ns |
| | | | 0 V | 0 V | 10 V | | | 160 | 320 | |
| | | | 0 V | 0 V | 15 V | | | 120 | 240 | |
| | | | – 10 V | 0 V | 5 V | | | 200 | 400 | |
| Propagation Delay Time | Inhibit-to-Signal OUT (Channel Turning OFF) (See Figure 17) | $t_r$ , $t_f$ = 20 ns, $C_L$ = 50 pF, $R_L$ = 10 kΩ | 0 V | 0 V | 5 V | | | 200 | 450 | ns |
| | | | 0 V | 0 V | 10 V | | | 90 | 210 | |
| | | | 0 V | 0 V | 15 V | | | 70 | 160 | |
| | | | – 10 V | 0 V | 5 V | | | 130 | 300 | |
| Input Capacitance, $C_{IN}$ (Any Address or Inhibit Input) | | | – 5 V | 0 V | 5 V | 25°C | | 5 | 7.5 | pF |

(1) Peak-to-Peak voltage symmetrical about ($V_{DD}$ – $V_{EE}$) / 2.
(2) Determined by minimum feasible leakage measurement for automatic testing.

## 5.6 AC Performance Characteristics - CD4051B-Q1

$V_{DD}$ = +15 V, $V_{SS}$ = $V_{EE}$ = 0 V,
$T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | | | | TYP | UNIT |
|---|---|---|---|---|---|---|---|
| | **$V_{IS}$ (V)** | **$V_{DD}$ (V)** | **$R_L$ (kΩ)** | | | | |
| Cutoff (–3dB) Frequency Channel ON (Sine Wave Input) | 5(1) | 10 | 1 | $V_{OS}$ at Common OUT/IN | CD4051-Q1 | 20 | MHz |
| | $V_{EE}$ = $V_{SS}$ , 20Log($V_{OS}$/$V_{IS}$) = –3 dB | | | $V_{OS}$ at Any Channel | | 60 | MHz |
| Total Harmonic Distortion, THD | 2(1) | 5 | 10 | | | 0.3% | % |
| | 3(1) | 10 | 10 | | | 0.2% | % |
| | 5(1) | 15 | 10 | | | 0.12% | % |
| | $V_{EE}$ = $V_{SS}$, $f_{IS}$ = 1 kHz Sine Wave | | | | | | |
| –40dB Feedthrough Frequency (All Channels OFF) | 5(1) | 10 | 1 | $V_{OS}$ at Common OUT/IN | CD4051-Q1 | 12 | MHz |
| | $V_{EE}$ = $V_{SS}$ , 20Log($V_{OS}$/$V_{IS}$) = –40 dB | | | $V_{OS}$ at Any Channel | | 8 | MHz |
| –40dB Signal Crosstalk Frequency | 5(1) | 10 | 1 | | | 3 | MHz |
| Address-or-Inhibit-to-Signal Crosstalk | | 10 | 10(2) | | | 65 | $mV_{PEAK}$ |
| | $V_{EE}$ = 0, $V_{SS}$ = 0, $t_r$ , $t_f$ = 20 ns, mVPEAK $V_{CC}$ = $V_{DD}$ – $V_{SS}$ (Square Wave) | | | | | 65 | $mV_{PEAK}$ |

(1) Peak-to-Peak voltage symmetrical about ($V_{DD}$ - $V_{EE}$) / 2.
(2) Both ends of channel.

## 5.7 Typical Characteristics

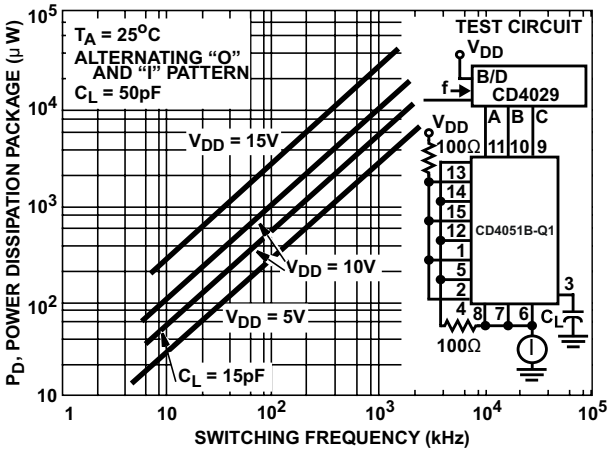



**图 5-1. Dynamic Power Dissipation vs Switching Frequency (CD4051B-Q1)**

# 6 Parameter Measurement Information

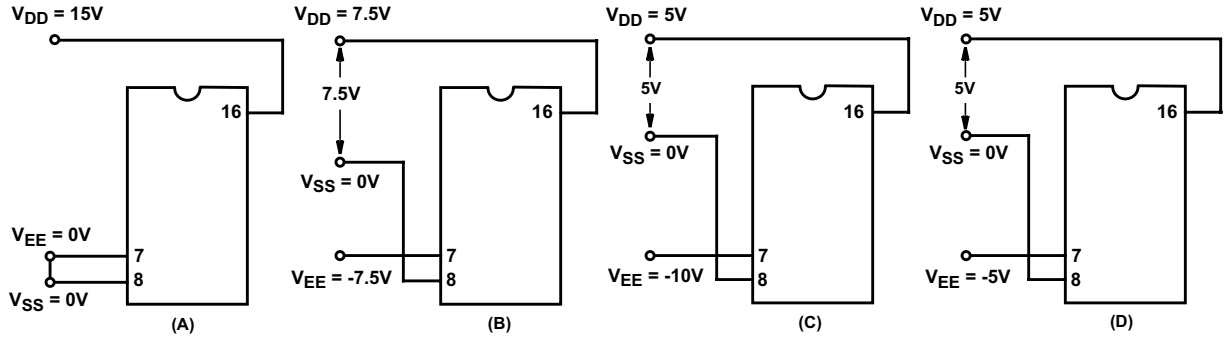



图 6-1. Typical Bias Voltages

备注

The ADDRESS (digital-control inputs) and INHIBIT logic levels are: 0 = $V_{SS}$ and 1 = $V_{DD}$. The analog signal (through the TG) may swing from $V_{EE}$ to $V_{DD}$.

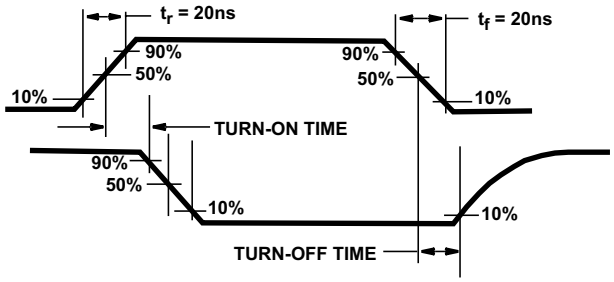



图 6-2. Waveforms, Channel Being Turned ON ($R_L$ = 1 kΩ)

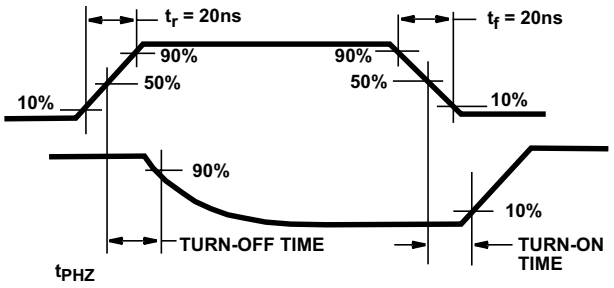



图 6-3. Waveforms, Channel Being Turned OFF ($R_L$ = 1 kΩ)

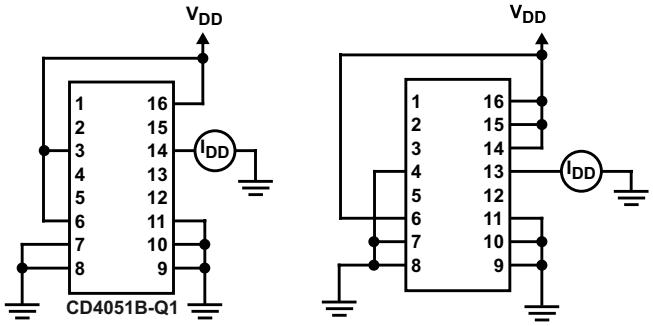



图 6-4. OFF Channel Leakage Current – Any Channel OFF

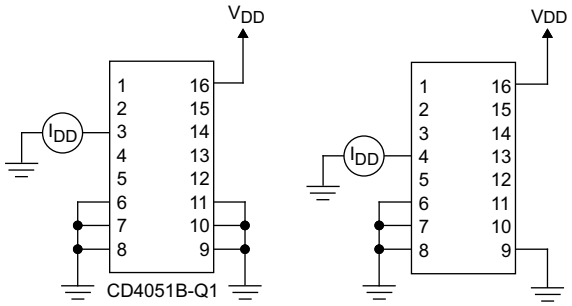



图 6-5. On Channel Leakage Current – Any Channel On

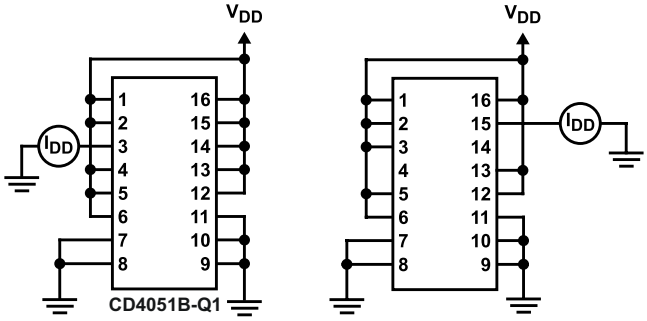



图 6-6. OFF Channel Leakage Current – All Channels OFF

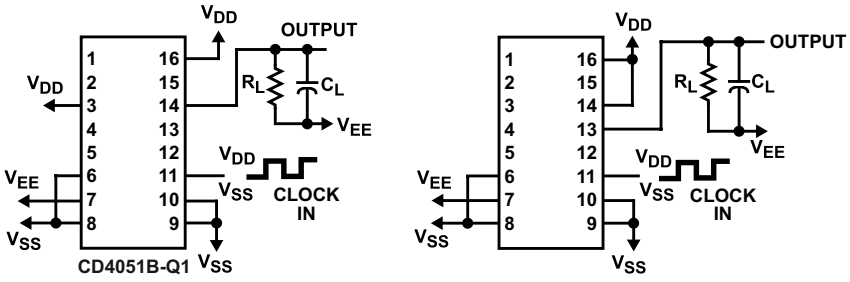



图 6-7. Propagation Delay – Address Input to Signal Output

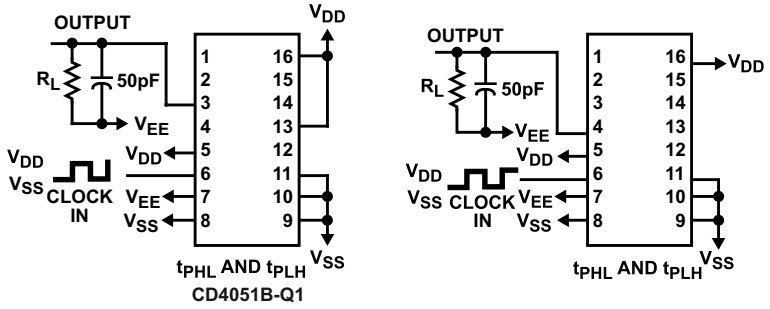



图 6-8. Propagation Delay – Inhibit Input to Signal Output

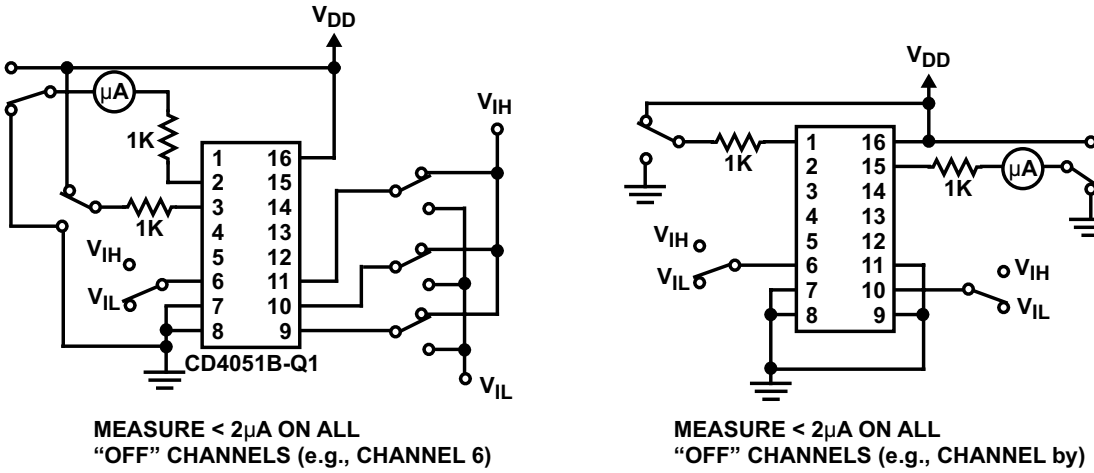



图 6-9. Input Voltage Test Circuits (Noise Immunity)

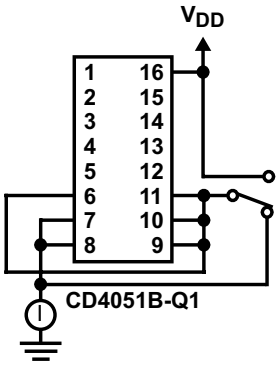



图 6-10. Quiescent Device Current

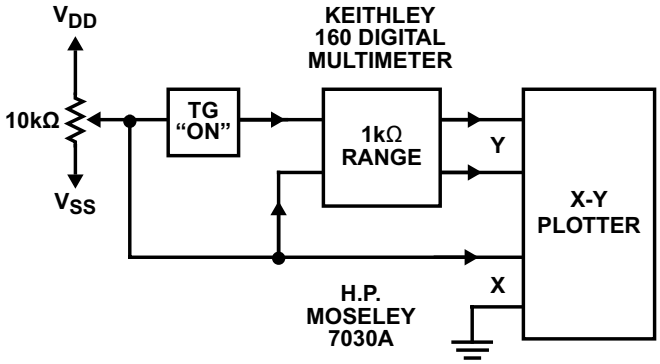



图 6-11. Channel ON Resistance Measurement Circuit

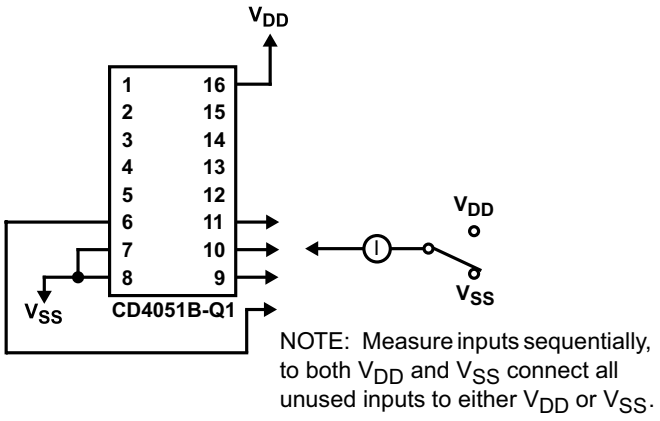



图 6-12. Input Current

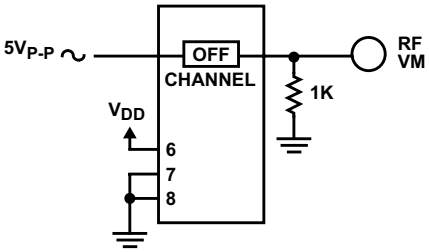



图 6-13. Feed-Through (All Types)

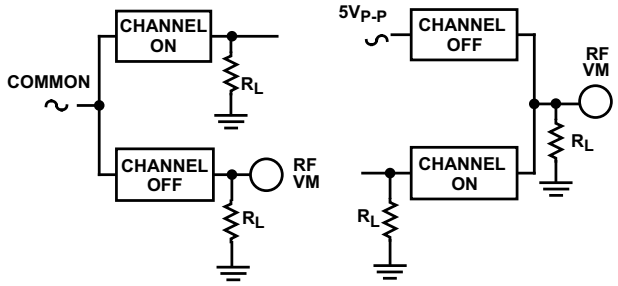



图 6-14. Crosstalk Between Any Two Channels (All Types)


图 6-15. Crosstalk Between Duals or Triplets ()

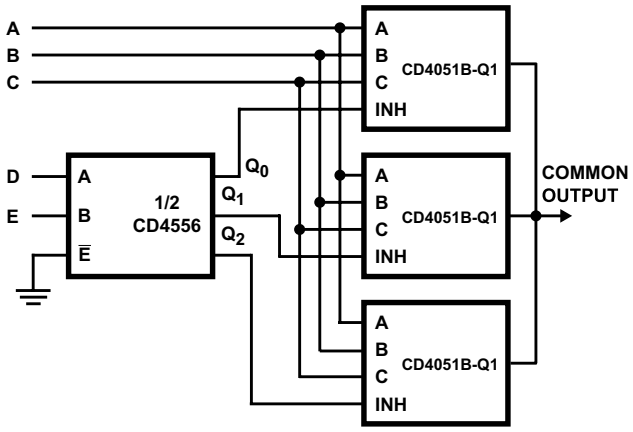



图 6-16. 24-to-1 MUX Addressing

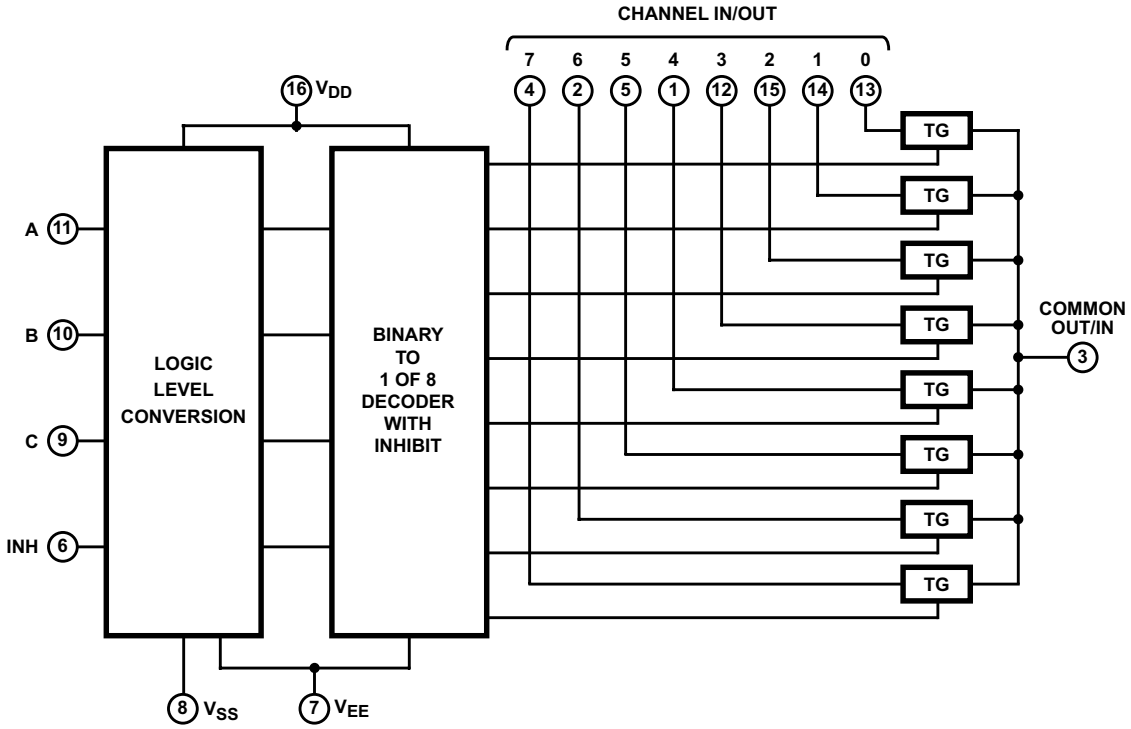
# 7 Detailed Description

## 7.1 Overview

The CD4051B-Q1 device is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

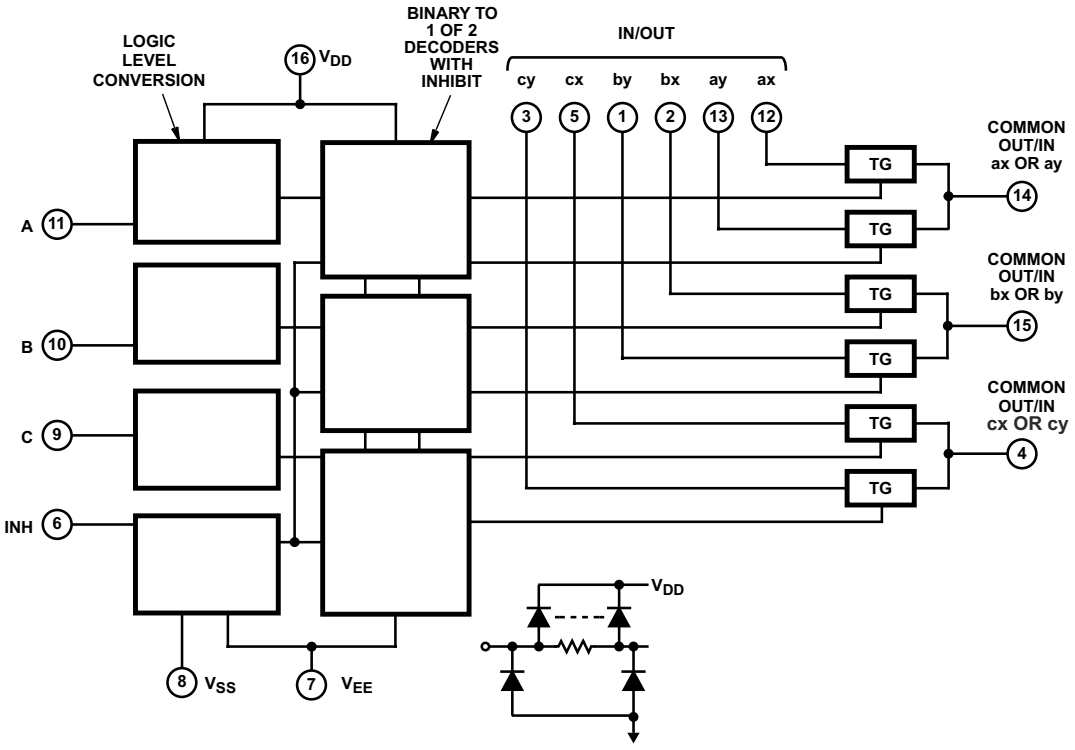
When these devices are used as demultiplexers, the CHANNEL IN/OUT terminals are the outputs and the COMMON OUT/IN terminals are the inputs.

## 7.2 Functional Block Diagrams




All inputs are protected by standard CMOS protection network.

**图 7-1. Functional Block Diagram, CD4051B-Q1**




All inputs are protected by standard CMOS protection network.

**图 7-2. Functional Block Diagram,**

## 7.3 Feature Description

The CD4051B-Q1 line of multiplexers and demultiplexers can accept a wide range of digital and analog signal levels. Digital signals range from 3V to 20V, and analog signals are accepted at levels ⩽ 20V. The devices have low ON resistance, typically 125Ω over $15V_{P-P}$ signal input range for $V_{DD}$ – $V_{EE}$ = 18V. This feature allows for very little signal loss through the switch.

The CD4051B-Q1 devices also have high OFF resistance, which keeps from the devices from wasting power when the switch is in the OFF position, with typical channel leakage of ±100pA at $V_{DD}$ – $V_{EE}$ = 18V.

Binary address decoding on the chip makes channel selection simple. When channels are changed, a break-before-make system eliminates channel overlap.

## 7.4 Device Functional Modes

**表 7-1. Truth Table**

| INPUT STATES | | | | ON CHANNEL(S) |
|---|---|---|---|---|
| INHIBIT | C | B | A | |
| **CD4051B-Q1** | | | | |
| L | L | L | L | 0 |
| L | L | L | H | 1 |
| L | L | H | L | 2 |
| L | L | H | H | 3 |
| L | H | L | L | 4 |
| L | H | L | H | 5 |
| L | H | H | L | 6 |
| L | H | H | H | 7 |

表 7-1. Truth Table（续）

| INPUT STATES | | | | ON CHANNEL(S) |
|---|---|---|---|---|
| INHIBIT | C | B | A | |
| H | X | X | X | None |

# 8 Application and Implementation

**备注**

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

## 8.1 Application Information

The CD4051B-Q1 multiplexers and demultiplexers can be used for a wide variety of applications.

## 8.2 Typical Application

One application of the CD4051B-Q1 is to use it in conjunction with a microcontroller to poll a keypad. 图 8-1 shows the basic schematic for such a polling system. The microcontroller uses the channel select pins to cycle through the different channels while reading the input to see if a user is pressing any of the keys. This application is a very robust setup, allowing for multiple simultaneous key-presses with very little power consumption. This setup also uses very few pins on the microcontroller. The down side of polling is that the microcontroller must continually scan the keys for a press and can do little else during this process.

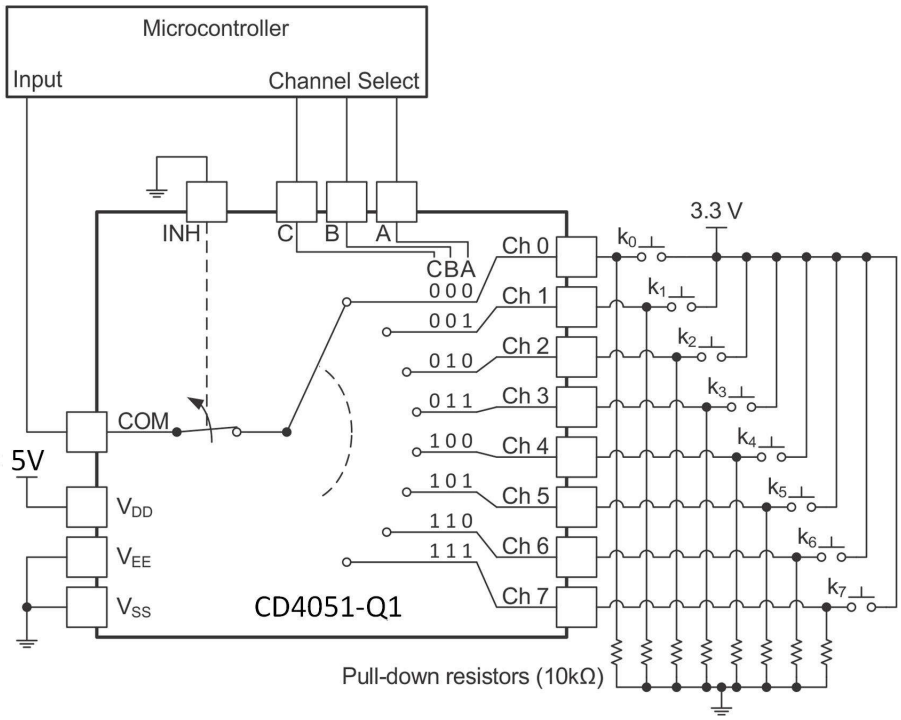



**图 8-1. The CD4051B-Q1 Being Used to Help Read Button Presses on a Keypad**

### *8.2.1 Design Requirements*

These devices use CMOS technology and have balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

### *8.2.2 Detailed Design Procedure*

1. Recommended Input Conditions:
   - For switch time specifications, see propagation delay times in 节 5.5.
   - Inputs should not be pushed more than 0.5V above $V_{DD}$ or below $V_{EE}$.
   - For input voltage level specifications for control inputs, see $V_{IH}$ and $V_{IL}$ in 节 5.5.

2. Recommended Output Conditions:
   - Outputs should not be pulled above $V_{DD}$ or below $V_{EE}$.
3. Input or output current consideration:
   - The CD4051B-Q1 series of parts do not have internal current drive circuitry and thus cannot sink or source current. Any current will be passed through the device.

### *8.2.3 Application Curve*

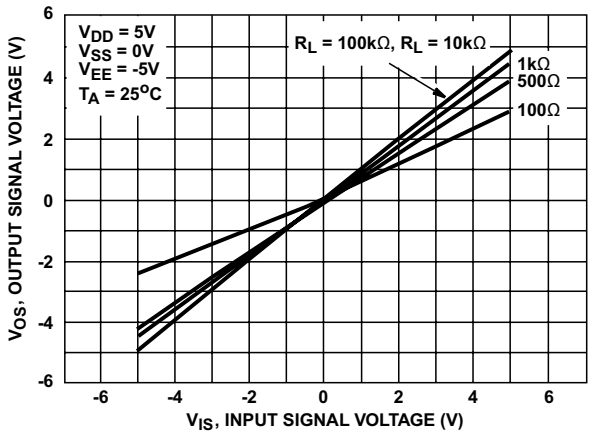



**图 8-2. ON Characteristics for 1 of 8 Channels (CD4051B-Q1)**

## 8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the 节 5.5.

Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 μF bypass capacitor is recommended. If there are multiple pins labeled $V_{CC}$, then a 0.01 μF or 0.022 μF capacitor is recommended for each $V_{CC}$ because the $V_{CC}$ pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example $V_{CC}$ and $V_{DD}$, a 0.1μF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1 μF and 1 μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 8.4 Layout

### 8.4.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This reflection is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self – inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. 图 8-3 shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

### 8.4.2 Layout Example

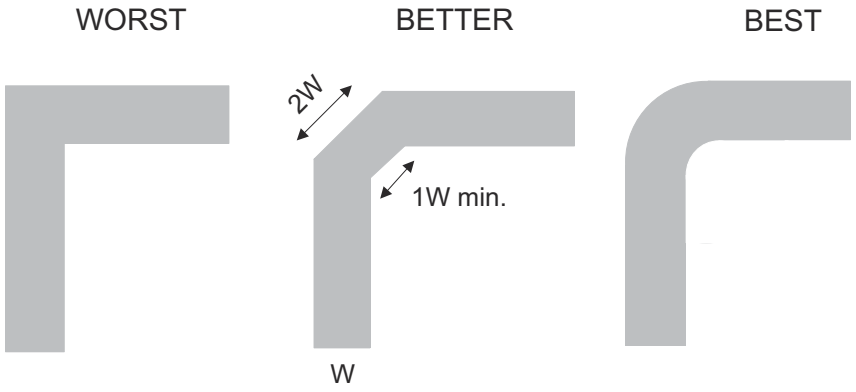



**图 8-3. Trace Example**

# 9 Device and Documentation Support

## 9.1 Documentation Support

### *9.1.1 Related Documentation*

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs*

## 9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

## 9.4 Trademarks

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## 9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

## 10 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision C (March 2023) to Revision D (March 2025) | Page |
|---|---|
| • 更新了节 1 | 1 |
| • 将 CD4053B-Q1 移到了 SCHS469 | 1 |
| • Updated HBM & CDM ESD values | 4 |
| • Updated Figure 8-1 to 5V VDD | 19 |

| Changes from Revision B (April 2019) to Revision C (March 2023) | Page |
|---|---|
| • 更新了整个文档中的表格、图和交叉参考的编号格式 | 1 |
| • 更新了整个数据表中的 CD4051-Q1 规格 | 1 |

| Changes from Revision A (January 2008) to Revision B (April 2019) | Page |
|---|---|
| • 添加了*引脚配置和功能*部分、*ESD 等级*表、*特性说明*部分、*器件功能模式*、*应用和实施*部分、*电源相关建议*部分、*布局*部分、*器件和文档支持*部分，以及*机械、封装和可订购信息*部分 | 1 |
| • 从数据表中删除了器件型号 CD4052B-Q1 | 1 |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| CD4051BQPWRG4Q1 | Obsolete | Production | TSSOP (PW) \| 16 | - | - | Call TI | Call TI | -40 to 125 | CM051BQ |
| CD4051BQPWRQ1 | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CM051BQ |
| CD4051BQPWRQ1.A | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CM051BQ |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.



**OTHER QUALIFIED VERSIONS OF CD4051B-Q1 :**

- Catalog : CD4051B

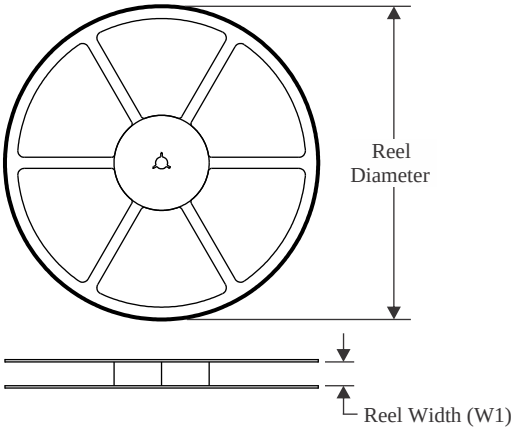
- Military : CD4051B-MIL

NOTE: Qualified Version Definitions:

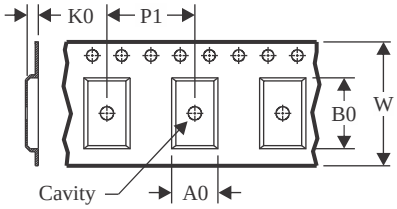
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

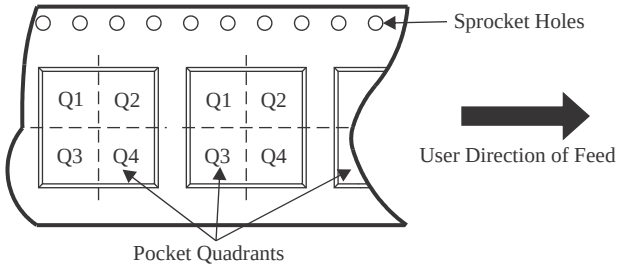



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

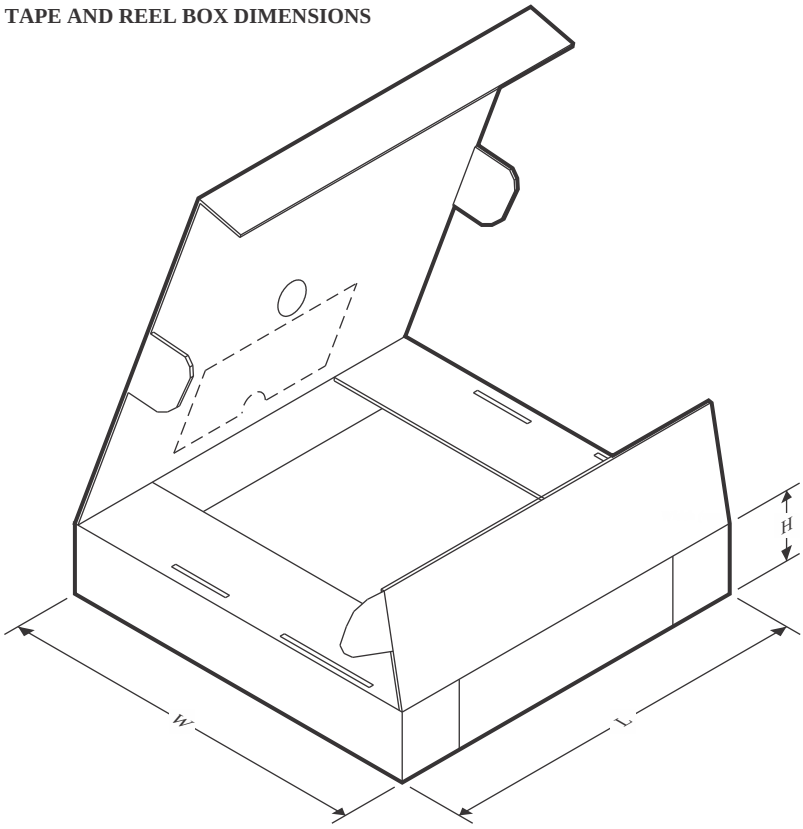
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD4051BQPWRQ1 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

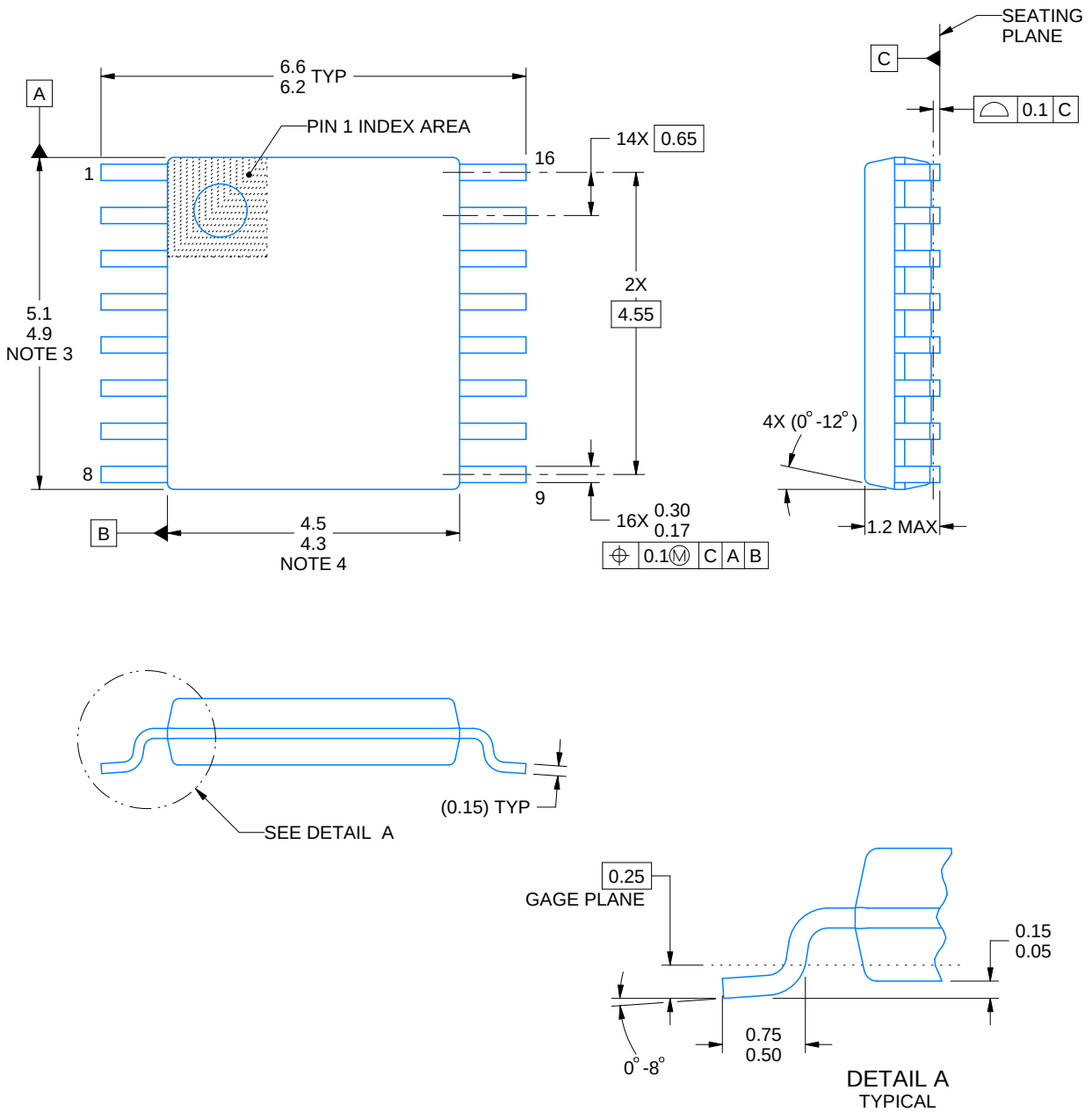
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD4051BQPWRQ1 | TSSOP | PW | 16 | 2000 | 353.0 | 353.0 | 32.0 |

# PACKAGE OUTLINE

## PW0016A

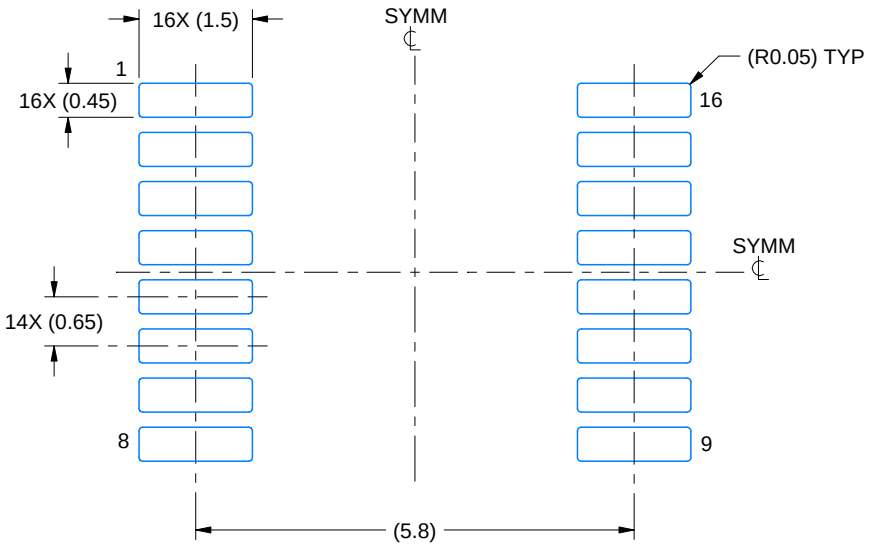
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



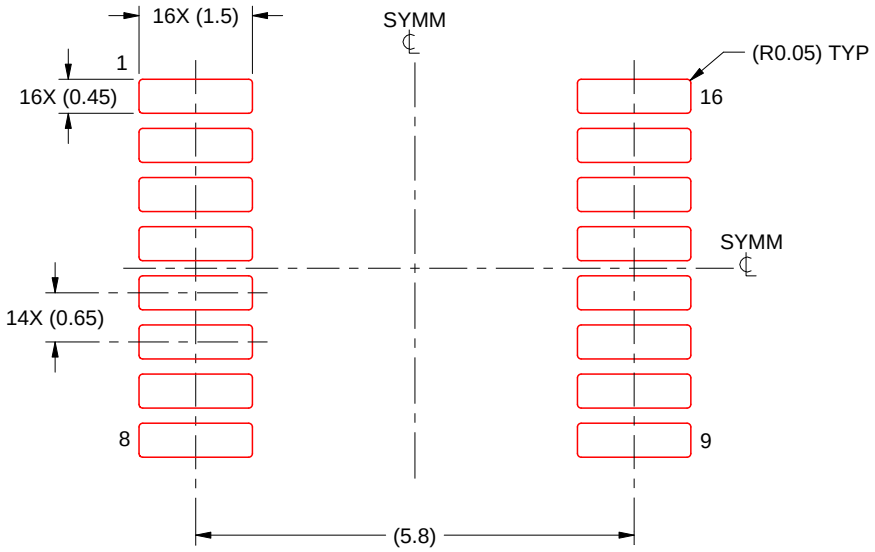

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# 重要通知和免责声明

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