

CD4027B CMOS 双路 J-K 触发器

1 特性

- 置位/复位功能
- 静态触发器运行 - 以高或低时钟电平无限期地保持状态
- 中速运行 - 在 10V 下具有 16MHz (典型值) 的时钟切换速度
- 标准化对称输出特性
- 针对 20V 下的静态电流进行了 100% 测试
- 在全封装温度范围内, 18V 时的最大输入电流为 1 μ A; 18V 和 25°C 时为 100nA
- 噪声容限 (在全封装温度范围内):
 - $V_{DD} = 5V$ 时为 1V
 - $V_{DD} = 10V$ 时为 2V
 - $V_{DD} = 15V$ 时为 2.5V
- 5V、10V 和 15V 参数额定值
- 符合 JEDEC 第 138 号暂行标准, 这是用于描述“B”系列 CMOS 器件的标准规范

2 应用

- 寄存器、计数器和控制电路

3 说明

CD4027B 是一款包含两个相同互补对称 J-K 触发器的单片芯片集成电路。每个触发器都提供了单独的 J、K、置位、复位和时钟输入信号, 以及缓冲 Q 和 $\bar{Q}$ 输出信号。借助此输入/输出, 可实现与 RCA-CD4013B 双路 D 型触发器的兼容操作。

CD4027B 适用于执行控制、寄存器和切换功能。J 和 K 输入端的逻辑电平以及内部自操纵控制每个触发器的状态; 触发器状态的变化与时钟脉冲的正向转换同步。置位和复位功能独立于时钟, 并在置位或复位输入端出现高电平信号时启动。

CD4027B 型采用 16 引脚气密性双列直插式陶瓷封装 (后缀为 F3A)、16 引脚双列直插式塑料封装 (后缀为 E)、16 引脚小外形封装 (后缀为 M、M96、MT 和 NSR) 和 16 引脚薄型紧缩小外形封装 (后缀为 PW 和 PWR)。

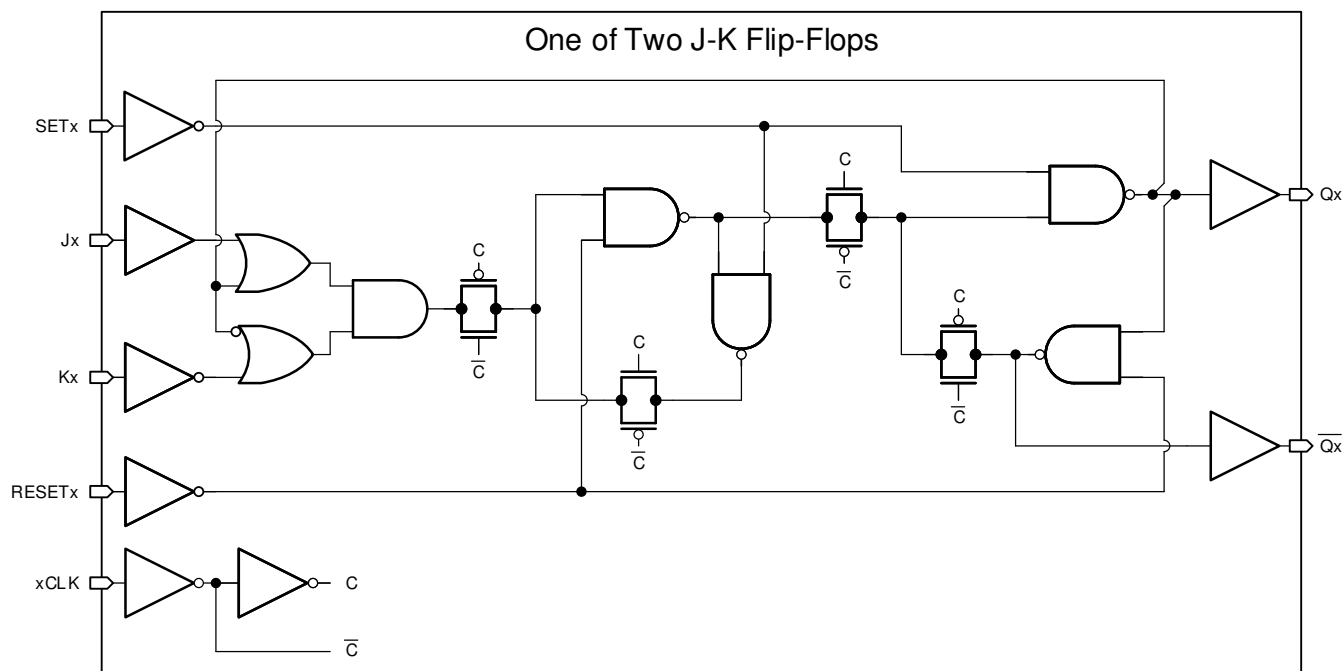


图 3-1. 逻辑图



Table of Contents

1 特性	1	8 Detailed Description	9
2 应用	1	8.1 Functional Block Diagram.....	9
3 说明	1	8.2 Device Functional Modes ⁽¹⁾	9
4 修订历史记录	2	9 Device and Documentation Support	10
5 Pin Configuration and Functions	3	9.1 接收文档更新通知.....	10
6 Specifications	4	9.2 支持资源.....	10
6.1 Absolute Maximum Ratings.....	4	9.3 Trademarks.....	10
6.2 Recommended Operating Conditions.....	4	9.4 Electrostatic Discharge Caution.....	10
6.3 Static Electrical Characteristics.....	5	9.5 术语表.....	10
6.4 Dynamic Electrical Characteristics.....	5	10 Mechanical, Packaging, and Orderable	
6.5 Typical Characteristics.....	7	Information	10
7 Parameter Measurement Information	8		

4 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (October 2003) to Revision D (July 2021)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1

5 Pin Configuration and Functions

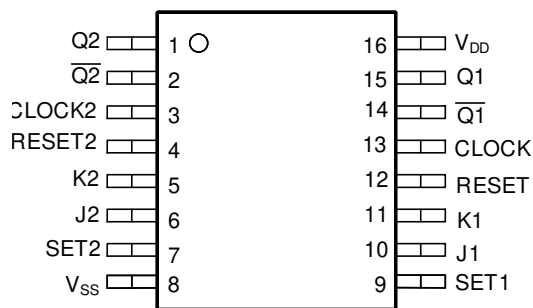


图 5-1. Terminal Assignment

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CLOCK1	13	I	Clock input for channel 1
CLOCK2	3	I	Clock input for channel 2
J1	10	I	J input for channel 1
J2	6	I	J input for channel 2
K1	11	I	K input for channel 1
K2	5	I	K input for channel 2
Q1	15	O	Q output for channel 1
Q1	14	O	Inverted Q output for channel 1
Q2	1	O	Q output for channel 2
Q2	2	O	Inverted Q output for channel 2
RESET1	12	I	Reset input for channel 1
RESET2	4	I	Reset input for channel 2
SET1	9	I	Set input for channel 1
SET2	7	I	Set input for channel 2
V _{DD}	16	—	Supply
V _{SS}	8	—	Ground

6 Specifications

6.1 Absolute Maximum Ratings

			MIN	MAX	UNIT
V _{DD}	DC Supply Voltage Range	Voltages referenced to V _{SS} Terminal	- 0.5	20	V
All Inputs	Input Voltage Range		- 0.5	V _{DD} + 0.5	V
Any One Input	DC Input Current			±10	mA
P _D	Power Dissipation per Package	For T _A = - 55°C to + 100°C		500	mW
		For T _A = +100°C to +125°C	12mW/°C	200	mW
	Device Dissipation per Output Transistor	For T _A = Full package-temperature range (all package types)		100	mW
T _A	Operating- Temperature Range		- 55	125	°C
T _{stg}	Storage temperature		- 65	150	°C
	Lead Temperatur (During Soldering)	At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max		265	°C

6.2 Recommended Operating Conditions

at T_A = 25°C, except as noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC			V _{DD} (V)	LIMITS		UNIT
				ALL PACKAGES		
				MIN	MAX	
	Supply-Voltage Range	For T _A = Full Package Temperature Range		3	18	V
t _S	Data Setup Time		5	200		ns
			10	75		
			15	50		
t _W	Clock Pulse Width		5	140		ns
			10	60		
			15	40		
f _{CL}	Clock Input Frequency (Toggle Mode)		5	3.5		MHz
			10	dc	8	
			15	12		
t _{rCL} , t _{fCL} ⁽¹⁾	Clock Rise or Fall Time		5	45		μ s
			10	5		
			15	2		
t _W	Set or Reset Pulse Width		5	180		ns
			10	80		
			15	50		

- (1) If more than one unite is cascaded in a parallel clocked operation, t_{rCL} should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transitiopn time of the output driving stage for the estimated capacitive load.

6.3 Static Electrical Characteristics

CHARACTERISTIC	TEST CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)						UNIT	
	V _O (V)	V _{IN} (V)	V _{DD} (V)	− 55	− 40	+85	+125	+25			
								MIN	TYP		MAX
Quiescent		0, 5	5	1	1	30	30	0.02		1	μ a
Device		0, 10	10	2	2	60	60	0.02		2	
Current		0, 15	15	4	4	120	120	0.02		4	
I _{DD} Max.		0, 20	20	20	20	600	600	0.04		20	
Output Low (Sink)	0.4	0, 5	5	0.64	0.61	0.42	0.36	0.51	1		mA
Current	0.5	0, 10	10	1.6	1.5	1.1	0.9	1.3	2.6		
I _{OL} Min.	1.5	0, 15	15	4.2	4	2.8	2.4	3.4	6.8		
Output High	4.6	0, 5	5	− 0.64	− 0.61	− 0.42	− 0.36	− 0.51	− 1		mA
(Source)	2.5	0, 5	5	− 2	− 1.8	− 1.3	− 1.15	− 1.6	− 3.2		
Current	9.5	0, 10	10	− 1.6	− 1.5	− 1.1	− 0.9	− 1.3	− 2.6		
I _{OH} Min.	13.5	0, 15	15	− 4.2	− 4	− 2.8	− 2.4	− 3.4	− 6.8		
Output Voltage		0, 5	5	0.05				0		0.05	V
Low-Level		0, 10	10	0.05				0		0.05	
V _{OL} Max.		0, 15	15	0.05				0		0.05	
Output Voltage		0, 5	5	4.95				4.95		5	V
High-Level		0, 10	10	9.95				9.95		10	
V _{OH} Min.		0, 15	15	14.95				14.95		15	
Input Low	0,5, 4,5		5	1.5				1.5			V
Voltage	1, 9		10	3				3			
V _{IL} Max.	1.5, 13,5		15	4				4			
Input High	0.5, 4,5		5	3.5				3.5			V
Voltage	1, 9		10	7				7			
V _{IH} Min.	1.5, 13,5		15	11				11			
Input Current, V _{IH} Max.		0, 18	18	±0.1	±0.1	±1	±1	±10 ^{− 5}		±0.1	μ A

6.4 Dynamic Electrical Characteristics

at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 k Ω

CHARACTERISTIC	V _{DD} (V)	LIMITS			UNIT
		ALL PACKAGES			
		MIN	TYP	MAX	
Propagation Delay Time	5		150	300	ns
Clock to Q or $\overline{Q}$ Outputs	10		65	130	
t _{PHL} , t _{PLH}	15		45	90	
Set to Q or Reset to $\overline{Q}$, t _{PLH}	5		150	300	ns
	10		65	130	
	15		45	90	
Set to $\overline{Q}$ or Reset to Q, t _{PHL}	5		200	400	ns
	10		85	170	
	15		60	120	
Transition Time t _{THL} , t _{TLH}	5		100	200	ns
	10		50	100	
	15		40	80	

6.4 Dynamic Electrical Characteristics (continued)

at $T_A = 25^\circ\text{C}$; Input $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	V _{DD} (V)	LIMITS			UNIT		
		ALL PACKAGES					
		MIN	TYP	MAX			
Maximum Clock Input Frequency (Toggle Mode) ⁽¹⁾ f _{CL}	5 10 15	3.5 8 12	7 16 24		MHz		
Minimum Clock Pulse Width, t _W	5 10 15		70 30 20	140 60 40			
	Minimum Set or Reset Pulse Width, t _W	5 10 15		90 40 25			180 80 50
		Minimum Data Setup Time, t _S	5 10 15		100 35 25		200 75 50
Clock Input Rise or Fall Time t _{rCL} , t _{fCL}			5 10 15			45 5 2	μ s
	Input Capacitance, C _I				5	7.5	

(1) Input $t_r, t_f = 5\text{ ns}$

6.5 Typical Characteristics

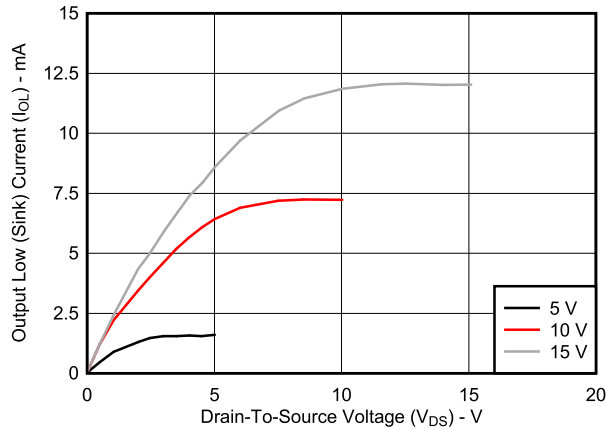


图 6-1. Typical Output Low (Sink) Current Characteristics

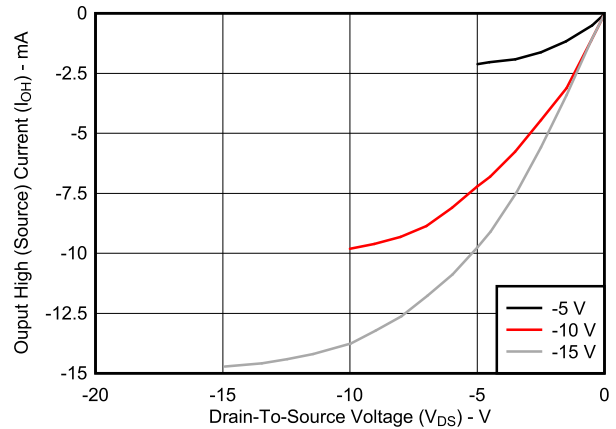


图 6-2. Typical Output High (Source) Current Characteristics

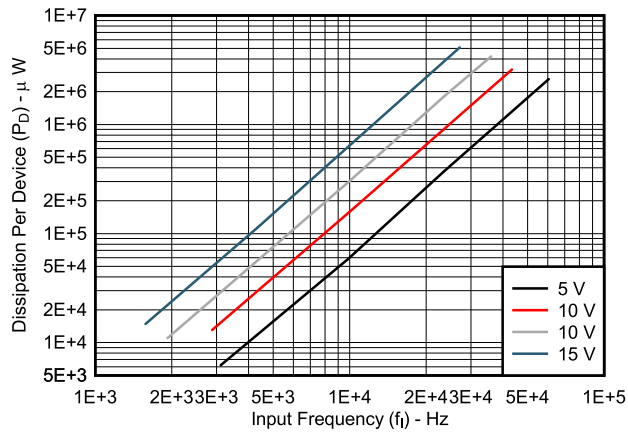


图 6-3. Typical Power Dissipation vs Frequency

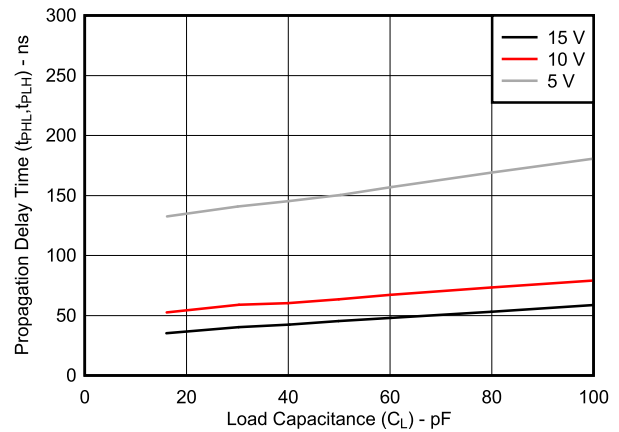


图 6-4. Typical Propagation Delay Time vs Load Capacitance (Clock or Set to Q, Clock or Reset to Q)

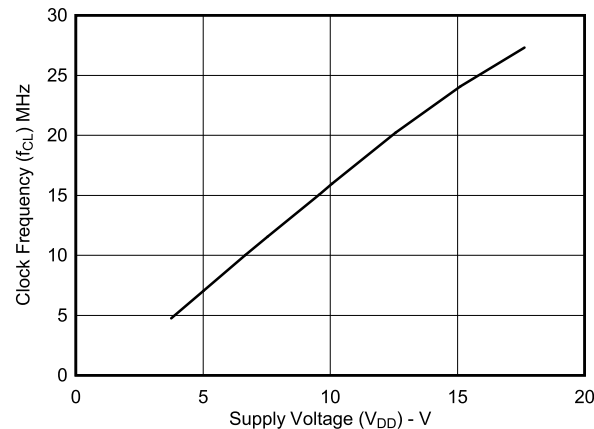


图 6-5. Typical Maximum Clock Frequency vs Supply Voltage (Toggle Mode)

7 Parameter Measurement Information

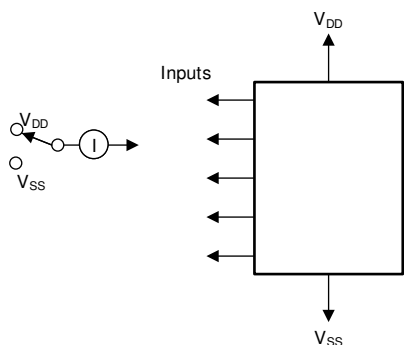


图 7-1. Input Current Test Circuit

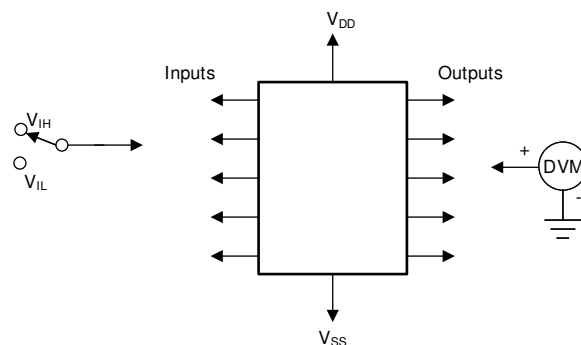


图 7-2. Input-Voltage Test Circuit

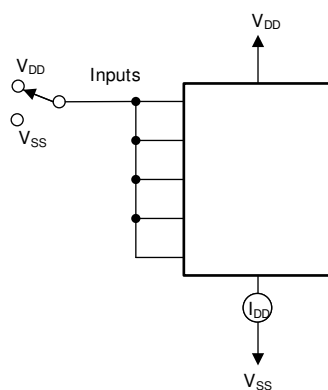
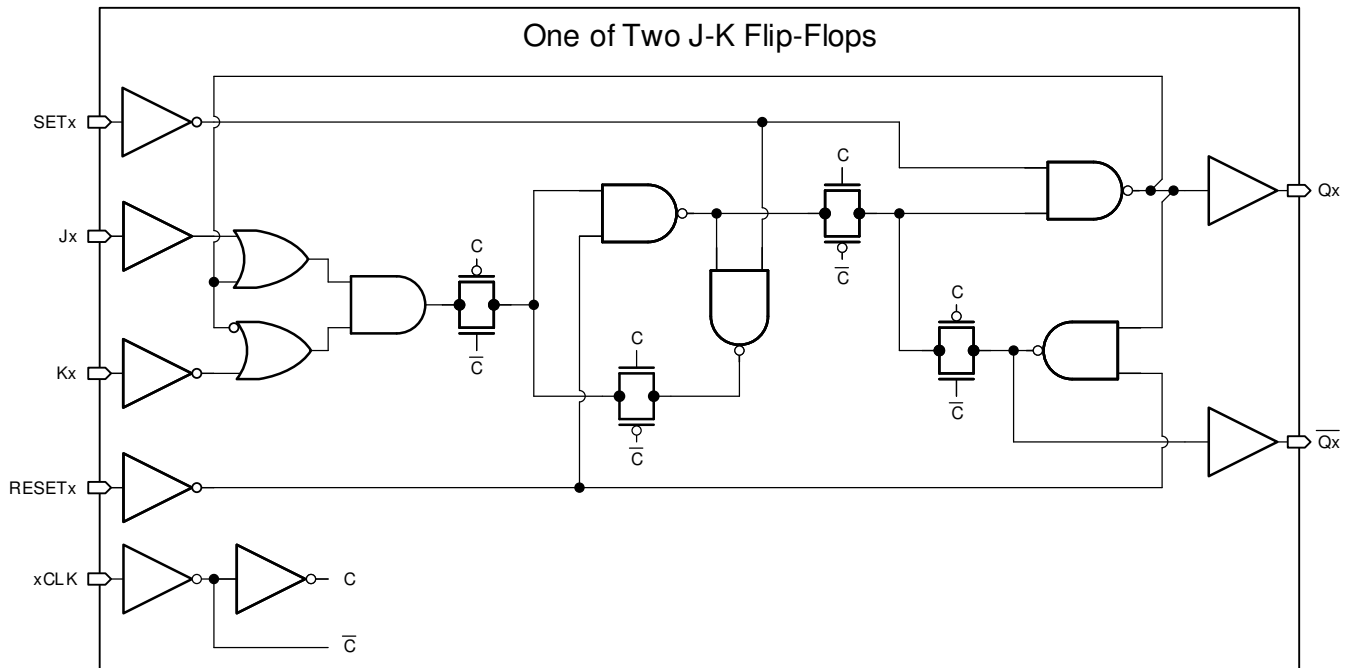


图 7-3. Quiescent Device Current Test Circuit

8 Detailed Description

8.1 Functional Block Diagram



8.2 Device Functional Modes⁽¹⁾

PRESENT STATE					CL ⁽²⁾	NEXT STATE	
INPUTS				OUTPUT		OUTPUTS	
J	K	S	R	O	$\underline{I}$	O	$\bar{O}$
I	X	O	O	O	$\underline{I}$	I	O
X	O	O	O	I	$\underline{I}$	I	O
O	X	O	O	O	$\underline{I}$	O	I
X	I	O	O	I	$\underline{I}$	O	I
X	X	O	O	X	$\bar{\underline{I}}$	No change	No change
X	X	I	O	X	X	I	O
X	X	O	I	X	X	O	I
X	X	I	I	X	X	I	I

(1) Logic I = High Level, Logic O = Low Level, X = Do not care

(2) Level change

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD4027BE	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4027BE
CD4027BE.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4027BE
CD4027BEE4	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4027BE
CD4027BF	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4027BF
CD4027BF.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4027BF
CD4027BF3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4027BF3A
CD4027BF3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4027BF3A
CD4027BM	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	CD4027BM
CD4027BM96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4027BM
CD4027BM96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4027BM
CD4027BM96E4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4027BM
CD4027BMT	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	CD4027BM
CD4027BNSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4027B
CD4027BNSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4027B
CD4027BPW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-55 to 125	CM027B
CD4027BPWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM027B
CD4027BPWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM027B
JM38510/05152BEA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 05152BEA
JM38510/05152BEA.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 05152BEA
M38510/05152BEA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 05152BEA

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD4027B, CD4027B-MIL :

- Catalog : [CD4027B](#)
- Military : [CD4027B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4027BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4027BNSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD4027BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4027BM96	SOIC	D	16	2500	353.0	353.0	32.0
CD4027BNSR	SOP	NS	16	2000	356.0	356.0	35.0
CD4027BPWR	TSSOP	PW	16	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD4027BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4027BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4027BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4027BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4027BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4027BEE4	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

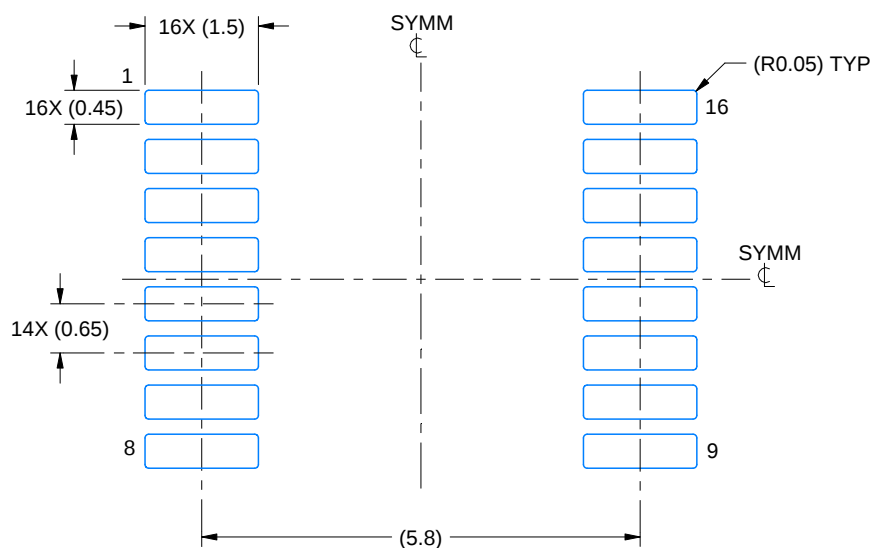
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

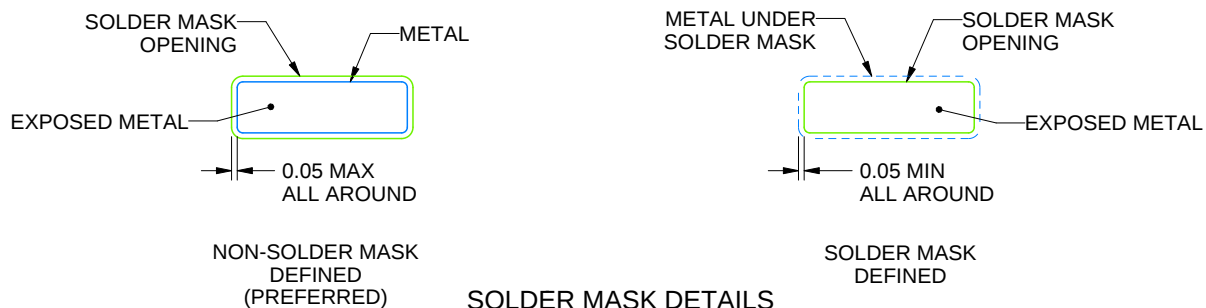
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

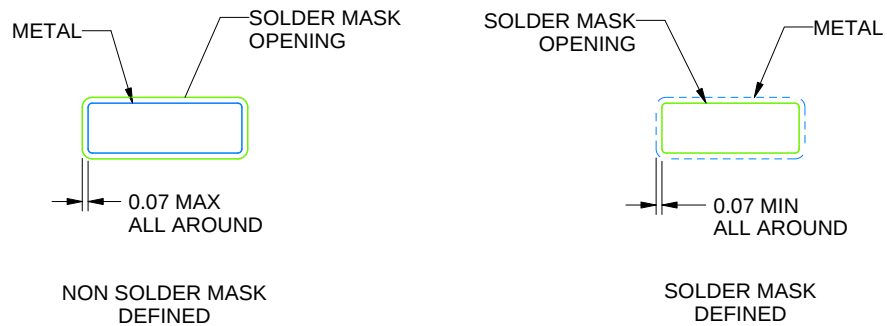
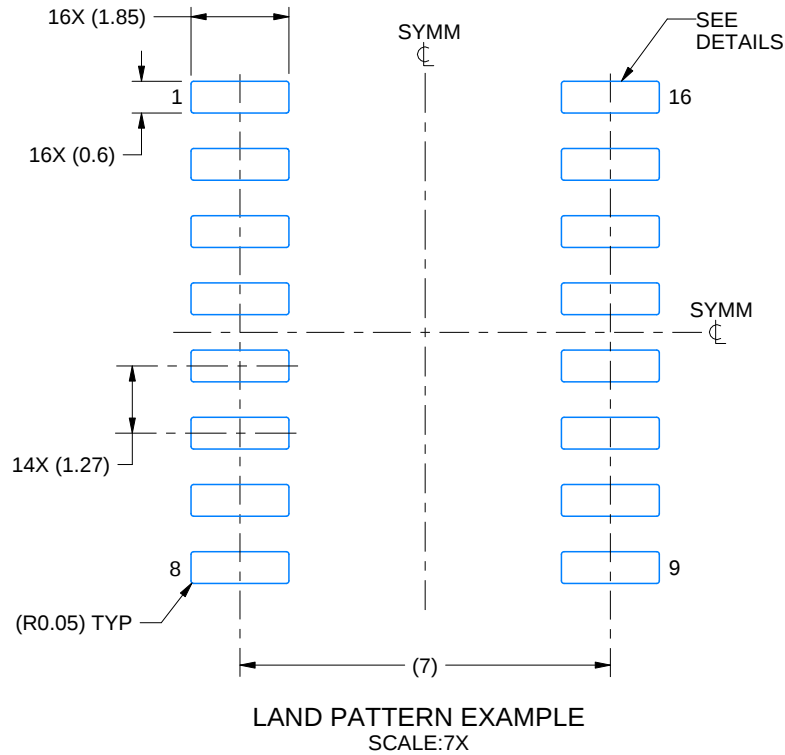
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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