

# CMOS 8-Stage Presettable Synchronous Down Counters

High-Voltage Types (20-Volt Rating)

CD40102B – 2-Decade BCD Type

CD40103B – 8-Bit Binary Type

■ CD40102B, and CD40103B consist of an 8-stage synchronous down counter with a single output which is active when the internal count is zero. The CD40102B is configured as two cascaded 4-bit BCD counters, and the CD40103B contains a single 8-bit binary counter. Each type has control inputs for enabling or disabling the clock, for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the CARRY-OUT/ZERO-DETECT output are active-low logic.

In normal operation, the counter is decremented by one count on each positive transition of the CLOCK. Counting is inhibited when the CARRY-IN/COUNTER ENABLE ( $\overline{CI/CE}$ ) input is high. The CARRY-OUT/ZERO-DETECT ( $\overline{CO/ZD}$ ) output goes low when the count reaches zero if the  $\overline{CI/CE}$  input is low, and remains low for one full clock period.

When the SYNCHRONOUS PRESET-ENABLE ( $\overline{SPE}$ ) input is low, data at the JAM input is clocked into the counter on the next positive clock transition regardless of the state of the  $\overline{CI/CE}$  input. When the ASYNCHRONOUS PRESET-ENABLE ( $\overline{APE}$ ) input is low, data at the JAM inputs is asynchronously forced into the counter regardless of the state of the  $\overline{SPE}$ ,  $\overline{CI/CE}$ , or CLOCK inputs. JAM inputs J0-J7 represent two 4-bit BCD words for the CD40102B and a single 8-bit binary word for the CD40103B.

When the CLEAR ( $\overline{CLR}$ ) input is low, the counter is asynchronously cleared to its maximum count (99<sub>10</sub> for the CD40102B and 255<sub>10</sub> for the CD40103B) regardless of the state of any other input. The precedence relationship between control inputs is indicated in the truth table.

If all control inputs except  $\overline{CI/CE}$  are high at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 100 or 256 clock pulses long.

This causes the  $\overline{CO/ZD}$  output to go low to enable the clock on each succeeding clock pulse.

The CD40102B and CD40103B may be cascaded using the  $\overline{CI/CE}$  input and the  $\overline{CO/ZD}$  output, in either a synchronous or ripple mode as shown in Figs.21 and 22.

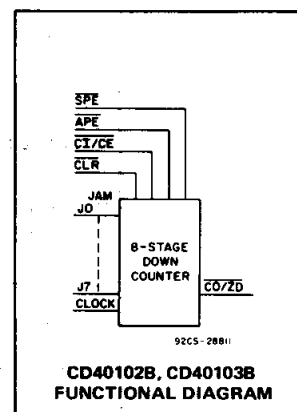
The CD40102B and CD40103B types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes). The CD40103B types also are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix).

## Features:

- Synchronous or asynchronous preset
- Medium-speed operation:  $f_{CL} = 3.6 \text{ MHz (typ.) @ } V_{DD} = 10 \text{ V}$
- Cascadable
- 100% tested for quiescent current at 20 V
- Maximum input current of 1  $\mu\text{A}$  at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) = 1 V at  $V_{DD} = 5 \text{ V}$   
2 V at  $V_{DD} = 10 \text{ V}$   
2.5 V at  $V_{DD} = 15 \text{ V}$
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

## Applications:

- Divide-by-"N" counters
- Programmable timers
- Interrupt timers
- Cycle/program counter



**RECOMMENDED OPERATING CONDITIONS AT  $T_A = 25^\circ\text{C}$ , Unless Otherwise Specified**  
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

| Characteristic                                                           | $V_{DD}$ | LIMITS |      | Units         |
|--------------------------------------------------------------------------|----------|--------|------|---------------|
|                                                                          |          | Min.   | Max. |               |
| Supply Voltage Range (At $T_A = \text{Full Package-Temperature Range}$ ) |          | 3      | 18   | V             |
| Clock Pulse Width, $t_W$                                                 | 5        | 300    | —    | ns            |
|                                                                          | 10       | 180    | —    |               |
|                                                                          | 15       | 80     | —    |               |
| $\overline{\text{Clear}}$ Pulse Width, $t_W$                             | 5        | 320    | —    | ns            |
|                                                                          | 10       | 160    | —    |               |
|                                                                          | 15       | 100    | —    |               |
| $\overline{\text{APE}}$ Pulse Width, $t_W$                               | 5        | 360    | —    | ns            |
|                                                                          | 10       | 160    | —    |               |
|                                                                          | 15       | 120    | —    |               |
| Clock Input Frequency, $f_{CL}$                                          | 5        | —      | 0.7  | MHz           |
|                                                                          | 10       | —      | 1.8  |               |
|                                                                          | 15       | —      | 2.4  |               |
| Clock Rise and Fall Time, $t_{rCL}$ , $t_{fCL}$                          | 5        | —      | —    | $\mu\text{s}$ |
|                                                                          | 10       | —      | 15   |               |
|                                                                          | 15       | —      | —    |               |
| $\overline{\text{SPE}}$ Setup Time, $t_{SU}$                             | 5        | 280    | —    | ns            |
|                                                                          | 10       | 140    | —    |               |
|                                                                          | 15       | 100    | —    |               |
| Jam Setup Time, $t_{SU}$                                                 | 5        | 200    | —    | ns            |
|                                                                          | 10       | 80     | —    |               |
|                                                                          | 15       | 60     | —    |               |
| $\overline{\text{CI/CE}}$ Setup Time, $t_{SU}$                           | 5        | 500    | —    | ns            |
|                                                                          | 10       | 250    | —    |               |
|                                                                          | 15       | 150    | —    |               |

# CD40102B, CD40103B Types

## MAXIMUM RATINGS, Absolute-Maximum Values:

### DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )

Voltages referenced to  $V_{SS}$  Terminal)

INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to +20V

DC INPUT CURRENT, ANY ONE INPUT .....  $\pm 10\text{mA}$

### POWER DISSIPATION PER PACKAGE ( $P_D$ ):

For  $T_A = -55^\circ\text{C}$  to  $+100^\circ\text{C}$  ..... 500mW

For  $T_A = +100^\circ\text{C}$  to  $+125^\circ\text{C}$  ..... Derate Linearly at  $12\text{mW}/^\circ\text{C}$  to 200mW

### DEVICE DISSIPATION PER OUTPUT TRANSISTOR

For  $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$  ..... 100mW

OPERATING-TEMPERATURE RANGE ( $T_A$ ) .....  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

STORAGE TEMPERATURE RANGE ( $T_{stg}$ ) .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$

### LEAD TEMPERATURE (DURING SOLDERING):

At distance  $1/16 \pm 1/32$  inch ( $1.59 \pm 0.79\text{mm}$ ) from case for 10s max .....  $+265^\circ\text{C}$

## STATIC ELECTRICAL CHARACTERISTICS

| CHARACTER-<br>ISTIC                                         | CONDITIONS            |                        |                        | LIMITS AT INDICATED TEMPERATURES (°C) |       |       |       |       |                   |      | UNITS |
|-------------------------------------------------------------|-----------------------|------------------------|------------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
|                                                             | V <sub>O</sub><br>(V) | V <sub>IN</sub><br>(V) | V <sub>DD</sub><br>(V) | +25                                   |       |       |       |       |                   |      |       |
|                                                             |                       |                        |                        | -55                                   | -40   | +85   | +125  | Min.  | Typ.              | Max. |       |
| Quiescent Device<br>Current,<br>I <sub>DD</sub> Max.        | —                     | 0,5                    | 5                      | 5                                     | 5     | 150   | 150   | —     | 0.04              | 5    | μA    |
|                                                             | —                     | 0,10                   | 10                     | 10                                    | 10    | 300   | 300   | —     | 0.04              | 10   |       |
|                                                             | —                     | 0,15                   | 15                     | 20                                    | 20    | 600   | 600   | —     | 0.04              | 20   |       |
|                                                             | —                     | 0,20                   | 20                     | 100                                   | 100   | 3000  | 3000  | —     | 0.08              | 100  |       |
| Output Low<br>(Sink) Current<br>I <sub>OL</sub> Min.        | 0.4                   | 0,5                    | 5                      | 0.64                                  | 0.61  | 0.42  | 0.36  | 0.51  | 1                 | —    | mA    |
|                                                             | 0.5                   | 0,10                   | 10                     | 1.6                                   | 1.5   | 1.1   | 0.9   | 1.3   | 2.6               | —    |       |
|                                                             | 1.5                   | 0,15                   | 15                     | 4.2                                   | 4     | 2.8   | 2.4   | 3.4   | 6.8               | —    |       |
| Output High<br>(Source)<br>Current,<br>I <sub>OH</sub> Min. | 4.6                   | 0,5                    | 5                      | -0.64                                 | -0.61 | -0.42 | -0.36 | -0.51 | -1                | —    | mA    |
|                                                             | 2.5                   | 0,5                    | 5                      | -2                                    | -1.8  | -1.3  | -1.15 | -1.6  | -3.2              | —    |       |
|                                                             | 9.5                   | 0,10                   | 10                     | -1.6                                  | -1.5  | -1.1  | -0.9  | -1.3  | -2.6              | —    |       |
|                                                             | 13.5                  | 0,15                   | 15                     | -4.2                                  | -4    | -2.8  | -2.4  | -3.4  | -6.8              | —    |       |
| Output Voltage:<br>Low-Level,<br>V <sub>OL</sub> Max.       | —                     | 0,5                    | 5                      | 0.05                                  |       |       |       | —     | 0                 | 0.05 | V     |
|                                                             | —                     | 0,10                   | 10                     | 0.05                                  |       |       |       | —     | 0                 | 0.05 |       |
|                                                             | —                     | 0,15                   | 15                     | 0.05                                  |       |       |       | —     | 0                 | 0.05 |       |
| Output Voltage:<br>High-Level,<br>V <sub>OH</sub> Min.      | —                     | 0,5                    | 5                      | 4.95                                  |       |       |       | 4.95  | 5                 | —    | V     |
|                                                             | —                     | 0,10                   | 10                     | 9.95                                  |       |       |       | 9.95  | 10                | —    |       |
|                                                             | —                     | 0,15                   | 15                     | 14.95                                 |       |       |       | 14.95 | 15                | —    |       |
| Input Low<br>Voltage,<br>V <sub>IL</sub> Max.               | 0.5, 4.5              | —                      | 5                      | 1.5                                   |       |       |       | —     | —                 | 1.5  | V     |
|                                                             | 1, 9                  | —                      | 10                     | 3                                     |       |       |       | —     | —                 | 3    |       |
|                                                             | 1.5, 13.5             | —                      | 15                     | 4                                     |       |       |       | —     | —                 | 4    |       |
| Input High<br>Voltage,<br>V <sub>IH</sub> Min.              | 0.5, 4.5              | —                      | 5                      | 3.5                                   |       |       |       | 3.5   | —                 | —    | V     |
|                                                             | 1, 9                  | —                      | 10                     | 7                                     |       |       |       | 7     | —                 | —    |       |
|                                                             | 1.5, 13.5             | —                      | 15                     | 11                                    |       |       |       | 11    | —                 | —    |       |
| Input Current<br>I <sub>IN</sub> Max.                       | —                     | 0,18                   | 18                     | ±0.1                                  | ±0.1  | ±1    | ±1    | —     | ±10 <sup>-5</sup> | ±0.1 | μA    |

Note 1: These parameters and limits also apply to the Synchronous Preset Mode should a Preset condition of JAM Zero on  $J_0$  to  $J_7$  exist.

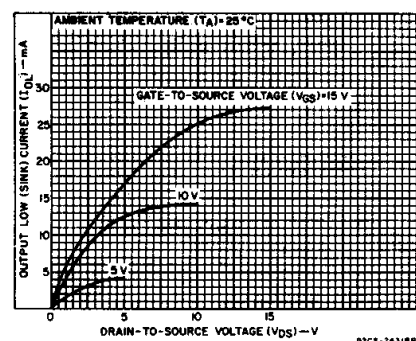


Fig. 1 — Typical output low (sink) current characteristics.

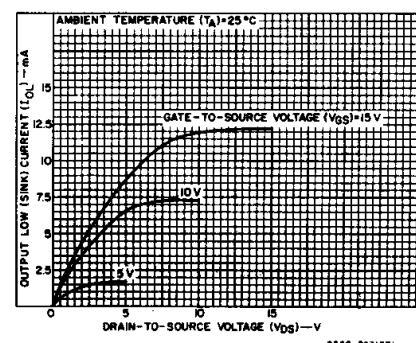


Fig. 2 — Minimum output low (sink) current characteristics.

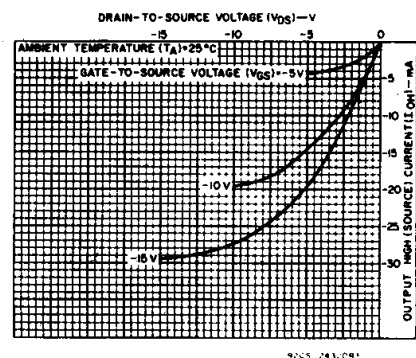


Fig. 3 — Typical output high (source) current characteristics.

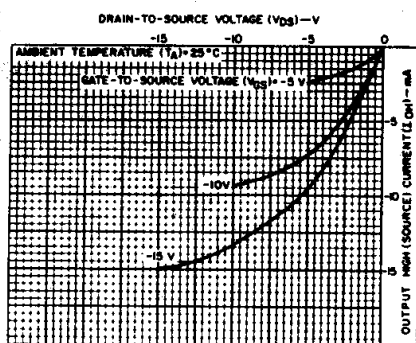


Fig. 4 — Minimum output high (source) current characteristics.

# CD40102B, CD40103B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$ ,  
Input  $t_r, t_f = 20\text{ ns}$ ,  $R_L = 200\text{ k}\Omega$

| Characteristic                                                   | Conditions<br>$V_{DD}$<br>(V) | Limits<br>All Packages |      |      | Units |
|------------------------------------------------------------------|-------------------------------|------------------------|------|------|-------|
|                                                                  |                               | Min.                   | Typ. | Max. |       |
| Propagation Delay Time ( $t_{PHL}, t_{PLH}$ ):                   |                               |                        |      |      |       |
| Clock-to-Output (See Fig. 6)                                     | 5                             | —                      | 300  | 600  | ns    |
| Note 1                                                           | 10                            | —                      | 130  | 260  |       |
|                                                                  | 15                            | —                      | 95   | 190  |       |
| Carry In/Counter Enable-to-Output                                | 5                             | —                      | 200  | 400  | ns    |
|                                                                  | 10                            | —                      | 90   | 180  |       |
|                                                                  | 15                            | —                      | 65   | 130  |       |
| Asynchronous Preset Enable-to-Output                             | 5                             | —                      | 650  | 1300 | ns    |
| Note 1                                                           | 10                            | —                      | 300  | 600  |       |
|                                                                  | 15                            | —                      | 200  | 400  |       |
| Clear-to-Output                                                  | 5                             | —                      | 375  | 750  | ns    |
|                                                                  | 10                            | —                      | 180  | 360  |       |
|                                                                  | 15                            | —                      | 100  | 200  |       |
| Transition Time ( $t_{THL}, t_{TLH}$ )                           | 5                             | —                      | 100  | 200  | ns    |
|                                                                  | 10                            | —                      | 50   | 100  |       |
|                                                                  | 15                            | —                      | 40   | 80   |       |
| Minimum Clock Pulse Width, ( $t_W$ )                             | 5                             | —                      | 150  | 300  | ns    |
|                                                                  | 10                            | —                      | 90   | 180  |       |
|                                                                  | 15                            | —                      | 40   | 80   |       |
| Minimum CLR Pulse Width ( $t_W$ )                                | 5                             | —                      | 160  | 320  | ns    |
|                                                                  | 10                            | —                      | 80   | 160  |       |
|                                                                  | 15                            | —                      | 50   | 100  |       |
| Minimum APE Pulse Width ( $t_W$ )                                | 5                             | —                      | 180  | 360  | ns    |
|                                                                  | 10                            | —                      | 80   | 160  |       |
|                                                                  | 15                            | —                      | 60   | 120  |       |
| Minimum APE Removal Time ( $t_{RM}$ )                            | 5                             | —                      | 110  | 220  | ns    |
|                                                                  | 10                            | —                      | 50   | 100  |       |
|                                                                  | 15                            | —                      | 35   | 70   |       |
| Minimum SPE Set-Up Time ( $t_{SU}$ )                             | 5                             | —                      | 140  | 280  | ns    |
|                                                                  | 10                            | —                      | 70   | 140  |       |
|                                                                  | 15                            | —                      | 50   | 100  |       |
| Minimum CI/CE Setup Time ( $t_{SU}$ )                            | 5                             | —                      | 250  | 500  | ns    |
|                                                                  | 10                            | —                      | 125  | 250  |       |
|                                                                  | 15                            | —                      | 75   | 150  |       |
| Minimum JAM Set-Up Time ( $t_{SU}$ )<br>(Synchronous presetting) | 5                             | —                      | 100  | 200  | ns    |
|                                                                  | 10                            | —                      | 40   | 80   |       |
|                                                                  | 15                            | —                      | 30   | 60   |       |
| Maximum Clock Input Frequency ( $f_{CL}$ )<br>(See Fig. 7)       | 5                             | 0.7                    | 1.4  | —    | MHz   |
|                                                                  | 10                            | 1.8                    | 3.6  | —    |       |
|                                                                  | 15                            | 2.4                    | 4.8  | —    |       |
| Input Capacitance ( $C_{IN}$ )                                   |                               | —                      | 5    | 7.5  | pF    |

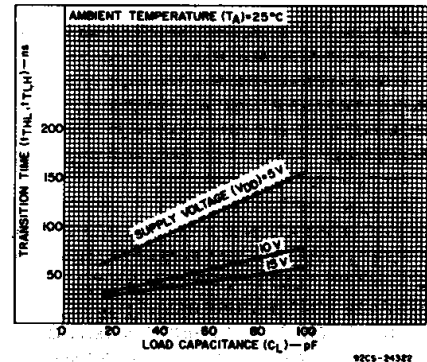


Fig. 5 - Typical transition time as a function of load capacitance.

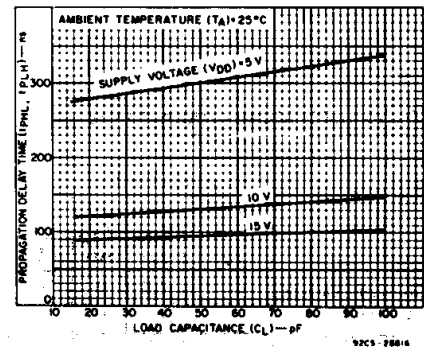


Fig. 6 - Typical propagation delay time as a function of load capacitance (clock to CO/ZD).

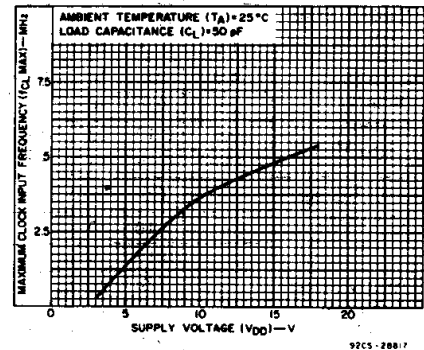


Fig. 7 - Typical maximum clock input frequency as a function of supply voltage.

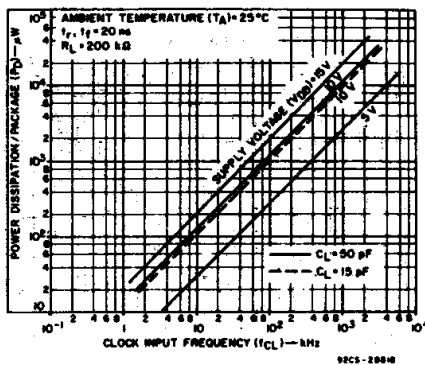


Fig. 8 - Typical dynamic power dissipation as a function of frequency.

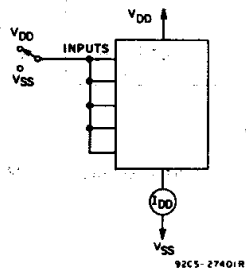


Fig. 9 - Quiescent device current test circuit.

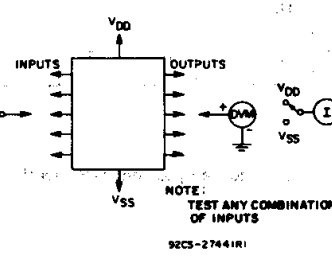


Fig. 10 - Input voltage test circuit.

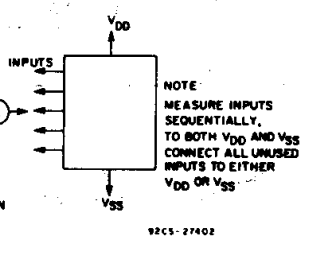


Fig. 11 - Input current test circuit.

## CD40102B, CD40103B Types

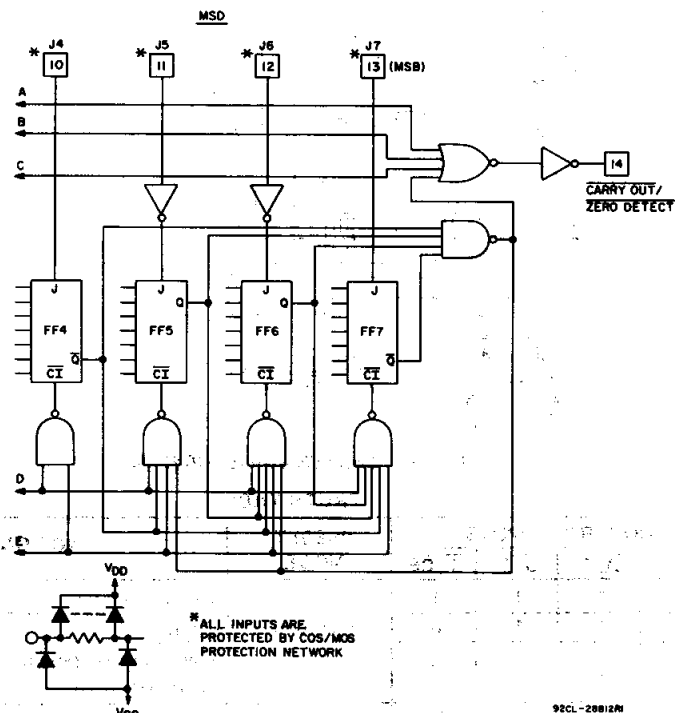
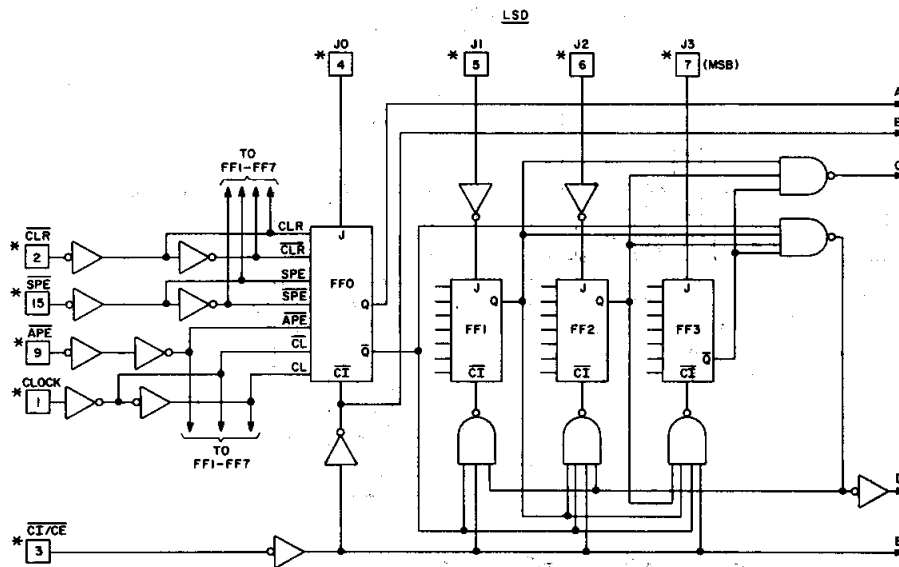


Fig. 12 — Logic diagram for CD40102B.

## CD40102B, CD40103B Types

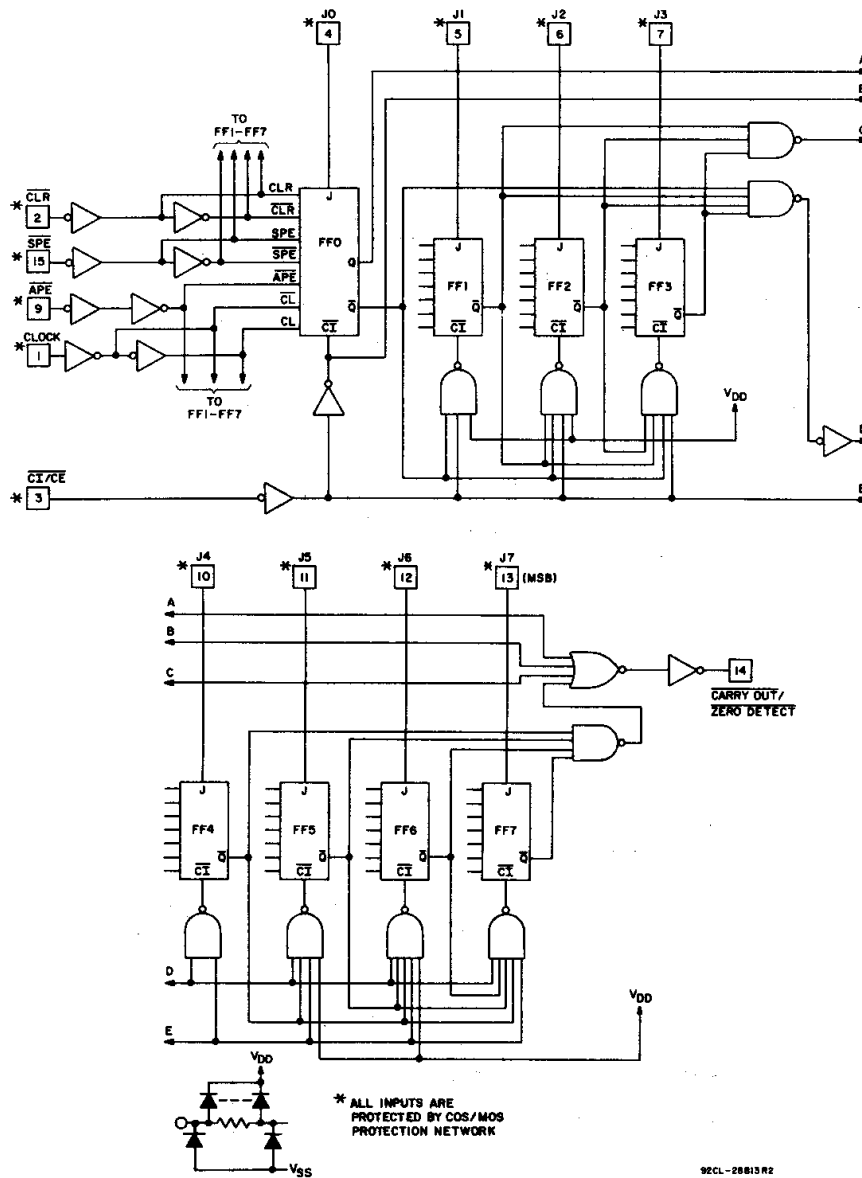


Fig. 13 — Logic diagram for CD40103B.

### TRUTH TABLE

| CONTROL INPUTS |     |     |       | PRESET MODE  | ACTION                                   |
|----------------|-----|-----|-------|--------------|------------------------------------------|
| CLR            | APE | SPE | CI/CE |              |                                          |
| 1              | 1   | 1   | 1     | Synchronous  | Inhibit counter                          |
| 1              | 1   | 1   | 0     |              | Count down*                              |
| 1              | 1   | 0   | X     |              | Preset on next positive clock transition |
| 1              | 0   | X   | X     | Asynchronous | Preset asynchronously                    |
| 0              | X   | X   | X     |              | Clear to maximum count                   |

Notes: 1. 0 = Low level  
1 = High level  
X = Don't care

2. Clock connected to clock input
3. Synchronous operation: changes occur on negative-to-positive clock transitions
4. JAM inputs: CD40102B BCD; MSD = J7,J6,J5,J4 (J7 is MSB)  
LSD = J3,J2,J1,J0 (J3 is MSB)  
CD40103B Binary; MSB = J7, LSB = J0

\*At zero count, the counters will jump to the maximum count on the next clock transition to "High."

## CD40102B, CD40103B Types

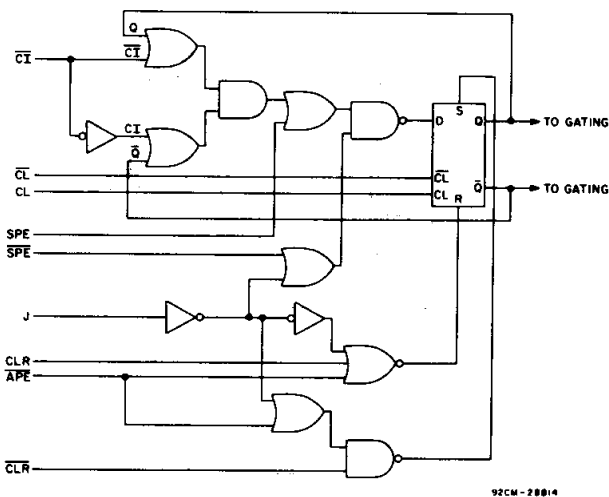


Fig. 14 - Detail logic diagram for flip-flops, FFO - FF7, used in logic diagrams for CD40102B and CD40103B.

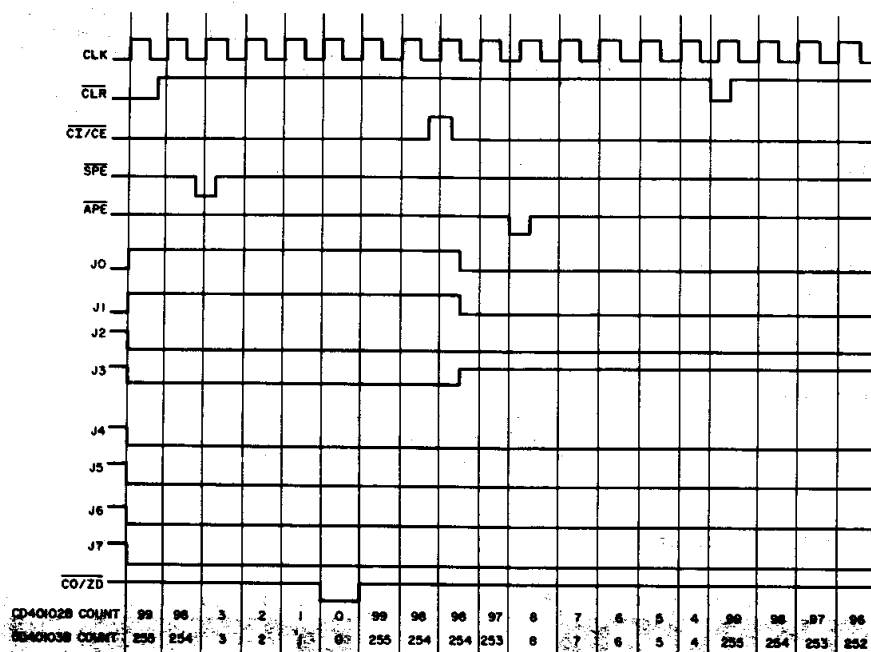
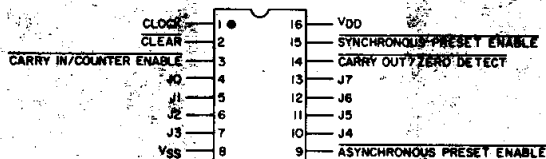


Fig. 15 - Timing diagram for CD40102B and CD40103B.



CD40102B,  
CD40103B  
TERMINAL ASSIGNMENT

## CD40102B, CD40103B Types

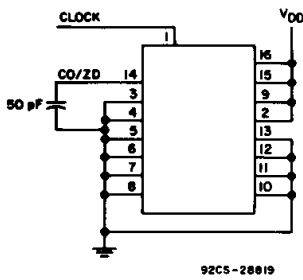


Fig. 16 - Maximum clock frequency test circuit.

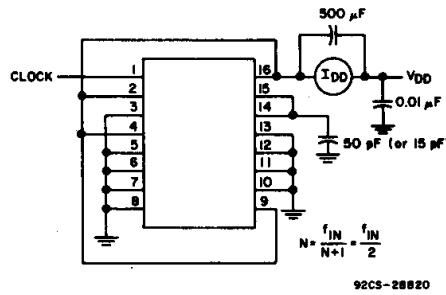


Fig. 17 - Dynamic power dissipation test circuit ( $\div 2$  mode).

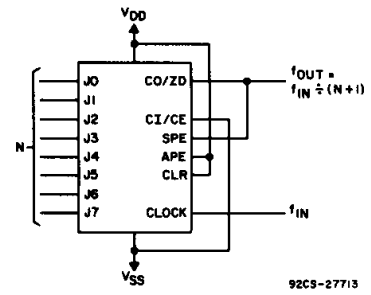


Fig. 18 - Divide-by-"N" counter.

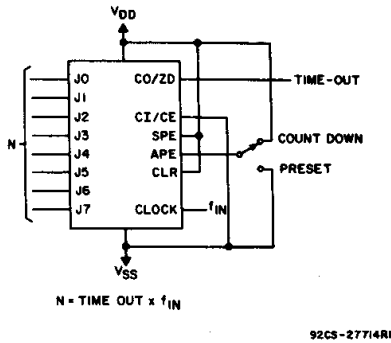


Fig. 19 - Programmable timer.

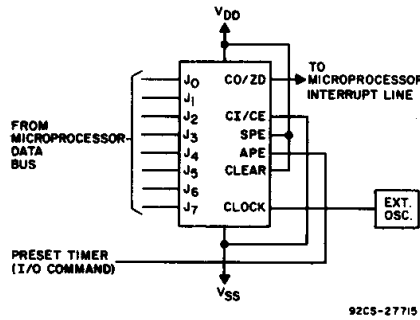
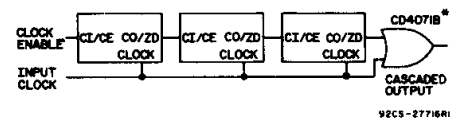


Fig. 20 - Microprocessor interrupt timer.



\* An output spike (160 ns @  $V_{DD} = 5$  V) occurs whenever two or more devices are cascaded in the parallel-clocked mode because the clock-to-carry out delay is greater than the carry-in-to-carry out delay. This spike is eliminated by gating the output of the last device with the clock as shown.

Fig. 21 - Synchronous cascading.

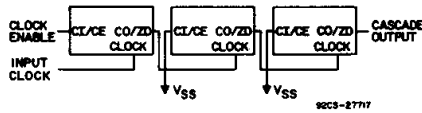
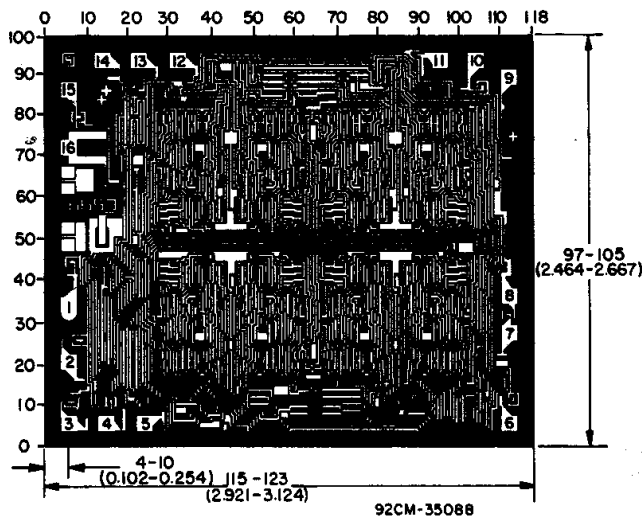


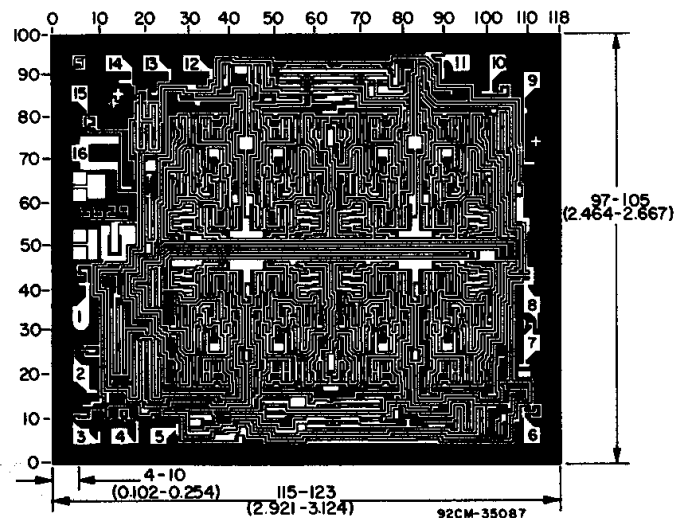
Fig. 22 - Ripple cascading.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

Dimensions and pad layout for CD40102B.



Dimensions and pad layout for CD40103B.



## PACKAGING INFORMATION

| Orderable part number       | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">CD40102BE</a>   | Active        | Production           | PDIP (N)   16   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD40102BE           |
| CD40102BE.A                 | Active        | Production           | PDIP (N)   16   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD40102BE           |
| <a href="#">CD40102BNSR</a> | Active        | Production           | SOP (NS)   16   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | CD40102B            |
| CD40102BNSR.A               | Active        | Production           | SOP (NS)   16   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | CD40102B            |
| <a href="#">CD40102BPW</a>  | Obsolete      | Production           | TSSOP (PW)   16 | -                     | -           | Call TI                              | Call TI                           | -55 to 125   | CM0102B             |
| <a href="#">CD40102BPWR</a> | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | CM0102B             |
| CD40102BPWR.A               | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | CM0102B             |
| <a href="#">CD40103BE</a>   | Active        | Production           | PDIP (N)   16   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD40103BE           |
| CD40103BE.A                 | Active        | Production           | PDIP (N)   16   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD40103BE           |
| CD40103BEE4                 | Active        | Production           | PDIP (N)   16   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -55 to 125   | CD40103BE           |
| <a href="#">CD40103BF</a>   | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD40103BF           |
| CD40103BF.A                 | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD40103BF           |
| <a href="#">CD40103BF3A</a> | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD40103BF3A         |
| CD40103BF3A.A               | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | CD40103BF3A         |
| <a href="#">CD40103BNSR</a> | Active        | Production           | SOP (NS)   16   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | CD40103B            |
| CD40103BNSR.A               | Active        | Production           | SOP (NS)   16   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | CD40103B            |
| <a href="#">CD40103BPW</a>  | Active        | Production           | TSSOP (PW)   16 | 90   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | CM0103B             |
| CD40103BPW.A                | Active        | Production           | TSSOP (PW)   16 | 90   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -55 to 125   | CM0103B             |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF CD40103B, CD40103B-MIL :**

- Catalog : [CD40103B](#)
- Military : [CD40103B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD40102BPWR | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| CD40103BNSR | SOP          | NS              | 16   | 2000 | 330.0              | 16.4               | 8.1     | 10.4    | 2.5     | 12.0    | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD40102BPWR | TSSOP        | PW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| CD40103BNSR | SOP          | NS              | 16   | 2000 | 353.0       | 353.0      | 32.0        |

**TUBE**


\*All dimensions are nominal

| Device       | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD40102BE    | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD40102BE    | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD40102BE.A  | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD40102BE.A  | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD40103BE    | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD40103BE    | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD40103BE.A  | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD40103BE.A  | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD40103BEE4  | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD40103BEE4  | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| CD40103BPW   | PW           | TSSOP        | 16   | 90  | 530    | 10.2   | 3600   | 3.5    |
| CD40103BPW.A | PW           | TSSOP        | 16   | 90  | 530    | 10.2   | 3600   | 3.5    |

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

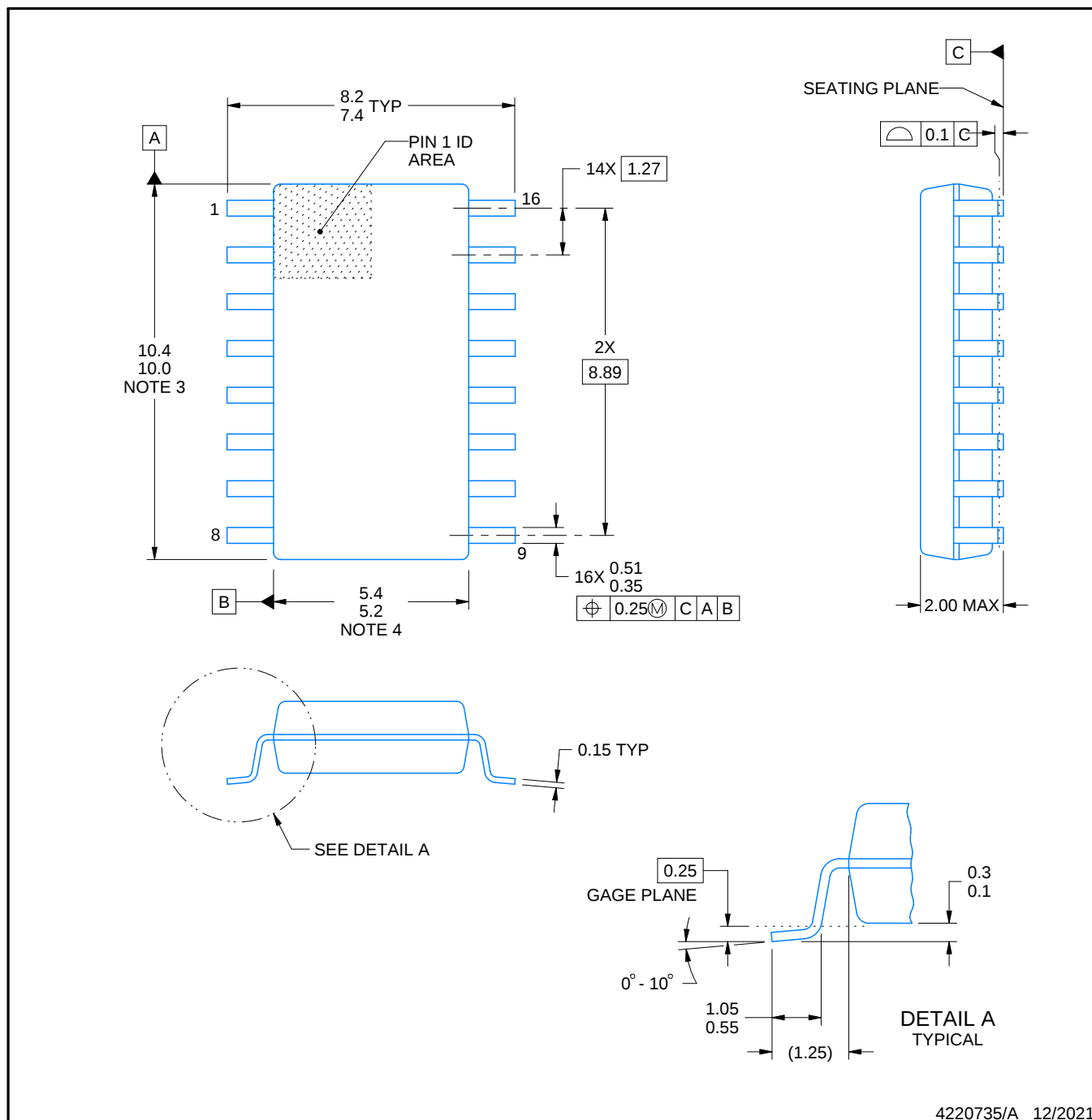


# PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.





SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

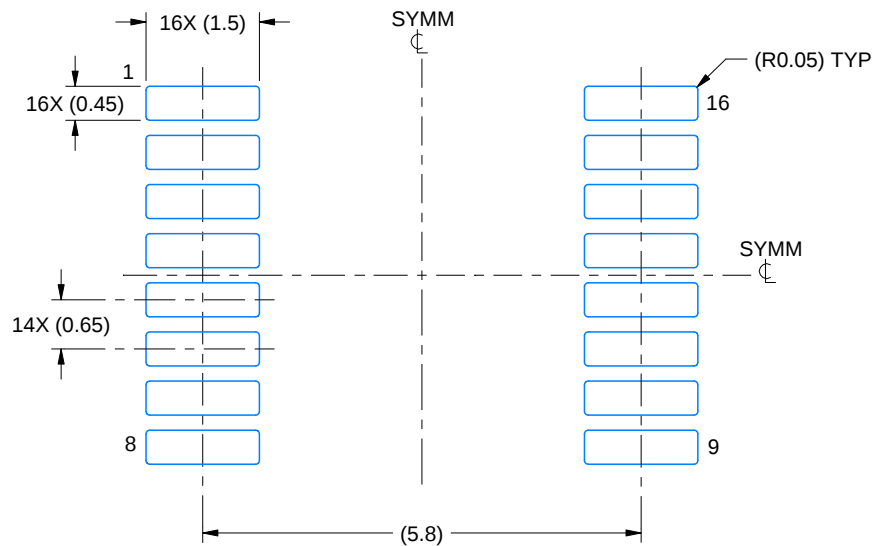


# EXAMPLE BOARD LAYOUT

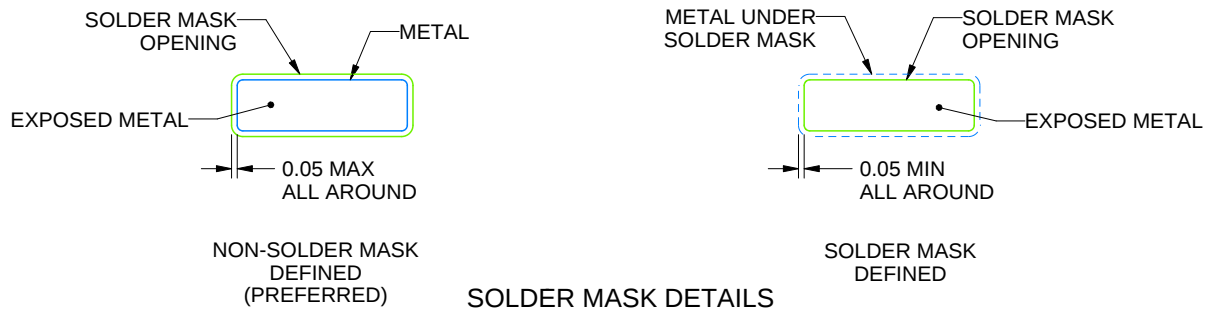
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

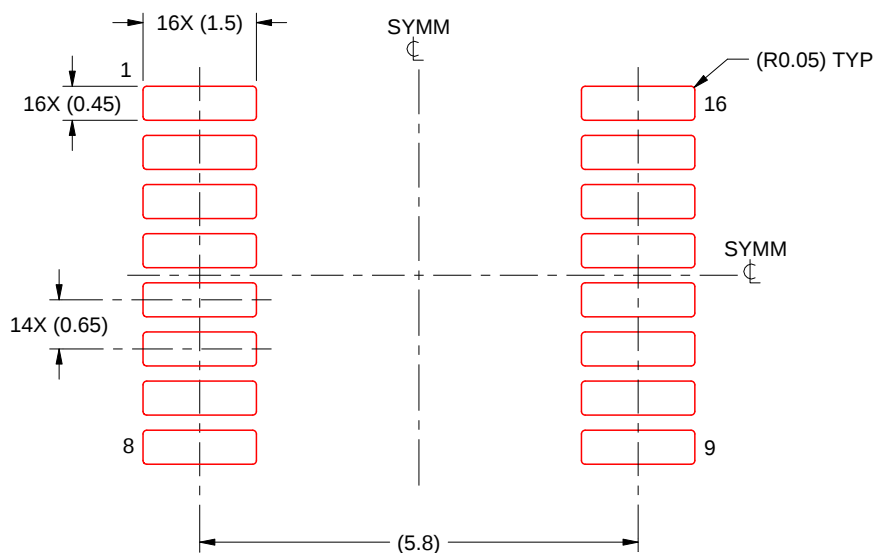
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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