bq24195 支持 5.1V/1A 和 5.1V/2.1A 同步升压操作的 I²C 控制 2.5A/4.5A 单节 USB/适配器充电器

1 特性

- 高效开关模式充电器
  - 2.5A (bq24195L) 或 4.5A (bq24195) 快速充电
  - 2A 充电电流下的充电效率达 92%；4A 充电电流下的充电效率达 90%
- 电池升压模式同步升压转换器
  - 5.1V/1A (bq24195L) 或 5.1V/2.1A (bq24195)
  - 5.1V/1A 条件下的升压效率达 94%；5.1V/2.1A 条件下的升压效率达 91%
- 借助 12mΩ 电池放电金属氧化物半导体场效应晶体管 (MOSFET) 实现最高电池放电效率，放电电流高达 9A
- 单输入 USB 兼容/适配器充电器
  - 与 USB 电池充电器技术规格 1.2 兼容的 USB 主机或充电端口 D+/D- 检测
  - 输入电压和电流限制支持 USB 2.0 和 USB 3.0
  - 输入电流限值：100mA、150mA、500mA、900mA、1.2A、1.5A、2A 和 3A
- 输入工作电压范围：3.9V 至 17V
  - 通过输入电压动态电源管理 (DPM) 调节功能支持所有类型的适配器
- 窄 VDC (NVDC) 电源路径管理
  - 与无电池或深度放电电池工作时可瞬时接通
  - 电池管理模式中的理想二极管运行
- 薄型电感的开关频率为 1.5MHz
- 具有或不具有主机管理的自主电池充电
  - 电池充电使能
  - 电池充电预调节
  - 充电终止和再充电
- 高精度（0°C 至 125°C）
  - 充电电压调节范围为 ±0.5%
  - 充电电流调节范围为 ±7%
  - 输入电流调节范围为 ±7.5%
  - 升压模式下输出调节范围 ±2%
- 高集成
  - 电源路径管理
  - 同步开关 MOSFET
  - 集成电流感测
  - 阴极负载二极管
  - 内部环路补偿
- 安全性
  - 电池温度感测和充电安全定时器
  - 热调节和热关断
  - 输入系统过压保护
  - MOSFET 过流保护
- 针对 LED 或主机处理器的充电状态输出
- 低电池泄漏电流并支持关闭模式
- 4.00mm x 4.00mm 四方扁平无引线 (QFN)-24 封装

2 应用

- 智能手机、平板电脑的移动电源
- 平板电脑和智能手机
- 便携式音频扬声器
- 便携式媒体播放器
- 互联网器件

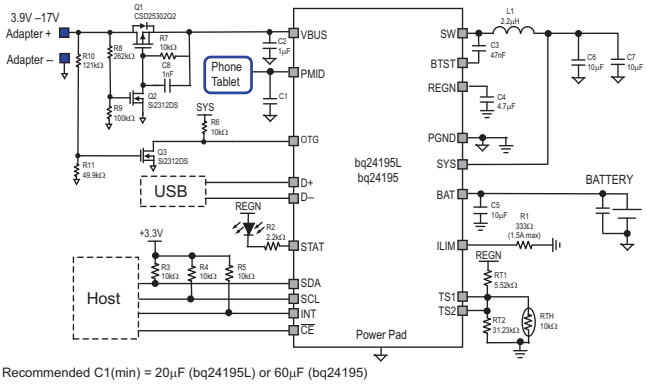
3 说明

bq24195L、bq24195 是高度集成的开关模式电池管理和系统电源路径管理器件，适用于各类移动电源、平板电脑和其他便携式设备的单节锂离子和锂聚合物电池。

器件信息(1)

产品型号	封装	封装尺寸（标称值）
bq24195	VQFN (24)	4.00mm x 4.00mm
bq24195L		

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。



Recommended C1(min) = 20µF (bq24195L) or 60µF (bq24195)

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4 修订历史记录

Changes from Original (October 2012) to Revision A **Page**

- 已添加 处理额定值表，特性 描述 部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分。 ... 1
- 已更改 V_{SLEEPZ}, $V_{BAT_DPL_HY}$, V_{BATGD} , I_{CHG_20pct}, V_{SHORT}, I_{ADPT_DPM}, K_{ILIM}, $V_{BTST_REFRESH}$ in Electrical Characteristics ... 6
- 已添加 –40°C to 85° to I_{BAT} Test Condition ... 6
- 已添加 REG00[6:3] = 0110 (4.36 V) or 1011 (4.76 V) to $V_{INDPM_REG_ACC}$ Test Conditions ... 8
- Added a MIN value of 435 to K_{ILIM} ... 8
- 已删除 $T_{Junction_REG}$ MIN and MAX ... 8
- 已更改 V_{OTG_ILIM} to I_{OTG_ILIM} ... 9
- 已更改 Functional Block Diagram ... 11
- 已更改 Charging Current in 表 3 ... 17
- 已更改 REG09[5:4] to REG08[5:4] in Charging Termination section ... 19
- 已更改 Charging Safety Timer description ... 20
- 已更改 Host Mode and Default Mode description ... 25
- 已更改 Charge Current Control Register REG02 Bit 0 description and note ... 29

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5 说明 （续）

它的低阻抗电源路径对开关模式运行效率进行了优化、减少了电池充电时间并延长了放电阶段的电池寿命。具有充电和系统设置的 I^2C 串行接口使得此器件成为一个真正地灵活解决方案。

此器件支持宽范围的输入源，其中包括标准 USB 主机端口，USB 充电端口和高功率 DC 适配器。为了设定缺省输入电流限值，bq24195L，bq24195 检测符合 USB 电池充电技术规格 1.2 的输入源。bq24195/bq24195L 符合带有输入电流和电压调节的 USB 2.0 和 USB 3.0 功率技术规格。bq24195L、bq24195 支持电池升压运行，在最小电流为 1.0A (bq24195L) 或 2.1A (bq24195) 时为 PMID 引脚提供 5.1V 电压。

电源路径管理将系统电压调节为稍稍高于电池电压，但是又不会下降到低于 3.5V 最小系统电压（可编程）。借助于这个特性，即使在电池电量完全耗尽或者电池被拆除时，系统也能保持运行。当达到输入电流限值或电压限值时，电源路径管理自动将充电电流减少为 0。随着系统负载持续增加，电源路径在满足系统电源需求之前将电池放电。这个补充模式运行防止输入源过载。

此器件在无需软件控制情况下启动并完成一个充电周期。它自动检测电池电压并通过三个阶段为电池充电：预充电、恒定电流和恒定电压。在充电周期的末尾，当充电电流低于在恒定电压阶段中预设定的限值时，充电器自动终止。当整个电池下降到低于再充电阈值时，充电器将自动启动另外一个充电周期。

此器件提供针对电池充电和系统运行的多种安全 特性， 其中包括负温度系数热敏电阻监控、充电安全定时器和过压/过流保护。当结温超过 120°C（可设定）时，热调节减少充电电流。

STAT 输出报告充电状态和任何故障条件。 当故障发生时，INT 会立即通知主机。

bq24195 和 bq24195L 采用 24 引脚、4.00mm x 4.00mm^2 超薄型四方扁平无引线 (VQFN) 封装。

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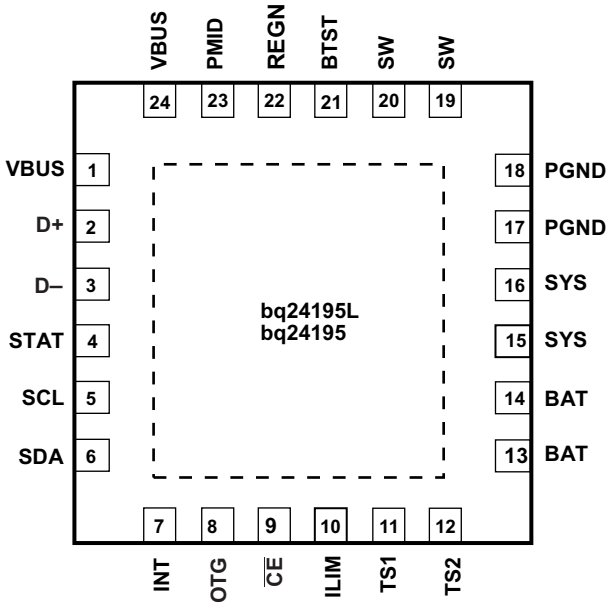
6 Pin Configuration and Functions

RGE Package
24-Pin VQFN With Exposed Thermal Pad
(Top View)



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
VBUS	1,24	P	Charger Input Voltage. The internal n-channel reverse block MOSFET (RBFET) is connected between VBUS and PMID with VBUS on source. Place a 1-µF ceramic capacitor from VBUS to PGND and place it as close as possible to IC. (Refer to Application Information Section for details)
D+	2	I Analog	Positive line of the USB data line pair. D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD) and primary detection in bc1.2.
D–	3	I Analog	Negative line of the USB data line pair. D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD) and primary detection in bc1.2.
STAT	4	O Digital	Open drain charge status output to indicate various charger operation. Connect to the pull up rail via 10-kΩ. LOW indicates charge in progress. HIGH indicates charge complete or charge disabled. When any fault condition occurs, STAT pin blinks at 1 Hz.
SCL	5	I Digital	I^2C Interface clock. Connect SCL to the logic rail through a 10-kΩ resistor.
SDA	6	I/O Digital	I^2C Interface data. Connect SDA to the logic rail through a 10-kΩ resistor.
INT	7	O Digital	Open-drain Interrupt Output. Connect the INT to a logic rail via 10-kΩ resistor. The INT pin sends active low, 256-us pulse to host to report charger device status and fault.
OTG	8	I Digital	USB current limit selection pin during buck mode, and active high enable pin during boost mode. In buck mode with USB host, when OTG = High, IIN limit = 500 mA and when OTG = Low, IIN limit = 100 mA. The boost mode is activated when the REG01[5:4] = 10 and OTG pin is High.
$\overline{CE}$	9	I Digital	Active low Charge Enable pin. Battery charging is enabled when REG01[5:4] = 01 and $\overline{CE}$ pin = Low. $\overline{CE}$ pin must be pulled high or low.
ILIM	10	I Analog	ILIM pin sets the maximum input current limit by regulating the ILIM voltage at 1 V. A resistor is connected from ILIM pin to ground to set the maximum limit as $I_{INMAX} = (1V/R_{ILIM}) \times 530$. The actual input current limit is the lower one set by ILIM and by I^2C REG00[2:0]. The minimum input current programmed on ILIM pin is 500 mA.
TS1	11	I Analog	Temperature qualification voltage input #1. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS1 to GND. Charge suspends when either TS pin is out of range. Recommend 103AT-2 thermistor. TS1 and TS2 pins have to be shorted together.
TS2	12	I Analog	Temperature qualification voltage input #2. TS1 and TS2 pins have to be shorted together.
BAT	13,14	P	Battery connection point to the positive terminal of the battery pack. The internal BATFET is connected between BAT and SYS. Connect a 10 µF closely to the BAT pin.

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Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
SYS	15,16	P	System connection point. The internal BATFET is connected between BAT and SYS. When the battery falls below the minimum system voltage, switch-mode converter keeps SYS above the minimum system voltage. (Refer to Application Information Section for inductor and capacitor selection.)
PGND	17,18	P	Power ground connection for high-current power converter node. Internally, PGND is connected to the source of the n-channel LSFET. On PCB layout, connect directly to ground connection of input and output capacitors of the charger. A single point connection is recommended between power PGND and the analog GND near the IC PGND pin.
SW	19,20	O Analog	Switching node connecting to output inductor. Internally SW is connected to the source of the n-channel HSFET and the drain of the n-channel LSFET. Connect the 0.047-µF bootstrap capacitor from SW to BTST.
BTST	21	P	PWM high side driver positive supply. Internally, the BTST is connected to the anode of the boost-strap diode. Connect the 0.047-µF bootstrap capacitor from SW to BTST.
REGN	22	P	PWM low side driver positive supply output. Internally, REGN is connected to the cathode of the boost-strap diode. Connect a 4.7-µF (10-V rating) ceramic capacitor from REGN to analog GND. The capacitor should be placed close to the IC. REGN also serves as bias rail of TS1 and TS2 pins.
PMID	23	P	Battery Boost Mode Output Voltage. Connected to the drain of the reverse blocking MOSFET and the drain of HSFET. The minimum capacitance required on PMID to PGND is 20 µF (bq24195L) or 60 µF (bq24195)
Thermal Pad	–	P	Exposed pad beneath the IC for heat dissipation. Always solder thermal pad to the board, and have vias on the thermal pad plane star-connecting to PGND and ground plane for high-current power converter.

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage range (with respect to GND)	VBUS	–2	22	V
	PMID	–0.3	22	V
	STAT,	–0.3	20	V
	BTST	–0.3	26	V
	SW	–2	20	V
	BAT, SYS (converter not switching)	–0.3	6	V
	SDA, SCL, INT, OTG, ILIM, REGN, TS1, TS2, $\overline{CE}$, D+, D–	–0.3	7	V
	BTST TO SW	–0.3	–7	V
	PGND to GND	–0.3	–0.3	V
Output sink current	INT, STAT		6	mA
Junction temperature		–40°C	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{IN}	Input voltage	3.9	17(1)	V

(1) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on either the BTST or SW pins. A tight layout minimizes switching noise.

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Recommended Operating Conditions (continued)

		MIN	MAX	UNIT
I_{IN}	Input current		3	A
I_{SYS}	Output current (SYS)		4.5 (bq24195) 2.5 (bq24195L)	A
V_{BAT}	Battery voltage		4.4	V
I_{BAT}	Fast charging current		4.5 (bq24195) 2.5 (bq24195L)	A
	Discharging current with internal MOSFET		6 continuous 9 peak (up to 1 sec duration)	A
T_A	Operating free-air temperature range	–40	85	°C

7.4 Thermal Information

THERMAL METRIC(1)		bq24195	UNIT
		RGE (24 PIN)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.2	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	29.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	9.1	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	9.1	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	2.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

$V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values unless other noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
I_{BAT}	Battery discharge current (BAT, SW, SYS)	$V_{VBUS} < V_{UVLO}$, VBAT = 4.2 V, leakage between BAT and VBUS			5	µA
		High-Z Mode, or no VBUS, BATFET disabled (REG07[5] = 1), –40°C to 85°C		12	20	µA
		High-Z Mode, or no VBUS, REG07[5] = 0, –40°C to 85°C		32	55	µA
I_{VBUS}	Input supply current (VBUS)	V_{VBUS} = 5 V, High-Z mode		15	30	µA
		V_{VBUS} = 17 V, High-Z mode		30	50	µA
		$V_{VBUS} > V_{UVLO}$, $V_{VBUS} > V_{BAT}$, converter not switching		1.5	3	mA
		$V_{VBUS} > V_{UVLO}$, $V_{VBUS} > V_{BAT}$, converter switching, V_{BAT} = 3.2 V, I_{SYS} = 0 A		4		mA
		$V_{VBUS} > V_{UVLO}$, $V_{VBUS} > V_{BAT}$, converter switching, V_{BAT} = 3.8 V, I_{SYS} = 0 A		15		mA
I_{BOOST}	Battery discharge current in boost mode	VBAT = 4.2 V, Boost mode, I_{PMID} = 0 A, converter switching		15		mA
VBUS/BAT POWER UP						
V_{VBUS_OP}	VBUS operating range		3.9		17	V
V_{VBUS_UVLOZ}	VBUS for active I^2C, no battery	V_{VBUS} rising	3.6			V
V_{SLEEP}	Sleep mode falling threshold	V_{VBUS} falling, $V_{VBUS-VBAT}$	35	80	120	mV
V_{SLEEPZ}	Sleep mode rising threshold	V_{VBUS} rising, $V_{VBUS-VBAT}$	170	250	350	mV
V_{ACOV}	VBUS over-voltage rising threshold	V_{VBUS} rising	17.4	18		V
V_{ACOV_HYST}	VBUS over-voltage falling hysteresis	V_{VBUS} falling		700		mV
V_{BAT_UVLOZ}	Battery for active I^2C, no VBUS	V_{BAT} rising	2.3			V
V_{BAT_DPL}	Battery depletion threshold	V_{BAT} falling		2.4	2.6	V

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Electrical Characteristics (接下页)

$V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values unless other noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{BAT_DPL_HY}$	Battery depletion rising hysteresis	V_{BAT} rising		170	260	mV
$V_{VBUSMIN}$	Bad adapter detection threshold	V_{VBUS} falling		3.8		V
I_{BADSRC}	Bad adapter detection current source			30		mA
t_{BADSRC}	Bad source detection duration			30		ms
POWER PATH MANAGEMENT						
V_{SYS_RANGE}	Typical system regulation voltage	Isys = 0 A, Q4 off, V_{BAT} up to 4.2 V, REG01[3:1] = 101, V_{SYSMIN} = 3.5 V	3.5		4.35	V
V_{SYS_MIN}	System voltage output	REG01[3:1] = 101, V_{SYSMIN} = 3.5 V	3.55	3.65		V
$R_{ON(RBFET)}$	Internal top reverse blocking MOSFET on-resistance	Measured between VBUS and PMID		23	38	mΩ
$R_{ON(HSFET)}$	Internal top switching MOSFET on-resistance between PMID and SW	T_J = –40°C to 85°C		30	38	mΩ
		T_J = -40°C to 125°C		30	48	
$R_{ON(LSFET)}$	Internal bottom switching MOSFET on-resistance between SW and PGND	T_J = –40°C to 85°C		35	48	mΩ
		T_J = -40°C to 125°C		35	51	
V_{FWD}	BATFET forward voltage in supplement mode	BAT discharge current 10 mA		30		mV
V_{SYS_BAT}	SYS/BAT Comparator	V_{SYS} falling		90		mV
V_{BATGD}	Battery good comparator rising threshold	V_{BAT} rising		3.55		V
V_{BATGD_HYST}	Battery good comparator falling threshold	V_{BAT} falling		100		mV
BATTERY CHARGER						
$V_{BAT_REG_ACC}$	Charge voltage regulation accuracy	V_{BAT} = 4.208 V	–0.5%		0.5%	
$I_{ICHG_REG_ACC}$	Fast charge current regulation accuracy	V_{BAT} = 3.8 V, I_{CHG} = 1792 mA, T_J = 25°C	–4%		4%	
		V_{BAT} = 3.8 V, I_{CHG} = 1792 mA, T_J = –20°C to 125°C	–7%		7%	
I_{CHG_20pct}	Charge current with 20% option on	V_{BAT} = 3.1 V, I_{CHG} = 104 mA, REG02 = 03	75	100	150	mA
$V_{BATLOWV}$	Battery LOWV falling threshold	Fast charge to precharge, REG04[1] = 1	2.6	2.8	2.9	V
$V_{BATLOWV_HYST}$	Battery LOWV rising threshold	Precharge to fast charge, REG04[1] = 1	2.8	3.0	3.1	V
I_{PRECHG_ACC}	Precharge current regulation accuracy	VBAT = 2.6 V, I_{CHG} = 256 mA	–20%		20%	
I_{TERM_ACC}	Termination current accuracy	I_{TERM} = 256 mA, I_{CHG} = 960 mA	–20%		20%	
V_{SHORT}	Battery Short Voltage	VBAT falling		2.0		V
V_{SHORT_HYST}	Battery Short Voltage hysteresis	VBAT rising		200		mV
I_{SHORT}	Battery short current	VBAT < 2.2V		100		mA
V_{RECHG}	Recharge threshold below VBAT_REG	VBAT falling, REG04[0] = 0		100		mV
t_{RECHG}	Recharge deglitch time	VBAT falling, REG04[0] = 0		20		ms
R_{ON_BATFET}	SYS-BAT MOSFET on-resistance	T_J = 25°C		12	15	mΩ
		T_J = –40°C to 125°C		12	20	

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Electrical Characteristics (接下页)

$V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values unless other noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE/CURRENT REGULATION						
$V_{INDPM_REG_ACC}$	Input voltage regulation accuracy	REG00[6:3] = 0110 (4.36 V) or 1011 (4.76 V)	–2%		2%	
I_{USB_DPM}	USB Input current regulation limit, VBUS = 5 V, current pulled from SW	USB100	85		100	mA
		USB150	125		150	mA
		USB500	440		500	mA
		USB900	750		900	mA
I_{ADPT_DPM}	Input current regulation accuracy		1.35	1.5	1.65	A
I_{IN_START}	Input current limit during system start up	VSYS < 2.2 V		100		mA
K_{ILIM}	$I_{IN} = K_{ILIM}/R_{ILIM}$	IINDPM = 1.5 A	435	485	530	A x Ω
D+/D- DETECTION						
V_{D+_SRC}	D+ voltage source		0.5	0.6	0.7	V
I_{D+_SRC}	D+ connection check current source		7		14	µA
I_{D-_SINK}	D– current sink		50	100	150	µA
I_{D_LKG}	Leakage current into D+/D–	D–, switch open	–1		1	µA
		D+, switch open	–1		1	µA
V_{D+_LOW}	D+ Low comparator threshold		0.7		0.8	V
$V_{D-_LOWdatref}$	D– Low comparator threshold		250		400	mV
R_{D-_DWN}	D– Pulldown for connection check		14.25		24.8	kΩ
$t_{SDP_DEFAULT}$	Charging timer with 100-mA USB host in default mode				45	mins
BAT OVER-VOLTAGE PROTECTION						
V_{BATOVP}	Battery over-voltage threshold	V_{BAT} rising, as percentage of V_{BAT_REG}		104%		
V_{BATOVP_HYST}	Battery over-voltage hysteresis	V_{BAT} falling, as percentage of V_{BAT_REG}		2%		
t_{BATOVP}	Battery over-voltage deglitch time to disable charge			1		µs
THERMAL REGULATION AND THERMAL SHUTDOWN						
$T_{Junction_REG}$	Junction temperature regulation accuracy	REG06[1:0] = 11		120		°C
T_{SHUT}	Thermal shutdown rising temperature	Temperature increasing		160		°C
T_{SHUT_HYS}	Thermal shutdown hysteresis			30		°C
	Thermal shutdown rising deglitch	Temperature increasing delay		1		ms
	Thermal shutdown falling deglitch	Temperature decreasing delay		1		ms
COLD/HOT THERMISTER COMPARATOR						
V_{LTF}	Cold temperature threshold, TS pin voltage rising threshold	Charger suspends charge. As percentage to V_{REGN}	73%	73.5 %	74%	
V_{LTF_HYS}	Cold temperature hysteresis, TS pin voltage falling	As percentage to V_{REGN}	0.2%	0.4%	0.6%	
V_{HTF}	Hot temperature TS pin voltage threshold	As percentage to V_{REGN}	46.6%	47.2 %	48.8%	
V_{TCO}	Cut-off temperature TS pin voltage falling threshold	As percentage to V_{REGN}	44.2%	44.7 %	45.2%	
	Deglitch time for temperature out of range detection	$V_{TS} > V_{LTF}$, or $V_{TS} < V_{TCO}$, or $V_{TS} < V_{HTF}$		10		ms
CHARGE OVER-CURRENT COMPARATOR						
I_{HSFET_OCP}	HSFET over-current threshold		5.3	7		A
I_{BATFET_OCP}	System over load threshold		9			A
CHARGE UNDER-CURRENT COMPARATOR (CYCLE-BY-CYCLE)						
V_{LSFET_UCP}	LSFET charge under-current falling threshold	From sync mode to non-sync mode		100		mA
PWM OPERATION						
F_{SW}	PWM Switching frequency, and digital clock		1300	1500	1700	kHz
D_{MAX}	Maximum PWM duty cycle			97%		

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Electrical Characteristics (接下页)

$V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to 125°C and T_J = 25°C for typical values unless other noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{BTST_REFRESH}$	Bootstrap refresh comparator threshold	VBTST-VSW when LSFET refresh pulse is requested, VBUS = 5 V		3.6		V
		VBTST-VSW when LSFET refresh pulse is requested, VBUS > 6 V		4.5		
BOOST MODE OPERATION						
V_{OTG_REG}	Boost mode output voltage	I(PMID) = 0		5.12		V
$V_{OTG_REG_ACC}$	Boost mode output voltage accuracy	I(PMID) = 0	–2%		2%	
I_{OTG}	Boost mode output current on PMID	bq24195L	1.0			A
		bq24195	2.1			A
V_{OTG_BAT}	Battery operating voltage for boost mode	bq24195L	3.0			V
		bq24195	3.2			V
I_{OTG_ILIM}	LSFET cycle-by-cycle current limit	bq24195L	2.76	3.8		A
		bq24195	4.83	6.5		A
REGN LDO						
V_{REGN}	REGN LDO output voltage	V_{VBUS} = 10 V, I_{REGN} = 40 mA	5.6	6	6.4	V
		V_{VBUS} = 5 V, I_{REGN} = 20 mA	4.75	4.8		V
I_{REGN}	REGN LDO current limit	V_{VBUS} = 10 V, V_{REGN} = 3.8 V	50			mA
LOGIC I/O PIN CHARACTERISTICS (OTG, $\overline{CE}$, STAT)						
V_{ILO}	Input low threshold				0.4	V
V_{IH}	Input high threshold		1.3			V
V_{OUT_LO}	Output low saturation voltage	Sink current = 5 mA			0.4	V
I_{BIAS}	High level leakage current	Pull up rail 1.8 V			1	µA
I^2C INTERFACE (SDA, SCL, INT)						
V_{IH}	Input high threshold level	VPULL-UP = 1.8 V, SDA and SCL	1.3			V
V_{IL}	Input low threshold level	VPULL-UP = 1.8 V, SDA and SCL			0.4	V
V_{OL}	Output low threshold level	Sink current = 5 mA			0.4	V
I_{BIAS}	High-level leakage current	VPULL-UP = 1.8 V, SDA and SCL			1	µA
f_{SCL}	SCL clock frequency				400	kHz
DIGITAL CLOCK AND WATCHDOG TIMER						
f_{HIZ}	Digital crude clock	REGN LDO disabled	15	35	50	kHz
f_{DIG}	Digital clock	REGN LDO enabled	1300	1500	1700	kHz
t_{WDT}	REG05[5:4] = 11	REGN LDO enabled	136	160		sec

7.6 Typical Characteristics

表 1. Table of Figures

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Boost Mode Efficiency vs PMID Load Current	图 2
Boost Mode PMID Voltage Regulation vs PMID Load Current	图 3
BAT Voltage vs Temperature	图 4
Input Current Limit vs Temperature	图 5
Charge Current vs Temperature	图 6

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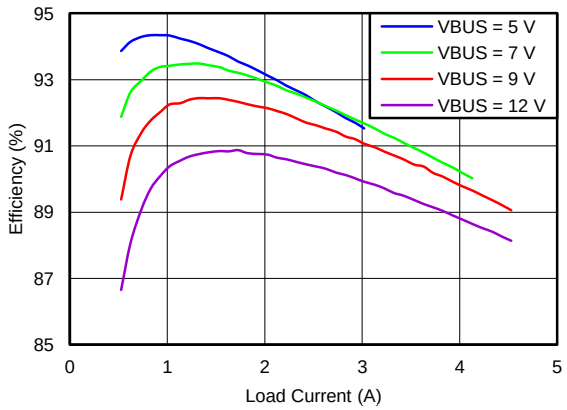

图 1. Charging Efficiency vs Charging Current

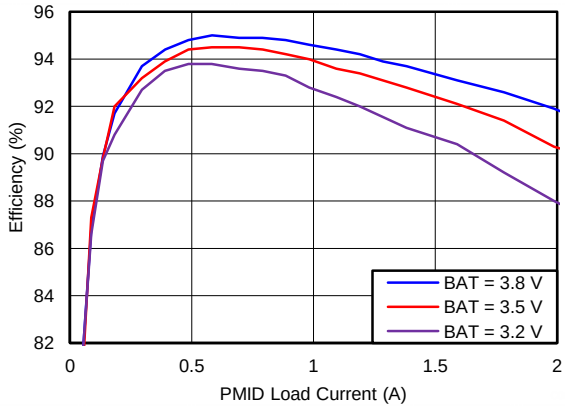

图 2. Boost Mode Efficiency vs PMID Load Current

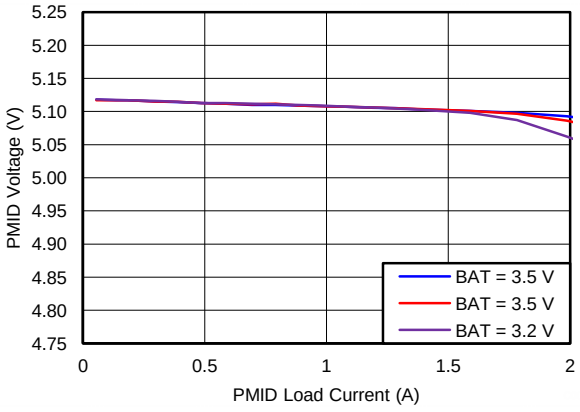

图 3. Boost Mode PMID Voltage Regulation vs PMID Load Current

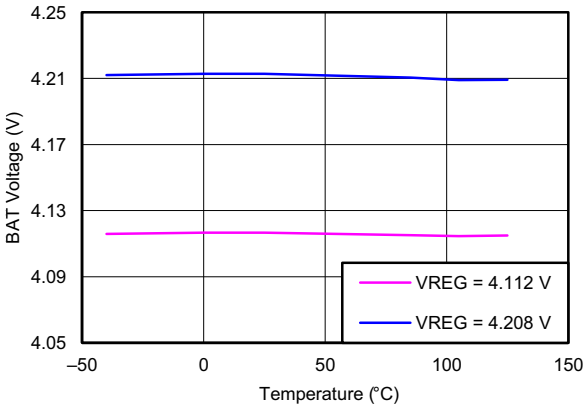

图 4. BAT Voltage vs Temperature

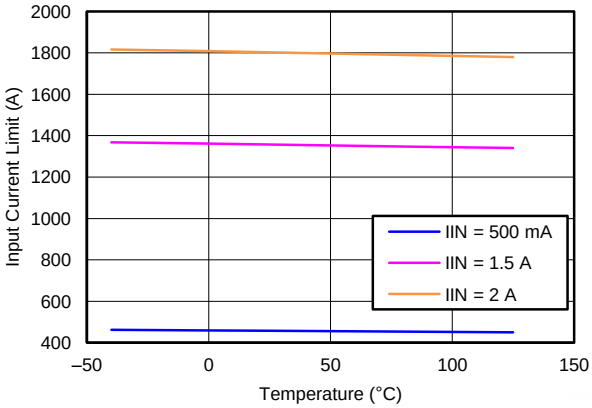

图 5. Input Current Limit vs Temperature

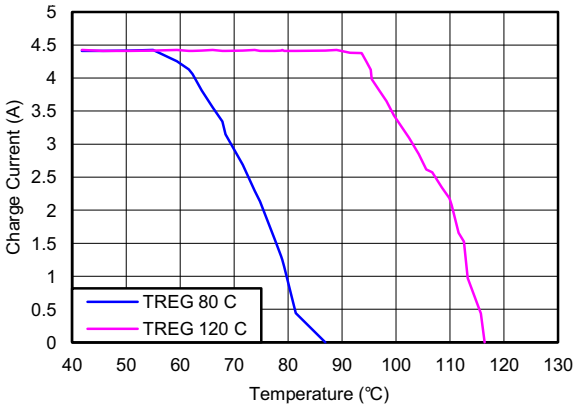

图 6. Charge Current vs Temperature

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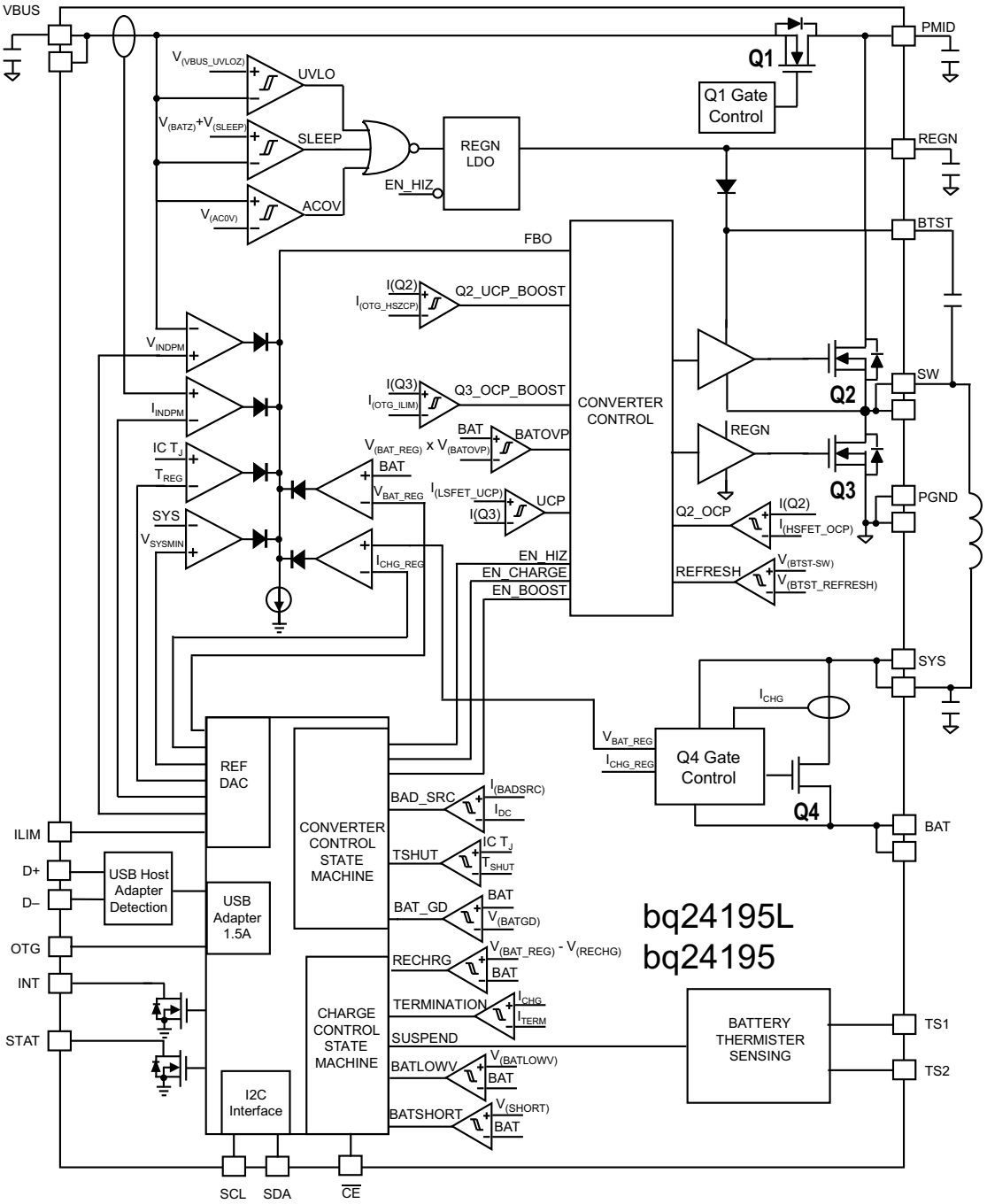
8 Detailed Description

8.1 Overview

The bq24195L, bq24195 is an I²C controlled power path management device and a single cell Li-Ion battery charger. It integrates the input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and BATFET (Q4) between system and battery. The device also integrates the bootstrap diode for the high-side gate drive.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Device Power Up

8.3.1.1 Power-On-Reset (POR)

The internal bias circuits are powered from the higher voltage of VBUS and BAT. When VBUS or VBAT rises above UVLOZ, the sleep comparator, battery depletion comparator and BATFET driver are active. I^2C interface is ready for communication and all the registers are reset to default value. The host can access all the registers after POR.

8.3.1.2 Power Up from Battery without DC Source

If only battery is present and the voltage is above depletion threshold (V_{BAT_DEPL}), the BATFET turns on and connects battery to system. The REGN LDO stays off to minimize the quiescent current. The low R_{DSON} in BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time. The device always monitors the discharge current through BATFET. When the system is overloaded or shorted, the device will immediately turn off BATFET and keep BATFET off until the input source plugs in again.

8.3.1.2.1 BATFET Turn Off

The BATFET can be forced off by the host through I^2C REG07[5]. This bit allows the user to independently turn off the BATFET when the battery condition becomes abnormal during charging. When BATFET is off, there is no path to charge or discharge the battery.

When battery is not attached, the BATFET should be turned off by setting REG07[5] to 1 to disable charging and supplement mode.

8.3.1.2.2 Shipping Mode

When end equipment is assembled, the system is connected to battery through BATFET. There will be a small leakage current to discharge the battery even when the system is powered off. In order to extend the battery life during shipping and storage, the device can turn off BATFET so that the system voltage is zero to minimize the leakage.

In order to keep BATFET off during shipping mode, the host has to disable the watchdog timer (REG05[5:4] = 00) and disable BATFET (REG07[5] = 1) at the same time.

Once the BATFET is disabled, the BATFET can be turned on by plugging in adapter.

8.3.1.3 Power Up from DC Source

When the DC source plugs in, the bq24195L, bq24195 checks the input source voltage to turn on REGN LDO and all the bias circuits. It also checks the input current limit before starts the buck converter.

8.3.1.3.1 REGN LDO

The REGN LDO supplies internal bias circuits as well as the HSFET and LSFET gate drive. The LDO also provides bias rail to TS1/TS2 external resistors. The pull-up rail of STAT can be connected to REGN as well.

The REGN is enabled when all the conditions are valid.

1. VBUS above UVLOZ
2. VBUS above battery + V_{SLEEPZ} in buck mode or VBUS below battery + V_{SLEEPZ} in boost mode
3. After typical 220ms delay (100ms minimum) is complete

If one of the above conditions is not valid, the device is in high impedance mode (HIZ) with REGN LDO off. The device draws less than 50 µA from VBUS during HIZ state. The battery powers up the system when the device is in HIZ.

8.3.1.3.2 Input Source Qualification

After REGN LDO powers up, the bq24195L, bq24195 checks the current capability of the input source. The input source has to meet the following requirements to start the buck converter.

1. VBUS voltage below 18 V (not in ACOV)

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Feature Description (接下页)

2. VBUS voltage above 3.8 V when pulling 30 mA (poor source detection)

Once the input source passes all the conditions above, the status register REG08[2] goes high. An INT is asserted to the host.

If the device fails the poor source detection, it will repeat the detection every 2 seconds.

8.3.1.3.3 Input Current Limit Detection

The USB ports on personal computers are convenient charging source for portable devices (PDs). If the portable device is attached to a USB host, the USB specification requires the portable device to draw limited current (100 mA/500 mA in USB 2.0, and 150 mA/900 mA in USB 3.0). If the portable device is attached to a charging port, it is allowed to draw up to 1.5 A.

After REG08[2] goes HIGH, the charger device always runs input current limit detection when a DC source plugs in unless the charger is in HIZ during host mode.

The bq24195L, bq24195 follows battery charging specification 1.2 (bc1.2) to detect input source through USB D+/D– lines. After the input current limit detection is done, the host can write to REG00[2:0] to change the input current limit.

8.3.1.3.4 D+/D– Detection Sets Input Current Limit

The bq24195L, bq24195 contains a D+/D– based input source detection to program the input current limit. The D+/D- detection has two steps: data contact detect (DCD) followed by primary detection.

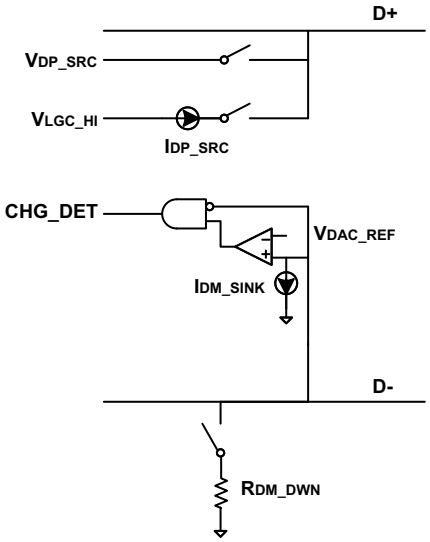

图 7. USB D+/D- Detection

DCD (Data Contact Detection) uses a current source to detect when the D+/D– pins have made contact during an attach event. The protocol for data contact detect is as follows:

- Detect VBUS present and REG08[2] = 1 (power good)
- Turn on D+ I_{DP_SRC} and the D– pull-down resistor R_{DM_DWN} for 40 ms
- If the USB connector is properly attached, the D+ line goes from HIGH to LOW, wait up to 0.5 sec.
- Turn off I_{DP_SRC} and disconnect R_{DM_DWN}

The primary detection is used to distinguish between USB host (Standard Down Stream Port, or SDP) and different type of charging ports (Charging Down Stream Port, or CDP, and Dedicated Charging Port, or DCP). The protocol for primary detection is as follows:

- Turn on V_{DP_SRC} on D+ and I_{DM_SINK} on D– for 40 ms
- If PD is attached to a USB host (SDP), the D– is low. If PD is attached to a charging port (CDP or DCP), the D– is high

Feature Description (接下页)

- Turn off V_{DP_SRC} and I_{DM_SINK}

表 2 shows the input current limit setting after D+/D– detection.

表 2. bq24195L, bq24195 USB D+/D– Detection

D+/D– DETECTION	OTG	INPUT CURRENT LIMIT	REG08[7:6]
0.5 sec timer expired in DCD (D+/D- floating)	—	100 mA	00
USB host	LOW	100 mA	01
USB host	HIGH	500 mA	01
Charging port	—	1.5 A	10

8.3.1.3.5 HIZ State wth 100mA USB Host

In battery charging spec, the good battery threshold is the minimum charge level of a battery to power up the portable device successfully. When the input source is 100-mA USB host, and the battery is above bat-good threshold (V_{BATGD}), the device follows battery charging spec and enters high impedance state (HIZ). In HIZ state, the device is in the lowest quiescent state with REGN LDO and the bias circuits off. The charger device sets REG00[7] to 1, and the VBUS current during HIZ state will be less than 30 µA. The system is supplied by the battery.

Once the charger device enters HIZ state in host mode, it stays in HIZ until the host writes REG00[7] = 0. When the processor host wakes up, it is recommended to first check if the charger is in HIZ state.

In default mode, the charger IC will reset REG00[7] back to 0 when input source is removed. When another source plugs in, the charger IC will run detection again, and update the input current limit.

8.3.1.3.6 Force Input Current Limit Detection

The host can force the charger device to run input current limit detection by setting REG07[7] = 1. After the detection is complete, REG07[7] will return to 0 by itself.

8.3.1.4 Converter Power-Up

After the input current limit is set, the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, BATFET turns off. Otherwise, BATFET stays on to charge the battery.

The bq24195L, bq24195 provides soft-start when ramp up the system rail. When the system rail is below 2.2 V, the input current limit is forced to 100 mA. After the system rises above 2.2 V, the charger device sets the input current limit set by the lower value between register and ILIM pin.

As a battery charger, the bq24195L, bq24195 deploys a 1.5-MHz step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

A type III compensation network allows using ceramic capacitors at the output of the converter. An internal saw-tooth ramp is compared to the internal error control signal to vary the duty cycle of the converter. The ramp height is proportional to the PMID voltage to cancel out any loop gain variation due to a change in input voltage.

In order to improve light-load efficiency, the device switches to PFM control at light load when battery is below minimum system voltage setting or charging is disabled. During the PFM operation, the switching duty cycle is set by the ratio of SYS and VBUS.

8.3.1.5 Boost Mode Operation from Battery

The bq24195L, bq24195 supports boost converter operation to deliver power from the battery to other portable devices through USB port. The boost mode output current rating meets the 1 A (bq24195L) or 2.1 A (bq24195) charging requirements for smartphone and tablet. The boost operation can be enabled if the following conditions are valid:

1. BAT above BATLOWV threshold ($V_{BATLOWV}$ set by REG04[1])
2. VBUS less than BAT+V_{SLEEP} (in sleep mode)

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3. Boost mode operation is enabled (OTG pin HIGH and REG01[5:4] = 10)
4. After 220-ms delay from boost mode enable

In battery boost mode, the bq24195L, bq24195 employs a 1.5-MHz step-up switching regulator. During boost mode, the status register REG08[7:6] is set to 11, the PMID output voltage is 5.1 V.

For power bank applications, the boost current is supported from PMID pin as in the application diagram. It is recommended to use the minimum PMID cap value 20 µF (bq24195L) or 60 µF (bq24195) for boost current. Please note that there is no boost current limit setting when the boost current is sourced from PMID pin, hence it is important not to overload the boost current under this condition.

8.3.2 Power Path Management

The bq24195L, bq24195 accommodates a wide range of input sources from USB, wall adapter, to car battery. The device provides automatic power path selection to supply the system (SYS) from input source (VBUS), battery (BAT), or both.

8.3.2.1 Narrow VDC Architecture

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by REG01[3:1]. Even with a fully depleted battery, the system is regulated above the minimum system voltage (default 3.5 V).

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is 150 mV above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, BATFET is fully on and the voltage difference between the system and battery is the V_{DS} of BATFET.

When the battery charging is disabled or terminated, the system is always regulated at 150 mV above the minimum system voltage setting. The status register REG08[0] goes high when the system is in minimum system voltage regulation.

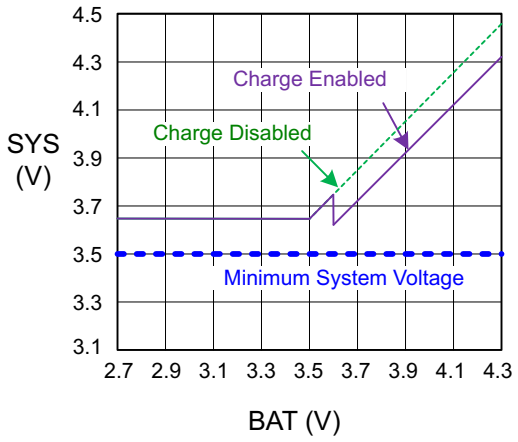

图 8. V(SYS) vs V(BAT)

8.3.2.2 Dynamic Power Management

To meet maximum current limit in USB spec and avoid over loading the adapter, the bq24195L, bq24195 features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage.

When input source is over-loaded, either the current exceeds the input current limit (REG00[2:0]) or the voltage falls below the input voltage limit (REG00[6:3]). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters the supplement mode where the BATFET turns on and battery starts discharging so that the system is supported from both the input source and battery.

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During DPM mode (either VINDPM or IINDPM), the status register REG08[3] will go high.

图 9 shows the DPM response with 9-V/1.2-A adapter, 3.2-V battery, 2.8-A charge current and 3.4-V minimum system voltage setting.

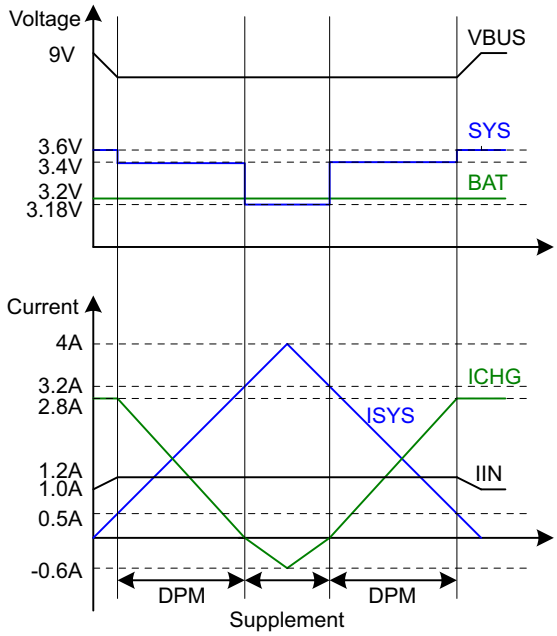

图 9. DPM Response

8.3.2.3 Supplement Mode

When the system voltage falls below the battery voltage, the BATFET turns on and the BATFET gate is regulated the gate drive of BATFET so that the minimum BATFET V_{DS} stays at 30 mV when the current is low. This prevents oscillation from entering and exiting the supplement mode. As the discharge current increases, the BATFET gate is regulated with a higher voltage to reduce R_{DSON} until the BATFET is in full conduction. At this point onwards, the BATFET V_{DS} linearly increases with discharge current. 图 10 shows the V-I curve of the BATFET gate regulation operation. BATFET turns off to exit supplement mode when the battery is below battery depletion threshold.

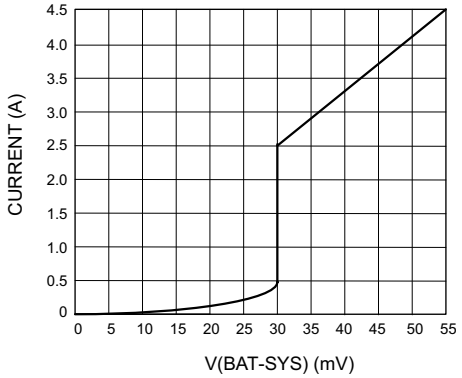

图 10. BATFET V-I Curve

8.3.3 Battery Charging Management

The bq24195L, bq24195 charges 1-cell Li-Ion battery with up to 2.5A/4.5A charge current for high capacity tablet battery. The 12-mΩ BATFET improves charging efficiency and minimizes the voltage drop during discharging.

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8.3.3.1 Autonomous Charging Cycle

With battery charging enabled at POR (REG01[5:4] = 01), the bq24195L, bq24195 can complete a charging cycle without host involvement. The device default charging parameters are listed in .

表 3. Charging Parameter Default Setting

DEFAULT MODE	bq24195L, bq24195
Charging voltage	4.208 V
Charging current	2.048 A
Pre-charge current	256 mA
Termination current	256 mA
Temperature profile	Hot/Cold
Safety timer	8 hours

A new charge cycle starts when the following conditions are valid:

- Converter starts
- Battery charging is enabled by I^2C register bit (REG01[5:4]) = 01 and $\overline{CE}$ is low
- No thermistor fault on TS1 and TS2
- No safety timer fault
- BATFET is not forced to turn off (REG07[5])

The charger device automatically terminates the charging cycle when the charging current is below termination threshold and charge voltage is above recharge threshold. When a full battery voltage is discharged below recharge threshold (REG04[0]), the bq24195L, bq24195 automatically starts another charging cycle.

The STAT output indicates the charging status of charging (LOW), charging complete or charge disable (HIGH) or charging fault (Blinking). The status register REG08[5:4] indicates the different charging phases: 00-charging disable, 01-precharge, 10-fast charge (constant current) and constant voltage mode, 11-charging done. Once a charging cycle is complete, an INT is asserted to notify the host.

The host can always control the charging operation and optimize the charging parameters by writing to the registers through I^2C.

8.3.3.2 Battery Charging Profile

The device charges the battery in three phases: preconditioning, constant current and constant voltage. At the beginning of a charging cycle, the device checks the battery voltage and applies current.

表 4. Charging Current Setting

VBAT	CHARGING CURRENT	REG DEFAULT SETTING	REG08[5:4]
< 2 V	100 mA	–	01
2 V - 3 V	REG03[7:4]	256 mA	01
> 3 V	REG02[7:2]	2048 mA	10

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If the charger device is in DPM regulation or thermal regulation during charging, the actual charging current will be less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate.

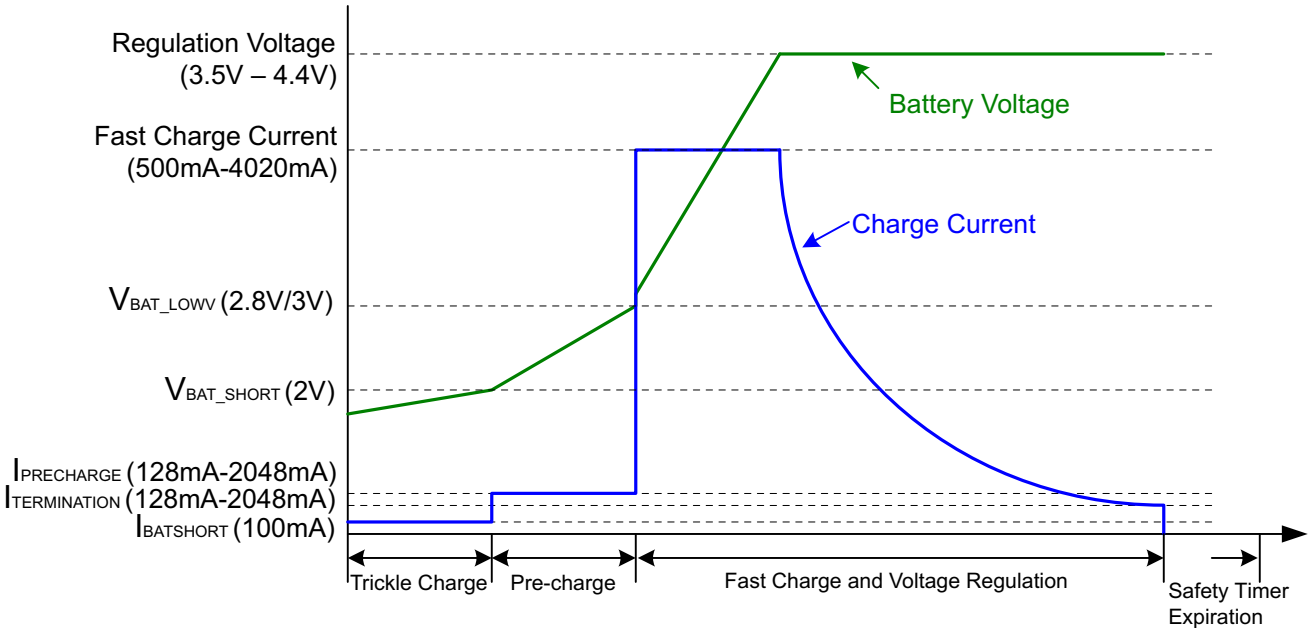

图 11. Battery Charging Profile

8.3.3.3 Thermistor Cold/Hot Temperature Window

The bq24195L, bq24195 continuously monitors battery temperature by measuring the voltage between the TS pins and ground, typically determined by a negative temperature coefficient thermistor and an external voltage divider. The device compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle, the battery temperature must be within the V_{LTF} to V_{HTF} thresholds. During the charge cycle the battery temperature must be within the V_{LTF} to V_{TCO} thresholds, else the device suspends charging and waits until the battery temperature is within the V_{LTF} to V_{HTF} range.

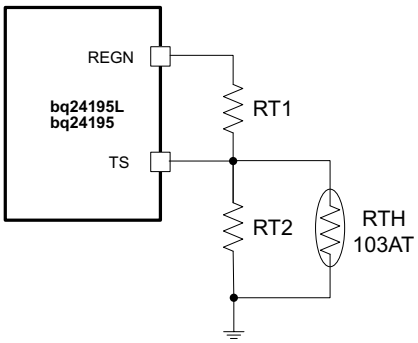

图 12. TS Resistor Network

When the TS fault occurs, the fault register REG09[2:0] indicates the actual condition on each TS pin and an INT is asserted to the host. The STAT pin indicates the fault when charging is suspended.

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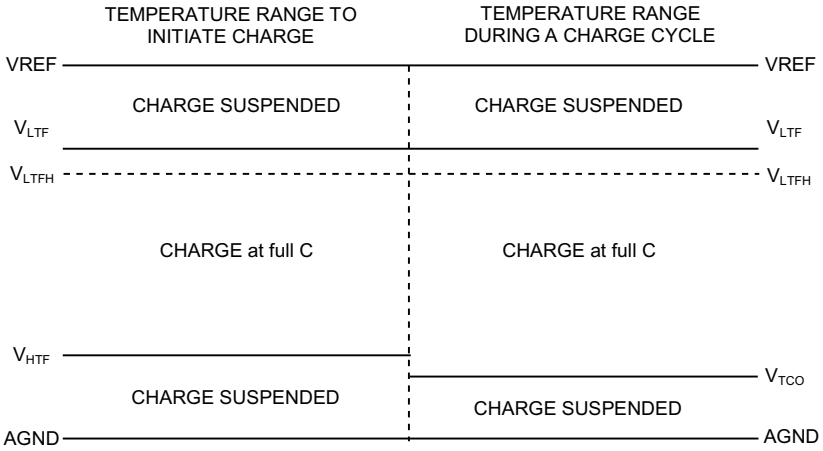

图 13. TS Pin Thermistor Sense Thresholds

Assuming a 103AT NTC thermistor is used on the battery pack, the value RT1 and RT2 can be determined by using the following equations:

$$RT2 = \frac{V_{VREF} \times RTH_{COLD} \times RTH_{HOT} \times \left(\frac{1}{V_{LTF}} - \frac{1}{V_{TCO}} \right)}{RTH_{HOT} \times \left(\frac{V_{VREF}}{V_{TCO}} - 1 \right) - RTH_{COLD} \times \left(\frac{V_{VREF}}{V_{LTF}} - 1 \right)}$$

$$RT1 = \frac{\frac{V_{VREF}}{V_{LTF}} - 1}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}} \quad (1)$$

Select 0°C to 45°C range for Li-ion or Li-polymer battery,
RTH_{COLD} = 27.28 kΩ
RTH_{HOT} = 4.911 kΩ
RT1 = 5.52 kΩ
RT2 = 31.23 kΩ

8.3.3.4 Charging Termination

The bq24195L, bq24195 terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below termination current. After the charging cycle is complete, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn back on to engage supplement mode.

When termination occurs, the status register REG08[5:4] is 11, and an INT is asserted to the host. Termination is temporarily disabled if the charger device is in input current/voltage regulation or thermal regulation. Termination can be disabled by writing 0 to REG05[7].

8.3.3.4.1 Termination when REG02[0] = 1

When REG02[0] is HIGH to reduce the charging current by 80%, the charging current could be less than the termination current. The charger device termination function should be disabled. When the battery is charged to fully capacity, the host disables charging through $\overline{CE}$ pin or REG01[5:4].

8.3.3.4.2 Termination when REG05[6] = 1

Usually the STAT bit indicates charging complete when the charging current falls below termination threshold. Write REG05[6] = 1 to enable an early “charge done” indication on STAT pin. The STAT pin goes high when the charge current reduces below 800 mA. The charging cycle is still on-going until the current falls below the termination threshold.

8.3.3.5 Charging Safety Timer

The bq24195L, bq24195 has safety timer to prevent extended charging cycle due to abnormal battery conditions.

In default mode, the device keeps charging the battery with 5-hour fast charging safety timer regardless of REG05[2:1] default value. At the end of the 5 hours, the EN_HIZ (REG00[7]) is set to signal the buck converter stops and the system load is supplied by the battery. The EN_HIZ bit can be cleared to restart the buck converter.

In host mode, the device keeps charging the battery until the fast charging safety timer expired. The duration of safety timer can be set by the REG05[2:1] bits (default = 8 hours). At the end of safety timer, the EN_HIZ (REG00[7]) is cleared to signal the buck converter continues to operation to supply system load.

The safety timer is 1 hour when the battery is below BATLOWV threshold. The user can program fast charge safety timer through I^2C (REG05[2:1]). When safety timer expires, the fault register REG09[5:4] goes 11 and an INT is asserted to the host. The safety timer feature can be disabled via I2C (REG05[3]).

The following actions restart the safety timer:

- At the beginning of a new charging cycle
- Toggle the $\overline{CE}$ pin HIGH to LOW to HIGH (charge enable)
- Write REG01[5:4] from 00 to 01 (charge enable)
- Write REG05[3] from 0 to 1 (safety timer enable)

During input voltage/current regulation or thermal regulation, or when FORCE_20PCT (REG02[0]) bit is set, the safety timer counts at half clock rate since the actual charge current is likely to be below the register setting. For example, if the charger is in input current regulation (IINDPM) throughout the whole charging cycle, and the safety time is set to 5 hours, the safety timer will expire in 10 hours. This feature can be disabled by writing 0 to REG07[6].

It is recommended to disable safety timer first by clearing REG05[3] bit before safety timer configuration is changed. The safety timer should be re-enabled by setting REG05[3] bit.

8.3.3.6 USB Timer when Charging from USB100mA Source

The total charging time in default mode from USB100-mA source is limited by a 45-min max timer. At the end of the timer, the device stops the converter and goes to HIZ.

8.3.4 Status Outputs (STAT and INT)

8.3.4.1 Charging Status Indicator (STAT)

The bq24195L, bq24195 indicates charging state on the open drain STAT pin. The STAT pin can drive LED as the application diagram shows.

表 5. STAT Pin State

CHARGING STATE	STAT
Charging in progress (including recharge)	LOW
Charging complete	HIGH
Sleep mode, charge disable	HIGH
Charge suspend (Input over-voltage, TS fault, timer fault, input or system over-voltage)	blinking at 1Hz

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8.3.4.2 Interrupt to Host (INT)

In some applications, the host does not always monitor the charger operation. The INT notifies the system on the device operation. The following events will generate 256-us INT pulse.

- USB/adapter source identified (through DPDM detection)
- Good input source detected
  - V_{VBUS} - V_{BAT} > V_{SLEEPZ}
  - V_{VBUS} > V_{ACOV}
  - current limit above I_{BADSRC}
- Input removed
- Charge Complete
- Any FAULT event in REG09

When a fault occurs, the charger device sends out INT and keeps the fault state in REG09 until the host reads the fault register. Before the host reads REG09 and all the faults are cleared, the charger device would not send any INT upon new faults. In order to read the current fault status, the host has to read REG09 two times consecutively. The 1st reads fault register status from the last read and the 2nd reads the current fault register status.

8.3.5 Protections

8.3.5.1 Input Current Limit on ILIM

For safe operation, the bq24195L, bq24195 has an additional hardware pin on ILIM to limit maximum input current on ILIM pin. The input maximum current is set by a resistor from ILIM pin to ground as:

$$I_{INMAX} = \frac{1V}{R_{ILIM}} \times 530 \quad (2)$$

The actual input current limit is the lower value between ILIM setting and register setting (REG00[2:0]). For example, if the register setting is 111 for 3 A, and ILIM has a 353-Ω resistor to ground for 1.5 A, the input current limit is 1.5 A. ILIM pin can be used to set the input current limit rather than the register settings.

The device regulates ILIM pin at 1 V. If ILIM voltage exceeds 1 V, the device enters input current regulation (Refer to *Dynamic Power Path Management* section).

The voltage on the ILIM pin is proportional to the input current. The ILIM pin can be used to monitor the input current per 公式 3:

$$I_{IN} = \frac{V_{ILIM}}{1V} \times I_{INMAX} \quad (3)$$

For example, if the ILIM pin sets 2 A, and the ILIM voltage is 0.6 V, the actual input current is 1.2 A. If the ILIM pin is open, the input current is limited to zero since ILIM voltage floats above 1 V. If the ILIM pin is short, the input current limit is set by the register.

8.3.5.2 Thermal Regulation and Thermal Shutdown

The bq24195L, bq24195 monitors the internal junction temperature T_J to avoid overheat the chip and limits the IC surface temperature. When the internal junction temperature exceeds the preset limit (REG06[1:0]), the device lowers down the charge current. The wide thermal regulation range from 60°C to 120°C allows the user to optimize the system thermal performance.

During thermal regulation, the actual charging current is usually below the programmed battery charging current. Therefore, termination is disabled, the safety timer runs at half the clock rate, and the status register REG08[1] goes high.

Additionally, the device has thermal shutdown to turn off the converter. The fault register REG09[5:4] is 10 and an INT is asserted to the host.

8.3.5.3 Voltage and Current Monitoring in Buck Mode

The bq24195L, bq24195 closely monitor the input and system voltage, as well as HSFET and LSFET current for safe buck mode operation.

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8.3.5.3.1 Input Over-Voltage (ACOV)

The maximum input voltage for buck mode operation is 18 V. If VBUS voltage exceeds 18 V, the device stops switching immediately. During input over voltage (ACOV), the fault register REG09[5:4] will be set to 01. An INT is asserted to the host.

8.3.5.3.2 System Over-Voltage Protection (SYSOVP)

The charger device monitors the voltage at SYS. When system over-voltage is detected, the converter is stopped to protect components connected to SYS from high voltage damage.

8.3.5.4 Current Monitoring in Boost Mode

The bq24195L, bq24195 closely monitors LSFET current to ensure safe boost mode operation.

8.3.5.5 Battery Protection

8.3.5.5.1 Battery Over-Current Protection (BATOVP)

The battery over-voltage limit is clamped at 4% above the battery regulation voltage. When battery over voltage occurs, the charger device immediately disables charge. The fault register REG09[5] goes high and an INT is asserted to the host.

8.3.5.5.2 Charging During Battery Short Protection

If the battery voltage falls below 2 V, the charge current is reduced to 100 mA for battery safety.

8.3.5.5.3 System Over-Current Protection

If the system is shorted or exceeds the over-current limit, the BATFET is latched off. DC source insertion on VBUS is required to reset the latch-off condition and turn on BATFET.

8.3.6 Serial Interface

The bq24195L, bq24195 uses I^2C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I^2C is a bi-directional 2-wire serial interface developed by Philips Semiconductor (now NXP Semiconductors). Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address 6BH, receiving control inputs from the master device like micro controller or a digital signal processor. The I^2C interface supports both standard mode (up to 100 kbits), and fast mode (up to 400 kbits).

Both SDA and SCL are bi-directional lines, connecting to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

8.3.6.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

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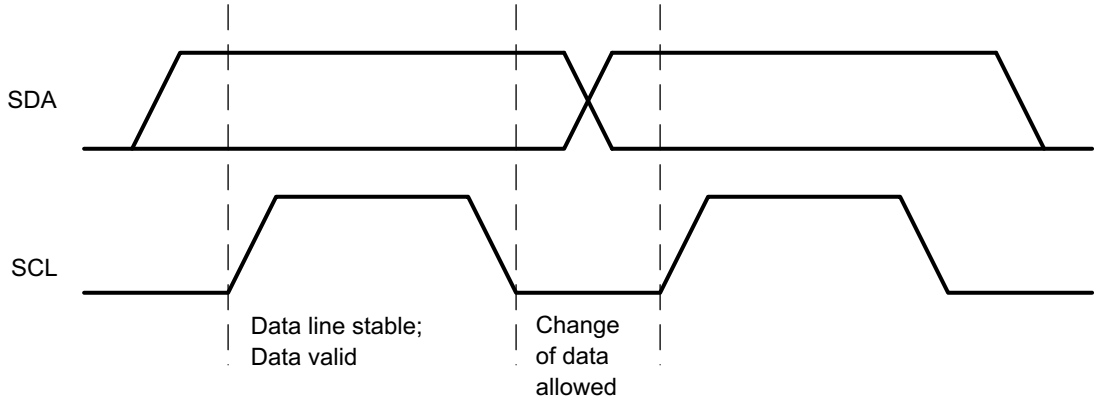

图 14. Bit Transfer on the I²C Bus

8.3.6.2 START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCl is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

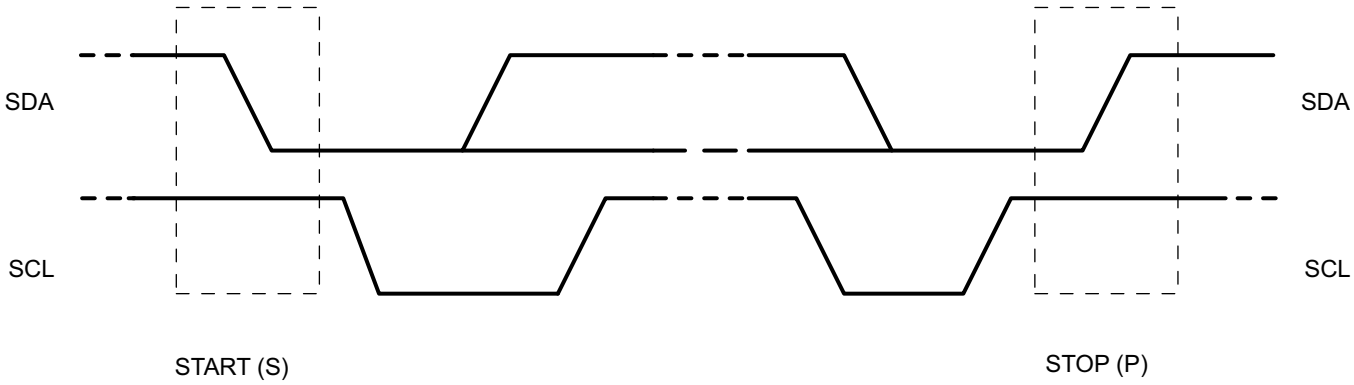

图 15. START and STOP conditions

8.3.6.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

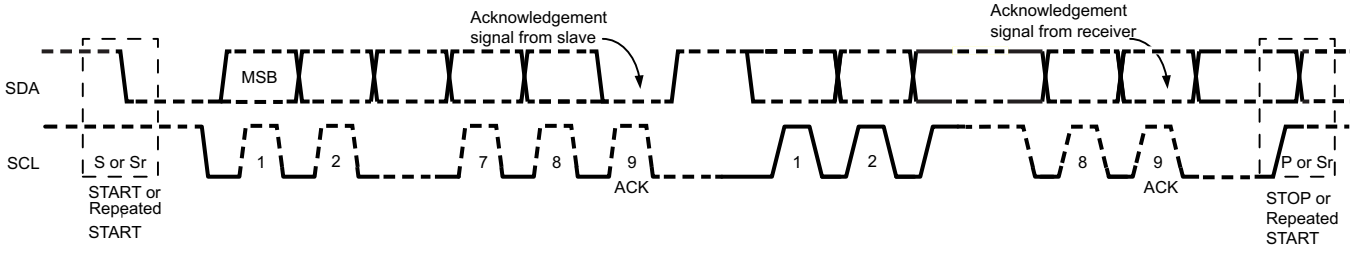

图 16. Data Transfer on the I²C Bus

8.3.6.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

8.3.6.5 Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

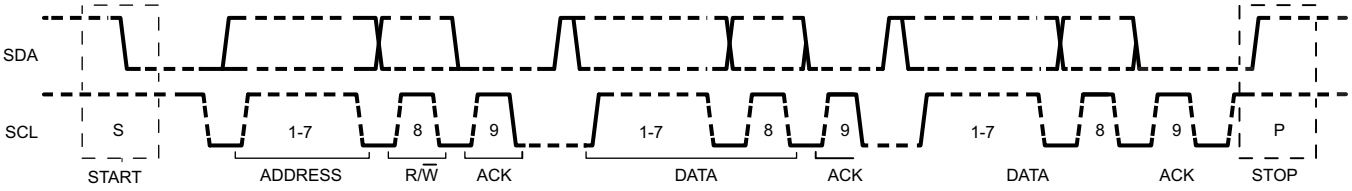

图 17. Complete Data Transfer

8.3.6.5.1 Single Read and Write

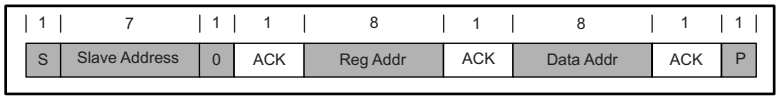

图 18. Single Write

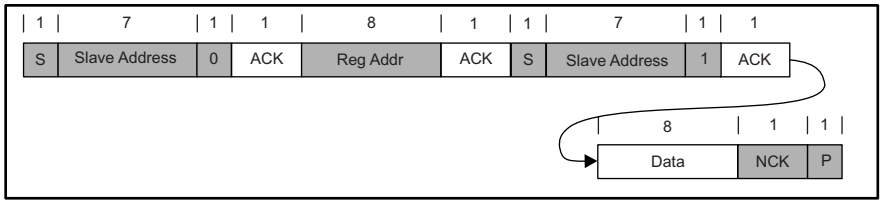

图 19. Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

8.3.6.5.2 Multi-Read and Multi-Write

The charger device supports multi-read and multi-write on REG00 through REG08.

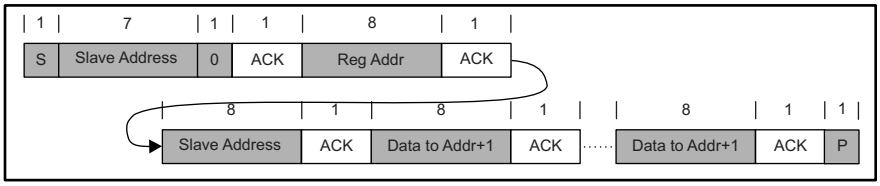

图 20. Multi-Write

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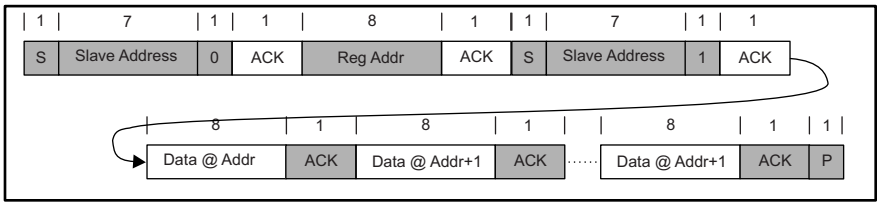

图 21. Multi-Read

The fault register REG09 locks the previous fault and only clears it after the register is read. For example, if Charge Safety Timer Expiration fault occurs but recovers later, the fault register REG09 reports the fault when it is read the first time, but returns to normal when it is read the second time. To verify real time fault, the fault register REG09 should be read twice to get the real condition. In addition, the fault register REG09 does not support multi-read or multi-write.

8.4 Device Functional Modes

8.4.1 Host Mode and Default Mode

The bq24195L, bq24195 is a host controlled device, but it can operate in default mode without host management. In default mode, bq24195L, bq24195 can be used as an autonomous charger with no host or with host in sleep.

When the charger is in default mode, REG09[7] is HIGH. When the charger is in host mode, REG09[7] is LOW. After power-on-reset, the device starts in watchdog timer expiration state, or default mode. All the registers are in the default settings.

Any write command to bq24195L, bq24195 transitions the device from default mode to host mode. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 twice to REG01[6] before the watchdog timer expires (REG05[5:4]), or disable watchdog timer by setting REG05[5:4] = 00.

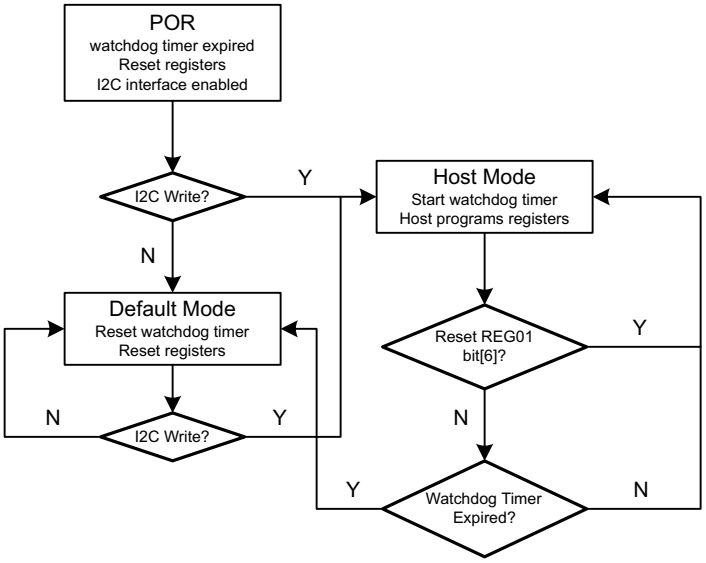

图 22. Watchdog Timer Flow Chart

8.4.1.1 Plug in USB100mA Source with Good Battery

When the input source is detected as 100-mA USB host, and the battery voltage is above batgood threshold (V_{BATGD}), the charger device enters HIZ state to meet the battery charging spec requirement.

Device Functional Modes (接下页)

If the charger device is in host mode, it will stay in HIZ state even after the USB100-mA source is removed, and the adapter plugs in. During the HIZ state, REG00[7] is set HIGH and the system load is supplied from battery. It is recommended that the processor host always checks if the charger IC is in HIZ state when it wakes up. The host can write REG00[7] to 0 to exit HIZ state.

If the charger is in default mode, when the DC source is removed, the charger device will get out of HIZ state automatically. When the input source plugs in again, the charger IC runs detection on the input source and update the input current limit.

8.4.1.2 USB Timer when Charging from USB 100-mA Source

The total charging time in default mode from USB 100-mA source is limited by a 45-min max timer. At the end of the timer, the device stops the converter and goes to HIZ.

8.5 Register Map

表 6. Register Map

REGISTER	REGISTER NAME	RESET
REG00	Input Source Control Register	00110000, or 30
REG01	Power-On Configuration Register	00011011, or 1B
REG02	Charge Current Control Register	01100000, or 60
REG03	Pre-Charge/Termination Current Control Register	00010001, or 11
REG04	Charge Voltage Control Register	10110010, or B2
REG05	Charge Termination/Timer Control Register	10011010, or 9A
REG06	Thermal Regulation Control Register	00000011, or 03
REG07	Misc Operation Control Register	01001011, or 4B
REG08	System Status Register	—
REG09	Fault Register	—
REG0A	Vender / Part / Revision Status Register	—

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8.5.1 I²C Registers

Address: 6BH. REG00-07 support Read and Write. REG08-0A are read only.

8.5.1.1 Input Source Control Register REG00 (reset = 00110000, or 30)

图 23. REG00 Input Source Control Register Format

7	6	5	4	3	2	1	0
EN_HIZ	VINDPM[3]	VINDPM[2]	VINDPM[1]	VINDPM[0]	IINLIM[2]	IINLIM[1]	IINLIM[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7. REG00 Input Source Control Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION	
Bit 7	EN_HIZ	R/W	0	0 – Disable, 1 – Enable	Default: Disable (0)
Input Voltage Limit					
Bit 6	VINDPM[3]	R/W	0	640 mV	Offset 3.88 V, Range: 3.88 V to 5.08 V Default: 4.36 V (0110)
Bit 5	VINDPM[2]	R/W	1	320 mV	
Bit 4	VINDPM[1]	R/W	1	160 mV	
Bit 3	VINDPM[0]	R/W	0	80 mV	
Input Current Limit (Actual input current limit is the lower of I²C and ILIM)					
Bit 2	IINLIM[2]	R/W	0	000 – 100 mA, 001 – 150 mA, 010 – 500 mA, 011 – 900 mA, 100 – 1.2 A, 101 – 1.5 A, 110 – 2 A, 111 – 3 A	Default SDP: 100 mA (000)(OTG pin = 0) or 500 mA (010) (OTG pin = 1) Default DCP/CDP: 1.5 A (101)
Bit 1	IINLIM[1]	R/W	0		
Bit 0	IINLIM[0]	R/W	0		

8.5.1.2 Power-On Configuration Register REG01 (reset = 00011011, or 1B)

图 24. REG01 Power-On Configuration Register Format

7	6	5	4	3	2	1	0
Register Reset	I^2C Watchdog Timer Reset	CHG_CONFIG[1]	CHG_CONFIG[0]	SYS_MIN[2]	SYS_MIN[1]	SYS_MIN[0]	Reserved
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8. REG01 Power-On Configuration Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
Bit 7	Register Reset	R/W	0	0 – Keep current register setting, 1 – Reset to default	Default: Keep current register setting (0) Back to 0 after register reset
Bit 6	I^2C Watchdog Timer Reset	R/W	0	0 – Normal ; 1 – Reset	Default: Normal (0) Back to 0 after timer reset
Charger Configuration					
Bit 5	CHG_CONFIG[1]	R/W	0	00 – Charge Disable, 01 – Charge Battery, 10/11 – OTG	Default: Charge Battery (01)
Bit 4	CHG_CONFIG[0]	R/W	1		
Minimum System Voltage Limit					
Bit 3	SYS_MIN[2]	R/W	1	0.4 V	Offset: 3.0 V, Range 3.0 V to 3.7 V Default: 3.5 V (101)
Bit 2	SYS_MIN[1]	R/W	0	0.2 V	
Bit 1	SYS_MIN[0]	R/W	1	0.1 V	
Bit 0	Reserved	R/W	1	1 - Reserved	Reserved. Must write "1"

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8.5.1.3 Charge Current Control Register REG02 (reset = 01100000, or 60)

图 25. REG02 Charge Current Control Register Format

7	6	5	4	3	2	1	0
ICHG[5]	ICHG[4]	ICHG[3]	ICHG[2]	ICHG[1]	ICHG[0]	Reserved	FORCE_20PCT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9. REG02 Charge Current Control Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
Fast Charge Current Limit					
Bit 7	ICHG[5]	R/W	0	2048 mA	Offset: 512 mA Range: 512 to 4544 mA (bq24195) Range: 512 to 2496mA (bq24195L) Default: 2048 mA (011000)
Bit 6	ICHG[4]	R/W	1	1024 mA	
Bit 5	ICHG[3]	R/W	1	512 mA	
Bit 4	ICHG[2]	R/W	0	256 mA	
Bit 3	ICHG[1]	R/W	0	128 mA	
Bit 2	ICHG[0]	R/W	0	64 mA	
Bit 1	Reserved	R/W	0	0 - Reserved	Reserved. Must write "0"
Bit 0	FORCE_20PCT	R/W	0	0 - ICHG as REG02[7:2] (Fast Charge Current Limit) and REG03[7:4] (Pre-Charge Current Limit) programmed 1 - ICHG as 20% of REG02[7:2] (Fast Charge Current Limit) and 50% of REG03[7:4] (Pre-Charge Current Limit) programmed	Default: ICHG as REG02[7:2] (Fast Charge Current Limit) and REG03[7:4] (Pre-Charge Current Limit) programmed (0)

8.5.1.4 Pre-Charge/Termination Current Control Register REG03 (reset = 00010001, or 11)

图 26. REG03 Pre-Charge/Termination Current Control Register Format

7	6	5	4	3	2	1	0
IPRECHG[3]	IPRECHG[2]	IPRECHG[1]	IPRECHG[0]	ITERM[3]	ITERM[2]	ITERM[1]	ITERM[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 10. REG03 Pre-Charge/Termination Current Control Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
Pre-Charge Current Limit					
Bit 7	IPRECHG[3]	R/W	0	1024 mA	Offset: 128 mA, Range: 128 mA to 2048 mA Default: 256 mA (0001)
Bit 6	IPRECHG[2]	R/W	0	512 mA	
Bit 5	IPRECHG[1]	R/W	0	256 mA	
Bit 4	IPRECHG[0]	R/W	1	128 mA	
Termination Current Limit					
Bit 3	ITERM[3]	R/W	0	1024 mA	Offset: 128 mA Range: 128 mA to 2048 mA Default: 256 mA (0001)
Bit 2	ITERM[2]	R/W	0	512 mA	
Bit 1	ITERM[1]	R/W	0	256 mA	
Bit 0	ITERM[0]	R/W	1	128 mA	

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8.5.1.5 Charge Voltage Control Register REG04 (reset = 10110010, or B2)

图 27. REG04 Charge Voltage Control Register Format

7	6	5	4	3	2	1	0
VREG[5]	VREG[4]	VREG[3]	VREG[2]	VREG[1]	VREG[0]	BATLOWV	VRECHG
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 11. REG04 Charge Voltage Control Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
Charge Voltage Limit					
Bit 7	VREG[5]	R/W	1	512 mV	Offset: 3.504 V Range: 3.504 V to 4.400 V (111000) Default: 4.208 V (101100)
Bit 6	VREG[4]	R/W	0	256 mV	
Bit 5	VREG[3]	R/W	1	128 mV	
Bit 4	VREG[2]	R/W	1	64 mV	
Bit 3	VREG[1]	R/W	0	32 mV	
Bit 2	VREG[0]	R/W	0	16 mV	
Battery Precharge to Fast Charge Threshold					
Bit 1	BATLOWV	R/W	1	0 – 2.8 V, 1 – 3.0 V	Default: 3.0 V (1)
Battery Recharge Threshold (below battery regulation voltage)					
Bit 0	VRECHG	R/W	0	0 – 100 mV, 1 – 300 mV	Default: 100 mV (0)

8.5.1.6 Charge Termination/Timer Control Register REG05 (reset = 10011010, or 9A)

图 28. REG05 Charge Termination/Timer Control Register Format

7	6	5	4	3	2	1	0
EN_TERM	TERM_STAT	WATCHDOG[1]	WATCHDOG[0]	EN_TIMER	CHG_TIMER[1]	CHG_TIMER[0]	Reserved
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 12. REG05 Charge Termination/Timer Control Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
Charging Termination Enable					
Bit 7	EN_TERM	R/W	1	0 – Disable, 1 – Enable	Default: Enable termination (1)
Termination Indicator Threshold					
Bit 6	TERM_STAT	R/W	0	0 – Match ITERM, 1 – STAT pin high before actual termination when charge current below 800 mA	Default Match ITERM (0)
I2C Watchdog Timer Setting					
Bit 5	WATCHDOG[1]	R/W	0	00 – Disable timer, 01 – 40 s, 10 – 80 s, 11 – 160 s	Default: 40 s (01)
Bit 4	WATCHDOG[0]	R/W	1		
Charging Safety Timer Enable					
Bit 3	EN_TIMER	R/W	1	0 – Disable, 1 – Enable	Default: Enable (1)
Fast Charge Timer Setting					
Bit 2	CHG_TIMER[1]	R/W	0	00 – 5 hrs, 01 – 8 hrs, 10 – 12 hrs, 11 – 20 hrs	Default: 8 hours (01) (See Charging Safety Timer for details)
Bit 1	CHG_TIMER[0]	R/W	1		
Bit 0	Reserved	R/W	0	0 - Reserved	Reserved. Must write "0"

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8.5.1.7 Thermal Regulation Control Register REG06 (reset = 00000011, or 03)

图 29. REG06 Thermal Regulation Control Register Format

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	TREG[1]	TREG[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 13. REG06 Thermal Regulation Control Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
Bit 7	Reserved	R/W	0	0 - Reserved	Reserved. Must write "0"
Bit 6	Reserved	R/W	0	0 - Reserved	Reserved. Must write "0"
Bit 5	Reserved	R/W	0	0 - Reserved	Reserved. Must write "0"
Bit 4	Reserved	R/W	0	0 - Reserved	Reserved. Must write "0"
Bit 3	Reserved	R/W	0	0 - Reserved	Reserved. Must write "0"
Bit 2	Reserved	R/W	0	0 - Reserved	Reserved. Must write "0"
Thermal Regulation Threshold					
Bit 1	TREG[1]	R/W	1	00 – 60°C, 01 – 80°C, 10 – 100°C, 11 – 120°C	Default: 120°C (11)
Bit 0	TREG[0]	R/W	1		

8.5.1.8 Misc Operation Control Register REG07 (reset = 01001011, or 4B)

图 30. REG07 Misc Operation Control Register Format

7	6	5	4	3	2	1	0
DPDM_EN	TMR2X_EN	BATFET_Disable	Reserved	Reserved	Reserved	INT_MASK[1]	INT_MASK[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 14. REG07 Misc Operation Control Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
Force DPDM detection					
Bit 7	DPDM_EN	R/W	0	0 – Not in D+/D– detection; 1 – Force D+/D– detection	Default: Not in D+/D– detection (0), Back to 0 after detection complete
Safety Timer Setting during Input DPM and Thermal Regulation					
Bit 6	TMR2X_EN	R/W	1	0 – Safety timer not slowed by 2X during input DPM or thermal regulation, 1 – Safety timer slowed by 2X during input DPM or thermal regulation	Default: Safety timer slowed by 2X (1)
Force BATFET Off					
Bit 5	BATFET_Disable	R/W	0	0 – Allow Q4 turn on, 1 – Turn off Q4	Default: Allow Q4 turn on(0)
Bit 4	Reserved	R/W	0	0 – Reserved. Must write "0"	
Bit 3	Reserved	R/W	1	1 – Reserved. Must write "1"	
Bit 2	Reserved	R/W	0	0 – Reserved. Must write "0"	
Bit 1	INT_MASK[1]	R/W	1	0 – No INT during CHRG_FAULT, 1 – INT on CHRG_FAULT	Default: INT on CHRG_FAULT (1)
Bit 0	INT_MASK[0]	R/W	1	0 – No INT during BAT_FAULT, 1 – INT on BAT_FAULT	Default: INT on BAT_FAULT (1)

8.5.1.9 System Status Register REG08

图 31. REG08 System Status Register Format

7	6	5	4	3	2	1	0
VBUS_STAT[1]	VBUS_STAT[0]	CHRG_STAT[1]	CHRG_STAT[0]	DPM_STAT	PG_STAT	THERM_STAT	VSYS_STAT
R	R	R	R	R	R	R	R

LEGEND: R = Read only; -n = value after reset

表 15. REG08 System Status Register Description

BIT	FIELD	TYPE	DESCRIPTION
Bit 7	VBUS_STAT[1]	R	00 – Unknown (no input, or DPDM detection incomplete), 01 – USB host, 10 – Adapter port, 11 – OTG
Bit 6	VBUS_STAT[0]	R	
Bit 5	CHRG_STAT[1]	R	00 – Not Charging, 01 – Pre-charge (<$V_{BATLOWV}$), 10 – Fast Charging, 11 – Charge Termination Done
Bit 4	CHRG_STAT[0]	R	
Bit 3	DPM_STAT	R	0 – Not DPM, 1 – VINDPM or IINDPM
Bit 2	PG_STAT	R	0 – Not Power Good, 1 – Power Good
Bit 1	THERM_STAT	R	0 – Normal, 1 – In Thermal Regulation
Bit 0	VSYS_STAT	R	0 – Not in VSYSMIN regulation (BAT > VSYSMIN), 1 – In VSYSMIN regulation (BAT < VSYSMIN)

8.5.1.10 Fault Register REG09

图 32. REG09 Fault Register Format

7	6	5	4	3	2	1	0
WATCHDOG_ FAULT	Reserved	CHRG_FAULT[1]	CHRG_FAULT[0]	BAT_FAULT	NTC_FAULT[2]	NTC_FAULT[1]	NTC_FAULT[0]
R	R	R	R	R	R	R	R

LEGEND: R = Read only; -n = value after reset

表 16. REG09 Fault Register Description

BIT	FIELD	TYPE	DESCRIPTION
Bit 7	WATCHDOG_FAULT	R	0 – Normal, 1- Watchdog timer expiration
Bit 6	Reserved	R	0 - Reserved
Bit 5	CHRG_FAULT[1]	R	00 – Normal, 01 – Input fault (VBUS OVP or VBAT < VBUS < 3.8 V), 10 - Thermal shutdown, 11 – Charge Safety Timer Expiration
Bit 4	CHRG_FAULT[0]	R	
Bit 3	BAT_FAULT	R	0 – Normal, 1 – BATOVP
Bit 2	NTC_FAULT[2]	R	000 – Normal, 101 – Cold, 110 – Hot
Bit 1	NTC_FAULT[1]	R	
Bit 0	NTC_FAULT[0]	R	

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8.5.1.11 Vender / Part / Revision Status Register REG0A (reset = 00100011, or 23)

图 33. REG0A Vender / Part / Revision Status Register Format

7	6	5	4	3	2	1	0
Reserved	Reserved	PN[2]	PN[1]	PN[0]	TS_PROFILE	DEV_REG[0]	DEV_REG[1]
R	R	R	R	R	R	R	R

LEGEND: R = Read only; -n = value after reset

表 17. REG0A Vender / Part / Revision Status Register Description

BIT	FIELD	TYPE	RESET	DESCRIPTION
Bit 7	Reserved	R	0	0 - Reserved
Bit 6	Reserved	R	0	0 - Reserved
Device Configuration				
Bit 5	PN[2]	R	1	100
Bit 4	PN[1]	R	0	
Bit 3	PN[0]	R	0	
Bit 2	TS_PROFILE	R	0	0 - Cold/Hot window
Bit 1	DEV_REG[0]	R	1	11
Bit 0	DEV_REG[1]	R	1	

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9 Application and Implementation

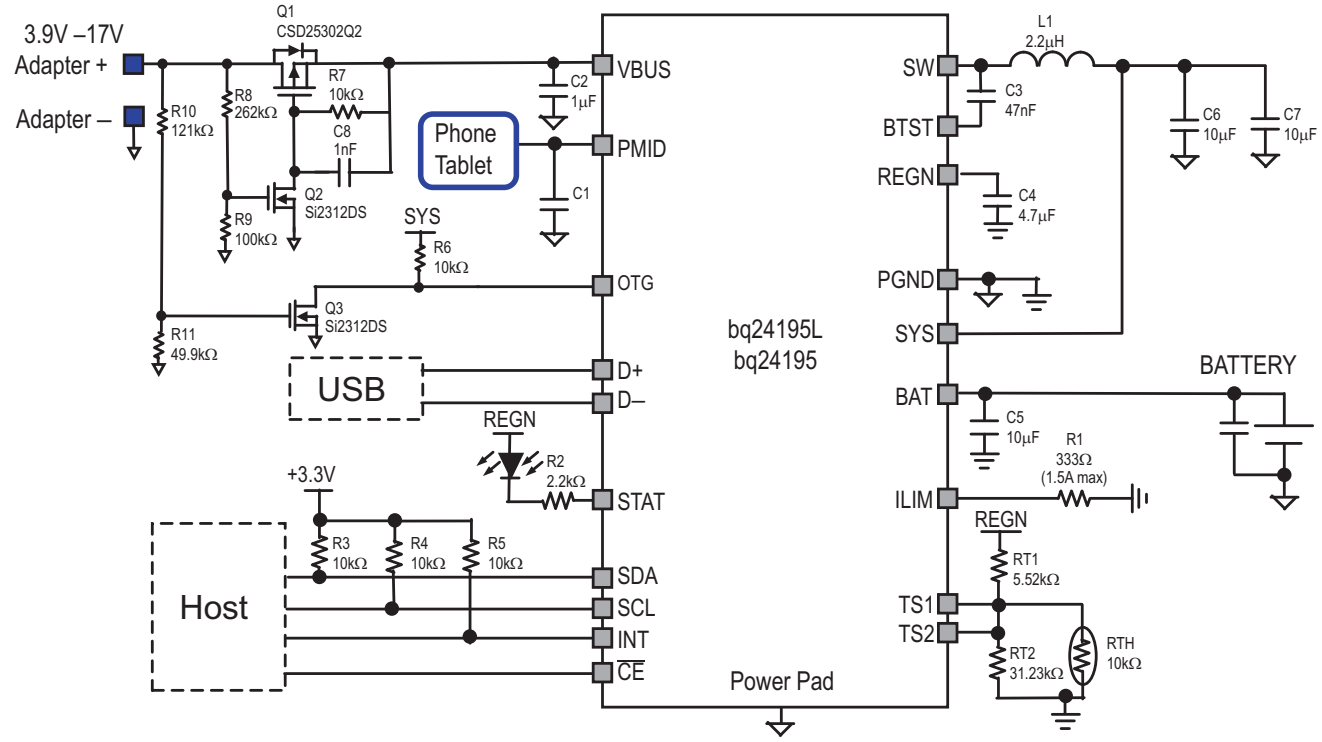
注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

A typical application consists of the device configured as an I^2C controlled power path management device and a single cell Li-Ion battery charger for single cell Li-Ion and Li-polymer batteries used in a wide range of tablets and other portable devices. It integrates an input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and BATFET (Q4) between the system and battery. The device also integrates a bootstrap diode for the high-side gate drive.

9.2 Typical Application



Recommended C1(min) = 20µF (bq24195L) or 60µF (bq24195)

9.2.1 Design Requirements

表 18. Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	3.9 V to 17 V
Input current limit	1.5 A
Fast charge current	2048 mA
Boost mode output current	2.5 A (bq24195L) or 4.5 A (bq24195)

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9.2.2 Detailed Design Procedure

9.2.2.1 Inductor Selection

The bq24195L, bq24195 has 1.5-MHz switching frequency to allow the use of small inductor and capacitor values. The Inductor saturation current should be higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2) I_{RIPPLE} \quad (4)$$

The inductor ripple current depends on input voltage (VBUS), duty cycle (D = V_{BAT}/V_{VBUS}), switching frequency (fs) and inductance (L):

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1-D)}{fs \times L} \quad (5)$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. Usually inductor ripple is designed in the range of (20 to 40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design. Typical inductor value is 2.2 µH.

9.2.2.2 Input Capacitor

Input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current I_{CIN} occurs where the duty cycle is closest to 50% and can be estimated by the following equation:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1-D)} \quad (6)$$

For best performance, VBUS should be decouple to PGND with 1-µF capacitance. The remaining input capacitor should be place on PMID.

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high side MOSFET and source of the low side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. 25-V rating or higher capacitor is preferred for 15-V input voltage.

9.2.2.3 Output Capacitor

Output capacitor also should have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current I_{COUT} is given:

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (7)$$

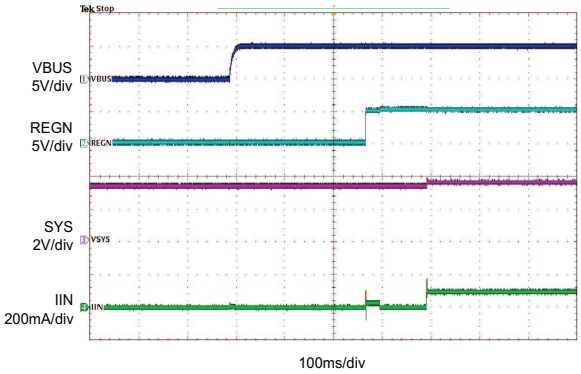
The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_O = \frac{V_{OUT}}{8LCfs^2}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

At certain input/output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC.

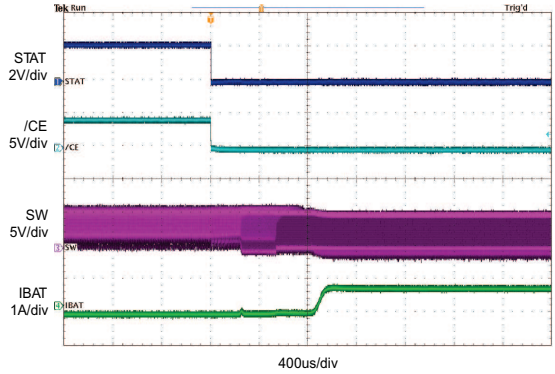
The charger device has internal loop compensator. To get good loop stability, the resonant frequency of the output inductor and output capacitor should be designed between 15 kHz and 25 kHz. With 2.2-µH inductor, the typical output capacitor value is 20 µF. The preferred ceramic capacitor is 6 V or higher rating, X7R or X5R.

9.2.3 Application Performance Plots



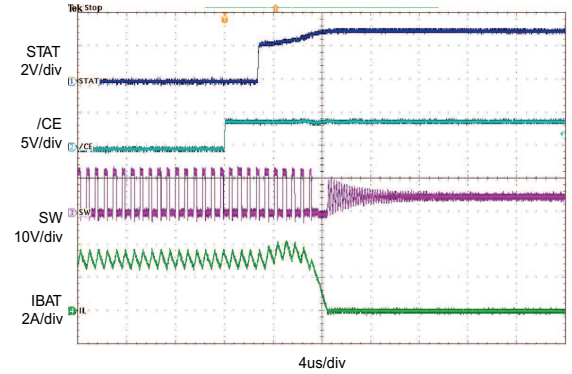
VBAT 3.2 V

图 34. Power Up from USB100 mA



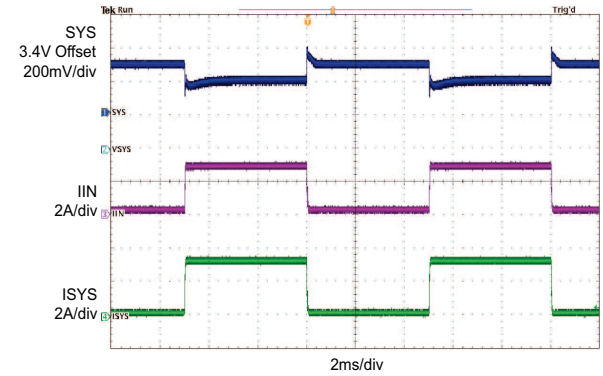
VBUS 5 V

图 35. Charge Enable



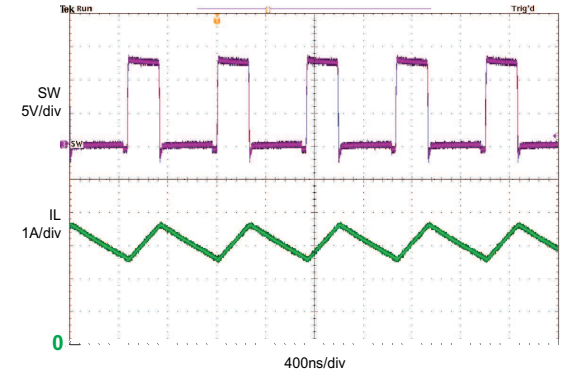
VBUS 12 V

图 36. Charge Disable



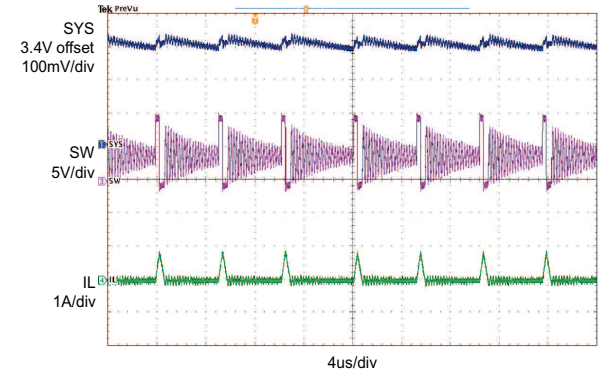
VBUS 5 V, IIN 3 A, Charge Disable

图 37. Input Current DPM Response without Battery



VBUS 12 V, VBAT 3.8 V, ICHG 3 A

图 38. PWM Switching Waveform



VBUS 9 V, No Battery, ISYS 10 mA, Charge Disable

图 39. PFM Switching Waveform

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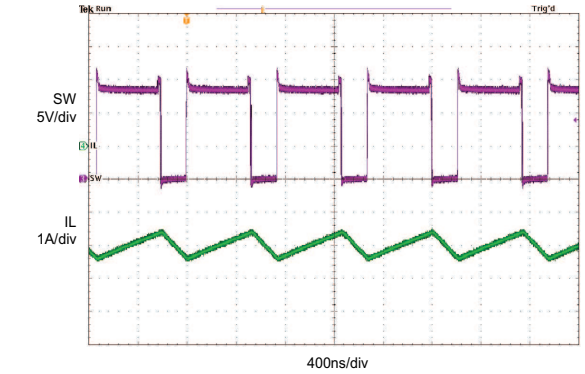
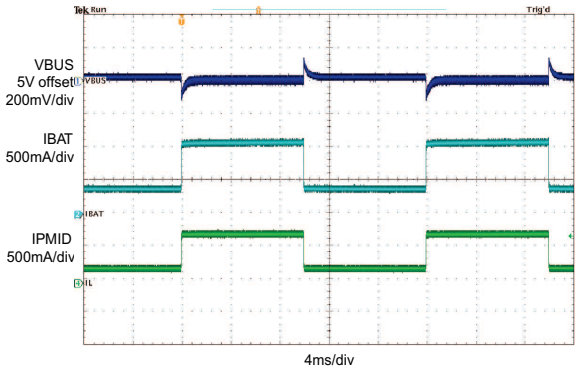


VBAT 3.8 V, ILOAD 1 A

图 40. Boost Mode Switching Waveform



VBAT 3.8 V

图 41. Boost Mode Load Transient

10 Power Supply Recommendations

In order to provide an output voltage on SYS, the devices require a power supply between 3.9 V and 17 V input with at least 100-mA current rating connected to VBUS; or, a single-cell Li-Ion battery with voltage > VBAT_UVLOZ connected to BAT.

11 Layout

11.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see 图 42) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Place input capacitor as close as possible to PMID pin and GND pin connections and use shortest copper trace connection or GND plane.
2. Place inductor input terminal to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
3. Put output capacitor near to the inductor and the IC. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
4. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using power pad as the single ground connection point. Or using a 0-Ω resistor to tie analog ground to power ground.
5. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the IC. Use ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling.
6. Decoupling capacitors should be placed next to the IC pins and make trace connection as short as possible.
7. It is critical that the exposed power pad on the backside of the IC package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
8. The via size and number should be enough for a given current path.

See the EVM design for the recommended component placement with trace and via locations. For the VQFN information, refer to SCBA017 and SLUA271.

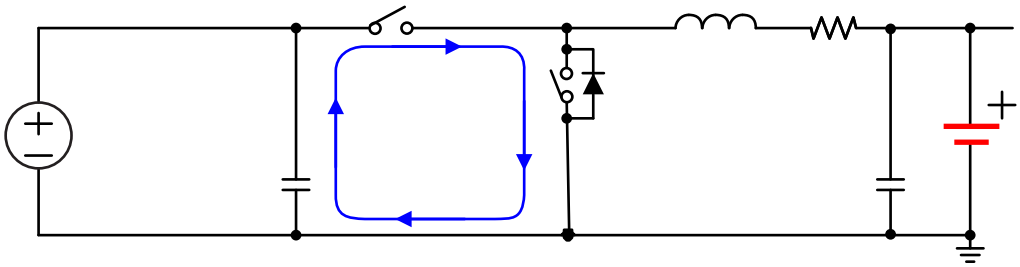


图 42. High Frequency Current Path

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11.2 Layout Example

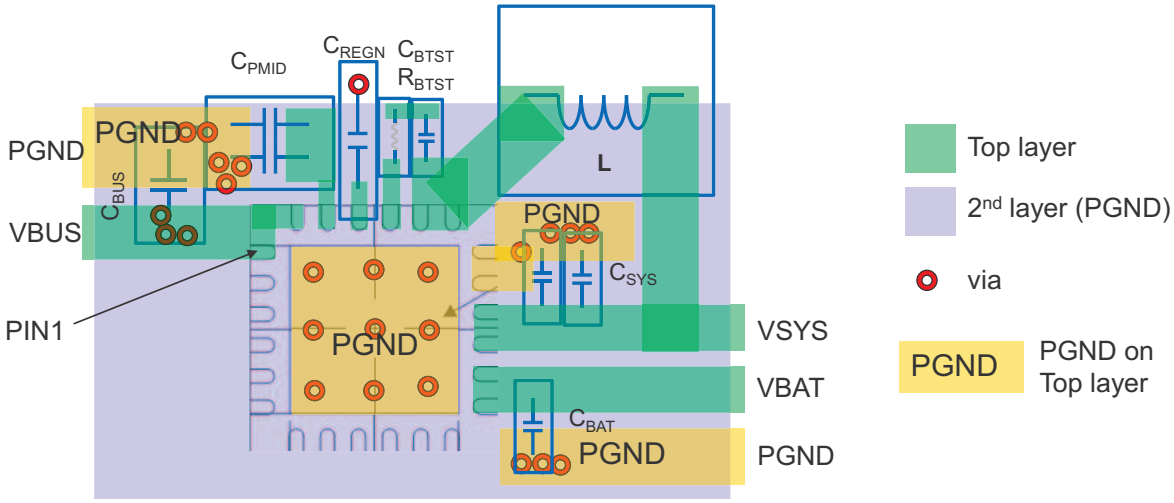

图 43. Layout Example Diagram

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

《bq24195/L EVM (PWR021) 用户指南》（文献编号：SLUUA18）

《四方扁平无引线逻辑器件封装应用报告》(SCBA017)

《QFN/SON PCB 连接应用报告》(SLUA271)

12.2 相关链接

以下表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **19.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
bq24195	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
bq24195L	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.3 商标

All trademarks are the property of their respective owners.

12.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

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13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ24195LRGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24195L
BQ24195LRGER.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24195L
BQ24195LRGERG4	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24195L
BQ24195LRGERG4.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24195L
BQ24195LRGET	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24195L
BQ24195LRGET.A	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24195L
BQ24195RGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ24195
BQ24195RGER.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ24195
BQ24195RGET	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ24195
BQ24195RGET.A	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ24195

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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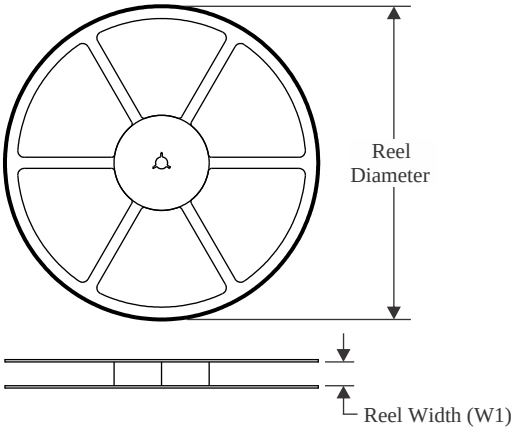
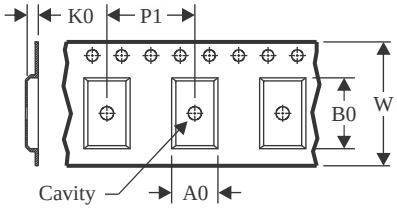
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

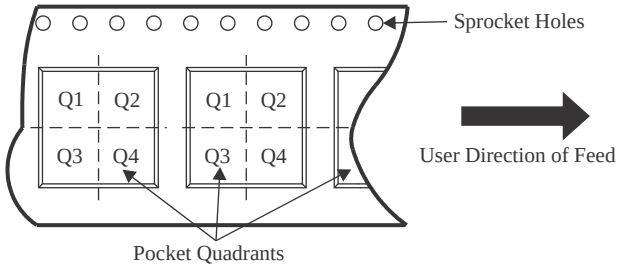


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

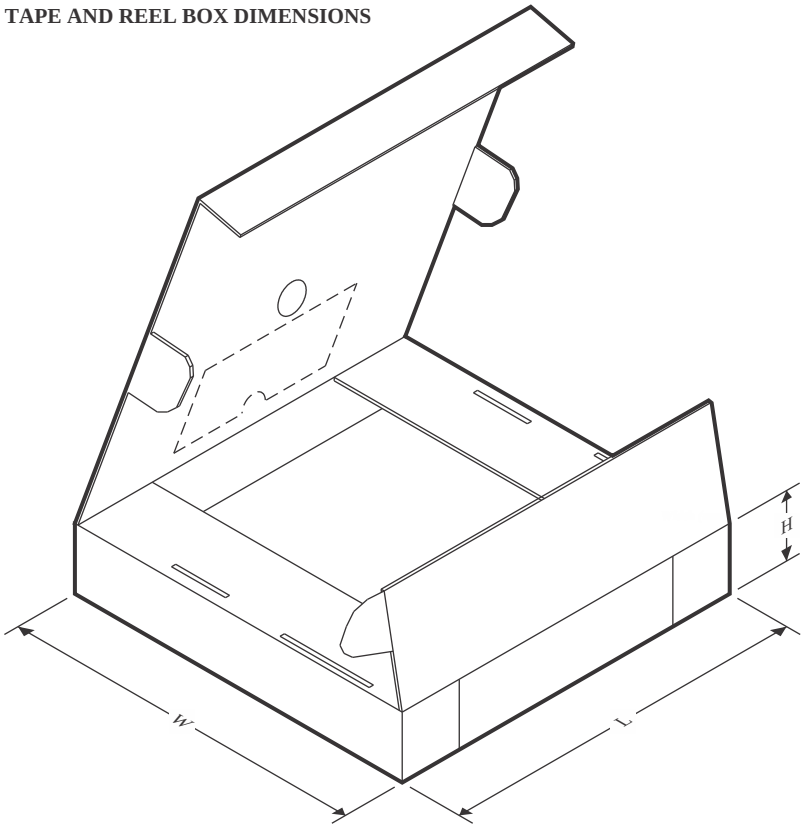
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24195LRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24195LRGERG4	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24195LRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24195RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24195RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



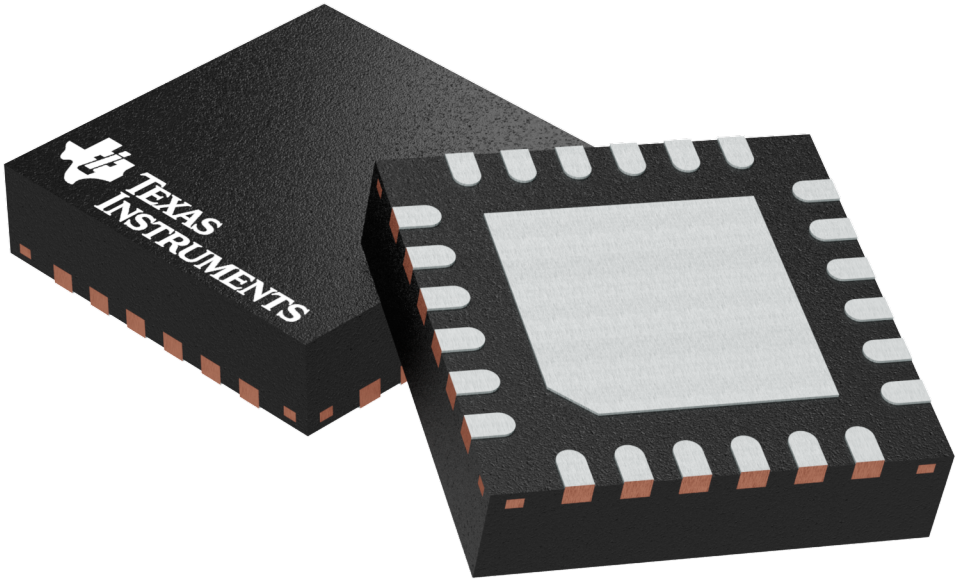
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24195LRGER	VQFN	RGE	24	3000	346.0	346.0	33.0
BQ24195LRGERG4	VQFN	RGE	24	3000	346.0	346.0	33.0
BQ24195LRGET	VQFN	RGE	24	250	210.0	185.0	35.0
BQ24195RGER	VQFN	RGE	24	3000	346.0	346.0	33.0
BQ24195RGET	VQFN	RGE	24	250	210.0	185.0	35.0

RGE 24

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



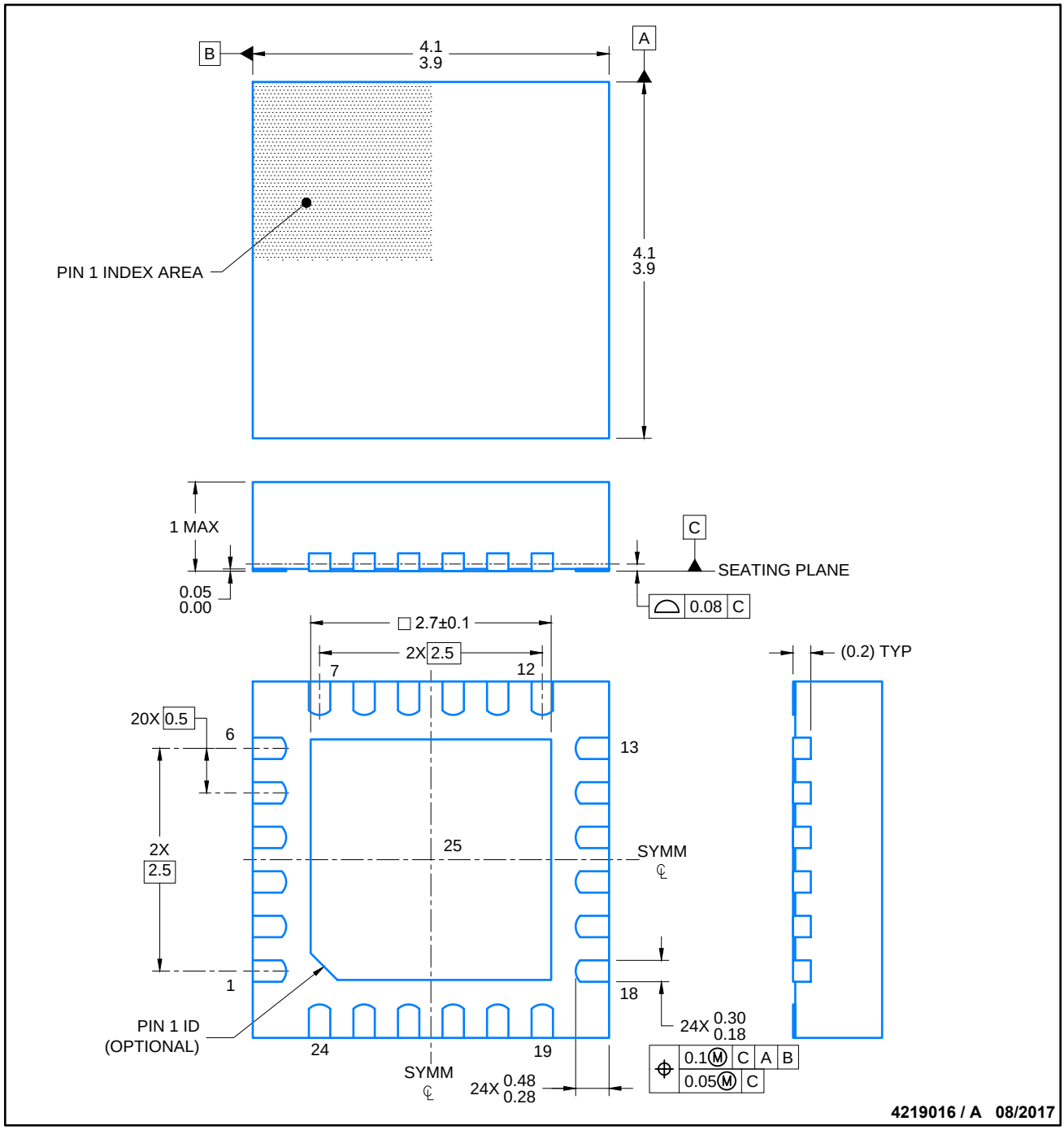
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGE0024H

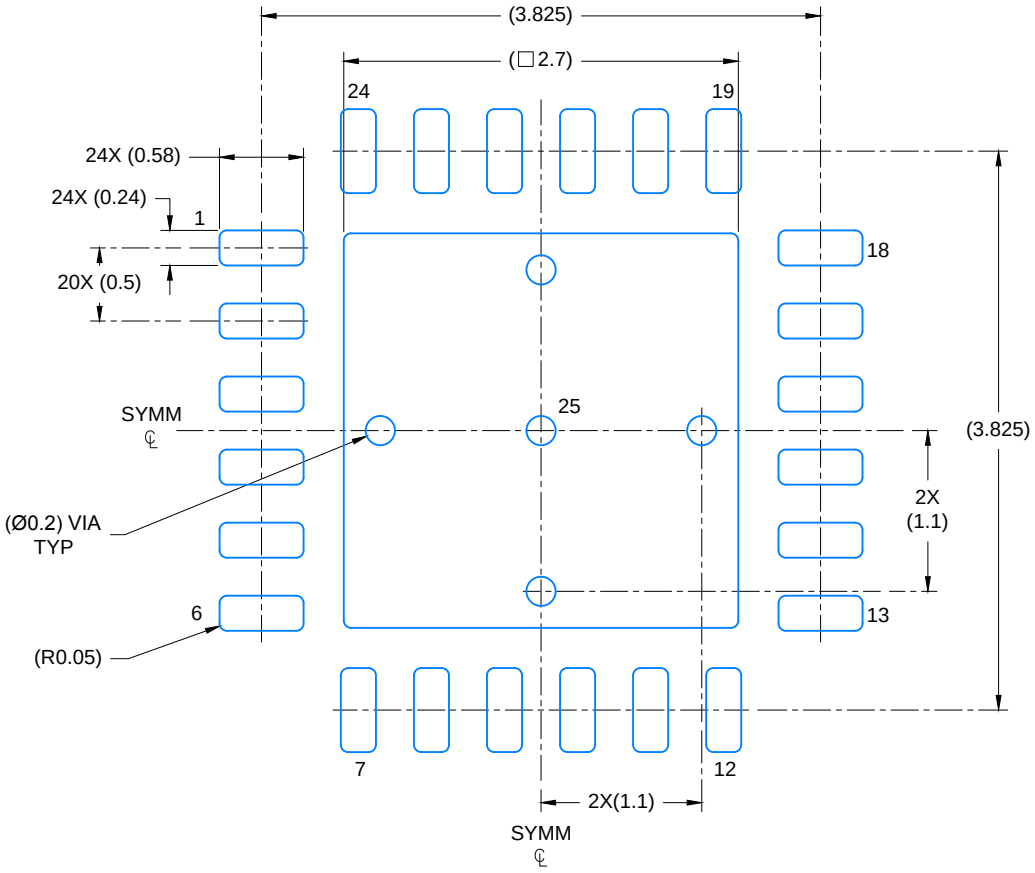
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



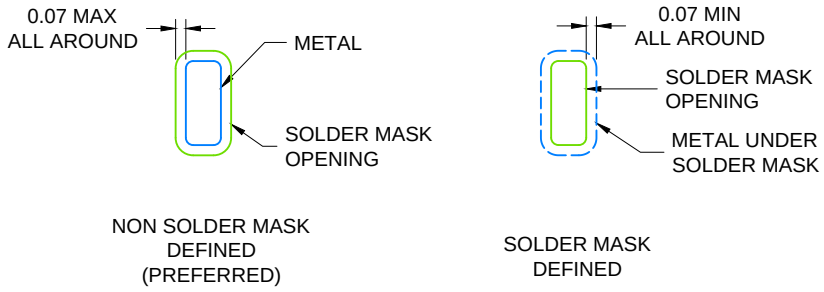
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X



SOLDER MASK DETAILS

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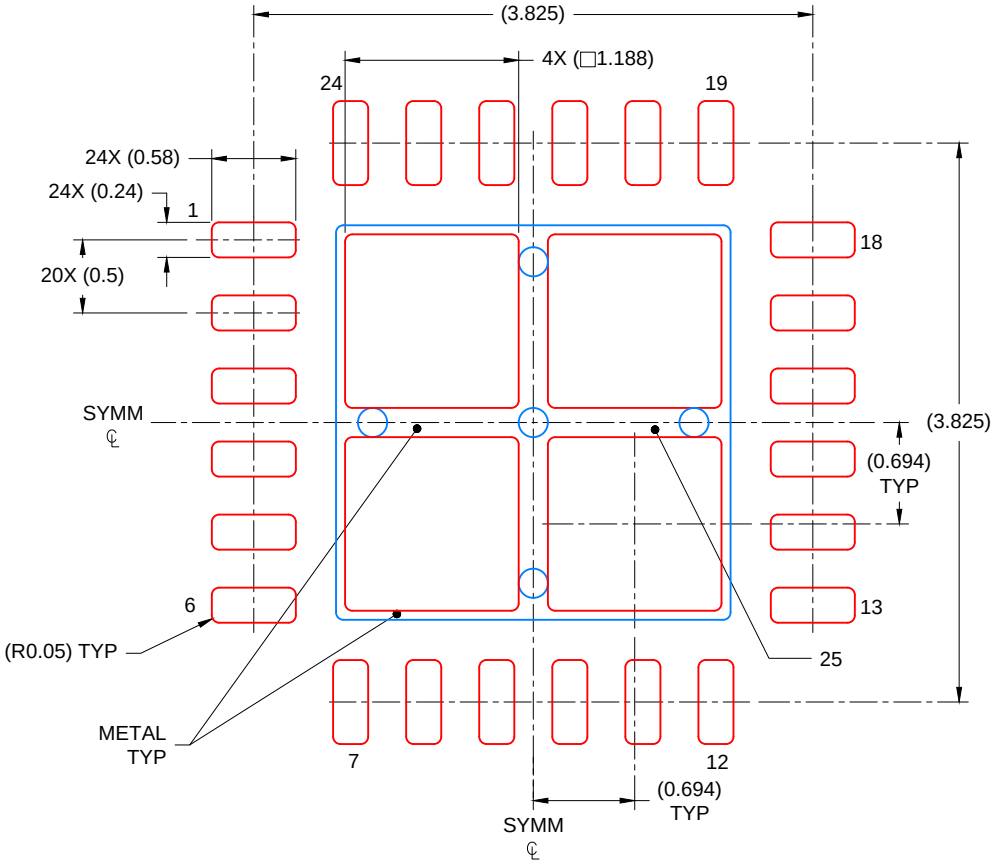
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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