

# 带双输入选择器的 BQ24179 I<sup>2</sup>C 控制、1 节至 4 节、5A 降压/升压电池充电器

## 1 特性

- 高功率密度、高集成降压/升压充电器，用于 1-4 节电池，支持任何 USB PD 3.0 概要文件
  - 集成四个开关 MOSFET、BATFET
  - 集成输入和充电电流检测
- 高效
  - 750kHz 或 1.5MHz 开关频率
  - 为 2s 电池充电进行效率优化，在 3A ICHG 下，9V 输入达到 96.5% 的效率，15V 输入达到 94.5% 效率
  - 5A 充电电流，精度 10mA
    - 效率高达 96.5%：在 3A 电流下从 20V 输入为 16V 电池充电
- 支持宽输入源
  - 3.6V 至 24V 宽输入工作电压范围，绝对最大额定电压为 30V
  - 最大功率跟踪，输入电压动态电源管理 (VINDPM) 高达 22V，输入电流动态电源管理 (IINDPM) 高达 3.3A
  - 检测 USB BC1.2、SDP、CDP、DCP、HVDCCP 以及非标准适配器
- 用于源选择的双输入电源多路复用器控制器 (可选)
- 窄电压 DC (NVDC) 电源路径管理
- 灵活的自主和 I<sup>2</sup>C 模式，可实现出色系统性能
- 用于电压、电流和温度监控的集成 16 位 ADC
- 低电池静态电流
  - 仅使用电池工作时典型为 30μA
- 高准确度
  - 2s 电池充电电压调节范围为 ±1%
  - 充电电流调节范围为 ±10%
  - 输入电流调节范围为 ±5%
- 安全
  - 热调节和热关断
  - 输入/电池 OVP 和 OCP
  - 转换器 MOSFET OCP
  - 充电安全计时器
- 封装
  - 56 引脚，2.9mm × 3.3mm WCSP

## 2 应用

- 智能手机、平板电脑、无线真空吸尘器、医疗设备、无人机
- 无线扬声器、数码相机
- 移动打印机、电子销售终端 (EPOS)

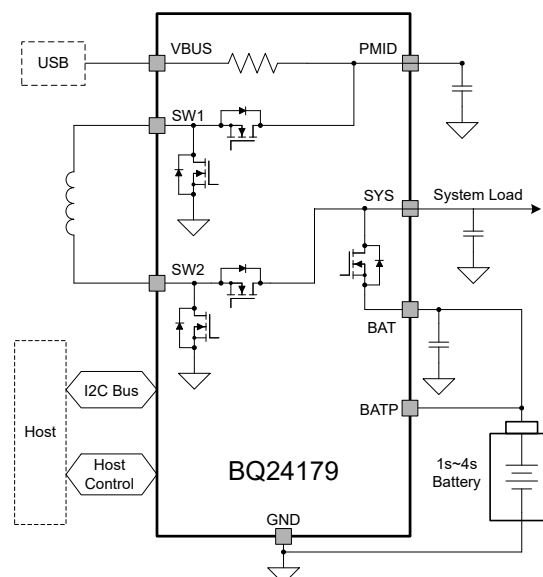
## 3 说明

BQ24179 是一个完全集成的开关模式降压/升压充电器，用于 1-4 节锂离子电池和锂聚合物电池。该集成包括 4 开关 MOSFET (Q<sub>1</sub>、Q<sub>2</sub>、Q<sub>3</sub>、Q<sub>4</sub>)、输入和充电电流感应电路、电池 FET (Q<sub>BAT</sub>) 以及降压/升压转换器的环路补偿。

### 器件信息(1)

| 器件型号    | 封装         | 封装尺寸 (标称值)      |
|---------|------------|-----------------|
| BQ24179 | DSBGA (56) | 2.90mm x 3.30mm |

- (1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版原理图



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## 4 Revision History

| DATE       | REVISION | NOTES            |
|------------|----------|------------------|
| March 2021 | *        | Initial release. |

## 5 说明 (续)

它使用窄范围 VDC 电源路径管理，将系统电压调节至稍高于电池电压的水平，但是不会下降至低于可配置的最小系统电压。当系统功率超过输入源额定值时，电池补充模式支持系统，不会使输入源过载。

充电器支持 NVDC 电源路径管理，将系统电压调节至稍高于电池电压的水平，但是不下降至低于最小系统电压。即便在电池完全放电或被取出时，系统仍会继续工作。当负载功率超过输入源额定值时，电池会进入补充模式并防止输入源过载和系统崩溃。

该器件从传统 USB 适配器到高电压 USB PD 适配器和传统桶形适配器等各种输入源为电池充电。在没有主机控制时，充电器基于输入电压和电池电压自动将转换器设置为降压、升压或降压-升压配置。双输入源选择器管理来自两个不同输入源的电源流入。输入选择由主机通过 I<sup>2</sup>C 来控制，默认源 1 (VAC1) 作为主输入，源 2 (VAC2) 作为辅助输入。

为支持通过可调节高电压适配器进行快速充电，该器件提供了 D+/D- 握手机制。该器件符合 USB 2.0 和 USB 3.0 功率传输规范，具有输入电流和电压调节功能。此外，输入电流优化器 (ICO) 还能够检测未知输入源的最大功率点。

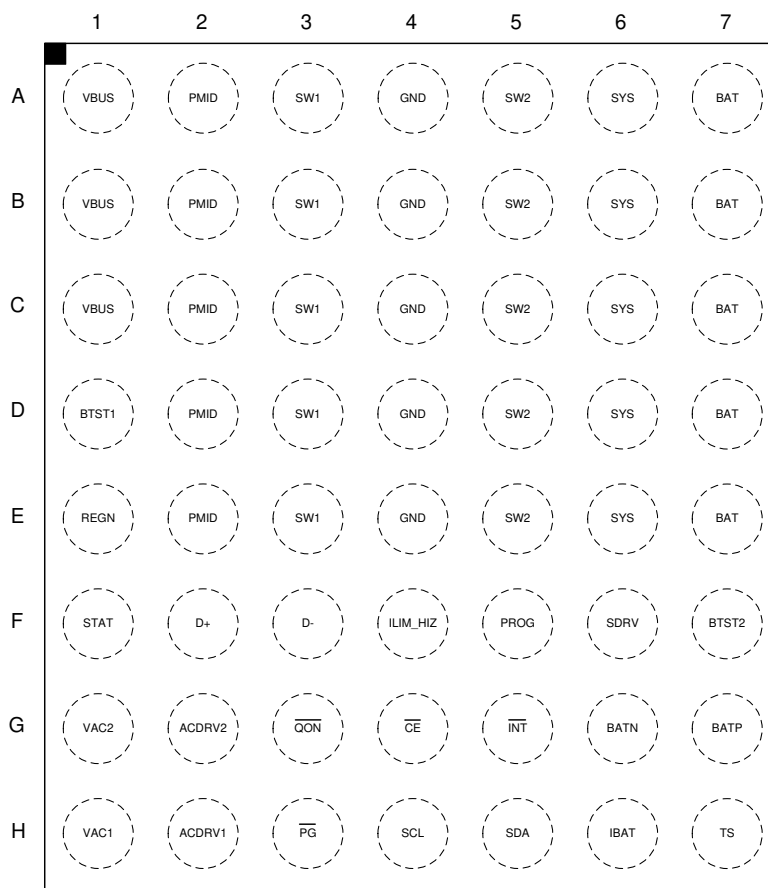
除了 I<sup>2</sup>C 主机控制的充电模式，此充电器还支持自动充电模式。上电之后，使用默认寄存器设置启用充电。此器件可以在无需软件参与的情况下完成充电周期。它检测电池电压并在不同阶段为电池充电：涓流充电、预充电、恒定电流 (CC) 充电和恒定电压 (CV) 充电。在充电周期的末尾，当充电电流低于在恒定电压阶段中预设定的限值 (终止电流) 时，充电器自动终止。当整个电池下降到低于再充电阈值时，充电器将自动启动另一个充电周期。

该充电器提供针对电池充电和系统运行的多种安全特性，其中包括电池负温度系数热敏电阻监视、涓流充电、预充电和快速充电计时器以及电池和输入上的过压/过流保护。当结温超过可编程的阈值时，热调节会减小充电电流。器件的 STAT 输出报告充电状态和任何故障状况。PG 输出指示电源是否正常。当发生故障时，INT 引脚会立即通知主机。

该器件还提供了一个 16 位模数转换器 (ADC)，用于监视充电电流和输入/电池/系统 (VAC、VBUS、BAT、SYS、TS) 电压。

该器件采用 56 引脚 2.9mm × 3.3mm WCSP 封装。

## 6 Pin Configuration and Functions



Top View = Xray through a soldered down part with A1 starting in upper left corner

图 6-1. YBG Package 56-Pin DSBGA Top View

表 6-1. Pin Functions

| PIN  |     | I/O | DESCRIPTION   |
|------|-----|-----|---|
| NAME | NO. |     |   |
| VBUS | A1  | P   | <b>Charger Input Voltage</b> – The power input terminal of the charger. An input current sensing circuit is connected between VBUS and PMID. Place a 0.1- $\mu$ F ceramic capacitor from VBUS to power GND as close as possible to the charger IC. The recommended capacitors at VBUS are two piece of 10- $\mu$ F and one piece of 0.1- $\mu$ F ceramic capacitors.              |
|      | B1  |     |   |
|      | C1  |     |   |
| PMID | A2  | P   | <b>Q1 MOSFET Drain Connection</b> – An internal N-channel high side MOSFET (Q1) is connected between PMID and SW1 with drain on PMID and source on SW1. Place a 0.1- $\mu$ F ceramic capacitor from PMID to power GND as close as possible to the charger IC. The recommended capacitors at PMID are three piece of 10- $\mu$ F and one piece of 0.1- $\mu$ F ceramic capacitors. |
|      | B2  |     |   |
|      | C2  |     |   |
|      | D2  |     |   |
|      | E2  |     |   |
| SW1  | A3  | P   | <b>Buck Side Half Bridge Switching Node</b>   |
|      | B3  |     |   |
|      | C3  |     |   |
|      | D3  |     |   |
|      | E3  |     |   |

**表 6-1. Pin Functions (continued)**

| PIN    |     | I/O | DESCRIPTION  |
|--------|-----|-----|--|
| NAME   | NO. |     |  |
| GND    | A4  | P   | <b>Ground Return</b>   |
|        | B4  |     |  |
|        | C4  |     |  |
|        | D4  |     |  |
|        | E4  |     |  |
| SW2    | A5  | P   | <b>Boost Side Half Bridge Switching Node</b>   |
|        | B5  |     |  |
|        | C5  |     |  |
|        | D5  |     |  |
|        | E5  |     |  |
| SYS    | A6  | P   | <b>The Charger Output Voltage to System</b> – The internal N-channel high-side MOSFET (Q4) is connected between SYS and SW2 with drain on SYS and source on SW2. Place a 0.1- $\mu$ F ceramic capacitor from SYS to power GND as close as possible to the charger IC. The recommended capacitors at SYS are five piece of 10- $\mu$ F and one piece of 0.1- $\mu$ F ceramic capacitors.                |
|        | B6  |     |  |
|        | C6  |     |  |
|        | D6  |     |  |
|        | E6  |     |  |
| BAT    | A7  | P   | <b>The Battery Charging Power Connection</b> – Connect to the positive terminal of the battery pack. The internal charging current sensing circuit is connected between SYS and BAT. The recommended capacitors at BAT are two piece of 10- $\mu$ F ceramic capacitors.  |
|        | B7  |     |  |
|        | C7  |     |  |
|        | D7  |     |  |
|        | E7  |     |  |
| BTST1  | D1  | P   | <b>Input High Side Power MOSFET Gate Driver Power Supply</b> – Connect a 10-V or higher rating, 47-nF ceramic capacitor between SW1 and BTST1 as the bootstrap capacitor for driving high-side switching MOSFET (Q1).  |
| REGN   | E1  | P   | <b>The Charger Internal Linear Regulator Output</b> – It is supplied from either VBUS or BAT dependent on which voltage is higher. Connect a 10-V, 4.7- $\mu$ F ceramic capacitor from REGN to power ground. The REGN LDO output is used for the internal MOSFETs gate driving voltage and the voltage bias for TS pin resistor divider.   |
| BTST2  | F7  | P   | <b>Output High Side Power MOSFET Gate Driver Power Supply</b> – Connect a 10-V or higher rating, 47-nF ceramic capacitor between SW2 and BTST2 as the bootstrap capacitor for driving high-side switching MOSFET (Q4).   |
| ACDRV1 | H2  | P   | <b>Input FETs Driver Pin 1</b> – The charge pump output to drive the port #1 input N-channel MOSFET (ACFET1) and the reverse blocking N-channel MOSFET (RBFET1). The charger turns on the back-to-back MOSFETs by increasing the ACDRV1 voltage 5 V above the common drain connection of the ACFET1 and RBFET1 when the turn-on condition is met. Tie ACDRV1 to GND if no ACFET1 and RBFET1 installed. |
| VAC1   | H1  | P   | <b>VAC1 Input Detection</b> – When a voltage between 3.6 V and 24 V apply on VAC1, it represents a valid input is plugged in port 1. Connect to VBUS if the ACFET1 and RBFET1 are not installed.   |
| ACDRV2 | G2  | P   | <b>Input FETs Driver Pin 2</b> – The charge pump output to drive the port #2 input N-channel MOSFET (ACFET2) and the reverse blocking N-channel MOSFET (RBFET2). The charger turns on the back-to-back MOSFETs by increasing the ACDRV2 voltage 5 V above the common drain connection of the ACFET2 and RBFET2 when the turn-on condition is met. Tie ACDRV2 to GND if no ACFET2 and RBFET2 installed. |
| VAC2   | G1  | P   | <b>VAC2 Input Detection</b> – When a voltage between 3.6 V and 24 V is applied on VAC2, it represents a valid input being plugged in port #2. Connect to VBUS if the ACFET2 and RBFET2 are not present.  |
| STAT   | F1  | DO  | <b>Open Drain Charge Status Output</b> – It indicates various charger operations. Connect to the pull up rail via 10-k $\Omega$ resistor. LOW indicates charging in progress. HIGH indicates charging completed or charging disabled. When any fault condition occurs, STAT pin blinks at 1Hz. The STAT pin function can be disabled when DIS_STAT bit is set to 1.                                    |
| PG     | H3  | DO  | <b>Open Drain Active Low Power Good Indicator</b> – Connected to the pull up rail via 10-k $\Omega$ resistor. LOW indicates a good input source if the VBUS voltage is above 3.6 V and below 24 V.   |

表 6-1. Pin Functions (continued)

| PIN      |     | I/O | DESCRIPTION  |
|----------|-----|-----|--|
| NAME     | NO. |     |  |
| D+       | F2  | AIO | <b>Positive Line of the USB Data Line Pair</b> – D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2, and the adjustable high voltage adapter.   |
| D-       | F3  | AIO | <b>Negative Line of the USB Data Line Pair</b> – D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2, and the adjustable high voltage adapter.   |
| SDRV     | F6  | P   | <b>External N-channel Ship FET (SFET) Gate Driver Output</b> – The driver pin of the external ship FET. The ship FET is always turned on when the ship mode is disabled, and it keeps off when the charger is in ship mode or shutdown mode. Connect a 0402 / 50-V / 1-nF ceramic capacitor from SDRV to GND when the ship FET is not used.  |
| QON      | G3  | DI  | <b>Ship FET Enable or System Power Reset Control Input</b> – When the device is in ship mode or in the shutdown mode, the SDRV turns off the external ship FET to minimize the battery leakage current. A logic low on this pin with $t_{SM\_EXIT}$ duration turns on ship FET to force the device exit the ship mode. A logic low on this pin with $t_{RST}$ duration resets system power by turning off the ship FET for $t_{RST\_SFET}$ (also set the charger in HIZ mode when VBUS is high) and then turning on ship FET (also disable the charger HIZ mode) to provide full system power reset. During $t_{RST\_SFET}$ when the ship FET is off, the charger applies a 30-mA discharging current on SYS to discharge system voltage. The pin contains an internal pull-up to maintain default high logic. |
| PROG     | F5  | DI  | <b>Charger POR Default Settings Program</b> – At power up, the charger detects the resistance tied to PROG pin to determine the default switching frequency and the default battery charging profile. The surface mount resistor with $\pm 1\%$ or $\pm 2\%$ tolerance is recommended. Please refer to more details in the section of PROG Pin Configuration.  |
| SCL      | H4  | DI  | <b>I<sup>2</sup>C Interface Clock</b> – Connect SCL to the logic rail through a 10-k $\Omega$ resistor.  |
| SDA      | H5  | DIO | <b>I<sup>2</sup>C Interface Data</b> – Connect SDA to the logic rail through a 10-k $\Omega$ resistor.   |
| INT      | G5  | DO  | <b>Open Drain Interrupt Output.</b> – Connect the $\overline{INT}$ pin to a logic rail via a 10-k $\Omega$ resistor. The $\overline{INT}$ pin sends an active low, 256- $\mu$ s pulse to the host to report the charger device status and faults.  |
| ILIM_HIZ | F4  | AI  | <b>Input Current Limit Setting and HIZ Mode Control Pin</b> – Program ILIM_HIZ voltage by connecting a resistor divider from pull up rail to ILIM_HIZ pin to ground. The pin voltage is calculated as: $V_{(ILIM\_HIZ)} = 1\text{ V} + 800\text{ m}\Omega \times I_{INDPM}$ , in which $I_{INDPM}$ is the target input current. The input current limit used by the charger is the lower setting of ILIM_HIZ pin and the IINDPM register. When the pin voltage is below 0.75 V, the buck-boost converter enters non-switching mode with REGN on. When the pin voltage is above 1 V, the converter resumes switching.   |
| IBAT     | H6  | AO  | <b>Charging Current Sensing Output</b> – A current source output pin with the output current value as a ratio of charging current. The typical ratio is 25- $\mu$ A output current when the charging current is 1 A. The recommended application case is connecting this pin to GND through a 10-k $\Omega$ resistor, in order to achieve a 250 mV/A voltage to charging current gain. The maximum voltage at this pin is clamped at 3.3 V.  |
| CE       | G4  | DI  | <b>Active Low Charge Enable Pin</b> – Battery charging is enabled when EN_CHG bit is 1 and $\overline{CE}$ pin is LOW. $\overline{CE}$ pin must be pulled HIGH or LOW, do not leave floating.  |
| BATP     | G7  | P   | <b>Positive Input for Battery Voltage Sensing</b> – Connect to the positive terminal of battery pack. Place 100- $\Omega$ series resistance between this pin and the battery positive terminal.  |
| BATN     | G6  | AI  | <b>Negative Input for Battery Voltage Sensing</b> – Connect to the negative terminal of battery pack. Place 100- $\Omega$ series resistance between this pin and the battery negative terminal.  |
| TS       | H7  | AI  | <b>Temperature Qualification Voltage Input</b> – Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS to GND. Charge suspends when TS pin voltage is out of range. Recommend a 103AT-2 10-k $\Omega$ thermistor.  |

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                     |  | MIN       | MAX | UNIT |
|-------------------------------------|--|-----------|-----|------|
| Voltage range (with respect to GND) | VAC1, VAC2   | -2        | 30  | V    |
|                                     | VBUS (converter not switching)   | -2        | 30  | V    |
|                                     | PMID (converter not switching)   | -0.3      | 30  | V    |
|                                     | ACDRV1, ACDRV2, BTST1  | -0.3      | 32  | V    |
|                                     | SYS (converter not switching)  | -0.3      | 23  | V    |
|                                     | BATP, BAT  | -0.3      | 20  | V    |
|                                     | BTST2  | -0.3      | 29  | V    |
|                                     | SDRV   | -0.3      | 26  | V    |
|                                     | SW1  | -2 (50ns) | 30  | V    |
|                                     | SW2  | -2 (50ns) | 23  | V    |
|                                     | PG, QON, D+, D-, CE, STAT, SCL, SDA, INT, ILIM_HIZ, PROG, TS, REGN, IBAT, BATN | -0.3      | 6   | V    |
| Output Sink Current                 | INT, STAT  |           | 6   | mA   |
| Differential Voltage                | BTST1-SW1, BTST2-SW2   | -0.3      | 6   | V    |
|                                     | PMID-VBUS  | -0.3      | 6   | V    |
|                                     | SYS-BAT  | -0.3      | 16  | V    |
|                                     | SDRV-BAT   | -0.3      | 6   | V    |
| T <sub>J</sub>                      | Junction temperature   | -40       | 150 | °C   |
| T <sub>stg</sub>                    | Storage temperature  | -55       | 150 | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

|                    |                         |  | VALUE | UNIT |
|--------------------|-------------------------|--|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              | ±2000 | V    |
|                    |                         | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> | ±250  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                   |                                      | MIN | NOM | MAX  | UNIT |
|-------------------|--------------------------------------|-----|-----|------|------|
| V <sub>VBUS</sub> | Input voltage                        | 3.6 |     | 24   | V    |
| V <sub>BAT</sub>  | Battery voltage                      |     |     | 18.8 | V    |
| I <sub>VBUS</sub> | Input current                        |     |     | 3.3  | A    |
| I <sub>SW</sub>   | Output current (SW)                  |     |     | 5    | A    |
| I <sub>BAT</sub>  | Fast charging current                |     |     | 5    | A    |
|                   | RMS discharge current (continuously) |     |     | 6    | A    |
|                   | Peak discharge current (up to 1 sec) |     |     | 10   | A    |
| T <sub>A</sub>    | Ambient temperature                  | -40 |     | 85   | °C   |
| T <sub>J</sub>    | Junction temperature                 | -40 |     | 125  | °C   |



### 7.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

|            |                            | MIN | NOM | MAX | UNIT          |
|------------|----------------------------|-----|-----|-----|---------------|
| $C_{VBUS}$ | Effective VBUS capacitance |     | 2   |     | $\mu\text{F}$ |
| $C_{PMID}$ | Effective PMID capacitance |     | 4   |     | $\mu\text{F}$ |
| $C_{SYS}$  | Effective SYS capacitance  |     | 6   |     | $\mu\text{F}$ |
| $C_{BAT}$  | Effective BAT capacitance  |     | 3   |     | $\mu\text{F}$ |

### 7.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | BQ24179     | UNIT |
|-------------------------------|--|-------------|------|
|                               |  | YBG (DSBGA) |      |
|                               |  | 56-BALL     |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 46.1        | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 0.2         | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 9.5         | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.1         | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 9.3         | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | N/A         | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 7.5 Electrical Characteristics

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$ ,  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , and  $T_J = 25^{\circ}\text{C}$  for typical values (unless otherwise noted)

| PARAMETER                 |  | TEST CONDITIONS   | MIN | TYP | MAX | UNIT          |
|---------------------------|--|---|-----|-----|-----|---------------|
| <b>QUIESCENT CURRENTS</b> |  |   |     |     |     |               |
| $I_{Q\_BAT\_ON}$          | Quiescent battery current (BATP, BAT, SYS) when the charger is in the battery only mode, battery FET is enabled, ADC is disabled | VBAT = 8V, No VBUS, BATFET is enabled, I2C enabled, ADC disabled, system is powered by battery. |     | 30  |     | $\mu\text{A}$ |
| $I_{Q\_BAT\_OFF}$         | Quiescent battery current (BATP) when the charger is in ship mode.   | VBAT = 8V, No VBUS, I2C enabled, ADC disabled, in ship mode.                                    |     | 20  |     | $\mu\text{A}$ |
| $I_{SD\_BAT}$             | Shutdown battery current (BATP) when charger is in shut down mode.   | VBAT = 8V, No VBUS, I2C disabled, ADC disabled, in shut down mode.                              |     |     | 0.7 | $\mu\text{A}$ |
| $I_{Q\_VBUS}$             | Quiescent input current (VBUS)   | VBUS = 15V, VBAT = 8V, charge disabled, converter switching, ISYS = 0A, OOA disabled            |     | 3   |     | mA            |
|                           |  | VBUS = 15V, VBAT = 8V, charge disabled, converter switching, ISYS = 0A, OOA enabled             |     | 5   |     | mA            |
| $I_{SD\_VBUS}$            | Shutdown input current (VBUS) in HIZ   | VBUS = 5V, HIZ mode, no battery, ADC disabled, ACDRV disabled                                   |     | 354 |     | $\mu\text{A}$ |
| <b>VBUS / VBAT SUPPLY</b> |  |   |     |     |     |               |
| $V_{VAC\_PRESENT}$        | VAC present rising threshold to turnon the ACFET-RBFET   | For both VAC1 and VAC2  |     | 3.4 | 3.5 | V             |
|                           | VAC present falling threshold to turnoff the ACFET-RBFET   | For both VAC1 and VAC2  | 3.1 | 3.2 |     | V             |



## 7.5 Electrical Characteristics (continued)

 $V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$ ,  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , and  $T_J = 25^{\circ}\text{C}$  for typical values (unless otherwise noted)

|                              | PARAMETER   | TEST CONDITIONS                                  | MIN  | TYP  | MAX  | UNIT |
|------------------------------|---|--|------|------|------|------|
| $V_{VAC\_OVP}$               | VAC overvoltage rising threshold, when VAC_OVP[1:0]=00            | For both VAC1 and VAC2                           | 25.2 | 26   | 26.8 | V    |
|                              | VAC overvoltage falling threshold, when VAC_OVP[1:0]=00           | For both VAC1 and VAC2                           | 24.4 | 25.2 | 26.0 | V    |
|                              | VAC overvoltage rising threshold, when VAC_OVP[1:0]=01            | For both VAC1 and VAC2                           | 21.1 | 21.7 | 22.3 | V    |
|                              | VAC overvoltage falling threshold, when VAC_OVP[1:0]=01           | For both VAC1 and VAC2                           | 20.6 | 21.2 | 21.8 | V    |
|                              | VAC overvoltage rising threshold, when VAC_OVP[1:0]=10            | For both VAC1 and VAC2                           | 11.6 | 12   | 12.4 | V    |
|                              | VAC overvoltage falling threshold, when VAC_OVP[1:0]=10           | For both VAC1 and VAC2                           | 11.2 | 11.6 | 12.0 | V    |
|                              | VAC overvoltage rising threshold, when VAC_OVP[1:0]=11            | For both VAC1 and VAC2                           | 6.7  | 7    | 7.3  | V    |
|                              | VAC overvoltage falling threshold, when VAC_OVP[1:0]=11           | For both VAC1 and VAC2                           | 6.5  | 6.8  | 7.1  | V    |
| $V_{VBUS\_OP}$               | VBUS operating range  |  | 3.6  |      | 24   | V    |
| $V_{VBUS\_UVLOZ}$            | VBUS rising for active I2C, no battery                            | VBUS rising                                      | 3.25 | 3.4  | 3.55 | V    |
| $V_{VBUS\_UVLO}$             | VBUS falling to turnoff I2C, no battery                           | VBUS falling                                     | 3.05 | 3.2  | 3.35 | V    |
| $V_{VBUS\_PRESENT}$          | VBUS to start switching   | VBUS rising                                      | 3.3  | 3.4  | 3.5  | V    |
| $V_{VBUS\_PRESENTZ}$         | VBUS to stop switching  | VBUS falling                                     | 3.1  | 3.2  | 3.3  | V    |
| $V_{VBUS\_OVP}$              | VBUS overvoltage rising threshold                                 | VBUS rising                                      | 25.2 | 25.7 | 26.2 | V    |
| $V_{VBUS\_OVPZ}$             | VBUS overvoltage falling threshold                                | VBUS falling                                     | 24.0 | 24.4 | 24.8 | V    |
| $I_{BUS\_OCP}$               | IBUS over-current rising threshold                                |  | 7.0  | 8.0  | 9.0  | A    |
| $I_{BUS\_OCPZ}$              | IBUS over-current falling threshold                               |  | 6.5  | 7.5  | 8.5  | A    |
| $V_{BAT\_UVLOZ}$             | BAT voltage for active I2C and turning on BATFET, no VBUS, no VAC | VBAT rising, when the charger is in ship mode    | 3.25 | 3.40 | 3.55 | V    |
|                              |   | VBAT rising, when the charger is in normal mode  | 2.50 | 2.60 | 2.71 | V    |
| $V_{BAT\_UVLO}$              | BAT voltage to turn off I2C and BATFET, no VBUS, no VAC           | VBAT falling, when the charger is in ship mode   | 3.05 | 3.20 | 3.31 | V    |
|                              |   | VBAT falling, when the charger is in normal mode | 2.30 | 2.40 | 2.50 | V    |
| $V_{POORSRC}$                | Bad adapter detection threshold                                   | VBUS falling                                     | 3.3  | 3.4  | 3.5  | V    |
| $V_{POORSRC}$                | Bad adapter detection threshold hysteresis                        | VBUS rising above $V_{POORSRC}$                  | 150  | 200  | 250  | mV   |
| $I_{POORSRC}$                | Bad adapter detection current source                              |  |      | 30   |      | mA   |
| <b>POWER-PATH MANAGEMENT</b> |   |  |      |      |      |      |
| $V_{SYS\_MAX\_REG\_RNG}$     | System voltage regulation range, measured on SYS                  |  | 3.2  |      | 19   | V    |

## 7.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$ ,  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , and  $T_J = 25^{\circ}\text{C}$  for typical values (unless otherwise noted)

| PARAMETER               |   | TEST CONDITIONS   | MIN   | TYP   | MAX   | UNIT |
|-------------------------|---|---|-------|-------|-------|------|
| $V_{SYSMAX\_REG\_ACC}$  | System voltage regulation accuracy (when $V_{BAT} > V_{SYSMIN}$ , charging disabled, PFM disabled)  | $V_{BAT} = 16.8\text{V}$ (4s default)   | 16.82 | 17.00 | 17.25 | V    |
|                         |   | $V_{BAT} = 12.6\text{V}$ (3s default)   | 12.62 | 12.80 | 13.04 | V    |
|                         |   | $V_{BAT} = 8.4\text{V}$ (2s default)  | 8.44  | 8.60  | 8.77  | V    |
|                         |   | $V_{BAT} = 4.2\text{V}$ (1s default)  | 4.268 | 4.40  | 4.550 | V    |
| $V_{SYSMIN\_REG\_RNG}$  | $V_{SYSMIN}$ regulation range, measured on SYS  |   | 2.5   |       | 16    | V    |
| $V_{SYSMIN\_REG\_STEP}$ | $V_{SYSMIN}$ regulation step size   |   |       | 250   |       | mV   |
| $V_{SYSMIN\_REG\_ACC}$  | System voltage regulation accuracy (when $V_{BAT} < V_{SYSMIN}$ )   | 4s battery  | 11.9  | 12.2  | 12.5  | V    |
|                         |   | 3s battery  | 9.0   | 9.2   | 9.4   | V    |
|                         |   | 2s battery  | 7.12  | 7.2   | 7.32  | V    |
|                         |   | 1s battery  | 3.5   | 3.7   | 3.9   | V    |
| $V_{SYS\_OVP}$          | VSYS overvoltage rising threshold   | As a percentage of the system regulation voltage, to turnoff the converter.   | 105.5 | 110.0 | 112.3 | %    |
|                         | VSYS overvoltage falling threshold  | As a percentage of the system regulation voltage, to re-enable the converter. | 95.5  | 100   | 102   | %    |
| $V_{SYS\_SHORT}$        | VSYS short voltage falling threshold  |   | 2.1   | 2.2   | 2.3   | V    |
| <b>BATTERY CHARGER</b>  |   |   |       |       |       |      |
| $V_{REG\_RANGE}$        | Typical charge voltage regulation range   |   | 3     |       | 18.8  | V    |
| $V_{REG\_STEP}$         | Typical charge voltage step   |   |       | 10    |       | mV   |
| $V_{REG\_ACC}$          | Charge voltage accuracy, $T_J = -40^{\circ}\text{C} - 85^{\circ}\text{C}$   | $V_{REG} = 16.8\text{V}$  | -1.0  |       | 1.0   | %    |
|                         |   | $V_{REG} = 12.6\text{V}$  | -1.0  |       | 1.0   | %    |
|                         |   | $V_{REG} = 8.4\text{V}$   | -1.0  |       | 1.0   | %    |
|                         |   | $V_{REG} = 4.2\text{V}$   | -1.0  |       | 1.0   | %    |
| $I_{CHG\_RANGE}$        | Typical charge current regulation range   |   | 0.05  |       | 5     | A    |
| $I_{CHG\_STEP}$         | Typical charge current regulation step  |   |       | 10    |       | mA   |
| $I_{CHG\_ACC}$          | Typical boost mode PWM charge current accuracy, $V_{BUS} < V_{BAT}$ , $T_J = -40^{\circ}\text{C} - 85^{\circ}\text{C}$  | $ICHG = 2\text{A}$ ; $V_{BAT}=8\text{V}$                                      | -10   |       | 10    | %    |
|                         |   | $ICHG = 1\text{A}$ ; $V_{BAT}=8\text{V}$                                      | -10   |       | 10    | %    |
|                         |   | $ICHG = 0.5\text{A}$ ; $V_{BAT}=8\text{V}$                                    | -10   |       | 10    | %    |
| $I_{CHG\_ACC}$          | Typical buck mode PWM charge current accuracy, $V_{BUS} > V_{BAT}$ , $T_J = -40^{\circ}\text{C} - 85^{\circ}\text{C}$   | $ICHG = 4\text{A}$ ; $V_{BAT}=8\text{V}$                                      | -10   |       | 10    | %    |
|                         |   | $ICHG = 1\text{A}$ ; $V_{BAT}=8\text{V}$                                      | -10   |       | 10    | %    |
|                         |   | $ICHG = 0.5\text{A}$ ; $V_{BAT}=8\text{V}$                                    | -10   |       | 10    | %    |
| $I_{PRECHG\_RANGE}$     | Typical pre-charge current range  |   | 40    |       | 2000  | mA   |
| $I_{PRECHG\_STEP}$      | Typical pre-charge current step   |   |       | 40    |       | mA   |
| $I_{PRECHG\_ACC}$       | Typical LDO mode charge current accuracy when $V_{BATP}-V_{BATN}$ below $V_{SYSMIN}$ , $V_{BUS} < V_{BAT}$ , $T_J = -40^{\circ}\text{C} - 85^{\circ}\text{C}$ | $IPRECHG = 480\text{mA}$ , $V_{BAT} = 6.5\text{V}$                            | -10   |       | 10    | %    |
|                         |   | $IPRECHG = 200\text{mA}$ , $V_{BAT} = 6.5\text{V}$                            | -20   |       | 20    | %    |
|                         |   | $IPRECHG = 120\text{mA}$ , $V_{BAT} = 6.5\text{V}$                            | -35   |       | 35    | %    |
| $I_{PRECHG\_ACC}$       | Typical LDO mode charge current accuracy when $V_{BATP}-V_{BATN}$ below $V_{SYSMIN}$ , $V_{BUS} > V_{BAT}$ , $T_J = -40^{\circ}\text{C} - 85^{\circ}\text{C}$ | $IPRECHG = 1000\text{mA}$ , $V_{BAT} = 6.5\text{V}$                           | -10   |       | 10    | %    |
|                         |   | $IPRECHG = 200\text{mA}$ , $V_{BAT} = 6.5\text{V}$                            | -20   |       | 20    | %    |
|                         |   | $IPRECHG = 120\text{mA}$ , $V_{BAT} = 6.5\text{V}$                            | -30   |       | 30    | %    |

## 7.5 Electrical Characteristics (continued)

 $V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$ ,  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , and  $T_J = 25^{\circ}\text{C}$  for typical values (unless otherwise noted)

| PARAMETER                          |   | TEST CONDITIONS  | MIN  | TYP  | MAX  | UNIT |
|------------------------------------|---|--|------|------|------|------|
| I <sub>BAT_ACC</sub>               | IBAT pin current sensing accuracy with 25μA/A gain. The accuracy is applied to forward charging mode for charging current sensing, T <sub>J</sub> = - 40°C - 85°C | IBAT = 4A, VBAT = 8V   | -5   |      | 5    | %    |
|                                    |   | IBAT = 1A, VBAT = 8V   | -10  |      | 10   | %    |
|                                    |   | IBAT = 0.5A, VBAT = 8V   | -20  |      | 20   | %    |
| I <sub>TERM_RANGE</sub>            | Typical termination current range   |  | 40   |      | 1000 | mA   |
| I <sub>TERM_STEP</sub>             | Typical termination current step  |  |      | 40   |      | mA   |
| I <sub>TERM_ACC</sub>              | Termination current accuracy, T <sub>J</sub> = - 40°C - 85°C  | ITERM = 120mA  | -20  |      | 20   | %    |
|                                    |   | ITERM = 480mA  | -14  |      | 14   | %    |
| V <sub>BAT_SHORTZ</sub>            | Battery short voltage rising threshold to start pre-charge  | VBAT rising  |      | 2.25 |      | V    |
| V <sub>BAT_SHORT</sub>             | Battery short voltage falling threshold to stop pre-charge  | VBAT falling   |      | 2.06 |      | V    |
| I <sub>BAT_SHORT</sub>             | Battery trickle charging current  | VBAT < V <sub>BAT_SHORTZ</sub>   |      | 100  |      | mA   |
| V <sub>BAT_LOWV_RISE</sub>         | Battery voltage rising threshold to start fast-charge, as percentage of V <sub>REG</sub>  | VBAT_LOWV=15%VREG, VBAT_LOWV_1:0=00                                      | 13   | 15   | 17   | %    |
|                                    |   | VBAT_LOWV=62.2%VREG, VBAT_LOWV_1:0=01                                    | 61.5 | 63.0 | 64.5 | %    |
|                                    |   | VBAT_LOWV=66.7%VREG, VBAT_LOWV_1:0=10                                    | 67.0 | 68.0 | 69.0 | %    |
|                                    |   | VBAT_LOWV=71.4%VREG, VBAT_LOWV_1:0=11                                    | 71.0 | 72.5 | 74.0 | %    |
| V <sub>BAT_LOWV_HYS</sub>          | Battery voltage threshold to stop fast-charge hysteresis  | VBAT falling, as percentage of VREG, VBAT_LOWV_1:0=11                    |      | 1.4  |      | %    |
| V <sub>RECHG</sub>                 | Battery recharge threshold  | VBAT falling, VRECHG=0011, VREG=8.4V                                     |      | 200  |      | mV   |
|                                    |   | VBAT falling, VRECHG=0111, VREG=16.8V                                    |      | 400  |      | mV   |
| BATFET                             |   |  |      |      |      |      |
| R <sub>BATFET</sub>                | MOSFET on resistance from SYS to BAT  | T <sub>J</sub> = -40°C-85°C  |      | 8    | 9.69 | mΩ   |
| BATTERY PROTECTIONS                |   |  |      |      |      |      |
| V <sub>BAT_OVP</sub>               | Battery overvoltage threshold   | VBAT rising, as percentage of VREG                                       | 103  | 104  | 105  | %    |
|                                    |   | VBAT falling, as percentage of VREG                                      | 101  | 102  | 103  | %    |
| V <sub>BAT_SHORT</sub>             | Battery short voltage   | VBAT falling, to clamp the charging current as trickle charging current. |      | 2.06 |      | V    |
|                                    |   | VBAT rising, to release the trickle charging current clamp               |      | 2.25 |      | V    |
| I <sub>BAT_OCP</sub>               | Battery discharging over-current rising threshold   |  | 9.3  | 11.4 |      | A    |
| INPUT VOLTAGE / CURRENT REGULATION |   |  |      |      |      |      |
| V <sub>INDPM_RANGE</sub>           | Typical input voltage regulation range  |  | 3.6  |      | 22   | V    |
| V <sub>INDPM_STEP</sub>            | Typical input voltage regulation step   |  |      | 100  |      | mV   |
| V <sub>INDPM_ACC</sub>             | Input voltage regulation accuracy   | VINDPM=18.6V   | -2   |      | 2    | %    |
|                                    |   | VINDPM=10.6V   | -3   |      | 3    | %    |
|                                    |   | VINDPM=4.3V  | -5   |      | 5    | %    |
| I <sub>INDPM_RANGE</sub>           | Typical input current regulation range  |  | 0.1  |      | 3.3  | A    |

## 7.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$ ,  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , and  $T_J = 25^{\circ}\text{C}$  for typical values (unless otherwise noted)

| PARAMETER  |   | TEST CONDITIONS   | MIN  | TYP  | MAX  | UNIT               |
|--|---|---|------|------|------|--------------------|
| $I_{INDPM\_STEP}$                                | Typical input current regulation step                         |   |      | 10   |      | mA                 |
| $I_{INDPM\_ACC}$                                 | Input current regulation accuracy                             | $I_{INDPM} = 500\text{mA}$ , $V_{BUS} = 9\text{V}$                | 415  | 460  | 500  | mA                 |
|  |   | $I_{INDPM} = 1000\text{mA}$ , $V_{BUS} = 9\text{V}$               | 880  | 940  | 1000 | mA                 |
|  |   | $I_{INDPM} = 2000\text{mA}$ , $V_{BUS} = 9\text{V}$               | 1800 | 1880 | 1960 | mA                 |
|  |   | $I_{INDPM} = 3000\text{mA}$ , $V_{BUS} = 9\text{V}$               | 2720 | 2820 | 2920 | mA                 |
| $V_{ILIM\_REG\_RNG}$                             | Voltage range for input current regulation at $ILIM\_HIZ$ pin |   | 1    |      | 4    | V                  |
| $I_{LEAK\_ILIM}$                                 | $ILIM\_HIZ$ pin leakage current                               | $V_{ILIM\_HIZ} = 4\text{V}$                                       | -1.5 |      | 1.5  | $\mu\text{A}$      |
| <b>D+ / D- DETECTION</b>                         |   |   |      |      |      |                    |
| $V_{D+\_600\text{MVSRC}}$                        | D+ voltage source (600 mV)                                    |   | 500  | 600  | 700  | mV                 |
| $I_{D+\_10\text{UASRC}}$                         | D+ current source (10 $\mu\text{A}$ )                         | $V_{D+} = 200\text{ mV}$ ,  | 7    | 10   | 14   | $\mu\text{A}$      |
| $I_{D+\_100\text{UASNK}}$                        | D+ current sink (100 $\mu\text{A}$ )                          | $V_{D+} = 500\text{ mV}$ ,  | 50   | 90   | 150  | $\mu\text{A}$      |
| $V_{D+\_0\text{P}325}$                           | D+ comparator threshold for Secondary Detection               | D+ pin rising, $DPDM\_NSCOMP2$                                    | 250  |      | 400  | mV                 |
| $V_{D+\_0\text{P}8}$                             | D+ comparator threshold for Data Contact Detection            | D+ pin rising, $DPDM\_NSCOMP2$                                    | 775  | 850  | 925  | mV                 |
| $I_{D+\_LKG}$                                    | Leakage current into D+                                       | HiZ mode  | -1   |      | 1    | $\mu\text{A}$      |
| $V_{D-\_600\text{MVSRC}}$                        | D- voltage source (600 mV)                                    |   | 500  | 600  | 700  | mV                 |
| $I_{D-\_100\text{UASNK}}$                        | D- current sink (100 $\mu\text{A}$ )                          | $V_{D-} = 500\text{ mV}$ ,  | 50   | 90   | 150  | $\mu\text{A}$      |
| $V_{D-\_0\text{P}325}$                           | D- comparator threshold for Primary Detection                 | D- pin Rising, $DPDM\_NSCOMP2$                                    | 250  |      | 400  | mV                 |
| $I_{D-\_LKG}$                                    | Leakage current into D-                                       | HiZ mode  | -1   |      | 1    | $\mu\text{A}$      |
| $V_{D+\_2\text{p}8}$                             | D+ comparator threshold for non-standard adapter              | (combined $V_{D+\_2\text{p}8\_hi}$ and $V_{D+\_2\text{p}8\_lo}$ ) | 2.55 |      | 2.85 | V                  |
| $V_{D-\_2\text{p}8}$                             | D- comparator threshold for non-standard adapter              | (combined $V_{D-\_2\text{p}8\_hi}$ and $V_{D-\_2\text{p}8\_lo}$ ) | 2.55 |      | 2.85 | V                  |
| $V_{D+\_2\text{p}0}$                             | D+ comparator threshold for non-standard adapter              | (combined $V_{D+\_2\text{p}0\_hi}$ and $V_{D+\_2\text{p}0\_lo}$ ) | 1.85 |      | 2.15 | V                  |
| $V_{D-\_2\text{p}0}$                             | D- comparator threshold for non-standard adapter              | (combined $V_{D-\_2\text{p}0\_hi}$ and $V_{D-\_2\text{p}0\_lo}$ ) | 1.85 |      | 2.15 | V                  |
| $V_{D+\_1\text{p}2}$                             | D+ comparator threshold for non-standard adapter              | (combined $V_{D+\_1\text{p}2\_hi}$ and $V_{D+\_1\text{p}2\_lo}$ ) | 1.05 |      | 1.35 | V                  |
| $V_{D-\_1\text{p}2}$                             | D- comparator threshold for non-standard adapter              | (combined $V_{D-\_1\text{p}2\_hi}$ and $V_{D-\_1\text{p}2\_lo}$ ) | 1.05 |      | 1.35 | V                  |
| <b>THERMAL REGULATION AND THERMAL SHUTDOWN</b>   |   |   |      |      |      |                    |
| $T_{REG}$  | Junction temperature regulation accuracy                      | $T_{REG} = 120^{\circ}\text{C}$                                   |      | 120  |      | $^{\circ}\text{C}$ |
|  |   | $T_{REG} = 100^{\circ}\text{C}$                                   |      | 100  |      | $^{\circ}\text{C}$ |
|  |   | $T_{REG} = 80^{\circ}\text{C}$                                    |      | 80   |      | $^{\circ}\text{C}$ |
|  |   | $T_{REG} = 60^{\circ}\text{C}$                                    |      | 60   |      | $^{\circ}\text{C}$ |
| $T_{SHUT}$                                       | Thermal Shutdown Rising Threshold                             | Temperature Increasing ( $TSHUT[1:0]=00$ )                        | 130  | 150  | 170  | $^{\circ}\text{C}$ |
|  |   | Temperature Increasing ( $TSHUT[1:0]=01$ )                        | 110  | 130  | 150  | $^{\circ}\text{C}$ |
|  |   | Temperature Increasing ( $TSHUT[1:0]=10$ )                        | 100  | 120  | 140  | $^{\circ}\text{C}$ |
|  |   | Temperature Increasing ( $TSHUT[1:0]=11$ )                        | 65   | 85   | 105  | $^{\circ}\text{C}$ |
| $T_{SHUT\_HYS}$                                  | Thermal Shutdown Falling Hysteresis                           | Temperature Decreasing by $T_{SHUT\_HYS}$                         |      | 30   |      | $^{\circ}\text{C}$ |
| <b>JEITA THERMISTOR COMPARATOR (CHARGE MODE)</b> |   |   |      |      |      |                    |

## 7.5 Electrical Characteristics (continued)

 $V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$ ,  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , and  $T_J = 25^{\circ}\text{C}$  for typical values (unless otherwise noted)

| PARAMETER                         |  | TEST CONDITIONS   | MIN  | TYP  | MAX  | UNIT |
|-----------------------------------|--|---|------|------|------|------|
| V <sub>T1_RISE</sub>              | T1 comparator rising threshold, charge suspended above this voltage.     | As Percentage to V <sub>REGN</sub> (0°C w/ 103AT)           | 72.4 | 73.3 | 74.2 | %    |
| V <sub>T1_FALL</sub>              | T1 comparator falling threshold, charge re-enabled below this voltage.   | As Percentage to V <sub>REGN</sub> (3°C w/ 103AT)           | 71.5 | 72   | 72.5 | %    |
| V <sub>T2_RISE</sub>              | T2 comparator rising threshold.  | As Percentage to V <sub>REGN</sub> , JEITA_T2=5°C w/ 103AT  | 70.6 | 71.1 | 71.6 | %    |
|                                   |  | As Percentage to V <sub>REGN</sub> , JEITA_T2=10°C w/ 103AT | 67.9 | 68.4 | 68.9 | %    |
|                                   |  | As Percentage to V <sub>REGN</sub> , JEITA_T2=15°C w/ 103AT | 65.0 | 65.5 | 66.0 | %    |
|                                   |  | As Percentage to V <sub>REGN</sub> , JEITA_T2=20°C w/ 103AT | 61.9 | 62.4 | 62.9 | %    |
| V <sub>T2_FALL</sub>              | T2 comparator falling threshold.   | As Percentage to V <sub>REGN</sub> , JEITA_T2=5°C w/ 103AT  | 69.3 | 69.8 | 70.3 | %    |
|                                   |  | As Percentage to V <sub>REGN</sub> , JEITA_T2=10°C w/ 103AT | 66.6 | 67.1 | 67.6 | %    |
|                                   |  | As Percentage to V <sub>REGN</sub> , JEITA_T2=15°C w/ 103AT | 63.7 | 64.2 | 64.7 | %    |
|                                   |  | As Percentage to V <sub>REGN</sub> , JEITA_T2=20°C w/ 103AT | 60.6 | 61.1 | 61.6 | %    |
| V <sub>T3_RISE</sub>              | T3 comparator rising threshold.  | As Percentage to V <sub>REGN</sub> , JEITA_T3=40°C w/ 103AT | 49.2 | 49.7 | 50.2 | %    |
|                                   |  | As Percentage to V <sub>REGN</sub> , JEITA_T3=45°C w/ 103AT | 45.6 | 46.1 | 46.6 | %    |
|                                   |  | As Percentage to V <sub>REGN</sub> , JEITA_T3=50°C w/ 103AT | 42.0 | 42.5 | 43.0 | %    |
|                                   |  | As Percentage to V <sub>REGN</sub> , JEITA_T3=55°C w/ 103AT | 38.5 | 39   | 39.5 | %    |
| V <sub>T3_FALL</sub>              | T3 comparator falling threshold.   | As Percentage to V <sub>REGN</sub> , JEITA_T3=40°C w/ 103AT | 47.9 | 48.4 | 48.9 | %    |
|                                   |  | As Percentage to V <sub>REGN</sub> , JEITA_T3=45°C w/ 103AT | 44.3 | 44.8 | 45.3 | %    |
|                                   |  | As Percentage to V <sub>REGN</sub> , JEITA_T3=50°C w/ 103AT | 40.7 | 41.2 | 41.7 | %    |
|                                   |  | As Percentage to V <sub>REGN</sub> , JEITA_T3=55°C w/ 103AT | 37.2 | 37.7 | 38.2 | %    |
| V <sub>T5_FALL</sub>              | T5 comparator falling threshold, charge suspended below this voltage.    | As Percentage to V <sub>REGN</sub> (60°C w/ 103AT)          | 33.7 | 34.2 | 34.7 | %    |
| V <sub>T5_RISE</sub>              | T5 comparator rising threshold, charge is re-enabled above this voltage. | As Percentage to V <sub>REGN</sub> (58°C w/ 103AT)          | 35   | 35.5 | 36   | %    |
| SWITCHING CONVERTER               |  |   |      |      |      |      |
| F <sub>SW</sub>                   | PWM switching frequency  |   | 1.3  | 1.5  | 1.7  | MHz  |
|                                   |  |   | 650  | 750  | 850  | kHz  |
| SENSE RESISTANCE and MOSFET Rdson |  |   |      |      |      |      |
| R <sub>SNS</sub>                  | VBUS to PMID input sensing resistance                                    | T <sub>j</sub> = -40°C-85°C                                 |      | 6    |      | m Ω  |
| R <sub>Q1_ON</sub>                | Buck high-side switching MOSFET turnon resistance between PMID and SW1   | T <sub>j</sub> = -40°C-85°C                                 |      | 20   |      | m Ω  |

## 7.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$ ,  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , and  $T_J = 25^{\circ}\text{C}$  for typical values (unless otherwise noted)

| PARAMETER   |  | TEST CONDITIONS                                    | MIN | TYP | MAX  | UNIT             |
|---|--|--|-----|-----|------|------------------|
| $R_{Q2\_ON}$  | Buck low-side switching MOSFET turnon resistance between SW1 and PGND  | $T_J = -40^{\circ}\text{C}$ - $85^{\circ}\text{C}$ |     | 30  |      | $\text{m}\Omega$ |
| $R_{Q3\_ON}$  | Boost low-side switching MOSFET turnon resistance between SW2 and PGND | $T_J = -40^{\circ}\text{C}$ - $85^{\circ}\text{C}$ |     | 22  |      | $\text{m}\Omega$ |
| $R_{Q4\_ON}$  | Boost high-side switching MOSFET turnon resistance between SW2 and SYS | $T_J = -40^{\circ}\text{C}$ - $85^{\circ}\text{C}$ |     | 13  |      | $\text{m}\Omega$ |
| <b>REGN LDO</b>   |  |  |     |     |      |                  |
| $V_{REGN}$  | REGN LDO output voltage  | $V_{VBUS} = 5\text{V}$ , $I_{REGN} = 20\text{mA}$  | 4.6 | 4.8 | 5    | V                |
|   |  | $V_{VBUS} = 15\text{V}$ , $I_{REGN} = 20\text{mA}$ | 4.8 | 5   | 5.2  | V                |
| $I_{REGN}$  | REGN LDO current limit   | $V_{VBUS} = 5\text{V}$ , $V_{REGN} = 4.5\text{V}$  | 30  |     |      | mA               |
| <b>I2C INTERFACE (SCL, SDA)</b>   |  |  |     |     |      |                  |
| $V_{IH\_SDA}$   | Input high threshold level, SDA  | Pull up rail 1.8V                                  | 1.3 |     |      | V                |
| $V_{IL\_SDA}$   | Input low threshold level  | Pull up rail 1.8V                                  |     |     | 0.4  | V                |
| $V_{OL\_SDA}$   | Output low threshold level   | Sink current = 5mA                                 |     |     | 0.4  | V                |
| $I_{BIAS\_SDA}$   | High-level leakage current   | Pull up rail 1.8V                                  |     |     | 1    | $\mu\text{A}$    |
| $V_{IH\_SCL}$   | Input high threshold level, SDA  | Pull up rail 1.8V                                  | 1.3 |     |      | V                |
| $V_{IL\_SCL}$   | Input low threshold level  | Pull up rail 1.8V                                  |     |     | 0.4  | V                |
| $V_{OL\_SCL}$   | Output low threshold level   | Sink current = 5mA                                 |     |     | 0.4  | V                |
| $I_{BIAS\_SCL}$   | High-level leakage current   | Pull up rail 1.8V                                  |     |     | 1    | $\mu\text{A}$    |
| <b>LOGIC I PIN ( <math>\overline{\text{CE}}</math>, <math>\text{ILIM\_HIZ}</math>, <math>\overline{\text{QON}}</math> )</b> |  |  |     |     |      |                  |
| $V_{IH\_CE}$  | Input high threshold level, $\overline{\text{CE}}$                     |  | 1.3 |     |      | V                |
| $V_{IL\_CE}$  | Input low threshold level, $\overline{\text{CE}}$                      |  |     |     | 0.4  | V                |
| $I_{IN\_BIAS\_CE}$  | High-level leakage current, $\overline{\text{CE}}$                     | Pull up rail 1.8V                                  |     |     | 1    | $\mu\text{A}$    |
| $V_{IH\_QON}$   | Input high threshold level, $\overline{\text{QON}}$                    |  | 1.3 |     |      | V                |
| $V_{IL\_QON}$   | Input low threshold level, $\overline{\text{QON}}$                     |  |     |     | 0.4  | V                |
| $V_{QON}$   | Internal $\overline{\text{QON}}$ pull up                               | $\overline{\text{QON}}$ is pulled up internally    |     | 3.2 |      | V                |
| $R_{QON}$   | Internal $\overline{\text{QON}}$ pull up resistance                    |  |     | 200 |      | $\text{k}\Omega$ |
| $V_{IH\_ILIM\_HIZ}$   | Input high threshold level, $\text{ILIM\_HIZ}$                         |  | 1   |     |      | V                |
| $V_{IL\_ILIM\_HIZ}$   | Input low threshold level, $\text{ILIM\_HIZ}$                          |  |     |     | 0.75 | V                |
| <b>LOGIC O PIN ( <math>\text{INT}</math>, <math>\overline{\text{PG}}</math>, <math>\text{STAT}</math> )</b>                 |  |  |     |     |      |                  |
| $V_{OL\_INT}$   | Output low threshold level, $\text{INT}$ pin                           | Sink current = 5mA                                 |     |     | 0.4  | V                |
| $I_{OUT\_BIAS\_INT}$  | High-level leakage current, $\text{INT}$ pin                           | Pull up rail 1.8V                                  |     |     | 1    | $\mu\text{A}$    |
| $V_{OL\_PG}$  | Output low threshold level, $\overline{\text{PG}}$ pin                 | Sink current = 5mA                                 |     |     | 0.4  | V                |
| $I_{OUT\_BIAS\_PG}$   | High-level leakage current, $\overline{\text{PG}}$ pin                 | Pull up rail 1.8V                                  |     |     | 1    | $\mu\text{A}$    |
| $V_{OL\_STAT}$  | Output low threshold level, $\text{STAT}$ pin                          | Sink current = 5mA                                 |     |     | 0.4  | V                |
| $I_{OUT\_BIAS\_STAT}$   | High-level leakage current, $\text{STAT}$ pin                          | Pull up rail 1.8V                                  |     |     | 1    | $\mu\text{A}$    |
| <b>ADC MEASUREMENT ACCURACY AND PERFORMANCE</b>   |  |  |     |     |      |                  |
| $t_{\text{ADC\_CONV}}$  | Conversion-time, Each Measurement                                      | ADC_SAMPLE[1:0] = 00                               |     | 24  |      | ms               |
|   |  | ADC_SAMPLE[1:0] = 01                               |     | 12  |      | ms               |
|   |  | ADC_SAMPLE[1:0] = 10                               |     | 6   |      | ms               |
|   |  | ADC_SAMPLE[1:0] = 11                               |     | 3   |      | ms               |

## 7.5 Electrical Characteristics (continued)

 $V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$ ,  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , and  $T_J = 25^{\circ}\text{C}$  for typical values (unless otherwise noted)

| PARAMETER                     |                             | TEST CONDITIONS      | MIN | TYP   | MAX  | UNIT |
|-------------------------------|-----------------------------|----------------------|-----|-------|------|------|
| ADC <sub>RES</sub>            | Effective Resolution        | ADC_SAMPLE[1:0] = 00 | 14  | 15    |      | bits |
|                               |                             | ADC_SAMPLE[1:0] = 01 | 13  | 14    |      | bits |
|                               |                             | ADC_SAMPLE[1:0] = 10 | 12  | 13    |      | bits |
|                               |                             | ADC_SAMPLE[1:0] = 11 | 10  | 11    |      | bits |
| ADC MEASUREMENT RANGE AND LSB |                             |                      |     |       |      |      |
| IBUS_ADC                      | ADC Bus Current Reading     | Range                | 0   |       | 5    | A    |
|                               |                             | LSB                  |     | 1     |      | mA   |
| VBUS_ADC                      | ADC Bus Voltage Reading     | Range                | 0   |       | 30   | V    |
|                               |                             | LSB                  |     | 1     |      | mV   |
| VAC_ADC                       | ADC VAC Voltage Reading     | Range                | 0   |       | 30   | V    |
|                               |                             | LSB                  |     | 1     |      | mV   |
| VBAT_ADC                      | ADC BAT Voltage Reading     | Range                | 0   |       | 20   | V    |
|                               |                             | LSB                  |     | 1     |      | mV   |
| VSYST_ADC                     | ADC SYS Voltage Reading     | Range                | 0   |       | 24   | V    |
|                               |                             | LSB                  |     | 1     |      | mV   |
| IBAT_ADC                      | ADC BAT Current Reading     | Range                | 0   |       | 8    | A    |
|                               |                             | LSB                  |     | 1     |      | mA   |
| TS_ADC                        | ADC TS Voltage Reading      | Range                | 0   |       | 99.9 | %    |
|                               |                             | LSB                  |     | 0.098 |      | %    |
| TDIE_ADC                      | ADC Die Temperature Reading | Range                | -40 |       | 150  | °C   |
|                               |                             | LSB                  |     | 0.5   |      | °C   |

## 7.6 Timing Requirements

| PARAMETER                  |   | TEST CONDITIONS | MIN  | NOM | MAX  | UNIT |
|----------------------------|---|-----------------|------|-----|------|------|
| <b>BATTERY CHARGER</b>     |   |                 |      |     |      |      |
| t <sub>TOP_OFF</sub>       | Typical top-off timer accuracy                      |                 | 12   | 15  | 18   | min  |
|                            |   |                 | 24   | 30  | 36   | min  |
|                            |   |                 | 36   | 45  | 54   | min  |
| t <sub>SAFETY_TRKCHG</sub> | Charge safety timer in trickle charge               |                 | 0.9  | 1   | 1.1  | hr   |
| t <sub>SAFETY_PRECHG</sub> | Charge safety timer in pre-charge, PRECHG_TMR = 1hr |                 | 1.8  | 2   | 2.2  | hr   |
| t <sub>SAFETY</sub>        | Charge safety timer accuracy, CHG_TMR = 5hr         |                 | 4.5  | 5   | 5.5  | hr   |
|                            | Charge safety timer accuracy, CHG_TMR = 8hr         |                 | 7.2  | 8   | 8.8  | hr   |
|                            | Charge safety timer accuracy, CHG_TMR = 12hr        |                 | 10.8 | 12  | 13.2 | hr   |
|                            | Charge safety timer accuracy, CHG_TMR = 24hr        |                 | 21.6 | 24  | 26.4 | hr   |
| <b>THERMAL SHUTDOWN</b>    |   |                 |      |     |      |      |
| <b>I2C INTERFACE</b>       |   |                 |      |     |      |      |
| f <sub>SCL</sub>           | SCL clock frequency                                 |                 |      |     | 1000 | kHz  |
| <b>WATCHDOG TIMER</b>      |   |                 |      |     |      |      |
| t <sub>LP_WDT</sub>        | Watchdog Reset time (EN_HIZ = 1, WATCHDOG = 160s)   |                 | 100  | 160 |      | s    |

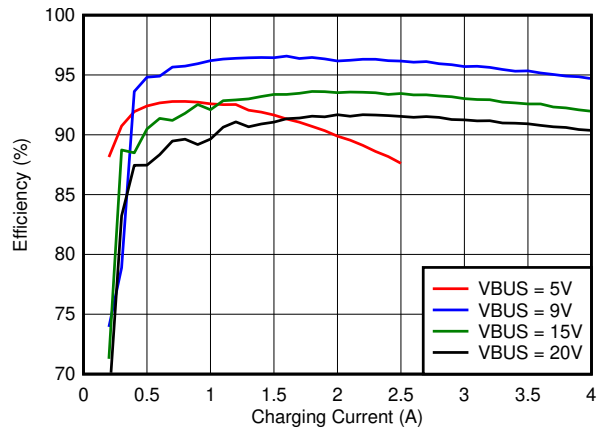


## 7.6 Timing Requirements (continued)

| PARAMETER        |   | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|------------------|---|-----------------|-----|-----|-----|------|
| $t_{\text{WDT}}$ | Watchdog Reset time (EN_HIZ = 0, WATCHDOG = 160s) |                 | 136 | 160 |     | s    |

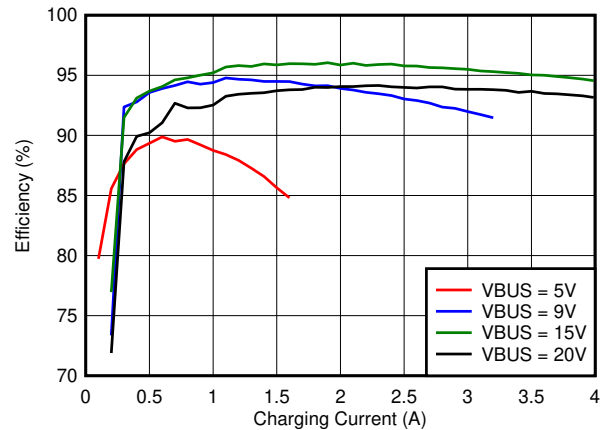
## 7.7 Typical Characteristics

$C_{VBUS} = 2 \times 10 \mu\text{F}$ ,  $C_{PMID} = 3 \times 10 \mu\text{F}$ ,  $C_{SYS} = 5 \times 10 \mu\text{F}$ ,  $C_{BAT} = 2 \times 10 \mu\text{F}$ ,  $L1 = 1 \mu\text{H}$  (SPM6530T-1R0M120) and  $L2 = 2.2 \mu\text{H}$  (WE-LHMI-74437346022)



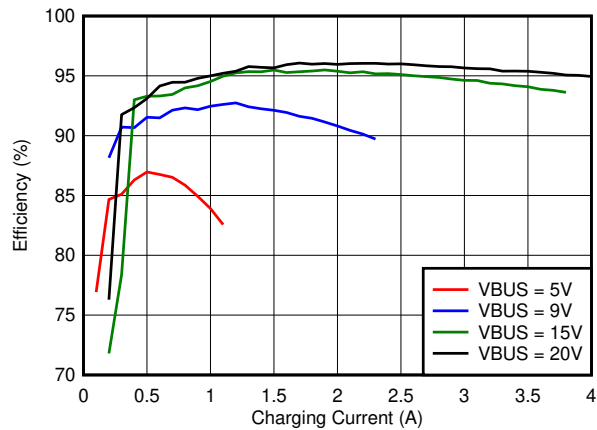
VBAT = 8 V, Fsw = 1.5 MHz with L1 = 1  $\mu\text{H}$ , PFM disabled

**图 7-1. 2s Battery Charge Efficiency vs. Charge Current**



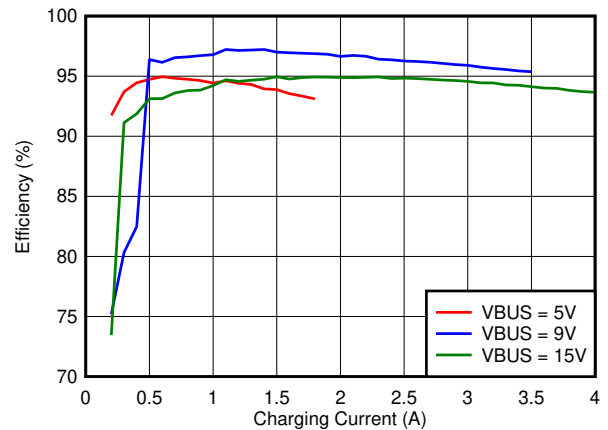
VBAT = 12 V, Fsw = 1.5 MHz with L1 = 1  $\mu\text{H}$ , PFM disabled

**图 7-2. 3s Battery Charge Efficiency vs. Charge Current**



VBAT = 16 V, Fsw = 1.5 MHz with L1 = 1  $\mu\text{H}$ , PFM disabled

**图 7-3. 4s Battery Charge Efficiency vs. Charge Current**



VBAT = 8 V, Fsw = 750 kHz with L2 = 2.2  $\mu\text{H}$ , PFM disabled

**图 7-4. 2s Battery Charge Efficiency vs. Charge Current**

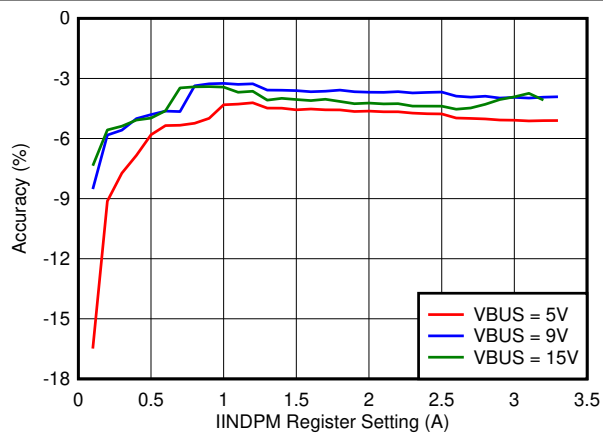


图 7-5. Input Current Regulation (IINDPM) Accuracy

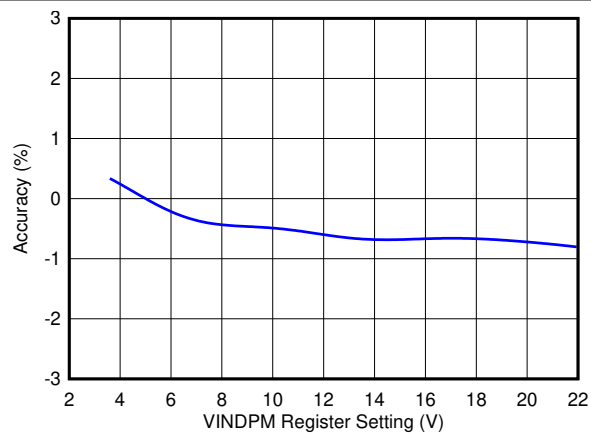


图 7-6. Input Voltage Regulation (VINDPM) Accuracy

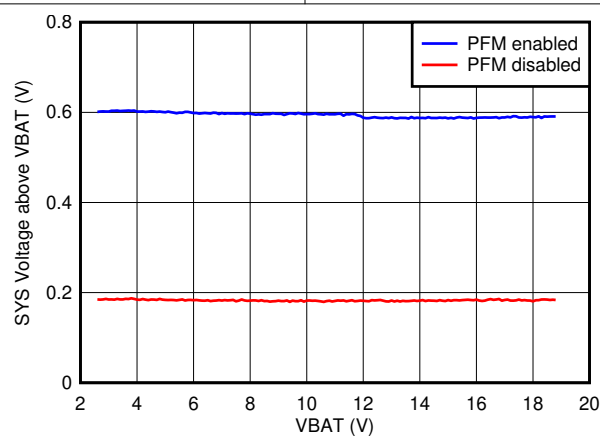


图 7-7. Offset Voltage of SYS Regulation Above VBAT

## 8 Detailed Description

### 8.1 Overview

The BQ24179 is a fully integrated switch-mode buck-boost charger for 1-cell to 4-cell Li-ion battery and Li-polymer battery. For compact design and minimum components count, the charger integrates the 4 switching MOSFETs (Q<sub>1</sub>, Q<sub>2</sub>, Q<sub>3</sub>, Q<sub>4</sub>), input and charging current sensing circuits, the battery FET (BATFET) and all the loop compensation of the buck-boost converter. It provides high power density and design flexibility to charge batteries across the full input voltage range for USB Type-C™ and USB-PD applications such as digital cameras, drones and mobile printers.

The charger supports narrow VDC (NVDC) power path management, in which the system is regulated at a voltage slightly higher than the battery voltage, but not drop below the minimum system voltage. The system keeps operating even when the battery is completely discharged or removed. When load power exceeds the input source rating, the battery gets into supplement mode and prevents the input source from being overloaded and the system from crashing.

The device charges a battery from a wide range of input sources including legacy USB adapter to high voltage USB-PD adapter and traditional barrel adapter. The charger seamlessly transitions between buck, boost and buck-boost modes based on input voltage and battery voltage without host control. The optional dual-input source selector manages the power flowing from two different input sources. The host controls the input source selection through I<sup>2</sup>C with prioritizing the first available input source.

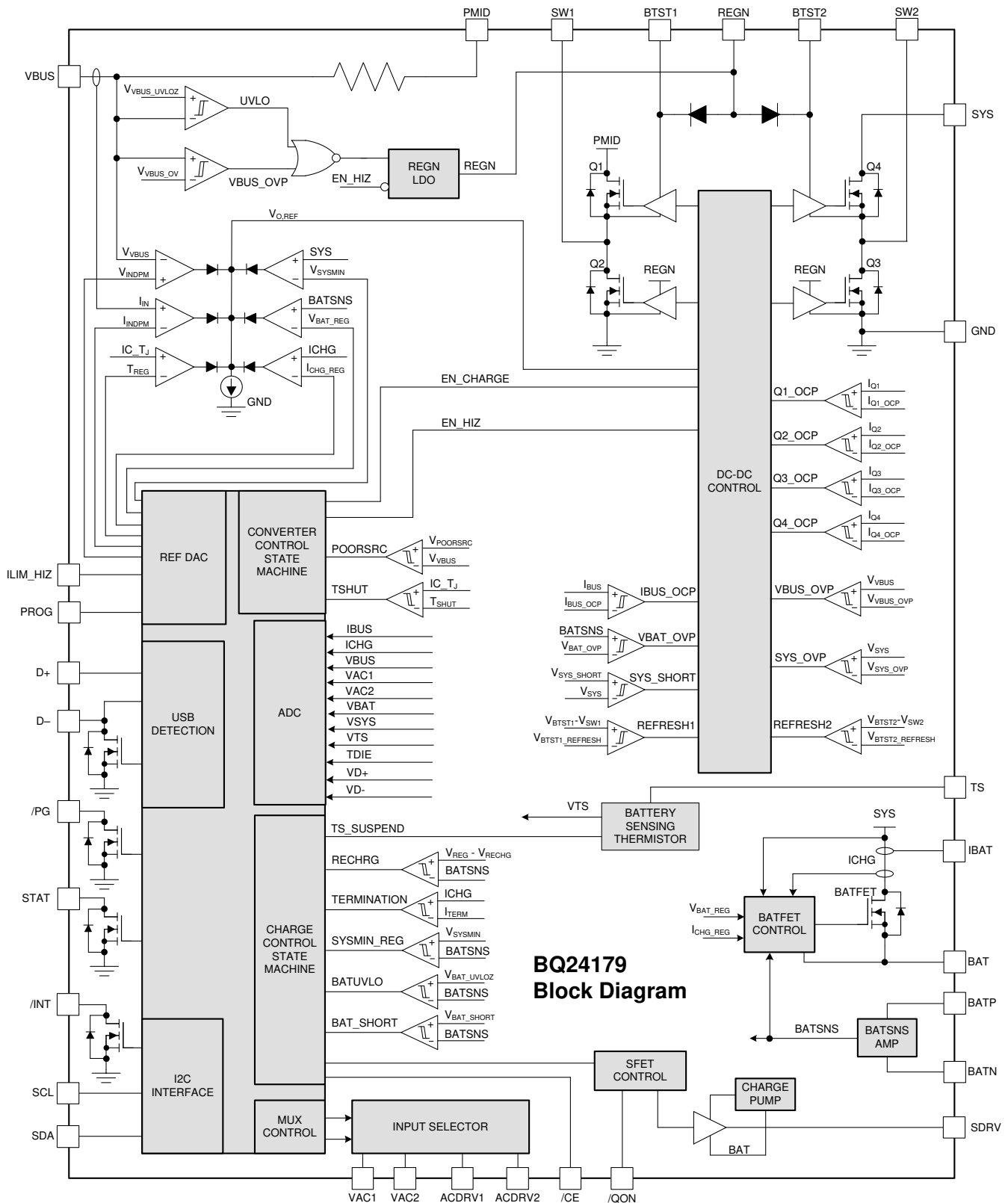
To support fast charging using adjustable high voltage adapter (HVDCP), the device provides D+/D- handshake. The device is compliant with USB 2.0 and USB 3.0 power delivery specification with input current and voltage regulation. In addition, the Input Current Optimizer (ICO) allows the detection of maximum power point of an unknown input source.

Besides the I<sup>2</sup>C host controlled charging mode, BQ24179 also supports autonomous charging mode. After power up, the charging is defaulted enabled with all the registers default settings. The device can complete a charging cycle without any software engagements. It detects battery voltage and charges the battery in different phases: trickle charging, pre-charging, constant current (CC) charging and constant voltage (CV) charging. At the end of the charging cycle, the charger automatically terminates when the charge current is below a pre-set limit (termination current) in the constant voltage phase. When the full battery falls below the recharge threshold, the charger will automatically start another charging cycle.

The charger provides various safety features for battery charging and system operations, including battery temperature negative thermistor (NTC) monitoring, trickle charge, pre-charge and fast charge timers and over-voltage/over-current protections on the battery and the charger power input pin. The thermal regulation reduces charge current when the die temperature exceeds a programmable threshold. The STAT output of the device reports the charging status and any fault conditions. The  $\overline{\text{PG}}$  output indicates if a good power source is present. The  $\overline{\text{INT}}$  pin immediately notifies host when fault occurs.

The device also provides a 16-bit analog-to-digital converter (ADC) for monitoring charge current and input/battery/system voltages, the TS pin voltage and the die temperature. It is available in a WCSP 2.9 mm x 3.3 mm 56-pin package.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Device Power-On-Reset

The internal bias circuits are powered from the higher voltage, whichever  $V_{VBUS}$  or  $V_{BAT}$  through an integrated power selector. The valid voltage to power up the device has to be greater than either  $V_{VBUS\_UVLOZ}$  or  $V_{BAT\_UVLOZ}$  thresholds. When  $V_{VBUS} < V_{VBUS\_UVLOZ}$ ,  $V_{BAT} < V_{BAT\_UVLOZ}$  and a voltage higher than  $V_{AC\_PRESENT}$  is present at either VAC1 or VAC2, the device will be powered from  $V_{AC1}$  or  $V_{AC2}$ , depending on which comes first.

Typically 5 ms after a valid voltage is first present at either  $V_{BAT}$ ,  $V_{BUS}$  or  $V_{AC1} / V_{AC2}$ , the charger wakes up, starts the ACFET-RBFET detection, reading the resistance at PROG pin, then configures the charger power on reset (POR) register setting accordingly. Approximately 20 ms after input voltage presence, the I<sup>2</sup>C registers become accessible to the host.

### 8.3.2 PROG Pin Configuration

At POR, the charger detect the PROG pin pull down resistance, then sets the charger default POR switching frequency and the battery cell count. Follow the resistance list in the table below to set the desired POR switching frequency and battery cell count. The surface mount resistor with  $\pm 1\%$  or  $\pm 2\%$  tolerance is recommended.

**表 8-1. PROG Pin Resistance to Set Default Switching Frequency and Battery Cell Count**

| SWITCHING FREQUENCY | CELL COUNT | TYPICAL RESISTANCE AT PROG PIN |
|---------------------|------------|--------------------------------|
| 1.5 MHz             | 1s         | 3.0 k $\Omega$                 |
| 750 kHz             | 1s         | 4.7 k $\Omega$                 |
| 1.5 MHz             | 2s         | 6.04 k $\Omega$                |
| 750 kHz             | 2s         | 8.2 k $\Omega$                 |
| 1.5 MHz             | 3s         | 10.5 k $\Omega$                |
| 750 kHz             | 3s         | 13.7 k $\Omega$                |
| 1.5 MHz             | 4s         | 17.4 k $\Omega$                |
| 750 kHz             | 4s         | 27.0 k $\Omega$                |

Some of the charging parameters default values are determined by the battery cell count identified by PROG pin configuration, which are summarized in the table below.

**表 8-2. Charging Parameters Dependent on Battery Cell Count**

| CELL (REG0x0A[7:6])    | 1s           | 2s           | 3s             | 4s            |
|------------------------|--------------|--------------|----------------|---------------|
| ICHG (REG0x03/04)      | 2 A          | 2 A          | 1 A            | 1 A           |
| VSYSMIN (REG0x00[5:0]) | 3.5 V        | 7 V          | 9 V            | 12 V          |
| VREG (REG0x01/02)      | 4.2 V        | 8.4 V        | 12.6 V         | 16.8 V        |
| VREG Range             | 3 V - 4.99 V | 5 V - 9.99 V | 10 V - 13.99 V | 14 V - 18.8 V |

After POR, the host can program the ICHG and VSYSMIN registers to any values within the ranges defined in the register tables. However, when programming the battery charging voltage (VREG), the host must ensure the VREG value falling into the right range associated with the CELL register (REG0x0A[7:6]) setting defined in the table above. When the CELL register is changed, the ICHG, VSYSMIN and VREG registers are reset to the POR default values associated with the CELL setting.

For example, if the PROG pin resistance is a 2s battery configuration, the default POR CELL, ICHG, VSYSMIN and VREG settings will be 2s, 2 A, 7 V and 8.4 V respectively. After POR, the host can change ICHG and VSYSMIN to any other values, and change VREG to any other values between 5 V and 9.99 V. With the CELL bits stay at 2s battery configuration, when REG\_RST bit or watchdog timer expired, the registers are reset to default values with ICHG, VSYSMIN and VREG automatically return to 2 A, 7 V, 8.4 V respectively.

When the CELL register is 2s battery configuration, any write out of the range of VREG (5 V - 9.99 V) is ignored by the charger. If VREG needs to be programmed out of the 5 V - 9.9 V range, like 11 V, the CELL bits have to be changed to 3s setting. The ICHG, VSYSMIN and VREG registers are reset to the 3s POR default values first, which are 1 A, 9 V and 12.6 V. After that, the host can program VREG in the range of 10 V - 13.99 V. In addition, when the CELL setting is changed to 3s, ICHG, VSYSMIN and VREG return to 1 A, 9 V and 12.6 V, when the registers are reset to the default values by REG\_RST bit or the watchdog timer expiration.

### 8.3.3 Dual-Input Power Mux

The BQ24179 has two ACDRV drivers to control two optional sets of back-to-back power N-FETs, selecting and managing the power from two different input sources. In the POR sequence, the charger detects whether the ACFETs-RBFETs are present, then updates the ACRB1\_STAT or ACRB2\_STAT status bits accordingly. The ACFET1-RBFET1 or ACFET2-RBFET2 can be controlled by setting the register bit EN\_ACDRV1 or EN\_ACDRV2. If the external ACFET-RBFET is not present, then tie VAC1 / VAC2 to VBUS and connect ACDRV1 / ACDRV2 to GND. The power MUX drivers support three different application cases, which are elaborated in detail below.

#### 8.3.3.1 VBUS Input Only

In this scenario, only single input is connected to VBUS directly, no back-to-back power MOSFETs are required. VAC1 and VAC2 are recommended to be shorted to VBUS. Both ACDRV1 and ACDRV2 need to be pulled down to GND, as shown in the figure below.

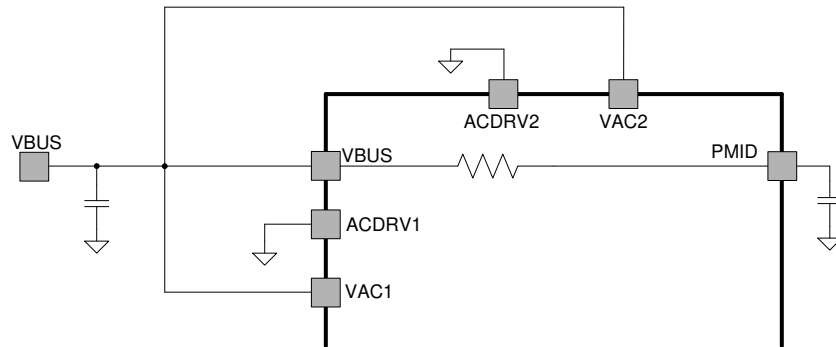


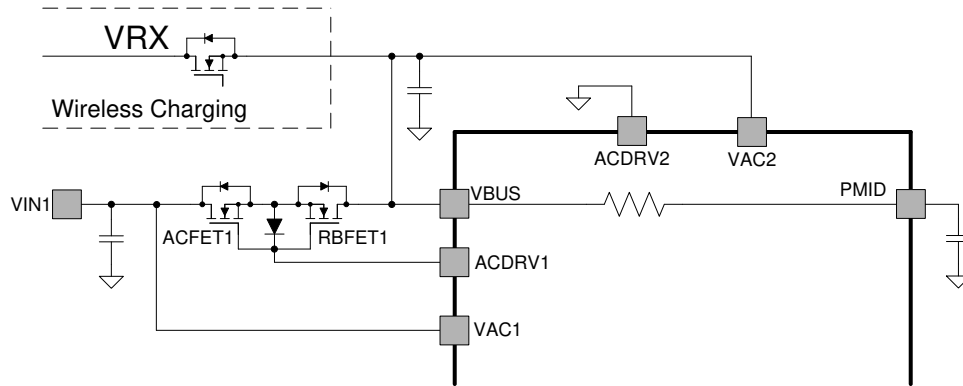
图 8-1. Single Input Connected to VBUS Directly Without ACFET-RBFET

- At POR, the charger detects no ACFETs-RBFETs are present by sensing that the ACDRV1 and ACDRV2 pins both shorted to GND.
- The charger updates the status bits ACRB1\_STAT and ACRB2\_STAT to 0, and locks EN\_ACDRV1 = 0 and EN\_ACDRV2 = 0.
- VAC1 and VAC2 are connected to VBUS directly. The ACDRV1 and ACDRV2 pins always stay low.

#### 8.3.3.2 One ACFET-RBFET

In this configuration, only ACFET1-RBFET1 is present, ACFET2-RBFET2 is not. VAC1 is tied to the drain of ACFET1, ACDRV1 is connected to the gate of ACFET1. VAC2 is shorted to VBUS, ACDRV2 is pulled down to GND. This structure is illustrated in the figure below, which is able to support either single input (one from VAC1 to VBUS through ACFET1-RBFET1, or one to VBUS directly) or dual-input (one from VAC1 to VBUS through ACFET1-RBFET1, the other one connected to VBUS directly) applications.



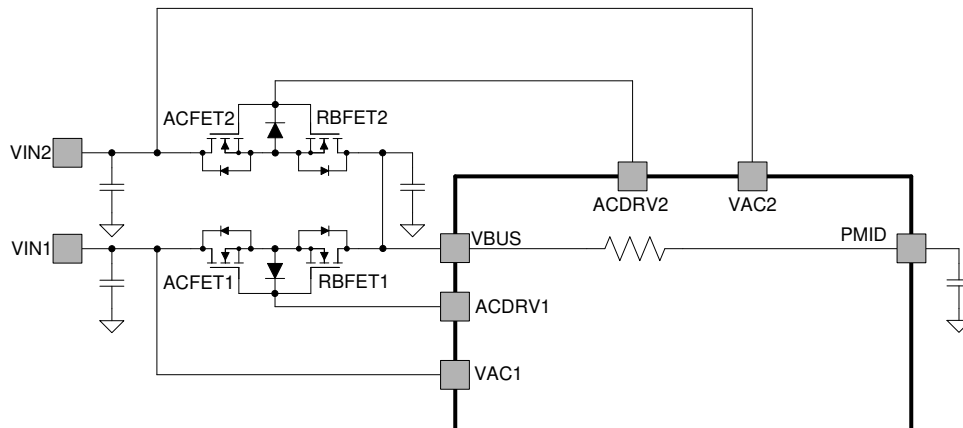


**图 8-2. One ACFET-RBFET Structure Supporting One Input at VAC1 and/or One Input at VBUS**

- At POR, the charger detects only ACFET1-RBFET1 presented, updates ACRB1\_STAT to 1 and keeps ACRB2\_STAT as 0.
- The charger locks the register bit EN\_ACDRV2 at 0, and the ACDRV2 pin will always stay low.
- When a valid input is presented at VAC1, the charger will set EN\_ACDRV1 = 1 and turn ACFET1-RBFET1 on.
- To swap from the input at VAC1 to the input at VBUS, the host has to turn off the ACFET1-RBFET1 first by setting DIS\_ACDRV = 1 (forcing EN\_ACDRV1 = 0), then enable the other input source which is connected to VBUS directly.
- In contrast, to swap from the input at VBUS to the input at VAC1, the host has to disable the input source connected to VBUS first, then turn on the ACFET1-RBFET1 by setting DIS\_ACDRV = 0.

### 8.3.3.3 Two ACFETs-RBFETs

In this scenario, both ACFET1-RBFET1 and ACFET2-RBFET2 are present. VAC1 / VAC2 is tied to the drain of ACFET1 / ACFET2, ACDRV1 / ACDRV2 is connected to the gate of ACFET1 / ACFET2. This structure is developed to support dual-input connected at VAC1 and VAC2.



**图 8-3. Two ACFETs-RBFETs Structure Supporting One Input at VAC1 and One Input at VAC2**

- At POR, the charger detects both ACFET1-RBFET1 and ACFET2-RBFET2 presented, then updates ACRB1\_STAT and ACRB2\_STAT to 1.
- EN\_ACDRV1 and EN\_ACDRV2 are programmable in this case.
- The ACDRV turns on the ACFET-RBFET of the port with a valid input presented first. The other ACFET-RBFET stays off, even if there is an adapter being plugged in later.
- Programming EN\_ACDRV1 = 1, EN\_ACDRV2 = 1 at the same time to turn on both ACFET1-RBFET1 and ACFET2-RBFET2 is not allowed, which will be ignored by the charger.

- Assuming two valid voltages are presented at VAC1 and VAC2, ACFET1-RBFET1 turns on, connecting the input source at VAC1 to VBUS. If the voltage at VAC1 becomes invalid because of VAC\_UVLO, VAC\_OV or IBUS\_OC, the charger swaps the input from VAC1 to VAC2, by turning off ACFET1-RBFET1 and then turning on ACFET2-RBFET2, without any host engagement. Swapping the input from VAC1 to VAC2 also can be controlled by the host. For example, to swap VAC1 to VAC2, the host can program REG0x13[7:6] (EN\_ACDRV2, EN\_ACDRV1) from 01b to 10b. The same control logic is applied to the input swapping from VAC2 to VAC1.

The waveforms below show the charger input transition from VAC1 to VAC2 when VAC1 is disconnected. At the beginning, VAC1 = 12 V and VAC2 = 8 V are both present. When VAC1 = 12 V is gone, the charger accomplishes the input source auto transition from VAC1 to VAC2 without host control.

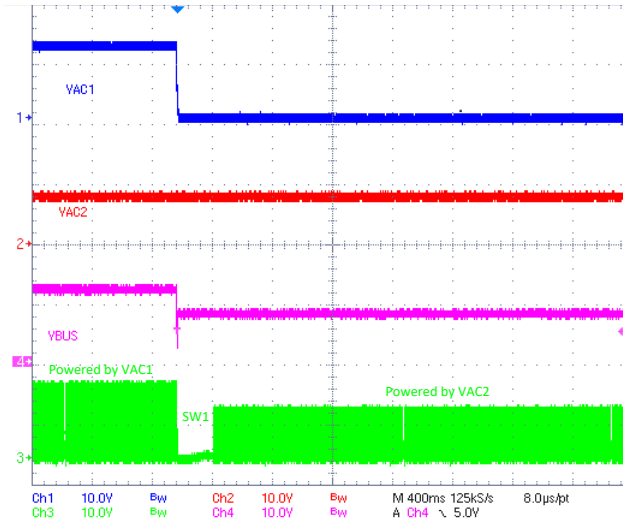


图 8-4. Input Source Auto Transition from VAC1 to VAC2 when VAC1 is Gone

When VAC2 has been connected, even if VAC1 is re-plugged in again later, the charger still stays connecting VAC2 as the input source, which is illustrated as the waveforms below. The host has to be involved to swap the input source from VAC2 back to VAC1 if necessary.

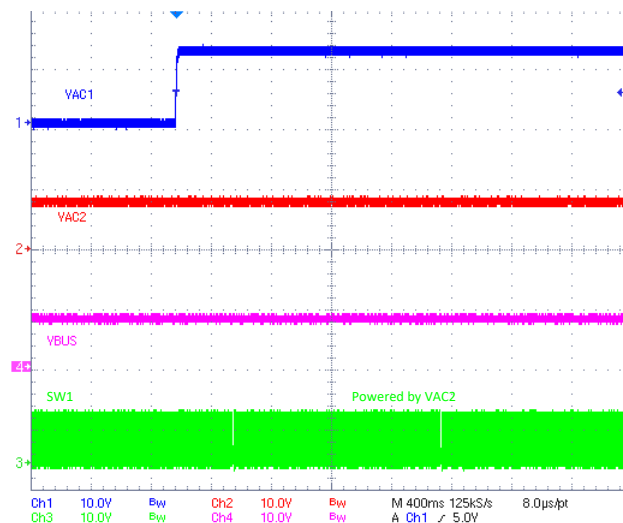


图 8-5. VAC1 Re-Plugged in When VAC2 Connected as the Charger Input

Some other critical notes for the application of this dual input power MUX are list below:

- The register bits, EN\_ACDRV1 and EN\_ACDRV2, are not only to control the turning on / off of ACFETs-RBFETs but also to indicate the on / off status of the FETs.
- The charger also provides the fault protection by turning ACFETs-RBFETs off, such as VAC\_OVP and IBUS\_OCP.
- With only one valid input presented at either VAC1 or VAC2, the ACFET1-RBFET1 and ACFET2-RBFET2 can not be both turned off by setting REG0x13[7:6] = 00b, because the charger is always trying to connect the only one input voltage available to power the charger. At this condition, the host has to set DIS\_ACDRV = 1 to force both two ACFETs-RBFETs off. With two input sources presented at both VAC1 and VAC2, the host can turn off the two ACFETs-RBFETs by setting either REG0x13[7:6] = 00 or DIS\_ACDRV = 1.
- In the transition from one input to the other one, after one ACFET-RBFET is turned off, the other one turns on until the VBUS voltage drops lower than  $V_{BUS\_PRESENT}$ . The converter stops switching for a short time period. When no battery presented or battery depleted, the system output would fall. The user has to be aware of this and avoid the input source swap when the battery voltage is too low.

### 8.3.4 Device Power Up from Battery without Input Source

If only the battery is present and the battery voltage is above the UVLO threshold ( $V_{BAT\_UVLOZ}$ ), the BATFET turns on and connects the battery to the system through the internal BATFET. The REGN LDO stays off to minimize the quiescent current. The low  $R_{DS(ON)}$  of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time. The device always monitors discharge current through the BATFET.

### 8.3.5 Device Power Up from Input Source

When an input source is present at VBUS, the device checks the input source voltage to turn on the REGN LDO and all the bias circuits. It detects and sets the input current limit before the buck-boost converter is started. The power up sequence from input source is as listed below:

1. Power up REGN LDO
2. Poor source qualification
3. Set the input current limit based on ILIM\_HIZ pin voltage, and set the POR default VINDPM according to the VBUS open circuit voltage.
4. Input Source Type Detection based on D+/D- to set default Input Current Limit (IINDPM) register and input source type
5. Converter power-up

#### 8.3.5.1 Power Up REGN LDO

When the device is powered up from VBUS, the LDO is turned on when  $V_{VBUS\_PRESENT} < VBUS < V_{VBUS\_OVP}$ . When the device is powered up from battery only condition, the LDO is turned on if VBAT is higher than 3.2 V, and ADC TS channel is on (ADC\_EN = 1 and TS\_ADC\_DIS = 0)

The REGN LDO supplies internal bias circuits and the MOSFETs gate drivers. The pull-up rails of ILIM\_HIZ, TS, and STAT can be connected to REGN. The  $\overline{INT}$  pin pull-up rail is recommended to be an external 1.8 V or 3.3 V voltage source, rather than REGN, because at battery only condition, the REGN might not be available. Except the charger related pull up rails, the REGN is not recommended to source any other external circuit. The REGN has to power the internal MOSFETs gate drivers, which is very critical for the charger normal operation.

#### 8.3.5.2 Poor Source Qualification

After the REGN LDO powers up, the device checks the current capability of the input source. The input source has to meet the following requirements in order to move forward to the next power on steps.

1. VBUS voltage below  $V_{VBUS\_OVP}$
2. VBUS voltage above  $V_{POORSRC}$  when pulling  $I_{POORSRC}$  (typical 30 mA)

Once the conditions are met, the status register bit PG\_STAT is set high and the  $\overline{INT}$  pin is pulsed to signal the host. The  $\overline{PG}$  pin goes LOW.

If VBUS\_OVP is detected (condition 1 above), the device automatically retries detection once the over-voltage fault goes away. If a poor source is detected (when pulling  $I_{POORSRC}$ , the VBUS voltage drops below  $V_{POORSRC}$ ), the device repeats poor source qualification routine every 2 seconds. After 7 consecutive failures, the device

sets EN\_HIZ = 1 and goes to HIZ mode. The battery must have enough charge to power the system while the device is in HIZ. Adapter re-plugin or EN\_HIZ bit toggle is required when the input source can be used to power the device. The EN\_HIZ bit is cleared automatically when the adapter is plugged in. Whenever the VBUS voltage does not meet either condition 1 or condition 2, it means the input source is not qualified anymore, the PG pin goes HIGH and the PG\_STAT bit goes low, at the same time, an INT pulse will be asserted and PG\_FLAG will be set to 1, if PG\_MASK = 0.

### 8.3.5.3 Input Current Optimizer (ICO)

The device provides Input Current Optimizer (ICO) to identify maximum power point in order to avoid overloading the input source. The algorithm automatically identifies maximum input current limit of an unknown power source and sets the charger IINDPM register properly, in order to prevent from entering the charger input voltage (VINDPM) regulation. This feature is disabled by default at POR (EN\_ICO = 0) and only activates when EN\_ICO bit is set to 1.

After DCP type input source is detected based on the procedures describe above (Input Source Type Detection), the algorithm runs automatically if EN\_ICO bit is set. The algorithm can also be forced to execute by setting FORCE\_ICO bit regardless of input source type detected. Please note that EN\_ICO = 1 is required for FORCE\_ICO to work.

The actual input current limit used by the Dynamic Power Management is reported in the ICO\_ILIM register whether set by ICO if enabled or IINDPM register if not. In addition, the current limit is clamped by ILIM pin unless EN\_EXT\_ILIM bit is 0 to disable ILIM\_HIZ pin function.

When the algorithm is enabled, it runs one time and then waits for the system load plus battery charge current to pull enough input current to force the charger into VINDPM. The algorithm adjusts the actual input current limit as shown in the ICO\_ILIM until the ICO\_STAT[1:0] and ICO\_FLAG bits are set (the ICO\_FLAG bit indicates any change in ICO\_STAT[1:0] bits). The algorithm operates depending on battery voltage:

1. When the battery voltage is below VSYSMIN, the algorithm starts ICO\_ILIM register with IINDPM which is the maximum input current limit allowed by system
2. When the battery voltage is above VSYSMIN, the algorithm starts ICO\_ILIM register with 500 mA which is the minimum input current limit to minimize adapter overload

Once the optimal input current is identified, the ICO\_STAT[1:0] and ICO\_FLAG bits are set. The actual input current is reported in the ICO\_ILIM register and does change unless the algorithm is triggered again by the following events :

1. A new input source is plugged-in, or EN\_HIZ bit is toggled
2. IINDPM register is changed
3. VINDPM register is changed
4. FORCE\_ICO bit is set to 1
5. VBUS\_OVP event

These events also reset the ICO\_STAT[1:0] bits to 01

### 8.3.5.4 Default VINDPM Setting

In the POR sequence, right after the D+/D- detection, the charger initiates ADC reading on the VBUS pin voltage without any load current (VBUS at no load condition, VBUS0) before the converter starts switching. The default VINDPM threshold is set to be VBUS0 - 1.4 V (VBUS0  $\geq$  7 V) or VBUS0 - 0.7 V (VBUS0 < 7 V).

If the converter already starts switching, the VBUS0 measurement can be performed by setting the register bit FORCE\_VINDPM\_DET = 1. The force VINDPM detection only can be done when VSYS\_STAT = 0 (VBAT > VSYSMIN). To measure the VBUS0 when the converter is running, the charger suspends charging (if enabled) and the converter stops switching. Then the ADC measures the VBUS voltage without any input load current and update the VINDPM register bit. After the VINDPM register bit is reset, the FORCE\_VINDPM\_DET bit returns to 0 automatically. If VSYS\_STAT = 1 (VBAT < VSYSMIN), VBUS0 measurement does not start, the FORCE\_VINDPM\_DET bit resets to 0 and the VINDPM register retains its current value. The host must ensure there is a battery presence prior to force VINDPM detection by setting FORCE\_VINDPM\_DET bit to allow system to be supported by the battery during detection.

When the measured VBUS0 is too low, for example 3.6 V, or too high, for example 25 V, the calculated VINDPM based on the equation list above is out of the VINDPM register range, and then the charger sets the VINDPM register to be the minimal value (3.6 V) or maximum (22 V) value.

### 8.3.5.5 Device HIZ State

The charger enters HIZ mode when EN\_HIZ bit is set to 1. The HIZ mode refers to a charger state, in which the REGN LDO is off, and the converter stops switching even if the adapter is present. Similar to the battery only condition, the charger is in a low quiescent current mode, turns off the ADC and turns on the BATFET to support the system load.

Some of the faults like VBUS\_OVP, VSYS\_OVP, and VBAT\_OVP, force only the converter to stop switching but keep the REGN on. While some of the faults like VSYS\_SHORT and IBUS\_OCP, force the charger into HIZ mode by setting EN\_HIZ = 1. More details could be found in the fault protection section.

### 8.3.5.6 ILIM\_HIZ Pin

At POR, before the charger converter starts switching, the charger ADC reads the ILIM\_HIZ pin voltage, and calculates the input current limit (ILIM) set by this ILIM\_HIZ pin, according to the equation  $V_{ILIM\_HIZ} = 1\text{ V} + 800\text{ m}\Omega \times ILIM$ . The ILIM\_HIZ pin sets a high clamp for the IINDPM register. If the IINDPM setting from the D+/D- detection or the POR default 3-A IINDPM setting is higher than the ILIM clamp, the IINDPM register stays at this ILIM clamp. In addition, the host cannot program the IINDPM register to any values higher than this ILIM clamp after POR, unless the register bit EN\_EXTILIM is set to 0.

The ILIM\_HIZ pin can be biased from an resistor voltage divider that can be tied to either the REGN or the other external voltage source. When the ILIM\_HIZ pin is pulled lower than 0.75 V, the charger stops switching and REGN stays on. The charger resumes switching if the ILIM\_HIZ pin voltage becomes higher than 1 V.

If the ADC reads the ILIM\_HIZ pin voltage is lower than 1.08 V ( $1\text{ V} + 800\text{ m}\Omega \times 100\text{ mA}$ ), the charger considers the ILIM clamp to be 100 mA, which is the minimal setting of the IINDPM register.

### 8.3.5.7 IBAT Pin for Battery Current Sensing

BQ24179 provides a high-accuracy battery charging / discharging current sensing pin, IBAT. It outputs a 25- $\mu$ A current when the battery charging / discharging current is 1 A. The IBAT pin output is valid when either VBUS or VBAT voltage is higher than its own ULVO voltage, and EN\_IBAT register bit is set to 1. The IBAT pin only provides the battery charging current in forward charging mode and the battery discharging current at battery only condition. When the charger is operated in forward charging mode, the output of the IBAT pin becomes zero when the battery is turning into the supplement mode.

### 8.3.5.8 Buck-Boost Converter Operation

The charger employs a synchronous buck-boost converter that allows charging the 1s to 4s battery from a legacy 5-V USB input source, HVDCP and USB-PD power sources. The charger operates in buck, buck-boost, or boost mode based on different input voltage and output voltage combinations. The converter can operate uninterruptedly and continuously across the Buck, Buck-boost, and Boost operating states.

#### 8.3.5.8.1 Pulse Frequency Modulation (PFM)

In order to improve converter light-load efficiency, the device switches to PFM control at light load condition. The effective switching frequency decreases accordingly as load current decreases. The PFM operation can be disabled by setting PFM\_FWD\_DIS = 1, the converter stays at the PWM mode switching frequency and go to DCM operation at light load condition. The minimum effective switching frequency in PFM can be limited to 25 kHz to eliminate the audible noise concern if the out of audio (OOA) feature is enabled by setting DIS\_FWD\_OOA = 0. The host can disable the OOA by setting DIS\_FWD\_OOA = 1, which may result in the converter effective switching frequency dropping below 25 kHz at extremely light load.

### 8.3.6 Power Path Management

The device accommodates a wide range of input voltage range from 3.6 V to 24 V covering the legacy 5-V USB input, HVDCP, USB-PD input and the wall adapter. The device provides automatic power path selection to supply the system (SYS) from input source (VBUS), battery (BAT) or both.

### 8.3.6.1 Narrow Voltage DC Architecture

The device deploys the NVDC architecture with a BATFET separating the system from the battery. Even with a fully depleted battery, the system is regulated above the minimum system voltage. The minimum system voltage is set by VSYSMIN bits. The default minimum system voltage at POR is determined according to different battery cell settings.

The NVDC architecture also provides the charging termination when the battery is fully charged. By turning off the BATFET, the adapter power is prioritized to support the system, which avoid the battery being continuously charged and discharged by the system load even if the adapter is present. This is very important to keep the battery in a healthy condition and extend the battery life time.

When the battery voltage is below the minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is regulated at around 200 mV above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, the BATFET is fully on and the voltage difference between the system and battery is the  $R_{ds(on)}$  of BATFET multiplied by the charging current. When battery charging is disabled and VBAT is above the minimum system voltage setting or charging is terminated, the system is always regulated at typically 200 mV (PFM disabled) or typical 600 mV (PFM enabled) above battery voltage. The status register VSYS\_STAT bit goes high when the system is in minimum system voltage regulation.

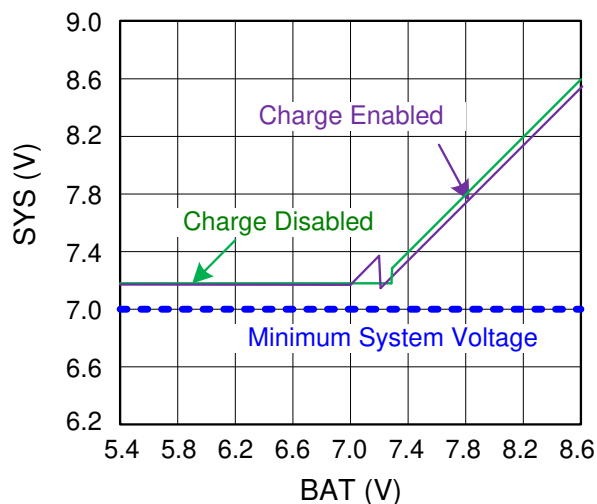


图 8-6. Typical System Voltage vs Battery Voltage for a 2S Battery Configuration

### 8.3.6.2 Dynamic Power Management

To meet the maximum current limit in USB spec and avoid over loading the adapter, the device features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage. When the input power at the VBUS pin is too low to support the load from SYS pin and the battery charge current from BAT pin, the charger engages either IINDPM to limit its current or VINDPM to prevent further reduction in VBUS pin voltage.

When the system voltage is regulated at VSYSMIN, the charger could be in trickle charge, pre-charge or fast charge stages, the SYS voltage drops lower than VSYSMIN, the VSYSMIN loop takes over and reduces the trickle charge, pre-charge or fast charge current, so that the SYS voltage remains at the VSYSMIN level.

If the charge current falls to zero, but the input source is still overloaded, the SYS voltage will drop. Once the SYS voltage falls below the battery voltage, the device automatically enters Supplement Mode in which the BATFET turns on. The battery starts discharging so that the system is supported from both the input source and battery. In supplement mode, the battery FET is operated in ideal diode mode in which the charger regulates the battery FET gate voltage to keep the BATFET minimum  $V_{DS}$  to approximately 25 mV when the current is low. This prevents SYS voltage oscillations from entering and exiting the supplement mode. As the discharge current



increases, the charger regulates the BATFET gate to a higher voltage, in order to reduce the battery FET  $R_{DS(on)}$  until the MOSFET is in full turn-on stage. At this point onwards, the  $V_{DS}$  of the battery FET linearly increase with the discharge current. The BATFET turns off to exit Supplement Mode when the battery is below battery depletion threshold.

During DPM mode, the status register bits VINDPM\_STAT (VINDPM) and/or IINDPM\_STAT (IINDPM) go high. The figure below shows the DPM response with 5-V/3-A adapter, 6.4-V battery, 1.5-A charge current and 6.8-V minimum system voltage setting.

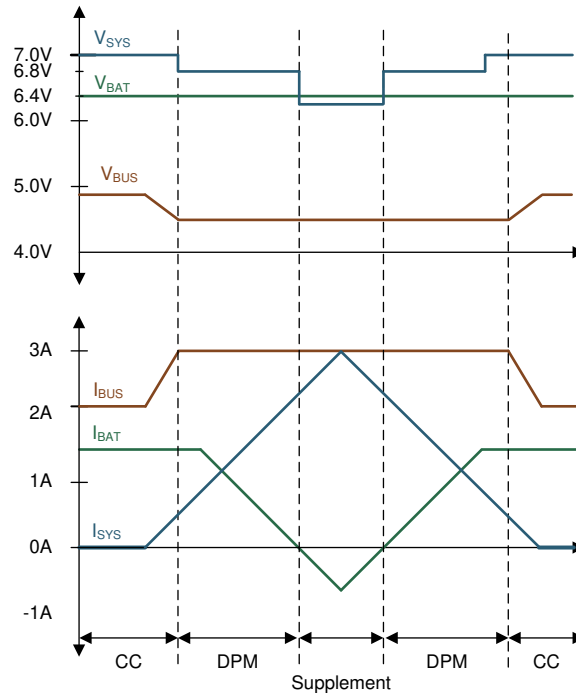


图 8-7. DPM Response

### 8.3.7 Battery Charging Management

BQ24179 charges 1S~4S Li-Ion batteries with up to 5-A charge current for high capacity cells. The battery charging in different stages is controlled by the integrated BATFET. The low  $R_{DS(on)}$  BATFET improves charging efficiency and minimizes the voltage drop during discharging.

#### 8.3.7.1 Autonomous Charging Cycle

When battery charging is enabled (EN\_CHG bit = 1 and  $\overline{CE}$  pin is LOW), the device autonomously completes a charging cycle without host involvement. The device default charging parameters are listed in the table below. The host can always control the charging operation and optimize the charging parameters by writing to the corresponding registers through I<sup>2</sup>C.

表 8-3. Charging Parameter Default Settings

| DEFAULT MODE                 | BQ24179  |
|------------------------------|--|
| Charging voltage             | 4.2 V (1S), 8.4 V (2S), 12.6 V (3S), 16.8 V (4S) |
| Recharging voltage threshold | 200 mV   |
| Fast charge current          | 2 A (1S and 2S), 1 A (3S and 4S)                 |
| Pre-charge current           | 120 mA   |
| Trickle charge current       | 100 mA   |
| Termination current          | 200 mA   |
| Temperature profile          | JEITA  |
| Fast charge safety timer     | 12 hours   |



**表 8-3. Charging Parameter Default Settings (continued)**

| DEFAULT MODE                | BQ24179 |
|-----------------------------|---------|
| Pre charge safety Timer     | 2 hours |
| Trickle charge safety Timer | 1 hour  |

A new charge cycle starts when the following conditions are valid:

- Converter starts up
- Battery charging is enabled by setting register bit EN\_CHG = 1 and keeping  $\overline{CE}$  pin LOW
- No thermistor fault on TS pin
- No safety timer fault

The charger automatically terminates the charging cycle when the charging current is below termination threshold, charge voltage is above recharge threshold, and the device is not in DPM mode or thermal regulation. When a fully charged battery voltage is discharged below recharge threshold (threshold selectable via VRECHG[1:0] bits), the device automatically starts a new charging cycle. After the charging terminates, toggling either  $\overline{CE}$  pin or EN\_CHG bit initiates a new charging cycle.

The STAT output indicates the charging status of: charging (LOW), charging complete or charging disabled (HIGH) or charging fault (Blinking). The STAT output can be disabled by setting DIS\_STAT = 1. In addition, the status register (CHG\_STAT) indicates the different charging phases as:

- 000 – Not Charging
- 001 – Trickle Charge ( $V_{BAT} < V_{BAT\_SHORTZ}$ )
- 010 – Pre-charge ( $V_{BAT\_SHORTZ} < V_{BAT} < V_{BAT\_LOWV}$ )
- 011 – Fast Charge (CC mode)
- 100 – Taper Charge (CV mode)
- 101 – Reserved
- 110 – Top-off Timer Active Charging
- 111 – Charge Termination Done

When the charger transitions to any of these states, including when the charge cycle completes, an  $\overline{INT}$  is asserted to notify the host.

### 8.3.7.2 Battery Charging Profile

The device charges the battery in five phases: trickle charge, pre-charge, constant current, constant voltage, and top-off trickle charging (optional). At the beginning of a charging cycle, the device checks the battery voltage and regulates current/voltage accordingly.

**表 8-4. Default Charging Current Setting**

| VBAT                                 | CHARGING CURRENT | REGISTER DEFAULT SETTING           | CHRG_STAT |
|--------------------------------------|------------------|------------------------------------|-----------|
| $< V_{BAT\_SHORT}$                   | $I_{BAT\_SHORT}$ | 100 mA                             | 001       |
| $V_{BAT\_SHORTZ}$ to $V_{BAT\_LOWV}$ | $I_{PRECHG}$     | 120 mA                             | 010       |
| $> V_{BAT\_LOWV}$                    | $I_{CHG}$        | 2 A (1S and 2S)<br>1 A (3S and 4S) | 011       |

If the charger is in DPM regulation or thermal regulation during charging, the actual charging current is less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate, as explained in Charging Safety Timer.

The BATFET LDO operation can be disabled by setting DIS\_LDO = 1. At this condition, the pre-charge current and fast charge current are both regulated by the buck-boost converter PWM current regulation loop. The SYS is not regulated at VSYSMIN any more when the LDO mode is disabled at the low battery voltage condition. When in trickle charge, setting DIS\_LDO = 1 does not affect  $I_{BAT\_SHORT}$  or VSYSMIN operation.

$V_{BAT\_LOWV}$  is the battery voltage threshold for the transition from pre-charge to fast charge. It is defined as a ratio of battery voltage regulation limit (VREG). The  $V_{BAT\_SHORTZ}$  is the battery voltage threshold for the transition from trickle charge to pre-charge, which is fixed value 2.2 V.

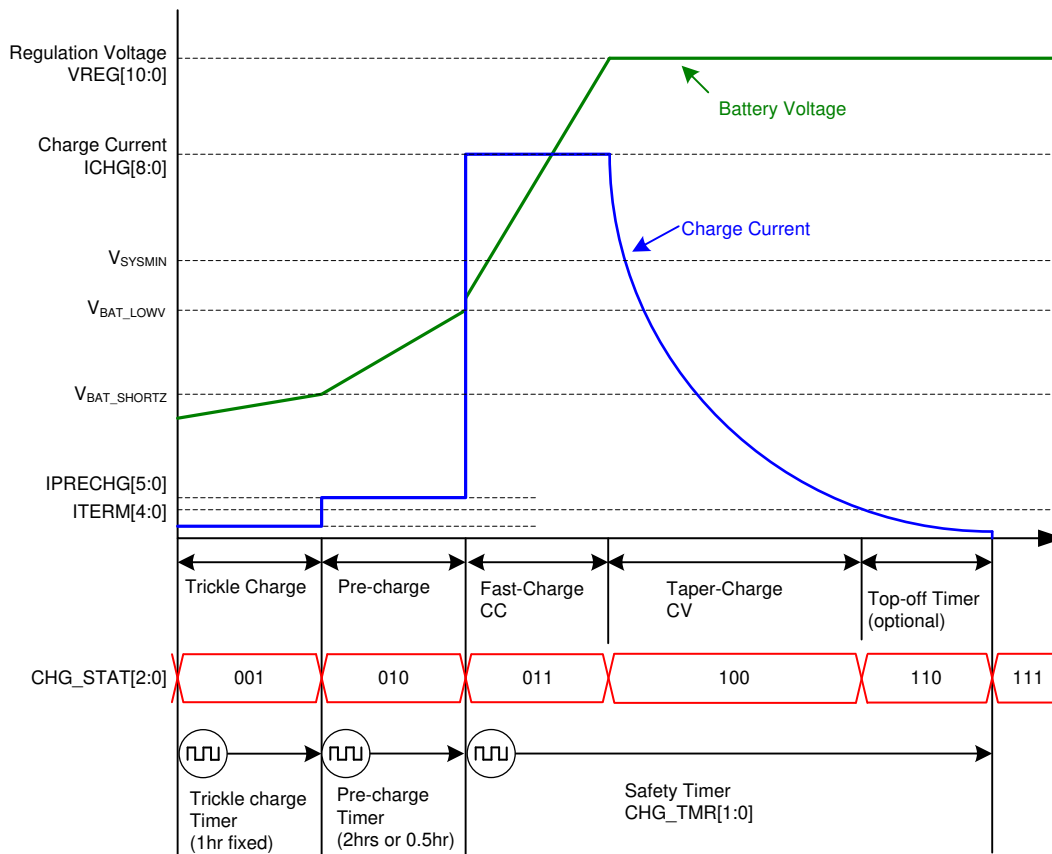


图 8-8. Battery Charging Profile

### 8.3.7.3 Charging Termination

The device terminates a charge cycle when the battery voltage is above the recharge threshold, the converter is operated in the battery constant voltage regulation loop and the current is below the termination current. After the charging cycle is completed, the BATFET turns off. The converter keeps running to power the system and the BATFET can turn on again if the supplement mode is triggered.

When termination is done, the status register  $CHG\_STAT$  is set to 111 and an  $\overline{INT}$  pulse is asserted to the host. Termination is temporarily disabled when the charger device is in input current (IINDPM), input voltage (VINDPM) or thermal (TREG) regulation. Termination can be permanently disabled by writing 0 to  $EN\_TERM$  bit prior to charging termination. Writing 0 to  $EN\_TERM$  when the termination already occurred or in the top-off charging stage does not disable termination, until the next charging cycle has been restarted. If termination is reenabled by setting  $EN\_TERM = 1$  during the current charge cycle, the change is applied immediately to the current charging cycle.

At low termination currents (like 40 mA to 160 mA), due to the comparator offset, the actual termination current may be up to 20%~40% higher than the termination target. In order to compensate for the comparator offset, a programmable top-off timer (default disabled) can be activated after termination is detected. While the top-off timer is running, the device continues to charge the battery in constant voltage mode (BATFET stays on) until the top-off time expires. The top-off timer follows safety timer constraints, such that if the safety timer is suspended, so is the top-off timer. And if the safety timer is doubled, so is the top-off timer.  $CHG\_STAT$  reports whether the top off timer is active via the 110 code. Once the top-off timer expires, the  $CHG\_STAT$  register is set to 111 and an  $\overline{INT}$  pulse is asserted to the host.

The top-off timer gets reset (set to 0 and counting resumes when appropriate) for any of the following conditions:

1. Charge disable to enable
2. Termination status low to high
3. REG\_RST register bit is set (disables top-off timer)

Once the charger detects termination, the charger reads the top-off timer (TOPOFF\_TMR) settings. Programming the top-off timer value after termination has no effect unless a recharge cycle is initiated. The top-off timer only starts to count when the charger's termination criteria are met. If EN\_TERM = 0, the charger never terminates charging, so the top-off timer does not start counting, even if it is enabled. An  $\overline{\text{INT}}$  is asserted to the host when the top-off timer starts counting as well as when the top-off timer expires. All charge cycle related  $\overline{\text{INT}}$  pulses (including top-off timer  $\overline{\text{INT}}$  pulse) can be masked by CHG\_MASK bit.

#### 8.3.7.4 Charging Safety Timer

The device has a built-in safety timer to prevent an extended charging cycle due to abnormal battery conditions. The user can program the fast charge safety timer through I<sup>2</sup>C (CHG\_TMR bits). When the fast charge safety timer expires, the fault register CHG\_TMR\_STAT bit is set to 1, and an  $\overline{\text{INT}}$  pulse is asserted to the host. The trickle charge timer is fixed 1 hour. The pre-charge safety timer is adjustable 2 hours (POR default) or 0.5 hour. The fast charging timer POR default setting is 12 hours.

The trickle charge, pre-charge and fast charge safety timers can be disabled by setting EN\_TRICHG\_TMR, EN\_PRECHG\_TMR or EN\_CHG\_TMR bit to 0. Each charging safety timer can be enabled anytime regardless of the current charging state. Each timer restarts counting when it is enabled. As soon as each charging stage is initiated, the associated safety timer starts to count, which is illustrated in the battery charging profile chart shown in the section Battery Charging Profile.

During input voltage, current or thermal regulation, the safety timer counts at half-clock rate as the actual charge current is likely to be below the register setting. For example, if the charger is in input current regulation (IINDPM\_STAT = 1) throughout the whole charging cycle, and the safety timer is set to 5 hours, then the timer will expire in 10 hours. This half-clock rate feature can be disabled by setting TMR2X\_EN = 0. If the host disables the half-clock rate while the charger is already running at half-clock rate, the charger keeps running at the half-clock rate and the half-clock rate is not disabled until the charger exit the voltage, current or thermal regulation.

During faults which disable charging, or supplement mode, the timer is suspended. Since the timer is not counting in this state, the TMR2X\_EN bit has no effect. Once the fault goes away, the safety timer resumes. If the charging cycle is stopped and started, the timer resets. The pre-charge safety timer and the trickle charge safety timer follow the same rules as the fast charge safety timer in terms of getting suspended, reset and counting at half-rate when TMR2X\_EN is set.

The fast charge timer is reset at the following events:

1. Charging cycle stop and restart (toggle  $\overline{\text{CE}}$  pin, EN\_CHG bit, or charged battery falls below recharge threshold after termination)
2. BAT voltage changes from pre-charge to fast-charge or vice versa (in host-mode or default mode)
3. A change of the value of CHG\_TMR[1:0] register bits

The pre-charge timer is reset at the following events:

1. Charging cycle stop and restart (toggle  $\overline{\text{CE}}$  pin, EN\_CHG bit, or charged battery falls below recharge threshold)
2. BAT voltage changes from trickle charge to pre-charge or vice versa, pre-charge to fast charge or vice versa (in host-mode or default mode)
3. A change of the value of PRECHG\_TMR register bit.

The trickle charge timer is reset at the following events:

1. Charging cycle stop and restart (toggle  $\overline{\text{CE}}$  pin, EN\_CHG bit, or charged battery falls below recharge threshold)
2. BAT voltage changes from trickle charge to pre-charge or vice versa (in host-mode or default mode)

### 8.3.7.5 Thermistor Qualification

The charger device provides a single thermistor input for battery temperature monitoring.

#### 8.3.7.5.1 JEITA Guideline Compliance in Charge Mode

To improve the safety of charging Li-ion batteries, the JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges.

To initiate a charge cycle, the voltage on the TS pin must be within the VT1 to VT5 thresholds. If TS voltage exceeds the VT1-VT5 range, the controller suspends charging and waits until the battery temperature is within the T1 to T5 range. At cool temperature T1-T2, JEITA recommends to reduce the charge current to be lower than half of the charge current at normal temperature T2-T3. The charger register bits JEITA\_ISETC[1:0] provide the charge current programmability at T1-T2, to be 20%, 40% or 100% of the charge current in the T2-T3 temperature range or charge suspend. At warm temperature T3-T5, JEITA recommends charge voltage less than 4.1V / cell. The charger register bits JEITA\_VSET[2:0] provide the charge voltage programmability at T3-T5, to be with a voltage offset less than charge voltage in the T2-T3 temperature range or charge suspend.

Charging termination is still enabled (when EN\_TERM = 1) at cool temperature T1-T2 and warm temperature T3-T5. The termination current remains the same in all different temperature ranges. In normal operation, battery charging terminates when the charge current is lower than the termination current, the battery voltage is higher than the battery recharge voltage and the charger is in the battery voltage CV regulation loop. When the temperature enters the T1-T2 or T3-T5 ranges, the charge current may reduce to 20% or 40% of that in the T2-T3 range, which might be lower than the termination current setting. If at this moment, the battery voltage is already higher than the battery recharge voltage and the charger is in the battery voltage CV regulation loop, the charger terminates charge.

In warm T3-T5 temperature range, the battery voltage regulation value become lower than that in the T2-T3 temperature range. If the battery voltage is already very close to the T2-T3 regulation value, the JEITA warm automatic regulation voltage reduction might cause a battery over-voltage (VBAT\_OVP) fault.

In cool T1-T2 temperature range or warm T3-T5 temperature range, the charge current is different from that at the normal T2-T3 temperature range, the safety timer must be adjusted accordingly. The safety timer is suspended when the charge is suspended, and runs at half of the clock rate when the charge current is reduced to 20% or 40%, but stays the same when the charge current is unchanged.

One typical JEITA charging values are shown as the figure below, in which the blue real line is the default setting and the red dash line is the programmable options.

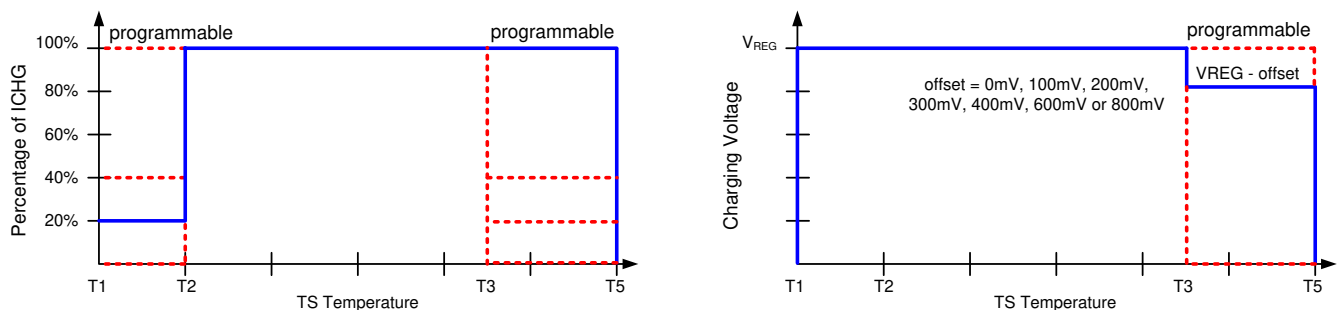


图 8-9. TS Charging Values

The NTC monitoring on the battery temperature can be ignored by the charger if TS\_IGNORE = 1. When the TS pin feedback is ignored, the charger considers the TS is always good for charging. The TS\_STAT including TS\_COLD\_STAT, TS\_COOL\_STAT, TS\_WARM\_STAT and TS\_HOT\_STAT, always report 000 with TS\_IGNORE = 1.

When TS\_IGNORE = 0, the charger adjusts the charging profile based on the TS pin feedback information. When the battery temperature jumps from one temperature range to the other one, the associated TS status bits are updated accordingly. The TS flag bits are set for the temperature range for which the TS voltage is reporting,

and an  $\overline{\text{INT}}$  pulse is asserted to alert the host if TS\_MASK is low. The FLAG and  $\overline{\text{INT}}$  pulse can be individually masked by properly setting the associated mask bit, to prevent the  $\overline{\text{INT}}$  pulse from alerting the host of battery temperature range changes.

The typical TS resistor network is illustrated in the figure below.

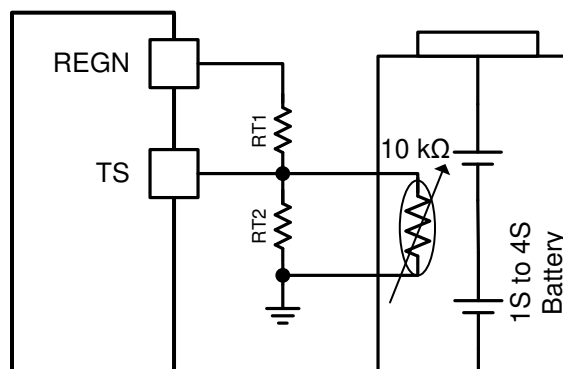


图 8-10. TS Resistor Network

Assuming a 103AT NTC thermistor on the battery pack as shown above, the value of RT1 and RT2 can be determined by:

$$RT2 = \frac{RTH_{COLD} \times RTH_{HOT} \times \left( \frac{1}{VT1} - \frac{1}{VT5} \right)}{RTH_{HOT} \times \left( \frac{1}{VT5} - 1 \right) - RTH_{COLD} \times \left( \frac{1}{VT1} - 1 \right)} \quad (1)$$

$$RT1 = \frac{\frac{1}{VT1} - 1}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}} \quad (2)$$

The BQ24179 provides the comparators with fixed thresholds for VT1 and VT5, and the comparators with programmable thresholds for VT2 and VT3. The thresholds for VT2 and VT3 are controlled by TS\_COOL[1:0] and TS\_WARM[1:0]. This programmability gives more flexibility for the configuration of the JEITA profile. Select T1 = 0°C and T5 = 60°C for Li-ion or Li-polymer battery, the RT1 and RT2 are calculated to be 5.24 KΩ and 30.31 KΩ respectively.

### 8.3.8 Integrated 16-Bit ADC for Monitoring

The integrated 16-bit ADC in the device allows the user to get critical system information for optimizing the behavior of the charger. The ADC control is through the ADC Control register. The ADC\_EN bit provides the ability to enable and disable the ADC in order to conserve power dissipation. The ADC\_RATE bit allows continuous conversion or one-shot behavior. After a 1-shot conversion finishes, the ADC\_EN bit is cleared, and must be re-asserted to start a new conversion. The ADC\_AVG bit enables or disables (default) averaging. ADC\_AVG\_INIT starts average using the existing (default) or using a new ADC value.

To enable the ADC, the ADC\_EN bit must be set to 1. The ADC is allowed to operate if either the VAC > 3.4 V or VBUS > 3.4 V or VBAT > 2.9 V is valid. If ADC\_EN is set to 1 before VAC1/VAC2, VBUS or VBAT reaches its valid threshold, then the ADC conversion is postponed until one of the power supplies reaches the threshold. If the charger is in HIZ mode, the ADC still can be enabled by setting ADC\_EN = 1. At battery only condition, if the TS\_ADC channel is enable, the ADC only works when battery voltage is higher than 3.2 V, otherwise, the ADC works when the battery voltage is higher than 2.9 V.

The ADC\_SAMPLE bits control the ADC sample speed, with conversion times of  $t_{ADC\_CONV}$ . If the host changes the sample speed in the middle of an ADC conversion, the ADC conversion stops the channel being converted, and that channel is reconverted at the new rate. At that point, some of the ADC register values might have been converted with one sample rate and others with a different sample rate.

By default, all ADC channels are enabled with 1-shot or continuous conversion mode unless the channel is disabled in the ADC\_Function\_Disable\_0 or ADC\_Function\_Disable\_1 register. If an ADC channel is disabled by setting the corresponding register bit, then the value in that register is from the last valid ADC conversion or the default POR value (all zeros if no conversions have been taken place). If an ADC channel is disabled in the middle of an ADC measurement cycle, the device finishes the conversion of that channel, but not convert the channel at the next conversion cycle. Even though no conversion takes place when all ADC channels are disabled, the ADC circuitry is active and ready to begin conversion as soon as one of the bits in the ADC\_Function\_Disable\_0 or ADC\_Function\_Disable\_1 register is set to 0.

The ADC\_DONE\_STAT and ADC\_DONE\_FLAG bits are set when a conversion is complete in 1-shot mode only. This event produces an  $\overline{INT}$  pulse, which can be masked with ADC\_DONE\_MASK. During continuous conversion mode, the ADC\_DONE\_STAT and ADC\_DONE\_FLAG bits have no meaning and remain 0.

ADC conversion operates independently of the faults present in the device. ADC conversion continues even after a fault has occurred (such as one that causes the power stage to be disabled) and the host must set  $ADC\_EN = 0$  to disable the ADC. ADC conversion is interrupted upon adapter plug-in and resumes after Input Source Type Detection default VINDPM setting are complete. ADC readings are only valid for DC states and not for transients.

Enabling ADC does not require to bring up REGN, however, when the ADC TS channel is enabled, the charger will turn on the REGN to bias the TS pin. For the ICHG channel, the ADC is able to read the battery pre-charge and fast charge current in forward charging mode when the adapter is present. It also can read the battery discharging current in battery only mode. When the charger is in trickle charge, supplement mode or charge disabled, the ICHG ADC reading is zero. In battery only mode, the battery current sensing amplifier (CSA) default turns off to minimize the quiescent current. Setting  $EN\_IBAT = 1$  is necessary to enable the CSA so that the ADC can read back the battery current information.

If the host wants to exit the ADC more gracefully, it is possible to do either of the following:

1. Write ADC\_RATE to one-shot in order to force the ADC to stop at the end of a complete cycle of conversions
2. Disable all ADC conversion channels so that the ADC stops at the end of the current measurement.

### 8.3.9 Status Outputs ( $\overline{PG}$ , STAT, and $\overline{INT}$ )

#### 8.3.9.1 Power Good Indicator ( $\overline{PG}$ )

The  $\overline{PG}$  pin goes low and the power good status register is set to 1 once a good input source is qualified. The PG\_STAT and PG\_FLAG change to 1 to indicate a good input source. An  $\overline{INT}$  is asserted low to alert the host unless masked by PG\_MASK when the following conditions are met:

1. VBUS above  $V_{VBUS\_UVLOZ}$
2. VBUS below  $V_{VBUS\_OVP}$  threshold
3. VBUS above  $V_{POORSRC}$  (typical 3.4 V) when  $I_{POORSRC}$  (typical 30 mA) current is applied (not a poor source)

#### 8.3.9.2 Charging Status Indicator (STAT Pin)

The device indicates charging state on the open drain STAT pin. The STAT pin can drive LED. The STAT pin function can be disabled via the DIS\_STAT bit.

**表 8-5. STAT Pin State**

| CHARGING STATE  | STAT INDICATOR |
|---|----------------|
| Charging in progress (including recharge and charging in top-off timer) | LOW            |
| Charging complete   | HIGH           |
| HIZ mode, charge disable  | HIGH           |
| Battery only mode   | HIGH           |



表 8-5. STAT Pin State (continued)

| CHARGING STATE  | STAT INDICATOR   |
|---|------------------|
| Charge suspend (A fault condition which disable charging) | Blinking at 1 Hz |

### 8.3.9.3 Interrupt to Host (INT)

In some applications, the host does not always monitor charger operation. The INT pin notifies the system host on the device operation. By default, the following events generate an active-low, 256-μs INT pulse.

- Good input source detected
  - $V_{VBUS} < V_{VBUS\_OVP}$  threshold
  - $V_{VBUS} > V_{POORSRC}$  (typical 3.4 V) when  $I_{POORSRC}$  (typical 30 mA) current is applied (not a poor source)
- VBUS\_STAT changes state (VBUS\_STAT any bit change)
- Good input source removed
- Entering IINDPM regulation
- Entering VINDPM regulation
- Entering IC junction temperature regulation (TREG)
- I<sup>2</sup>C Watchdog timer expired
  - At initial power up, this INT gets asserted to signal I<sup>2</sup>C is ready for communication
- Charger status changes state (CHRG\_STAT value change), including Charge Complete
- TS\_STAT changes state (TS\_STAT any bit change)
- VBUS over-voltage detected (VBUS\_OVP)
- VAC over-voltage detected (VAC\_OVP for VAC1 or VAC2)
- Junction temperature shutdown (TSHUT)
- Battery over-voltage detected (BATOVP)
- System over-voltage detected (VSYS\_OVP)
- IBUS over-current detected (IBUS\_OCP)
- IBAT over-current detected (IBAT\_OCP)
- Charge safety timer expired, including trickle charge and pre-charge and fast charge safety timer expired
- A rising edge on any of the \*\_STAT bits

Each one of these INT sources can be masked off to prevent INT pulses from being sent out when they occur. Three bits exist for each one of these events:

- The STAT bit holds the *current status* of each INT source
- The FLAG bit holds information on which source produced an INT, regardless of the *current status*
- The MASK bit is used to prevent the device from sending out INT for each particular event

When one of the above conditions occurs (a rising edge on any of the \*\_STAT bits), the device sends out an INT pulse and keeps track of which source generated the INT via the FLAG registers. The FLAG register bits are automatically reset to zero after the host reads them, and a new edge on STAT bit is required to re-assert the FLAG.



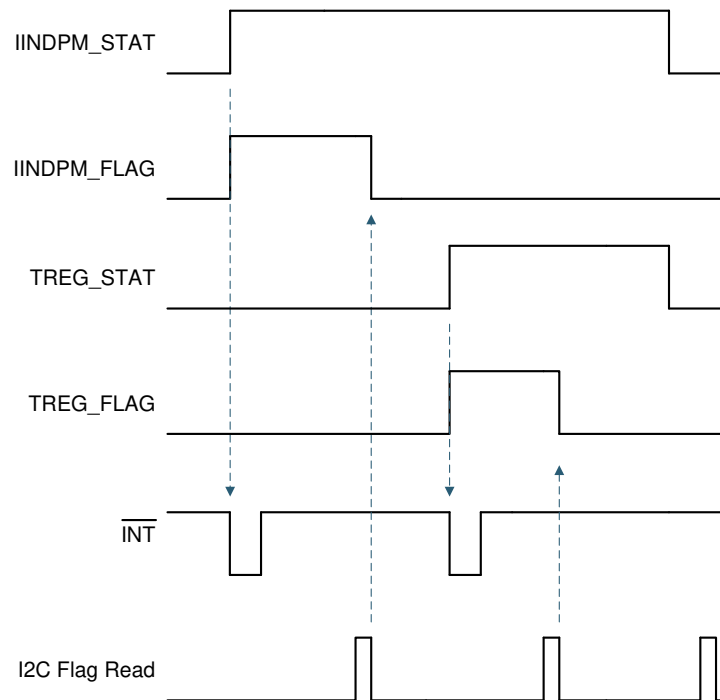


图 8-11.  $\overline{\text{INT}}$  Generation Behavior Example

### 8.3.10 Ship FET Control

The charger provides an N-FET driving pin (SDRV) to control an external ship FET. When this ship FET is off, it removes leakage current from the battery to the system. The ship FET is controlled by the SDRV\_CTRL[1:0] register bits, to support the shutdown mode, ship mode and the system power reset.

- **IDLE Mode** when SDRV\_CTRL[1:0] = 00, POR default. The external ship FET is fully on, I<sup>2</sup>C is enabled. The internal BATFET status is determined by the charging status. This mode could be for adapter present forward mode or battery only condition.
- **Shutdown Mode** when SDRV\_CTRL[1:0] = 01. The ship FET and the internal BATFET are both off. The I<sup>2</sup>C is disabled. The charger is totally shutdown and can only be woken up by an adapter plug-in. This mode is only for the battery only condition.
- **Ship Mode** when SDRV\_CTRL[1:0] = 10. The ship FET and the internal BATFET are both off. The I<sup>2</sup>C is still enabled. The charger can be woken up by setting SDRV\_CTRL[1:0] back to 00, or pulling the  $\overline{\text{QON}}$  pin low, or an adapter plug-in. This mode is only for the battery only condition.
- **System Power Reset** when SDRV\_CTRL[1:0] = 11. The ship FET is turned off for typical 350 ms to reset the system power (converter goes to HIZ mode if VBUS is high), then the ship FET is fully turned on again. The BATFET keeps the status unchanged during the system power reset. After the reset is done, SDRV\_CTRL[1:0] goes back to 00.

When the host changes SDRV\_CTRL[1:0] from 00 to the other values, the charger turns off the ship FET immediately or delays by  $t_{\text{SM\_DLY}}$  as configured by SDRV\_DLY bit. The application diagram when the battery is connected to the charger through an external ship FET is illustrated in the figure below.

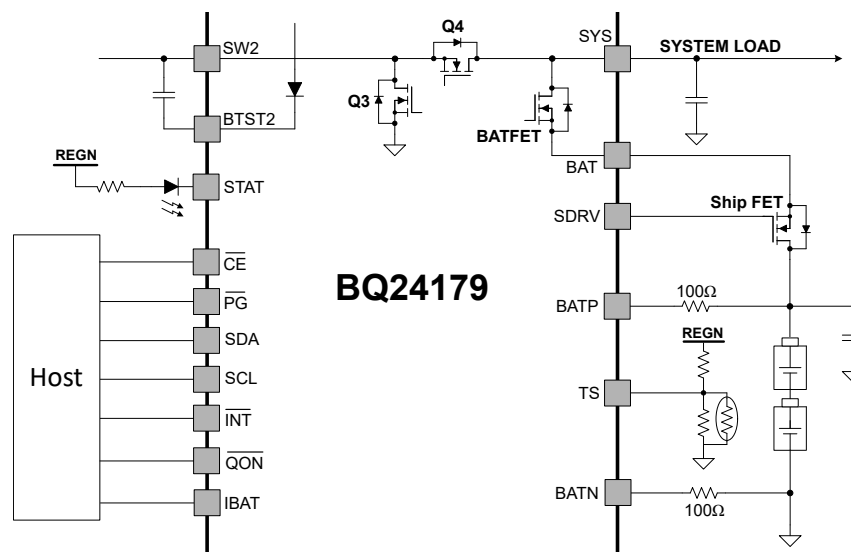


图 8-12. The Application Diagram for the External Ship FET

### 8.3.10.1 Shutdown Mode

To further reduce battery leakage current, the host can shut down the charger by setting the register bits `SDRV_CTRL[1:0]` to 01. In this mode, the  $I^2C$  is disabled and the charger is totally shut down. The device can only be woken up by plugging in an adapter.

After the `SDRV_CTRL[1:0]` is set to 01, the external ship FET turns off either immediately or after waiting for 10s as configured by `SDRV_DLY` register bit. When `VBUS` is high because of an adapter being present `SDRV_CTRL[1:0]` will be reset to 00 if the host writes it to 01.

When the device exits shutdown mode, the `SDRV_CTRL` bits are reset to the POR default values (00).

### 8.3.10.2 Ship Mode

To extend battery life and minimize the system power loss when system is powered off during idle, shipping or storage, the device can turn off `BATFET` and external ship FET to minimize the battery leakage current. The ship mode is enabled when the host sets `SDRV_CTRL[1:0]` to 10. The  $I^2C$  is still enabled, but the charger system clock slows down to minimize the device quiescent current.

After the `SDRV_CTRL[1:0]` is set to 10, the external ship FET is turned off either immediately or after waiting 10 seconds as configured by `SDRV_DLY` register bit. When `VBUS` is high because of an adapter being present `SDRV_CTRL[1:0]` automatically resets to 00 if the host writes it to 10.

The ship mode is disabled by one of the following events. The charger turns on ship FET and internal `BATFET` to reconnect the battery to the system, `SDRV_CTRL` bits are reset to the POR default values (00).

- Plug in an adapter
- Set `SDRV_CTRL[1:0] = 00`
- Set `REG_RST = 1`, to reset all the registers including `SDRV_CTRL` bits back to default (00)
- A logic low of  $t_{SM\_EXIT}$  (typical 1s or 15ms programmed by `WKUP_DLY` bit) duration on `QON` pin

### 8.3.10.3 System Power Reset

The host can reset the system power by:

- Set the register bits `SDRV_CTRL[1:0]` to 11
- A logic low of  $t_{RST}$  (typical 10s) duration on `QON` pin

When the system power reset is enabled, the device turns off the ship FET and also sets the charger in HIZ mode if `VBUS` is high for  $t_{RST\_SFET}$  (typical 350ms), then turns on the ship FET and also disable the charger HIZ

mode to provide full system power reset. When the SFET is off for  $t_{RST\_SFET}$ , the charger applies a typical 30-mA sink current on SYS to discharge system voltage down.

No matter the charger is at battery only condition or in the forward charging mode with adapter present, the charger resets the system power when the SDRV\_CTRL[1:0] bits are set to 11 or the QON pin is pulled low for  $t_{RST}$  duration.

### 8.3.11 Protections

#### 8.3.11.1 Voltage and Current Monitoring

The device closely monitors the input, system and battery voltage and current, as well as internal FET currents for safe converter operation. The charger provides the faults protection list below:

- VAC Over-voltage Protection (VAC\_OVP)
- VBUS Over-voltage Protection (VBUS\_OVP)
- VBUS Under-voltage Protection (POORSRC)
- System Over-voltage Protection (VSYS\_OVP)
- System Short Protection (VSYS\_SHORT)
- Battery Over-voltage Protection (VBAT\_OVP)
- Battery Over-current Protection (IBAT\_OCP)
- Input Over-current Protection (IBUS\_OCP)

#### 8.3.11.2 Thermal Regulation and Thermal Shutdown

The device monitors its internal junction temperature ( $T_J$ ) to avoid overheating and to limit the IC surface temperature. When the internal junction temperature exceeds the preset thermal regulation limit (TREG bits), the device reduces the charge current to maintain the junction temperature at the thermal regulation limit. A wide thermal regulation range from 60°C to 120°C allows optimization of the system thermal performance. During thermal regulation, the actual charging current is usually below the programmed value in the ICHG registers. Therefore, termination is disabled, the fast charging safety timer runs at half the clock rate, the status register TREG\_STAT bit goes high, TREG\_FLAG bit is set to 1, and an  $\overline{INT}$  is asserted to alert host unless TREG\_MASK is set to 1.

Additionally, the device has thermal shutdown to turn off the converter when the IC junction temperature exceeds the TSHUT threshold. The fault register bits TSHUT\_STAT and TSHUT\_FLAG are set and an  $\overline{INT}$  pulse is asserted to the host, unless TSHUT\_MASK is set to 1. The BATFET and the converter resumes normal operation when the IC die temperature decreases lower than TSHUT threshold by  $T_{SHUT\_HYS}$ .

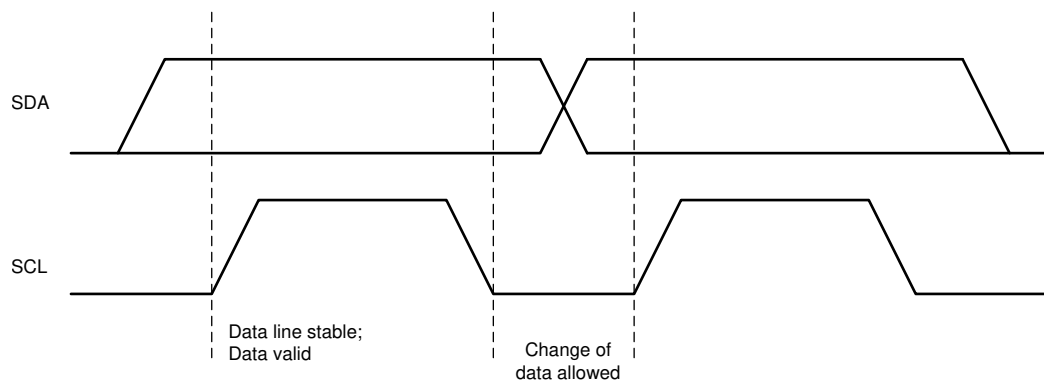
### 8.3.12 Serial Interface

The device uses I<sup>2</sup>C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I<sup>2</sup>C is a bi-directional 2-wire serial interface. Only two open-drain bus lines are required: a serial data line (SDA), and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is a device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address 0x6B, receiving control inputs from the master device like micro-controller or digital signal processor through REG00 – REG25. Register read beyond REG25 (0x25), returns 0xFF. The I<sup>2</sup>C interface supports both standard mode (up to 100 kbits/s), and fast mode (up to 400 kbits/s). When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain and must be connected to the positive supply voltage via a current source or pull-up resistor.

#### 8.3.12.1 Data Validity

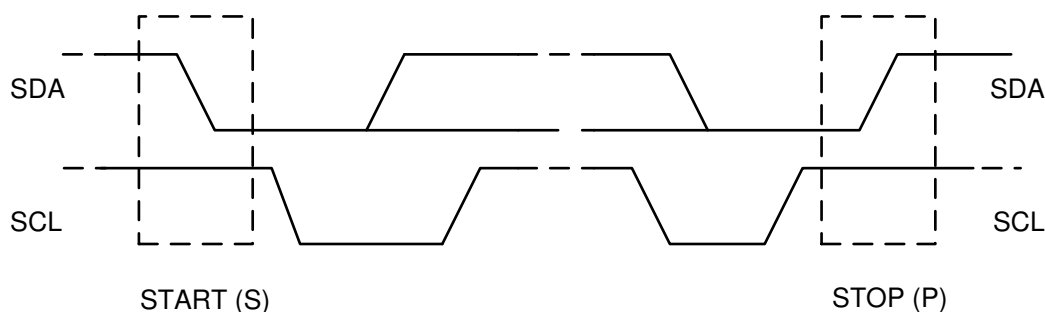
The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on SCL line is LOW. One clock pulse is generated for each data bit transferred.

图 8-13. Bit Transfers on the I<sup>2</sup>C Bus

### 8.3.12.2 START and STOP Conditions

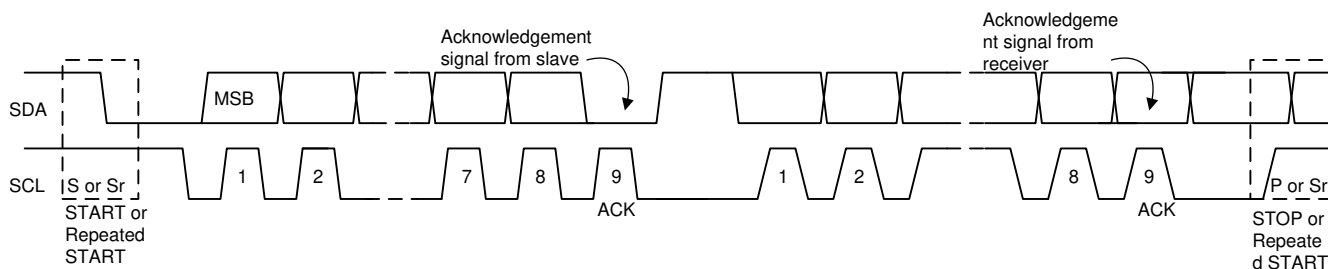
All transactions begin with a START (S) and are terminated with a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

图 8-14. START and STOP Conditions on the I<sup>2</sup>C Bus

### 8.3.12.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an ACKNOWLEDGE (ACK) bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the SCL line low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and releases the SCL line.

图 8-15. Data Transfer on the I<sup>2</sup>C Bus

#### 8.3.12.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The ACK signaling takes place after byte. The ACK bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9<sup>th</sup> clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this 9<sup>th</sup> clock pulse.

A NACK is signaled when the SDA line remains HIGH during the 9<sup>th</sup> clock pulse. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

#### 8.3.12.5 Slave Address and Data Direction Bit

After the START signal, a slave address is sent. This address is 7 bits long, followed by the 8 bit as a data direction bit (bit R/  $\overline{W}$ ). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ). The device 7-bit address is defined as 1101 011' (0x6B) by default. The address bit arrangement is shown below.

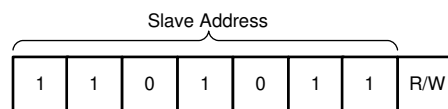


图 8-16. 7-Bit Addressing (0x6B)

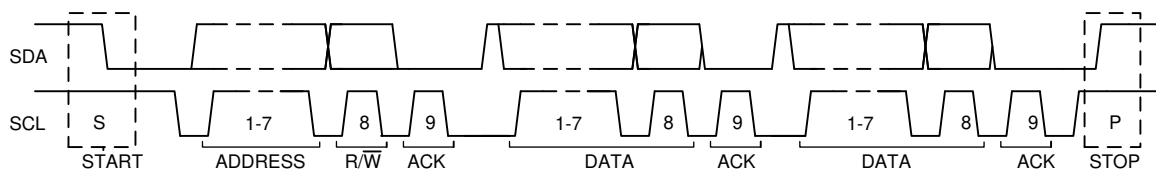


图 8-17. Complete Data Transfer on the I<sup>2</sup>C Bus

#### 8.3.12.6 Single Write and Read

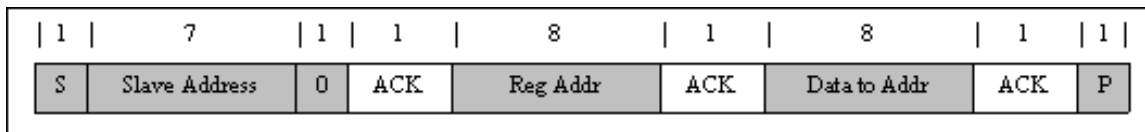


图 8-18. Single Write

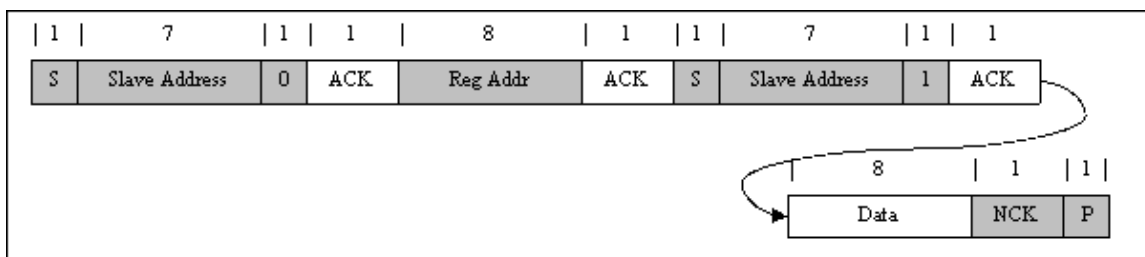


图 8-19. Single Read

If the register address is not defined, the charger IC sends back NACK and returns to the idle state.

#### 8.3.12.7 Multi-Write and Multi-Read

The charger device supports multi-read and multi-write of all registers.

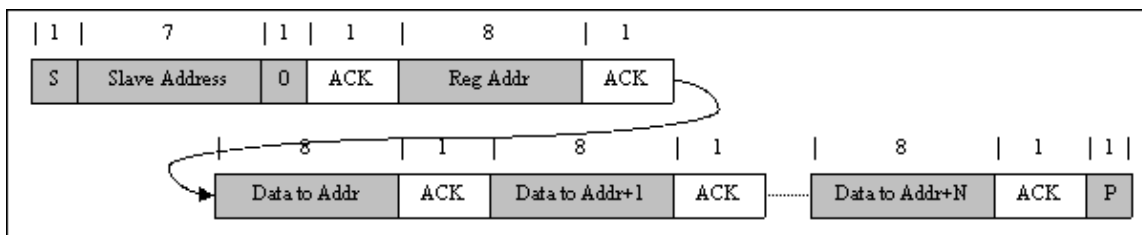


图 8-20. Multi-Write

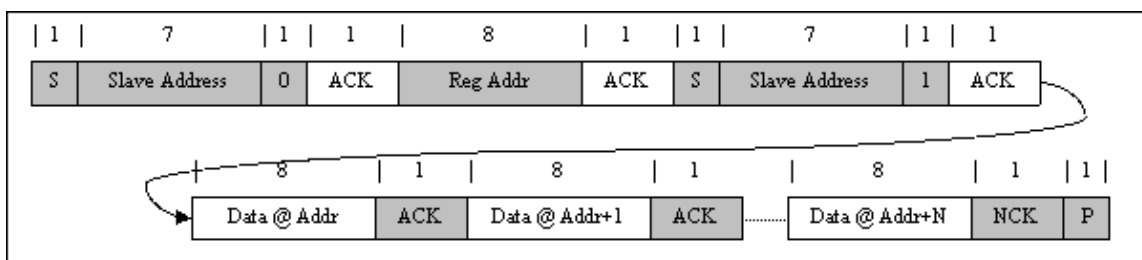


图 8-21. Multi-Read

## 8.4 Device Functional Modes

### 8.4.1 Host Mode and Default Mode

The device is a host controlled charger, but it can operate in default mode without host management. In default mode, the device can be used as an autonomous charger with no host or while host is in sleep mode. When the charger is in default mode, WD\_STAT bit becomes HIGH, WD\_FLAG is set to 1, and an  $\overline{\text{INT}}$  is asserted low to alert the host (unless masked by WD\_MASK). The WD\_FLAG bit would read as 1 upon the first read and then 0 upon subsequent reads. When the charger is in host mode, WD\_STAT bit is LOW.

After power-on-reset, the device starts in default mode with watchdog timer expired, or default mode. All the registers are in the default settings.

In default mode, the device keeps charging the battery with default 1-hour trickle charging safety timer, 2-hour pre-charging safety timer and the 12-hour fast charging safety timer. At the end of the 1-hour or 2-hour or 12-hour timer expired, the charging is stopped and the buck-boost converter continues to operate to supply system load.

A write to any I<sup>2</sup>C register transitions the charger from default mode to host mode, and initiates the watchdog timer. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD\_RST bit before the watchdog timer expires (WD\_STAT bit is set), or disable watchdog timer by setting WATCHDOG bits = 00.

When the watchdog timer is expired, the device returns to default mode and all registers are reset to default values except the ones described as detailed in the Register Map section. The Watchdog timer will be reset on any write if the watchdog timer has expired. When watchdog timer expires, WD\_STAT and WD\_FLAG is set to 1, and an  $\overline{\text{INT}}$  is asserted low to alert the host (unless masked by WD\_MASK).

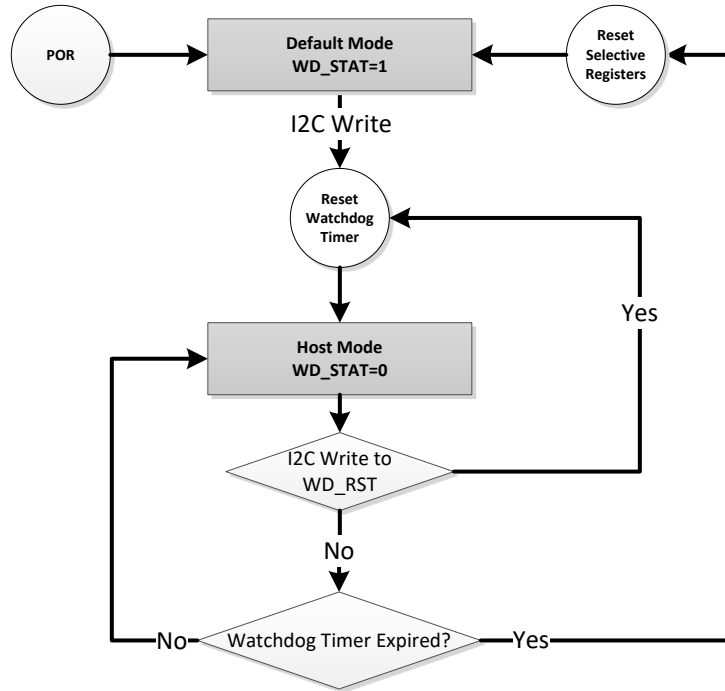


图 8-22. Watchdog Timer Flow Chart

#### 8.4.2 Register Bit Reset

Beside the register reset by the watchdog timer in the default mode, the register and the timer could be reset to the default value by writing the REG\_RST bit to 1. The register bits, which can be reset by the REG\_RST bit, are noted in the Register Map section. After the register reset, the REG\_RST bit will go back from 1 to 0 automatically.

The register reset by the REG\_RST bit will not initiate the ACFET-RBFET detection, which is only done at the charger first time POR. It will not repeat the open-circuit adapter measurements for the default VINDPM setting, which is only done when an adapter is plugged in. In addition, if the charger is in the process of forced ICO, the forced D+/D- detection or the forced open-circuit adapter measurements, set the REG\_RST to 1 will terminate all of these processes, because reset the register to default values will set FORCE\_ICO, FORCE\_INDET and FORCE\_VINDPM\_DET bits to 0.

## 8.5 Register Map

### 8.5.1 I<sup>2</sup>C Registers

表 8-6 lists the I<sup>2</sup>C registers. All register offset addresses not listed in 表 8-6 should be considered as reserved locations and the register contents should not be modified.

表 8-6. I2C Registers

| Offset | Acronym                      | Register Name          | Section    |
|--------|------------------------------|------------------------|------------|
| 0h     | REG00_Minimal_System_Voltage | Minimal System Voltage | 节 8.5.1.2  |
| 1h     | REG01_Charge_Voltage_Limit   | Charge Voltage Limit   | 节 8.5.1.3  |
| 3h     | REG03_Charge_Current_Limit   | Charge Current Limit   | 节 8.5.1.4  |
| 5h     | REG05_Input_Voltage_Limit    | Input Voltage Limit    | 节 8.5.1.5  |
| 6h     | REG06_Input_Current_Limit    | Input Current Limit    | 节 8.5.1.6  |
| 8h     | REG08_Precharge_Control      | Precharge Control      | 节 8.5.1.7  |
| 9h     | REG09_Termination_Control    | Termination Control    | 节 8.5.1.8  |
| Ah     | REG0A_Re-charge_Control      | Re-charge Control      | 节 8.5.1.9  |
| Bh     | REG0B_Reserved               | Reserved               | 节 8.5.1.10 |
| Dh     | REG0D_Pre-charge_Timer       | Pre-charge Timer       | 节 8.5.1.11 |
| Eh     | REG0E_Timer_Control          | Timer Control          | 节 8.5.1.12 |
| Fh     | REG0F_Charger_Control_0      | Charger Control 0      | 节 8.5.1.13 |
| 10h    | REG10_Charger_Control_1      | Charger Control 1      | 节 8.5.1.14 |
| 11h    | REG11_Charger_Control_2      | Charger Control 2      | 节 8.5.1.15 |
| 12h    | REG12_Charger_Control_3      | Charger Control 3      | 节 8.5.1.16 |
| 13h    | REG13_Charger_Control_4      | Charger Control 4      | 节 8.5.1.17 |
| 14h    | REG14_Charger_Control_5      | Charger Control 5      | 节 8.5.1.18 |
| 15h    | REG15_Reserved               | Reserved               | 节 8.5.1.19 |
| 16h    | REG16_Temperature_Control    | Temperature Control    | 节 8.5.1.20 |
| 17h    | REG17_NTC_Control_0          | NTC Control 0          | 节 8.5.1.21 |
| 18h    | REG18_NTC_Control_1          | NTC Control 1          | 节 8.5.1.22 |
| 19h    | REG19_ICO_Current_Limit      | ICO Current Limit      | 节 8.5.1.23 |
| 1Bh    | REG1B_Charger_Status_0       | Charger Status 0       | 节 8.5.1.24 |
| 1Ch    | REG1C_Charger_Status_1       | Charger Status 1       | 节 8.5.1.25 |
| 1Dh    | REG1D_Charger_Status_2       | Charger Status 2       | 节 8.5.1.26 |
| 1Eh    | REG1E_Charger_Status_3       | Charger Status 3       | 节 8.5.1.27 |
| 1Fh    | REG1F_Charger_Status_4       | Charger Status 4       | 节 8.5.1.28 |
| 20h    | REG20_FAULT_Status_0         | FAULT Status 0         | 节 8.5.1.29 |
| 21h    | REG21_FAULT_Status_1         | FAULT Status 1         | 节 8.5.1.30 |
| 22h    | REG22_Charger_Flag_0         | Charger Flag 0         | 节 8.5.1.31 |
| 23h    | REG23_Charger_Flag_1         | Charger Flag 1         | 节 8.5.1.32 |
| 24h    | REG24_Charger_Flag_2         | Charger Flag 2         | 节 8.5.1.33 |
| 25h    | REG25_Charger_Flag_3         | Charger Flag 3         | 节 8.5.1.34 |
| 26h    | REG26_FAULT_Flag_0           | FAULT Flag 0           | 节 8.5.1.35 |
| 27h    | REG27_FAULT_Flag_1           | FAULT Flag 1           | 节 8.5.1.36 |
| 28h    | REG28_Charger_Mask_0         | Charger Mask 0         | 节 8.5.1.37 |
| 29h    | REG29_Charger_Mask_1         | Charger Mask 1         | 节 8.5.1.38 |
| 2Ah    | REG2A_Charger_Mask_2         | Charger Mask 2         | 节 8.5.1.39 |



**表 8-6. I2C Registers (continued)**

| Offset | Acronym                      | Register Name          | Section                    |
|--------|------------------------------|------------------------|----------------------------|
| 2Bh    | REG2B_Charger_Mask_3         | Charger Mask 3         | <a href="#">节 8.5.1.40</a> |
| 2Ch    | REG2C_FAULT_Mask_0           | FAULT Mask 0           | <a href="#">节 8.5.1.41</a> |
| 2Dh    | REG2D_FAULT_Mask_1           | FAULT Mask 1           | <a href="#">节 8.5.1.42</a> |
| 2Eh    | REG2E_ADC_Control            | ADC Control            | <a href="#">节 8.5.1.43</a> |
| 2Fh    | REG2F_ADC_Function_Disable_0 | ADC Function Disable 0 | <a href="#">节 8.5.1.44</a> |
| 30h    | REG30_ADC_Function_Disable_1 | ADC Function Disable 1 | <a href="#">节 8.5.1.45</a> |
| 31h    | REG31_IBUS_ADC               | IBUS ADC               | <a href="#">节 8.5.1.46</a> |
| 33h    | REG33_IBAT_ADC               | IBAT ADC               | <a href="#">节 8.5.1.47</a> |
| 35h    | REG35_VBUS_ADC               | VBUS ADC               | <a href="#">节 8.5.1.48</a> |
| 37h    | REG37_VAC1_ADC               | VAC1 ADC               | <a href="#">节 8.5.1.49</a> |
| 39h    | REG39_VAC2_ADC               | VAC2 ADC               | <a href="#">节 8.5.1.50</a> |
| 3Bh    | REG3B_VBAT_ADC               | VBAT ADC               | <a href="#">节 8.5.1.51</a> |
| 3Dh    | REG3D_VSYS_ADC               | VSYS ADC               | <a href="#">节 8.5.1.52</a> |
| 3Fh    | REG3F_TS_ADC                 | TS ADC                 | <a href="#">节 8.5.1.53</a> |
| 41h    | REG41_TDIE_ADC               | TDIE_ADC               | <a href="#">节 8.5.1.54</a> |
| 43h    | REG43_D+_ADC                 | D+ ADC                 | <a href="#">节 8.5.1.55</a> |
| 45h    | REG45_D-_ADC                 | D- ADC                 | <a href="#">节 8.5.1.56</a> |
| 47h    | REG47_DPDM_Driver            | DPDM Driver            | <a href="#">节 8.5.1.57</a> |
| 48h    | REG48_Part_Information       | Part Information       | <a href="#">节 8.5.1.58</a> |

Complex bit access types are encoded to fit into small table cells. 表 8-7 shows the codes that are used for access types in this section.

**表 8-7. I2C Access Type Codes**

| Access Type              | Code | Description  |
|--------------------------|------|--|
| Read Type                |      |  |
| R                        | R    | Read   |
| Write Type               |      |  |
| W                        | W    | Write  |
| Reset or Default Value   |      |  |
| -n                       |      | Value after reset or the default value   |
| Register Array Variables |      |  |
| i,j,k,l,m,n              |      | When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula. |
| y                        |      | When this variable is used in a register name, an offset, or an address it refers to the value of a register array.  |

### 8.5.1.1 REG00\_Minimal\_System\_Voltage Register (Offset = 0h) [reset = X]

REG00\_Minimal\_System\_Voltage is shown in 图 8-23 and described in 表 8-8.

Return to the 表 8-6.

Minimal System Voltage

图 8-23. REG00\_Minimal\_System\_Voltage Register

| 7        | 6 | 5           | 4 | 3 | 2 | 1 | 0 |
|----------|---|-------------|---|---|---|---|---|
| RESERVED |   | VSYSMIN_5:0 |   |   |   |   |   |
| R/W-0h   |   | R/W-X       |   |   |   |   |   |

表 8-8. REG00\_Minimal\_System\_Voltage Register Field Descriptions

| Bit | Field       | Type | Reset | Notes                | Description   |
|-----|-------------|------|-------|----------------------|---|
| 7-6 | RESERVED    | R/W  | 0h    |                      | RESERVED  |
| 5-0 | VSYSMIN_5:0 | R/W  | X     | Reset by:<br>REG_RST | Minimal System Voltage:<br>During POR, the device reads the resistance tie to<br>PROG pin, to identify the default battery cell count and<br>determine the default power on VSYSMIN list below:<br>1s: 3.5 V<br>2s: 7 V<br>3s: 9 V<br>4s: 12 V<br>Type : RW<br>Range : 2500 mV-16000 mV<br>Fixed Offset : 2500 mV<br>Bit Step Size : 250 mV<br>Clamped High |

### 8.5.1.2 REG01\_Charge\_Voltage\_Limit Register (Offset = 1h) [reset = X]

REG01\_Charge\_Voltage\_Limit is shown in 图 8-24 and described in 表 8-9.

Return to the 表 8-6.

Charge Voltage Limit

图 8-24. REG01\_Charge\_Voltage\_Limit Register

|           |    |    |    |    |    |           |   |
|-----------|----|----|----|----|----|-----------|---|
| 15        | 14 | 13 | 12 | 11 | 10 | 9         | 8 |
| RESERVED  |    |    |    |    |    | VREG_10:0 |   |
| R-0h      |    |    |    |    |    | R/W-X     |   |
| 7         | 6  | 5  | 4  | 3  | 2  | 1         | 0 |
| VREG_10:0 |    |    |    |    |    |           |   |
| R/W-X     |    |    |    |    |    |           |   |

表 8-9. REG01\_Charge\_Voltage\_Limit Register Field Descriptions

| Bit   | Field     | Type | Reset | Notes                | Description  |
|-------|-----------|------|-------|----------------------|--|
| 15-11 | RESERVED  | R    | 0h    |                      | RESERVED   |
| 10-0  | VREG_10:0 | R/W  | X     | Reset by:<br>REG_RST | Battery Voltage Limit:<br>During POR, the device reads the resistance tie to PROG pin, to identify the default battery cell count and determine the default power-on battery voltage regulation limit:<br>1s: 4.2 V<br>2s: 8.4 V<br>3s: 12.6 V<br>4s: 16.8 V<br>Type : RW<br>Range : 3000 mV-18800 mV<br>Fixed Offset : 0 mV<br>Bit Step Size : 10 mV<br>Clamped Low |

### 8.5.1.3 REG03\_Charge\_Current\_Limit Register (Offset = 3h) [reset = X]

REG03\_Charge\_Current\_Limit is shown in 图 8-25 and described in 表 8-10.

Return to the 表 8-6.

Charge Current Limit

图 8-25. REG03\_Charge\_Current\_Limit Register

|          |    |    |    |    |    |   |          |
|----------|----|----|----|----|----|---|----------|
| 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8        |
| RESERVED |    |    |    |    |    |   | ICHG_8:0 |
| R-0h     |    |    |    |    |    |   | R/W-X    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1 | 0        |
| ICHG_8:0 |    |    |    |    |    |   |          |
| R/W-X    |    |    |    |    |    |   |          |

表 8-10. REG03\_Charge\_Current\_Limit Register Field Descriptions

| Bit  | Field    | Type | Reset | Notes                            | Description  |
|------|----------|------|-------|----------------------------------|--|
| 15-9 | RESERVED | R    | 0h    |                                  | RESERVED   |
| 8-0  | ICHG_8:0 | R/W  | X     | Reset by:<br>WATCHDOG<br>REG_RST | Charge Current Limit<br>During POR, the device reads the resistance tie to PROG pin, to identify the default battery cell count and determine the default power-on battery charging current:<br>1s and 2s: 2 A<br>3s and 4s: 1A<br>Type : RW<br>Range : 50 mA-5000 mA<br>Fixed Offset : 0 mA<br>Bit Step Size : 10 mA<br>Clamped Low |

#### 8.5.1.4 REG05\_Input\_Voltage\_Limit Register (Offset = 5h) [reset = 24h]

REG05\_Input\_Voltage\_Limit is shown in 图 8-26 and described in 表 8-11.

Return to the 表 8-6.

Input Voltage Limit

图 8-26. REG05\_Input\_Voltage\_Limit Register

| 7          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|---|---|---|---|---|---|---|
| VINDPM_7:0 |   |   |   |   |   |   |   |
| R/W-24h    |   |   |   |   |   |   |   |

表 8-11. REG05\_Input\_Voltage\_Limit Register Field Descriptions

| Bit | Field      | Type | Reset | Description   |
|-----|------------|------|-------|---|
| 7-0 | VINDPM_7:0 | R/W  | 24h   | Absolute VINDPM Threshold<br>VINDPM register is reset to 3600mV upon adapter unplugged and it is set to the value based on the VBUS measurement when the adapter plugs in. It is not reset by the REG_RST and the WATCHDOG<br>Type : RW<br>POR: 3600 mV (24h)<br>Range : 3600 mV-22000 mV<br>Fixed Offset : 0 mV<br>Bit Step Size : 100 mV<br>Clamped Low |

### 8.5.1.5 REG06\_Input\_Current\_Limit Register (Offset = 6h) [reset = 12Ch]

REG06\_Input\_Current\_Limit is shown in 图 8-27 and described in 表 8-12.

Return to the 表 8-6.

Input Current Limit

图 8-27. REG06\_Input\_Current\_Limit Register

|            |    |    |    |    |    |   |            |
|------------|----|----|----|----|----|---|------------|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8          |
| RESERVED   |    |    |    |    |    |   | IINDPM_8:0 |
| R-0h       |    |    |    |    |    |   | R/W-12Ch   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0          |
| IINDPM_8:0 |    |    |    |    |    |   |            |
| R/W-12Ch   |    |    |    |    |    |   |            |

表 8-12. REG06\_Input\_Current\_Limit Register Field Descriptions

| Bit  | Field      | Type | Reset | Notes                | Description   |
|------|------------|------|-------|----------------------|---|
| 15-9 | RESERVED   | R    | 0h    |                      | RESERVED  |
| 8-0  | IINDPM_8:0 | R/W  | 12Ch  | Reset by:<br>REG_RST | Based on D+/D- detection results:<br>USB SDP = 500 mA<br>USB CDP = 1.5 A<br>USB DCP = 3.25 A<br>Adjustable High Voltage DCP = 1.5 A<br>Unknown Adapter = 3 A<br>Non-Standard Adapter = 1 A/2 A/2.1 A/2.4 A<br>Type : RW<br>POR: 3000 mA (12Ch)<br>Range : 100 mA-3300 mA<br>Fixed Offset : 0 mA<br>Bit Step Size : 10 mA<br>Clamped Low |

### 8.5.1.6 REG08\_Precharge\_Control Register (Offset = 8h) [reset = C3h]

REG08\_Precharge\_Control is shown in 图 8-28 and described in 表 8-13.

Return to the 表 8-6.

Precharge Control

图 8-28. REG08\_Precharge\_Control Register

| 7             | 6 | 5 | 4           | 3 | 2 | 1 | 0 |
|---------------|---|---|-------------|---|---|---|---|
| VBAT_LOWV_1:0 |   |   | IPRECHG_5:0 |   |   |   |   |
| R/W-3h        |   |   | R/W-3h      |   |   |   |   |

表 8-13. REG08\_Precharge\_Control Register Field Descriptions

| Bit | Field         | Type | Reset | Notes                            | Description  |
|-----|---------------|------|-------|----------------------------------|--|
| 7-6 | VBAT_LOWV_1:0 | R/W  | 3h    | Reset by:<br>REG_RST             | Battery voltage thresholds for the transition from precharge to fast charge, which is defined as a ratio of battery regulation limit (VREG)<br>Type : RW<br>POR: 11b<br>0h = 15%*VREG<br>1h = 62.2%*VREG<br>2h = 66.7%*VREG<br>3h = 71.4%*VREG |
| 5-0 | IPRECHG_5:0   | R/W  | 3h    | Reset by:<br>WATCHDOG<br>REG_RST | Precharge current limit<br>Type : RW<br>POR: 120 mA (3h)<br>Range : 40 mA-2000 mA<br>Fixed Offset : 0 mA<br>Bit Step Size : 40 mA<br>Clamped Low   |



### 8.5.1.7 REG09\_Termination\_Control Register (Offset = 9h) [reset = 5h]

REG09\_Termination\_Control is shown in 图 8-29 and described in 表 8-14.

Return to the 表 8-6.

Termination Control

图 8-29. REG09\_Termination\_Control Register

| 7        | 6       | 5        | 4         | 3 | 2 | 1 | 0 |
|----------|---------|----------|-----------|---|---|---|---|
| RESERVED | REG_RST | RESERVED | ITERM_4:0 |   |   |   |   |
| R-0h     | R/W-0h  | R/W-0h   | R/W-5h    |   |   |   |   |

表 8-14. REG09\_Termination\_Control Register Field Descriptions

| Bit | Field     | Type | Reset | Notes                            | Description  |
|-----|-----------|------|-------|----------------------------------|--|
| 7   | RESERVED  | R    | 0h    |                                  | RESERVED   |
| 6   | REG_RST   | R/W  | 0h    |                                  | Reset registers to default values and reset timer<br>Type : RW<br>POR: 0b<br>0h = Not reset<br>1h = Reset                                    |
| 5   | RESERVED  | R/W  | 0h    |                                  | RESERVED   |
| 4-0 | ITERM_4:0 | R/W  | 5h    | Reset by:<br>WATCHDOG<br>REG_RST | Termination current<br>Type : RW<br>POR: 200 mA (5h)<br>Range : 40 mA-1000 mA<br>Fixed Offset : 0 mA<br>Bit Step Size : 40 mA<br>Clamped Low |

### 8.5.1.8 REG0A\_Re-charge\_Control Register (Offset = Ah) [reset = X]

REG0A\_Re-charge\_Control is shown in 图 8-30 and described in 表 8-15.

Return to the 表 8-6.

Re-charge Control

**图 8-30. REG0A\_Re-charge\_Control Register**

| 7        | 6 | 5          | 4 | 3          | 2 | 1 | 0 |
|----------|---|------------|---|------------|---|---|---|
| CELL_1:0 |   | TRECHG_1:0 |   | VRECHG_3:0 |   |   |   |
| R/W-X    |   | R/W-2h     |   | R/W-3h     |   |   |   |

**表 8-15. REG0A\_Re-charge\_Control Register Field Descriptions**

| Bit | Field      | Type | Reset | Notes                            | Description   |
|-----|------------|------|-------|----------------------------------|---|
| 7-6 | CELL_1:0   | R/W  | X     |                                  | At POR, the charger reads the PROG pin resistance to determine the battery cell count and update this CELL bits accordingly.<br>Type : RW<br>0h = 1s<br>1h = 2s<br>2h = 3s<br>3h = 4s |
| 5-4 | TRECHG_1:0 | R/W  | 2h    | Reset by:<br>WATCHDOG<br>REG_RST | Battery recharge deglich time<br>Type : RW<br>POR: 10b<br>0h = 64ms<br>1h = 256ms<br>2h = 1024ms (default)<br>3h = 2048ms   |
| 3-0 | VRECHG_3:0 | R/W  | 3h    | Reset by:<br>WATCHDOG<br>REG_RST | Battery Recharge Threshold Offset (Below VREG)<br>Type : RW<br>POR: 200 mV (3h)<br>Range : 50 mV-800 mV<br>Fixed Offset : 50 mV<br>Bit Step Size : 50 mV                              |

### 8.5.1.9 REG0B\_Reserved Register (Offset = Bh) [reset = DCh]

Return to the [表 8-6](#).

图 8-31. REG0B\_Reserved Register

|          |    |    |    |    |    |          |   |
|----------|----|----|----|----|----|----------|---|
| 15       | 14 | 13 | 12 | 11 | 10 | 9        | 8 |
| RESERVED |    |    |    |    |    | RESERVED |   |
| R-0h     |    |    |    |    |    | R-DCh    |   |
| 7        | 6  | 5  | 4  | 3  | 2  | 1        | 0 |
| RESERVED |    |    |    |    |    |          |   |
| R-DCh    |    |    |    |    |    |          |   |

表 8-16. REG0B\_Reserved Register Field Descriptions

| Bit   | Field    | Type | Reset | Notes | Description |
|-------|----------|------|-------|-------|-------------|
| 15-11 | RESERVED | R    | 0h    |       | RESERVED    |
| 10-0  | RESERVED | R    | DCh   |       | RESERVED    |

### 8.5.1.10 REG0D\_Pre-charge\_Timer Register(Offset = Dh) [reset = 4Bh]

Return to the [表 8-6](#).

**图 8-32. REG0D\_Pre-charge\_Timer Register**

| 7          | 6 | 5        | 4 | 3 | 2 | 1 | 0 |
|------------|---|----------|---|---|---|---|---|
| PRECHG_TMR |   | RESERVED |   |   |   |   |   |
| R/W-0h     |   | R-4Bh    |   |   |   |   |   |

**表 8-17. REG0D\_Pre-charge\_Timer Register Field Descriptions**

| Bit | Field      | Type | Reset | Notes                            | Description   |
|-----|------------|------|-------|----------------------------------|---|
| 7   | PRECHG_TMR | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | Pre-charge safety timer setting<br>Type : RW<br>POR: 0b<br>0h = 2 hrs (default)<br>1h = 0.5 hrs |
| 6-0 | RESERVED   | R    | 4Bh   |                                  | RESERVED  |

### 8.5.1.11 REG0E\_Timer\_Control Register (Offset = Eh) [reset = 3Dh]

REG0E\_Timer\_Control is shown in 图 8-33 and described in 表 8-18.

Return to the 表 8-6.

Timer Control

图 8-33. REG0E\_Timer\_Control Register

| 7              | 6 | 5             | 4             | 3          | 2           | 1 | 0        |
|----------------|---|---------------|---------------|------------|-------------|---|----------|
| TOPOFF_TMR_1:0 |   | EN_TRICHG_TMR | EN_PRECHG_TMR | EN_CHG_TMR | CHG_TMR_1:0 |   | TMR2X_EN |
| R/W-0h         |   | R/W-1h        | R/W-1h        | R/W-1h     | R/W-2h      |   | R/W-1h   |

表 8-18. REG0E\_Timer\_Control Register Field Descriptions

| Bit | Field          | Type | Reset | Notes                            | Description   |
|-----|----------------|------|-------|----------------------------------|---|
| 7-6 | TOPOFF_TMR_1:0 | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | Top-off timer control<br>Type : RW<br>POR: 00b<br>0h = Disabled (default)<br>1h = 15 mins<br>2h = 30 mins<br>3h = 45 mins   |
| 5   | EN_TRICHG_TMR  | R/W  | 1h    | Reset by:<br>WATCHDOG<br>REG_RST | Enable trickle charge timer (fixed as 1hr)<br>Type : RW<br>POR: 1b<br>0h = Disabled<br>1h = Enabled (default)   |
| 4   | EN_PRECHG_TMR  | R/W  | 1h    | Reset by:<br>WATCHDOG<br>REG_RST | Enable pre-charge timer<br>Type : RW<br>POR: 1b<br>0h = Disabled<br>1h = Enabled (default)  |
| 3   | EN_CHG_TMR     | R/W  | 1h    | Reset by:<br>WATCHDOG<br>REG_RST | Enable fast charge timer<br>Type : RW<br>POR: 1b<br>0h = Disabled<br>1h = Enabled (default)   |
| 2-1 | CHG_TMR_1:0    | R/W  | 2h    | Reset by:<br>WATCHDOG<br>REG_RST | Fast charge timer setting<br>Type : RW<br>POR: 10b<br>0h = 5 hrs<br>1h = 8 hrs<br>2h = 12 hrs (default)<br>3h = 24 hrs  |
| 0   | TMR2X_EN       | R/W  | 1h    | Reset by:<br>WATCHDOG<br>REG_RST | TMR2X_EN<br>Type : RW<br>POR: 1b<br>0h = Trickle charge, pre-charge and fast charge timer NOT slowed by 2X during input DPM or thermal regulation.<br>1h = Trickle charge, pre-charge and fast charge timer slowed by 2X during input DPM or thermal regulation (default) |

### 8.5.1.12 REG0F\_Charger\_Control\_0 Register (Offset = Fh) [reset = A2h]

REG0F\_Charger\_Control\_0 is shown in [图 8-34](#) and described in [表 8-19](#).

Return to the [表 8-6](#).

Charger Control 0

**图 8-34. REG0F\_Charger\_Control\_0 Register**

| 7               | 6             | 5      | 4      | 3         | 2      | 1       | 0        |
|-----------------|---------------|--------|--------|-----------|--------|---------|----------|
| EN_AUTO_IBATDIS | FORCE_IBATDIS | EN_CHG | EN_ICO | FORCE_ICO | EN_HIZ | EN_TERM | RESERVED |
| R/W-1h          | R/W-0h        | R/W-1h | R/W-0h | R/W-0h    | R/W-0h | R/W-1h  | R-0h     |

**表 8-19. REG0F\_Charger\_Control\_0 Register Field Descriptions**

| Bit | Field           | Type | Reset | Notes                            | Description  |
|-----|-----------------|------|-------|----------------------------------|--|
| 7   | EN_AUTO_IBATDIS | R/W  | 1h    | Reset by:<br>REG_RST             | Enable the auto battery discharging during the battery OVP fault<br>Type : RW<br>POR: 1b<br>0h = The charger will NOT apply a discharging current on BAT during battery OVP<br>1h = The charger will apply a discharging current on BAT during battery OVP |
| 6   | FORCE_IBATDIS   | R/W  | 0h    | Reset by:<br>REG_RST             | Force a battery discharging current<br>Type : RW<br>POR: 0b<br>0h = IDLE (default)<br>1h = Force the charger to apply a discharging current on BAT regardless the battery OVP status   |
| 5   | EN_CHG          | R/W  | 1h    | Reset by:<br>WATCHDOG<br>REG_RST | Charger Enable Configuration<br>Type : RW<br>POR: 1b<br>0h = Charge Disable<br>1h = Charge Enable (default)  |
| 4   | EN_ICO          | R/W  | 0h    | Reset by:<br>REG_RST             | Input Current Optimizer (ICO) Enable<br>Type : RW<br>POR: 0b<br>0h = Disable ICO (default)<br>1h = Enable ICO  |
| 3   | FORCE_ICO       | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | Force start input current optimizer (ICO)<br>Note: This bit can only be set and returns 0 after ICO starts. This bit only valid when EN_ICO = 1<br>Type : RW<br>POR: 0b<br>0h = Do NOT force ICO (Default)<br>1h = Force ICO start                         |
| 2   | EN_HIZ          | R/W  | 0h    | Reset by:<br>REG_RST             | Enable HIZ mode.<br>This bit will be also reset to 0, when the adapter is plugged in at VBUS.<br>Type : RW<br>POR: 0b<br>0h = Disable (default)<br>1h = Enable   |
| 1   | EN_TERM         | R/W  | 1h    | Reset by:<br>WATCHDOG<br>REG_RST | Enable termination<br>Type : RW<br>POR: 1b<br>0h = Disable<br>1h = Enable (default)  |

表 8-19. REG0F\_Charger\_Control\_0 Register Field Descriptions (continued)

| Bit | Field    | Type | Reset | Notes | Description |
|-----|----------|------|-------|-------|-------------|
| 0   | RESERVED | R    | 0h    |       | RESERVED    |



### 8.5.1.13 REG10\_Charger\_Control\_1 Register (Offset = 10h) [reset = 85h]

REG10\_Charger\_Control\_1 is shown in 图 8-35 and described in 表 8-20.

Return to the 表 8-6.

Charger Control 1

**图 8-35. REG10\_Charger\_Control\_1 Register**

| 7        | 6 | 5           | 4 | 3      | 2            | 1 | 0 |
|----------|---|-------------|---|--------|--------------|---|---|
| RESERVED |   | VAC_OVP_1:0 |   | WD_RST | WATCHDOG_2:0 |   |   |
| R-0h     |   | R/W-3h      |   | R/W-0h | R/W-5h       |   |   |

**表 8-20. REG10\_Charger\_Control\_1 Register Field Descriptions**

| Bit | Field        | Type | Reset | Notes                            | Description   |
|-----|--------------|------|-------|----------------------------------|---|
| 7-6 | RESERVED     | R    | 0h    |                                  | RESERVED  |
| 5-4 | VAC_OVP_1:0  | R/W  | 3h    | Reset by:<br>REG_RST             | VAC_OVP thresholds<br>Type : RW<br>POR: 11b<br>0h = 26 V<br>1h = 22 V<br>2h = 12 V<br>3h = 7 V (default)  |
| 3   | WD_RST       | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | I2C watch dog timer reset<br>Type : RW<br>POR: 0b<br>0h = Normal (default)<br>1h = Reset (this bit goes back to 0 after timer resets)                           |
| 2-0 | WATCHDOG_2:0 | R/W  | 5h    | Reset by:<br>REG_RST             | Watchdog timer settings<br>Type : RW<br>POR: 101b<br>0h = Disable<br>1h = 0.5s<br>2h = 1s<br>3h = 2s<br>4h = 20s<br>5h = 40s (default)<br>6h = 80s<br>7h = 160s |

### 8.5.1.14 REG11\_Charger\_Control\_2 Register (Offset = 11h) [reset = 40h]

REG11\_Charger\_Control\_2 is shown in 图 8-36 and described in 表 8-21.

Return to the 表 8-6.

Charger Control 2

图 8-36. REG11\_Charger\_Control\_2 Register

| 7           | 6             | 5      | 4      | 3        | 2             | 1 | 0        |
|-------------|---------------|--------|--------|----------|---------------|---|----------|
| FORCE_INDET | AUTO_INDET_EN | EN_12V | EN_9V  | HVDCP_EN | SDRV_CTRL_1:0 |   | SDRV_DLY |
| R/W-0h      | R/W-1h        | R/W-0h | R/W-0h | R/W-0h   | R/W-0h        |   | R/W-0h   |

表 8-21. REG11\_Charger\_Control\_2 Register Field Descriptions

| Bit | Field         | Type | Reset | Notes                            | Description   |
|-----|---------------|------|-------|----------------------------------|---|
| 7   | FORCE_INDET   | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | Force D+/D- detection<br>Type : RW<br>POR: 0b<br>0h = Do NOT force D+/D- detection (default)<br>1h = Force D+/D- algorithm, when D+/D- detection is done, this bit will be reset to 0                             |
| 6   | AUTO_INDET_EN | R/W  | 1h    | Reset by:<br>WATCHDOG<br>REG_RST | Automatic D+/D- Detection Enable<br>Type : RW<br>POR: 1b<br>0h = Disable D+/D- detection when VBUS is plugged-in<br>1h = Enable D+/D- detection when VBUS is plugged-in (default)                                 |
| 5   | EN_12V        | R/W  | 0h    | Reset by:<br>REG_RST             | EN_12V HVDC<br>Type : RW<br>POR: 0b<br>0h = Disable 12 V mode in HVDCP (default)<br>1h = Enable 12 V mode in HVDCP  |
| 4   | EN_9V         | R/W  | 0h    | Reset by:<br>REG_RST             | EN_9V HVDC<br>Type : RW<br>POR: 0b<br>0h = Disable 9 V mode in HVDCP (default)<br>1h = Enable 9 V mode in HVDCP   |
| 3   | HVDCP_EN      | R/W  | 0h    | Reset by:<br>REG_RST             | High voltage DCP enable.<br>Type : RW<br>POR: 0b<br>0h = Disable HVDCP handshake (default)<br>1h = Enable HVDCP handshake   |
| 2-1 | SDRV_CTRL_1:0 | R/W  | 0h    | Reset by:<br>REG_RST             | SFET control<br>The external ship FET control logic to force the device enter different modes.<br>Type : RW<br>POR: 00b<br>0h = IDLE (default)<br>1h = Shutdown Mode<br>2h = Ship Mode<br>3h = System Power Reset |

表 8-21. REG11\_Charger\_Control\_2 Register Field Descriptions (continued)

| Bit | Field    | Type | Reset | Notes                | Description   |
|-----|----------|------|-------|----------------------|---|
| 0   | SDRV_DLY | R/W  | 0h    | Reset by:<br>REG_RST | Delay time added to the taking action in bit [2:1] of the SFET control<br>Type : RW<br>POR: 0b<br>0h = Add 10s delay time (default)<br>1h = Do NOT add 10s delay time |

### 8.5.1.15 REG12\_Charger\_Control\_3 Register (Offset = 12h) [reset = 0h]

REG12\_Charger\_Control\_3 is shown in 图 8-37 and described in 表 8-22.

Return to the 表 8-6.

Charger Control 3

图 8-37. REG12\_Charger\_Control\_3 Register

| 7         | 6        | 5        | 4           | 3        | 2       | 1        | 0           |
|-----------|----------|----------|-------------|----------|---------|----------|-------------|
| DIS_ACDRV | RESERVED | RESERVED | PFM_FWD_DIS | WKUP_DLY | DIS_LDO | RESERVED | DIS_FWD_OOA |
| R/W-0h    | R-0h     | R/W-0h   | R/W-0h      | R/W-0h   | R/W-0h  | R/W-0h   | R/W-0h      |

表 8-22. REG12\_Charger\_Control\_3 Register Field Descriptions

| Bit | Field       | Type | Reset | Notes                            | Description  |
|-----|-------------|------|-------|----------------------------------|--|
| 7   | DIS_ACDRV   | R/W  | 0h    |                                  | When this bit is set, the charger will force both EN_ACDRV1 = 0 and EN_ACDRV2 = 0<br>Type : RW<br>POR: 0b  |
| 6   | RESERVED    | R    | 0h    |                                  |  |
| 5   | RESERVED    | R    | 0h    |                                  |  |
| 4   | PFM_FWD_DIS | R/W  | 0h    | Reset by:<br>REG_RST             | Disable PFM in forward mode<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable   |
| 3   | WKUP_DLY    | R/W  | 0h    | Reset by:<br>REG_RST             | When wake up the device from ship mode, how much time ( $t_{SM\_EXIT}$ ) is required to pull low the $\overline{QON}$ pin.<br>Type : RW<br>POR: 0b<br>0h = 1s (Default)<br>1h = 15ms |
| 2   | DIS_LDO     | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | Disable BATFET LDO mode in pre-charge stage.<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable  |
| 1   | RESERVED    | R    | 0h    |                                  |  |
| 0   | DIS_FWD_OOA | R/W  | 0h    | Reset by:<br>REG_RST             | Disable OOA in forward mode<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable   |

### 8.5.1.16 REG13\_Charger\_Control\_4 Register (Offset = 13h) [reset = X]

REG13\_Charger\_Control\_4 is shown in 图 8-38 and described in 表 8-23.

Return to the 表 8-6.

Charger Control 4

**图 8-38. REG13\_Charger\_Control\_4 Register**

| 7         | 6         | 5        | 4        | 3              | 2        | 1                | 0           |
|-----------|-----------|----------|----------|----------------|----------|------------------|-------------|
| EN_ACDRV2 | EN_ACDRV1 | PWM_FREQ | DIS_STAT | DIS_VSYS_SHORT | RESERVED | FORCE_VINDPM_DET | EN_IBUS_OCP |
| R/W-0h    | R/W-0h    | R/W-X    | R/W-0h   | R/W-0h         | R/W-0h   | R-0h             | R/W-1h      |

**表 8-23. REG13\_Charger\_Control\_4 Register Field Descriptions**

| Bit | Field            | Type | Reset | Notes                            | Description  |
|-----|------------------|------|-------|----------------------------------|--|
| 7   | EN_ACDRV2        | R/W  | 0h    |                                  | External ACFET2-RBFET2 gate driver control<br>At POR, if the charger detects that there is no ACFET2-RBFET2 populated, this bit will be locked at 0<br>Type : RW<br>POR: 0b<br>0h = turn off (default)<br>1h = turn on   |
| 6   | EN_ACDRV1        | R/W  | 0h    |                                  | External ACFET1-RBFET1 gate driver control<br>At POR, if the charger detects that there is no ACFET1-RBFET1 populated, this bit will be locked at 0<br>Type : RW<br>POR: 0b<br>0h = turn off (default)<br>1h = turn on   |
| 5   | PWM_FREQ         | R/W  | X     |                                  | Switching frequency selection, this bit POR default value is based on the PROG pin strapping.<br>Type : RW<br>0h = 1.5 MHz<br>1h = 750 kHz   |
| 4   | DIS_STAT         | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | Disable the STAT pin output<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable   |
| 3   | DIS_VSYS_SHORT   | R/W  | 0h    | Reset by:<br>REG_RST             | Disable forward mode VSYS short hiccup protection.<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable  |
| 2   | RESERVED         | R    | 0h    |                                  | RESERVED   |
| 1   | FORCE_VINDPM_DET | R/W  | 0h    | Reset by:<br>REG_RST             | Force VINDPM detection<br>Note: only when VBAT>VSYSMIN, this bit can be set to 1. Once the VINDPM auto detection is done, this bits returns to 0.<br>Type : RW<br>POR: 0b<br>0h = Do NOT force VINDPM detection (default)<br>1h = Force the converter stop switching, and ADC measures the VBUS voltage without input current, then the charger updates the VINDPM register accordingly. |

**表 8-23. REG13\_Charger\_Control\_4 Register Field Descriptions (continued)**

| Bit | Field       | Type | Reset | Notes                | Description  |
|-----|-------------|------|-------|----------------------|--|
| 0   | EN_IBUS_OCP | R/W  | 1h    | Reset by:<br>REG_RST | Enable IBUS_OCP in forward mode<br>Type : RW<br>POR: 1b<br>0h = Disable<br>1h = Enable (default) |

### 8.5.1.17 REG14\_Charger\_Control\_5 Register (Offset = 14h) [reset = 16h]

REG14\_Charger\_Control\_5 is shown in 图 8-39 and described in 表 8-24.

Return to the 表 8-6.

Charger Control 5

图 8-39. REG14\_Charger\_Control\_5 Register

| 7            | 6        | 5       | 4        | 3         | 2          | 1        | 0 |
|--------------|----------|---------|----------|-----------|------------|----------|---|
| SFET_PRESENT | RESERVED | EN_IBAT | RESERVED | EN_IINDPM | EN_EXTILIM | EN_BATOC |   |
| R/W-0h       | R-0h     | R/W-0h  | R-2h     | R/W-1h    | R/W-1h     | R/W-0h   |   |

表 8-24. REG14\_Charger\_Control\_5 Register Field Descriptions

| Bit | Field        | Type | Reset | Notes                            | Description  |
|-----|--------------|------|-------|----------------------------------|--|
| 7   | SFET_PRESENT | R/W  | 0h    |                                  | The user has to set this bit based on whether a ship FET is populated or not. The POR default value is 0, which means the charger does not support all the features associated with the ship FET. The register bits list below all are locked at 0.<br>EN_BATOC = 0<br>FORCE_SFET_OFF = 0<br>SDRV_CTRL = 00<br>When this bit is set to 1, the register bits list above become programmable, and the charger can support the features associated with the ship FET<br>Type : RW<br>POR: 0b<br>0h = No ship FET populated<br>1h = Ship FET populated |
| 6   | RESERVED     | R    | 0h    |                                  | RESERVED   |
| 5   | EN_IBAT      | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | IBAT pin output enable<br>Type : RW<br>POR: 0b<br>0h = IBAT pin output is disabled (default)<br>1h = IBAT pin output is enable   |
| 4-3 | RESERVED     | R    | 2h    |                                  | RESERVED   |
| 2   | EN_IINDPM    | R/W  | 1h    | Reset by:<br>WATCHDOG<br>REG_RST | Enable the internal IINDPM register input current regulation<br>Type : RW<br>POR: 1b<br>0h = Disable<br>1h = Enable (default)  |
| 1   | EN_EXTILIM   | R/W  | 1h    | Reset by:<br>REG_RST             | Enable the external ILIM_HIZ pin input current regulation<br>Type : RW<br>POR: 1b<br>0h = Disable<br>1h = Enable (default)   |
| 0   | EN_BATOC     | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | Enable the battery discharging current OCP<br>Type : RW<br>POR: 0b<br>0h = Disable (default)<br>1h = Enable  |



### 8.5.1.18 REG15\_Reserved Register (Offset = 15h) [reset = 00h]

REG15\_Reserved is shown in 图 8-40 and described in 表 8-25.

Return to the 表 8-6.

Reserved Register

图 8-40. REG15\_Reserved Register

|          |   |   |   |   |   |   |   |
|----------|---|---|---|---|---|---|---|
| 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved |   |   |   |   |   |   |   |
| R-0h     |   |   |   |   |   |   |   |

表 8-25. REG15\_Reserved Register Field Descriptions

| Bit | Field    | Type | Reset | Notes | Description |
|-----|----------|------|-------|-------|-------------|
| 7-0 | Reserved | R    | 0h    |       | Reserved    |

### 8.5.1.19 REG16\_Temperature\_Control Register (Offset = 16h) [reset = C0h]

REG16\_Temperature\_Control is shown in 图 8-41 and described in 表 8-26.

Return to the 表 8-6.

Temperature Control

**图 8-41. REG16\_Temperature\_Control Register**

| 7        | 6 | 5         | 4 | 3          | 2          | 1          | 0        |
|----------|---|-----------|---|------------|------------|------------|----------|
| TREG_1:0 |   | TSHUT_1:0 |   | VBUS_PD_EN | VAC1_PD_EN | VAC2_PD_EN | RESERVED |
| R/W-3h   |   | R/W-0h    |   | R/W-0h     | R/W-0h     | R/W-0h     | R-0h     |

**表 8-26. REG16\_Temperature\_Control Register Field Descriptions**

| Bit | Field      | Type | Reset | Notes                            | Description   |
|-----|------------|------|-------|----------------------------------|---|
| 7-6 | TREG_1:0   | R/W  | 3h    | Reset by:<br>WATCHDOG<br>REG_RST | Thermal regulation thresholds.<br>Type : RW<br>POR: 11b<br>0h = 60°C<br>1h = 80°C<br>2h = 100°C<br>3h = 120°C (default) |
| 5-4 | TSHUT_1:0  | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | Thermal shutdown thresholds.<br>Type : RW<br>POR: 00b<br>0h = 150°C (default)<br>1h = 130°C<br>2h = 120°C<br>3h = 85°C  |
| 3   | VBUS_PD_EN | R/W  | 0h    | Reset by:<br>REG_RST             | Enable VBUS pull down resistor (6k Ohm)<br>Type : RW<br>POR: 0b<br>0h = Disable (default)<br>1h = Enable                |
| 2   | VAC1_PD_EN | R/W  | 0h    | Reset by:<br>REG_RST             | Enable VAC1 pull down resistor<br>Type : RW<br>POR: 0b<br>0h = Disable (default)<br>1h = Enable                         |
| 1   | VAC2_PD_EN | R/W  | 0h    | Reset by:<br>REG_RST             | Enable VAC2 pull down resistor<br>Type : RW<br>POR: 0b<br>0h = Disable (default)<br>1h = Enable                         |
| 0   | RESERVED   | R    | 0h    |                                  | RESERVED  |

### 8.5.1.20 REG17\_NTC\_Control\_0 Register (Offset = 17h) [reset = 7Ah]

REG17\_NTC\_Control\_0 is shown in 图 8-42 and described in 表 8-27.

Return to the 表 8-6.

NTC Control 0

图 8-42. REG17\_NTC\_Control\_0 Register

| 7              | 6 | 5 | 4               | 3 | 2               | 1 | 0        |
|----------------|---|---|-----------------|---|-----------------|---|----------|
| JEITA_VSET_2:0 |   |   | JEITA_ISETH_1:0 |   | JEITA_ISETC_1:0 |   | RESERVED |
| R/W-3h         |   |   | R/W-3h          |   | R/W-1h          |   | R-0h     |

表 8-27. REG17\_NTC\_Control\_0 Register Field Descriptions

| Bit | Field           | Type | Reset | Notes                            | Description   |
|-----|-----------------|------|-------|----------------------------------|---|
| 7-5 | JEITA_VSET_2:0  | R/W  | 3h    | Reset by:<br>WATCHDOG<br>REG_RST | JEITA high temperature range (TWARN - THOT)<br>charge voltage setting<br>Type : RW<br>POR: 011b<br>0h = Charge Suspend<br>1h = Set VREG to VREG - 800 mV<br>2h = Set VREG to VREG - 600 mV<br>3h = Set VREG to VREG - 400 mV (default)<br>4h = Set VREG to VREG - 300 mV<br>5h = Set VREG to VREG - 200 mV<br>6h = Set VREG to VREG - 100 mV<br>7h = VREG unchanged |
| 4-3 | JEITA_ISETH_1:0 | R/W  | 3h    | Reset by:<br>WATCHDOG<br>REG_RST | JEITA high temperature range (TWARN - THOT)<br>charge current setting<br>Type : RW<br>POR: 11b<br>0h = Charge Suspend<br>1h = Set ICHG to 20%* ICHG<br>2h = Set ICHG to 40%* ICHG<br>3h = ICHG unchanged (default)  |
| 2-1 | JEITA_ISETC_1:0 | R/W  | 1h    | Reset by:<br>WATCHDOG<br>REG_RST | JEITA low temperature range (TCOLD - TCOOL)<br>charge current setting<br>Type : RW<br>POR: 01b<br>0h = Charge Suspend<br>1h = Set ICHG to 20%* ICHG (default)<br>2h = Set ICHG to 40%* ICHG<br>3h = ICHG unchanged  |
| 0   | RESERVED        | R    | 0h    |                                  | Reserved<br>Type : R<br>POR: 0b   |

### 8.5.1.21 REG18\_NTC\_Control\_1 Register (Offset = 18h) [reset = 54h]

REG18\_NTC\_Control\_1 is shown in 图 8-43 and described in 表 8-28.

Return to the 表 8-6.

NTC Control 1

图 8-43. REG18\_NTC\_Control\_1 Register

| 7           | 6 | 5           | 4 | 3        | 2 | 1        | 0         |
|-------------|---|-------------|---|----------|---|----------|-----------|
| TS_COOL_1:0 |   | TS_WARM_1:0 |   | RESERVED |   | RESERVED | TS_IGNORE |
| R/W-1h      |   | R/W-1h      |   | R-1h     |   | R-0h     | R/W-0h    |

表 8-28. REG18\_NTC\_Control\_1 Register Field Descriptions

| Bit | Field       | Type | Reset | Notes                            | Description   |
|-----|-------------|------|-------|----------------------------------|---|
| 7-6 | TS_COOL_1:0 | R/W  | 1h    | Reset by:<br>WATCHDOG<br>REG_RST | JEITA VT2 comparator voltage rising thresholds as a percentage of REGN. The corresponding temperature in the brackets is achieved when a 103AT NTC thermistor is used, RT1 = 5.24 k $\Omega$ and RT2 = 30.31 k $\Omega$ .<br>Type : RW<br>POR: 01b<br>0h = 71.1% (5°C)<br>1h = 68.4% (default) (10°C)<br>2h = 65.5% (15°C)<br>3h = 62.4% (20°C) |
| 5-4 | TS_WARM_1:0 | R/W  | 1h    | Reset by:<br>WATCHDOG<br>REG_RST | JEITA VT3 comparator voltage falling thresholds as a percentage of REGN. The corresponding temperature in the brackets is achieved when a 103AT NTC thermistor is used, RT1 = 5.24k $\Omega$ and RT2 = 30.31k $\Omega$ .<br>Type : RW<br>POR: 01b<br>0h = 48.4% (40°C)<br>1h = 44.8% (default) (45°C)<br>2h = 41.2% (50°C)<br>3h = 37.7% (55°C) |
| 3-2 | RESERVED    | R    | 1h    |                                  | RESERVED  |
| 1   | RESERVED    | R    | 0h    |                                  | RESERVED  |
| 0   | TS_IGNORE   | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | Ignore the TS feedback, the charger considers the TS is always good to allow charging. bITS [5:2] always stay at 0000 to report the normal condition.<br>Type : RW<br>POR: 0b<br>0h = NOT ignore (Default)<br>1h = Ignore   |

### 8.5.1.22 REG19\_ICO\_Current\_Limit Register (Offset = 19h) [reset = 0h]

REG19\_ICO\_Current\_Limit is shown in 图 8-44 and described in 表 8-29.

Return to the 表 8-6.

ICO Current Limit

图 8-44. REG19\_ICO\_Current\_Limit Register

|              |    |    |    |    |    |   |              |
|--------------|----|----|----|----|----|---|--------------|
| 15           | 14 | 13 | 12 | 11 | 10 | 9 | 8            |
| RESERVED     |    |    |    |    |    |   | ICO_ILIM_8:0 |
| R-0h         |    |    |    |    |    |   | R-0h         |
| 7            | 6  | 5  | 4  | 3  | 2  | 1 | 0            |
| ICO_ILIM_8:0 |    |    |    |    |    |   |              |
| R-0h         |    |    |    |    |    |   |              |

表 8-29. REG19\_ICO\_Current\_Limit Register Field Descriptions

| Bit  | Field        | Type | Reset | Description  |
|------|--------------|------|-------|--|
| 15-9 | RESERVED     | R    | 0h    | RESERVED   |
| 8-0  | ICO_ILIM_8:0 | R    | 0h    | Input Current Limit obtained from ICO or ILIM_HIZ pin setting<br>Type : R<br>POR: 0 mA (0h)<br>Range : 100 mA-3300 mA<br>Fixed Offset : 0 mA<br>Bit Step Size : 10 mA<br>Clamped Low |

### 8.5.1.23 REG1B\_Charger\_Status\_0 Register (Offset = 1Bh) [reset = 0h]

REG1B\_Charger\_Status\_0 is shown in [图 8-45](#) and described in [表 8-30](#).

Return to the [表 8-6](#).

Charger Status 0

**图 8-45. REG1B\_Charger\_Status\_0 Register**

| 7           | 6           | 5       | 4            | 3       | 2                | 1                | 0                 |
|-------------|-------------|---------|--------------|---------|------------------|------------------|-------------------|
| IINDPM_STAT | VINDPM_STAT | WD_STAT | POORSRC_STAT | PG_STAT | AC2_PRESENT_STAT | AC1_PRESENT_STAT | VBUS_PRESENT_STAT |
| R-0h        | R-0h        | R-0h    | R-0h         | R-0h    | R-0h             | R-0h             | R-0h              |

**表 8-30. REG1B\_Charger\_Status\_0 Register Field Descriptions**

| Bit | Field            | Type | Reset | Description   |
|-----|------------------|------|-------|---|
| 7   | IINDPM_STAT      | R    | 0h    | IINDPM status (forward mode)<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = In IINDPM regulation                   |
| 6   | VINDPM_STAT      | R    | 0h    | VINDPM status (forward mode)<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = In VINDPM regulation                   |
| 5   | WD_STAT          | R    | 0h    | I2C watch dog timer status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = WD timer expired                         |
| 4   | POORSRC_STAT     | R    | 0h    | Poor source detection status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Weak adaptor detected                  |
| 3   | PG_STAT          | R    | 0h    | Power Good Status<br>Type : R<br>POR: 0b<br><br>0h = NOT in power good status<br>1h = Power good                      |
| 2   | AC2_PRESENT_STAT | R    | 0h    | VAC2 insert status<br>Type : R<br>POR: 0b<br><br>0h = VAC2 NOT present<br>1h = VAC2 present (above present threshold) |

**表 8-30. REG1B\_Charger\_Status\_0 Register Field Descriptions (continued)**

| Bit | Field             | Type | Reset | Description  |
|-----|-------------------|------|-------|--|
| 1   | AC1_PRESENT_STAT  | R    | 0h    | VAC1 insert status<br>Type : R<br>POR: 0b<br><br>0h = VAC1 NOT present<br>1h = VAC1 present (above present threshold)  |
| 0   | VBUS_PRESENT_STAT | R    | 0h    | VBUS present status<br>Type : R<br>POR: 0b<br><br>0h = VBUS NOT present<br>1h = VBUS present (above present threshold) |

### 8.5.1.24 REG1C\_Charger\_Status\_1 Register (Offset = 1Ch) [reset = 0h]

REG1C\_Charger\_Status\_1 is shown in 图 8-46 and described in 表 8-31.

Return to the 表 8-6.

Charger Status 1

**图 8-46. REG1C\_Charger\_Status\_1 Register**

| 7            | 6 | 5 | 4             | 3 | 2 | 1 | 0               |
|--------------|---|---|---------------|---|---|---|-----------------|
| CHG_STAT_2:0 |   |   | VBUS_STAT_3:0 |   |   |   | BC1.2_DONE_STAT |
| R-0h         |   |   | R-0h          |   |   |   | R-0h            |

**表 8-31. REG1C\_Charger\_Status\_1 Register Field Descriptions**

| Bit | Field         | Type | Reset | Description  |
|-----|---------------|------|-------|--|
| 7-5 | CHG_STAT_2:0  | R    | 0h    | Charge Status bits<br>Type : R<br>POR: 000b<br><br>0h = Not Charging<br>1h = Trickle Charge<br>2h = Pre-charge<br>3h = Fast charge (CC mode)<br>4h = Taper Charge (CV mode)<br>5h = Reserved<br>6h = Top-off Timer Active Charging<br>7h = Charge Termination Done   |
| 4-1 | VBUS_STAT_3:0 | R    | 0h    | VBUS status bits<br>0h: No Input<br>1h: USB SDP (500 mA)<br>2h: USB CDP (1.5 A)<br>3h: USB DCP (3.25 A)<br>4h: Adjustable High Voltage DCP (HVDCP) (1.5 A)<br>5h: Unknown adaptor (3 A)<br>6h: Non-Standard Adapter (1 A/2 A/2.1 A/2.4 A)<br>7h: Reserved<br>8h: Not qualified adaptor<br>9h: Reserved<br>Ah: Reserved<br>Bh: Device directly powered from VBUS<br>Ch: Reserved<br>Dh: Reserved<br>Eh: Reserved<br>Fh: Reserved<br>Type : R<br>POR: 0h |



**表 8-31. REG1C\_Charger\_Status\_1 Register Field Descriptions (continued)**

| Bit | Field           | Type | Reset | Description   |
|-----|-----------------|------|-------|---|
| 0   | BC1.2_DONE_STAT | R    | 0h    | BC1.2 status bit<br>Type : R<br>POR: 0b<br><br>0h = BC1.2 or non-standard detection NOT complete<br>1h = BC1.2 or non-standard detection complete |

### 8.5.1.25 REG1D\_Charger\_Status\_2 Register (Offset = 1Dh) [reset = 0h]

REG1D\_Charger\_Status\_2 is shown in 图 8-47 and described in 表 8-32.

Return to the 表 8-6.

Charger Status 2

图 8-47. REG1D\_Charger\_Status\_2 Register

| 7            | 6 | 5        | 4 | 3 | 2         | 1         | 0                     |
|--------------|---|----------|---|---|-----------|-----------|-----------------------|
| ICO_STAT_1:0 |   | RESERVED |   |   | TREG_STAT | DPDM_STAT | VBAT_PRESEN<br>T_STAT |
| R-0h         |   | R-0h     |   |   | R-0h      | R-0h      | R-0h                  |

表 8-32. REG1D\_Charger\_Status\_2 Register Field Descriptions

| Bit | Field             | Type | Reset | Description  |
|-----|-------------------|------|-------|--|
| 7-6 | ICO_STAT_1:0      | R    | 0h    | Input Current Optimizer (ICO) status<br>Type : R<br>POR: 00b<br><br>0h = ICO disabled<br>1h = ICO optimization in progress<br>2h = Maximum input current detected<br>3h = Reserved |
| 5-3 | RESERVED          | R    | 0h    | RESERVED   |
| 2   | TREG_STAT         | R    | 0h    | IC thermal regulation status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Device in thermal regulation  |
| 1   | DPDM_STAT         | R    | 0h    | D+/D- detection status bits<br>Type : R<br>POR: 0b<br><br>0h = The D+/D- detection is NOT started yet, or the detection is done<br>1h = The D+/D- detection is ongoing             |
| 0   | VBAT_PRESENT_STAT | R    | 0h    | Battery present status ( $V_{BAT} > V_{BAT\_UVLOZ}$ )<br>Type : R<br>POR: 0b<br><br>0h = $V_{BAT}$ NOT present<br>1h = $V_{BAT}$ present   |

### 8.5.1.26 REG1E\_Charger\_Status\_3 Register (Offset = 1Eh) [reset = 0h]

REG1E\_Charger\_Status\_3 is shown in 图 8-48 and described in 表 8-33.

Return to the 表 8-6.

#### Charger Status 3

图 8-48. REG1E\_Charger\_Status\_3 Register

| 7          | 6          | 5             | 4         | 3            | 2               | 1               | 0        |
|------------|------------|---------------|-----------|--------------|-----------------|-----------------|----------|
| ACRB2_STAT | ACRB1_STAT | ADC_DONE_STAT | VSYS_STAT | CHG_TMR_STAT | TRICHG_TMR_STAT | PRECHG_TMR_STAT | RESERVED |
| R-0h       | R-0h       | R-0h          | R-0h      | R-0h         | R-0h            | R-0h            | R-0h     |

表 8-33. REG1E\_Charger\_Status\_3 Register Field Descriptions

| Bit | Field           | Type | Reset | Description  |
|-----|-----------------|------|-------|--|
| 7   | ACRB2_STAT      | R    | 0h    | The ACFET2-RBFET2 status<br>Type : R<br>POR: 0b<br><br>0h = ACFET2-RBFET2 is NOT placed<br>1h = ACFET2-RBFET2 is placed  |
| 6   | ACRB1_STAT      | R    | 0h    | The ACFET1-RBFET1 status<br>Type : R<br>POR: 0b<br><br>0h = ACFET1-RBFET1 is NOT placed<br>1h = ACFET1-RBFET1 is placed  |
| 5   | ADC_DONE_STAT   | R    | 0h    | ADC Conversion Status (in one-shot mode only)<br>Type : R<br>POR: 0b<br><br>0h = Conversion NOT complete<br>1h = Conversion complete   |
| 4   | VSYS_STAT       | R    | 0h    | VSYS Regulation Status (forward mode)<br>Type : R<br>POR: 0b<br><br>0h = Not in VSYSMIN regulation ( $V_{BAT} > V_{SYSMIN}$ )<br>1h = In VSYSMIN regulation ( $V_{BAT} < V_{SYSMIN}$ ) |
| 3   | CHG_TMR_STAT    | R    | 0h    | Fast charge timer status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Safety timer expired  |
| 2   | TRICHG_TMR_STAT | R    | 0h    | Trickle charge timer status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Safety timer expired   |

表 8-33. REG1E\_Charger\_Status\_3 Register Field Descriptions (continued)

| Bit | Field           | Type | Reset | Description  |
|-----|-----------------|------|-------|--|
| 1   | PRECHG_TMR_STAT | R    | 0h    | Pre-charge timer status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Safety timer expired |
| 0   | RESERVED        | R    | 0h    | RESERVED   |

### 8.5.1.27 REG1F\_Charger\_Status\_4 Register (Offset = 1Fh) [reset = 0h]

REG1F\_Charger\_Status\_4 is shown in 图 8-49 and described in 表 8-34.

Return to the 表 8-6.

Charger Status 4

图 8-49. REG1F\_Charger\_Status\_4 Register

| 7        | 6 | 5 | 4 | 3            | 2            | 1            | 0           |
|----------|---|---|---|--------------|--------------|--------------|-------------|
| RESERVED |   |   |   | TS_COLD_STAT | TS_COOL_STAT | TS_WARM_STAT | TS_HOT_STAT |
| R-0h     |   |   |   | R-0h         | R-0h         | R-0h         | R-0h        |

表 8-34. REG1F\_Charger\_Status\_4 Register Field Descriptions

| Bit | Field        | Type | Reset | Description  |
|-----|--------------|------|-------|--|
| 7-4 | RESERVED     | R    | 0h    | RESERVED   |
| 3   | TS_COLD_STAT | R    | 0h    | The TS temperature is in the cold range, lower than T1.<br>Type : R<br>POR: 0b<br><br>0h = TS status is NOT in cold range<br>1h = TS status is in cold range     |
| 2   | TS_COOL_STAT | R    | 0h    | The TS temperature is in the cool range, between T1 and T2.<br>Type : R<br>POR: 0b<br><br>0h = TS status is NOT in cool range<br>1h = TS status is in cool range |
| 1   | TS_WARM_STAT | R    | 0h    | The TS temperature is in the warm range, between T3 and T5.<br>Type : R<br>POR: 0b<br><br>0h = TS status is NOT in warm range<br>1h = TS status is in warm range |
| 0   | TS_HOT_STAT  | R    | 0h    | The TS temperature is in the hot range, higher than T5.<br>Type : R<br>POR: 0b<br><br>0h = TS status is NOT in hot range<br>1h = TS status is in hot range       |

### 8.5.1.28 REG20\_FAULT\_Status\_0 Register (Offset = 20h) [reset = 0h]

REG20\_FAULT\_Status\_0 is shown in 图 8-50 and described in 表 8-35.

Return to the 表 8-6.

FAULT Status 0

图 8-50. REG20\_FAULT\_Status\_0 Register

| 7             | 6             | 5             | 4             | 3             | 2             | 1             | 0             |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| IBAT_REG_STAT | VBUS_OVP_STAT | VBAT_OVP_STAT | IBUS_OCP_STAT | IBAT_OCP_STAT | CONV_OCP_STAT | VAC2_OVP_STAT | VAC1_OVP_STAT |
| R-0h          | R-0h          | R-0h          | R-0h          | R-0h          | R-0h          | R-0h          | R-0h          |

表 8-35. REG20\_FAULT\_Status\_0 Register Field Descriptions

| Bit | Field         | Type | Reset | Description   |
|-----|---------------|------|-------|---|
| 7   | IBAT_REG_STAT | R    | 0h    | IBAT regulation status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Device in battery discharging current regulation |
| 6   | VBUS_OVP_STAT | R    | 0h    | VBUS over-voltage status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Device in overvoltage protection               |
| 5   | VBAT_OVP_STAT | R    | 0h    | VBAT overvoltage status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Device in overvoltage protection                |
| 4   | IBUS_OCP_STAT | R    | 0h    | IBUS overcurrent status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Device in overcurrent protection                |
| 3   | IBAT_OCP_STAT | R    | 0h    | IBAT overcurrent status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Device in overcurrent protection                |
| 2   | CONV_OCP_STAT | R    | 0h    | Converter overcurrent status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Converter in overcurrent protection        |

表 8-35. REG20\_FAULT\_Status\_0 Register Field Descriptions (continued)

| Bit | Field         | Type | Reset | Description  |
|-----|---------------|------|-------|--|
| 1   | VAC2_OVP_STAT | R    | 0h    | VAC2 overvoltage status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Device in overvoltage protection |
| 0   | VAC1_OVP_STAT | R    | 0h    | VAC1 overvoltage status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Device in overvoltage protection |

### 8.5.1.29 REG21\_FAULT\_Status\_1 Register (Offset = 21h) [reset = 0h]

REG21\_FAULT\_Status\_1 is shown in [图 8-51](#) and described in [表 8-36](#).

Return to the [表 8-6](#).

FAULT Status 1

**图 8-51. REG21\_FAULT\_Status\_1 Register**

| 7               | 6             | 5        | 4 | 3 | 2          | 1        | 0 |
|-----------------|---------------|----------|---|---|------------|----------|---|
| VSYS_SHORT_STAT | VSYS_OVP_STAT | RESERVED |   |   | TSHUT_STAT | RESERVED |   |
| R-0h            | R-0h          | R-0h     |   |   | R-0h       | R-0h     |   |

**表 8-36. REG21\_FAULT\_Status\_1 Register Field Descriptions**

| Bit | Field           | Type | Reset | Description  |
|-----|-----------------|------|-------|--|
| 7   | VSYS_SHORT_STAT | R    | 0h    | VSYS short circuit status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Device in SYS short circuit protection     |
| 6   | VSYS_OVP_STAT   | R    | 0h    | VSYS overvoltage status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Device in SYS overvoltage protection         |
| 5-3 | RESERVED        | R    | 0h    | RESERVED   |
| 2   | TSHUT_STAT      | R    | 0h    | IC temperature shutdown status<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Device in thermal shutdown protection |
| 1-0 | RESERVED        | R    | 0h    | RESERVED   |



### 8.5.1.30 REG22\_Charger\_Flag\_0 Register (Offset = 22h) [reset = 0h]

REG22\_Charger\_Flag\_0 is shown in 图 8-52 and described in 表 8-37.

Return to the 表 8-6.

Charger Flag 0

图 8-52. REG22\_Charger\_Flag\_0 Register

| 7           | 6           | 5       | 4                | 3       | 2                    | 1                    | 0                     |
|-------------|-------------|---------|------------------|---------|----------------------|----------------------|-----------------------|
| IINDPM_FLAG | VINDPM_FLAG | WD_FLAG | POORSRC_FL<br>AG | PG_FLAG | AC2_PRESENT<br>_FLAG | AC1_PRESENT<br>_FLAG | VBUS_PRESE<br>NT_FLAG |
| R-0h        | R-0h        | R-0h    | R-0h             | R-0h    | R-0h                 | R-0h                 | R-0h                  |

表 8-37. REG22\_Charger\_Flag\_0 Register Field Descriptions

| Bit | Field            | Type | Reset | Description  |
|-----|------------------|------|-------|--|
| 7   | IINDPM_FLAG      | R    | 0h    | IINDPM flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = IINDPM signal rising edge detected   |
| 6   | VINDPM_FLAG      | R    | 0h    | VINDPM flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = VINDPM signal rising edge detected   |
| 5   | WD_FLAG          | R    | 0h    | I2C watchdog timer flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = WD timer signal rising edge detected                                       |
| 4   | POORSRC_FLAG     | R    | 0h    | Poor source detection flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Poor source status rising edge detected                                 |
| 3   | PG_FLAG          | R    | 0h    | Power good flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Any change in PG_STAT even (adapter good qualification or adapter good going away) |
| 2   | AC2_PRESENT_FLAG | R    | 0h    | VAC2 present flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = VAC2 present status changed  |

**表 8-37. REG22\_Charger\_Flag\_0 Register Field Descriptions (continued)**

| Bit | Field             | Type | Reset | Description   |
|-----|-------------------|------|-------|---|
| 1   | AC1_PRESENT_FLAG  | R    | 0h    | VAC1 present flag<br>Type : R<br>POR: 0b<br>0h = Normal<br>1h = VAC1 present status changed |
| 0   | VBUS_PRESENT_FLAG | R    | 0h    | VBUS present flag<br>Type : R<br>POR: 0b<br>0h = Normal<br>1h = VBUS present status changed |

### 8.5.1.31 REG23\_Charger\_Flag\_1 Register (Offset = 23h) [reset = 0h]

REG23\_Charger\_Flag\_1 is shown in 图 8-53 and described in 表 8-38.

Return to the 表 8-6.

Charger Flag 1

图 8-53. REG23\_Charger\_Flag\_1 Register

| 7        | 6        | 5        | 4         | 3        | 2         | 1                     | 0                   |
|----------|----------|----------|-----------|----------|-----------|-----------------------|---------------------|
| CHG_FLAG | ICO_FLAG | RESERVED | VBUS_FLAG | RESERVED | TREG_FLAG | VBAT_PRESEN<br>T_FLAG | BC1.2_DONE_<br>FLAG |
| R-0h     | R-0h     | R-0h     | R-0h      | R-0h     | R-0h      | R-0h                  | R-0h                |

表 8-38. REG23\_Charger\_Flag\_1 Register Field Descriptions

| Bit | Field             | Type | Reset | Description  |
|-----|-------------------|------|-------|--|
| 7   | CHG_FLAG          | R    | 0h    | Charge status flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Charge status changed                         |
| 6   | ICO_FLAG          | R    | 0h    | ICO status flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = ICO status changed                               |
| 5   | RESERVED          | R    | 0h    | RESERVED   |
| 4   | VBUS_FLAG         | R    | 0h    | VBUS status flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = VBUS status changed                             |
| 3   | RESERVED          | R    | 0h    | RESERVED   |
| 2   | TREG_FLAG         | R    | 0h    | IC thermal regulation flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = TREG signal rising threshold detected |
| 1   | VBAT_PRESENT_FLAG | R    | 0h    | VBAT present flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = VBAT present status changed                    |

表 8-38. REG23\_Charger\_Flag\_1 Register Field Descriptions (continued)

| Bit | Field           | Type | Reset | Description  |
|-----|-----------------|------|-------|--|
| 0   | BC1.2_DONE_FLAG | R    | 0h    | BC1.2 status Flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = BC1.2 detection status changed |

### 8.5.1.32 REG24\_Charger\_Flag\_2 Register (Offset = 24h) [reset = 0h]

REG24\_Charger\_Flag\_2 is shown in 图 8-54 and described in 表 8-39.

Return to the 表 8-6.

Charger Flag 2

图 8-54. REG24\_Charger\_Flag\_2 Register

| 7        | 6              | 5             | 4         | 3            | 2               | 1               | 0               |
|----------|----------------|---------------|-----------|--------------|-----------------|-----------------|-----------------|
| RESERVED | DPDM_DONE_FLAG | ADC_DONE_FLAG | VSYS_FLAG | CHG_TMR_FLAG | TRICHG_TMR_FLAG | PRECHG_TMR_FLAG | TOPOFF_TMR_FLAG |
| R-0h     | R-0h           | R-0h          | R-0h      | R-0h         | R-0h            | R-0h            | R-0h            |

表 8-39. REG24\_Charger\_Flag\_2 Register Field Descriptions

| Bit | Field           | Type | Reset | Description   |
|-----|-----------------|------|-------|---|
| 7   | RESERVED        | R    | 0h    | RESERVED  |
| 6   | DPDM_DONE_FLAG  | R    | 0h    | D+/D- detection is done flag.<br>Type : R<br>POR: 0b<br><br>0h = D+/D- detection is NOT started or still ongoing<br>1h = D+/D- detection is completed |
| 5   | ADC_DONE_FLAG   | R    | 0h    | ADC conversion flag (only in one-shot mode)<br>Type : R<br>POR: 0b<br><br>0h = Conversion NOT completed<br>1h = Conversion completed                  |
| 4   | VSYS_FLAG       | R    | 0h    | VSYSMIN regulation flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Entered or existed VSYSMIN regulation                                       |
| 3   | CHG_TMR_FLAG    | R    | 0h    | Fast charge timer flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Fast charge timer expired rising edge detected                               |
| 2   | TRICHG_TMR_FLAG | R    | 0h    | Trickle charge timer flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Trickle charger timer expired rising edge detected                        |
| 1   | PRECHG_TMR_FLAG | R    | 0h    | Pre-charge timer flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Pre-charge timer expired rising edge detected                                 |

表 8-39. REG24\_Charger\_Flag\_2 Register Field Descriptions (continued)

| Bit | Field           | Type | Reset | Description   |
|-----|-----------------|------|-------|---|
| 0   | TOPOFF_TMR_FLAG | R    | 0h    | Top off timer flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Top off timer expired rising edge detected |

### 8.5.1.33 REG25\_Charger\_Flag\_3 Register (Offset = 25h) [reset = 0h]

REG25\_Charger\_Flag\_3 is shown in 图 8-55 and described in 表 8-40.

Return to the 表 8-6.

Charger Flag 3

图 8-55. REG25\_Charger\_Flag\_3 Register

| 7        | 6 | 5 | 4 | 3            | 2            | 1            | 0           |
|----------|---|---|---|--------------|--------------|--------------|-------------|
| RESERVED |   |   |   | TS_COLD_FLAG | TS_COOL_FLAG | TS_WARM_FLAG | TS_HOT_FLAG |
| R-0h     |   |   |   | R-0h         | R-0h         | R-0h         | R-0h        |

表 8-40. REG25\_Charger\_Flag\_3 Register Field Descriptions

| Bit | Field        | Type | Reset | Description  |
|-----|--------------|------|-------|--|
| 7-4 | RESERVED     | R    | 0h    | RESERVED   |
| 3   | TS_COLD_FLAG | R    | 0h    | TS cold temperature flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = TS across cold temperature (T1) is detected |
| 2   | TS_COOL_FLAG | R    | 0h    | TS cool temperature flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = TS across cool temperature (T2) is detected |
| 1   | TS_WARM_FLAG | R    | 0h    | TS warm temperature flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = TS across warm temperature (T3) is detected |
| 0   | TS_HOT_FLAG  | R    | 0h    | TS hot temperature flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = TS across hot temperature (T5) is detected   |

### 8.5.1.34 REG26\_FAULT\_Flag\_0 Register (Offset = 26h) [reset = 0h]

REG26\_FAULT\_Flag\_0 is shown in 图 8-56 and described in 表 8-41.

Return to the 表 8-6.

FAULT Flag 0

**图 8-56. REG26\_FAULT\_Flag\_0 Register**

| 7                 | 6                 | 5                 | 4                 | 3                 | 2                 | 1                 | 0                 |
|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| IBAT_REG_FL<br>AG | VBUS_OVP_FL<br>AG | VBAT_OVP_FL<br>AG | IBUS_OCP_FL<br>AG | IBAT_OCP_FL<br>AG | CONV_OCP_F<br>LAG | VAC2_OVP_FL<br>AG | VAC1_OVP_FL<br>AG |
| R-0h              | R-0h              | R-0h              | R-0h              | R-0h              | R-0h              | R-0h              | R-0h              |

**表 8-41. REG26\_FAULT\_Flag\_0 Register Field Descriptions**

| Bit | Field         | Type | Reset | Description  |
|-----|---------------|------|-------|--|
| 7   | IBAT_REG_FLAG | R    | 0h    | IBAT regulation flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Enter or exit IBAT regulation |
| 6   | VBUS_OVP_FLAG | R    | 0h    | VBUS overvoltage flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Enter VBUS OVP               |
| 5   | VBAT_OVP_FLAG | R    | 0h    | VBAT overvoltage flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Enter VBAT OVP               |
| 4   | IBUS_OCP_FLAG | R    | 0h    | IBUS overcurrent flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Enter IBUS OCP               |
| 3   | IBAT_OCP_FLAG | R    | 0h    | IBAT overcurrent flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Enter discharged OCP         |
| 2   | CONV_OCP_FLAG | R    | 0h    | Converter overcurrent flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Enter converter OCP     |



表 8-41. REG26\_FAULT\_Flag\_0 Register Field Descriptions (continued)

| Bit | Field         | Type | Reset | Description  |
|-----|---------------|------|-------|--|
| 1   | VAC2_OVP_FLAG | R    | 0h    | VAC2 overvoltage flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Enter VAC2 OVP |
| 0   | VAC1_OVP_FLAG | R    | 0h    | VAC1 overvoltage flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Enter VAC1 OVP |

### 8.5.1.35 REG27\_FAULT\_Flag\_1 Register (Offset = 27h) [reset = 0h]

REG27\_FAULT\_Flag\_1 is shown in 图 8-57 and described in 表 8-42.

Return to the 表 8-6.

FAULT Flag 1

图 8-57. REG27\_FAULT\_Flag\_1 Register

| 7               | 6             | 5        | 4 | 3 | 2          | 1        | 0 |
|-----------------|---------------|----------|---|---|------------|----------|---|
| VSYS_SHORT_FLAG | VSYS_OVP_FLAG | RESERVED |   |   | TSHUT_FLAG | RESERVED |   |
| R-0h            | R-0h          | R-0h     |   |   | R-0h       | R-0h     |   |

表 8-42. REG27\_FAULT\_Flag\_1 Register Field Descriptions

| Bit | Field           | Type | Reset | Description   |
|-----|-----------------|------|-------|---|
| 7   | VSYS_SHORT_FLAG | R    | 0h    | VSYS short circuit flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Stop switching due to system short            |
| 6   | VSYS_OVP_FLAG   | R    | 0h    | VSYS over-voltage flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = Stop switching due to system overvoltage       |
| 5-3 | RESERVED        | R    | 0h    | RESERVED  |
| 2   | TSHUT_FLAG      | R    | 0h    | IC thermal shutdown flag<br>Type : R<br>POR: 0b<br><br>0h = Normal<br>1h = TS shutdown signal rising threshold detected |
| 1-0 | RESERVED        | R    | 0h    | RESERVED  |

### 8.5.1.36 REG28\_Charger\_Mask\_0 Register (Offset = 28h) [reset = 0h]

REG28\_Charger\_Mask\_0 is shown in 图 8-58 and described in 表 8-43.

Return to the 表 8-6.

Charger Mask 0

图 8-58. REG28\_Charger\_Mask\_0 Register

| 7           | 6           | 5       | 4            | 3       | 2                | 1                | 0                 |
|-------------|-------------|---------|--------------|---------|------------------|------------------|-------------------|
| IINDPM_MASK | VINDPM_MASK | WD_MASK | POORSRC_MASK | PG_MASK | AC2_PRESENT_MASK | AC1_PRESENT_MASK | VBUS_PRESENT_MASK |
| R/W-0h      | R/W-0h      | R/W-0h  | R/W-0h       | R/W-0h  | R/W-0h           | R/W-0h           | R/W-0h            |

表 8-43. REG28\_Charger\_Mask\_0 Register Field Descriptions

| Bit | Field            | Type | Reset | Notes                | Description   |
|-----|------------------|------|-------|----------------------|---|
| 7   | IINDPM_MASK      | R/W  | 0h    | Reset by:<br>REG_RST | IINDPM mask flag<br>Type : RW<br>POR: 0b<br>0h = Enter IINDPM does produce INT pulse<br>1h = Enter IINDPM does NOT produce INT pulse  |
| 6   | VINDPM_MASK      | R/W  | 0h    | Reset by:<br>REG_RST | VINDPM mask flag<br>Type : RW<br>POR: 0b<br>0h = Enter VINDPM does produce INT pulse<br>1h = Enter VINDPM does NOT produce INT pulse  |
| 5   | WD_MASK          | R/W  | 0h    | Reset by:<br>REG_RST | I2C watch dog timer mask flag<br>Type : RW<br>POR: 0b<br>0h = I2C watch dog timer expired does produce INT pulse<br>1h = I2C watch dog timer expired does NOT produce INT pulse |
| 4   | POORSRC_MASK     | R/W  | 0h    | Reset by:<br>REG_RST | Poor source detection mask flag<br>Type : RW<br>POR: 0b<br>0h = Poor source detected does produce INT<br>1h = Poor source detected does NOT produce INT                         |
| 3   | PG_MASK          | R/W  | 0h    | Reset by:<br>REG_RST | Power Good mask flag<br>Type : RW<br>POR: 0b<br>0h = PG toggle does produce INT<br>1h = PG toggle does NOT produce INT  |
| 2   | AC2_PRESENT_MASK | R/W  | 0h    | Reset by:<br>REG_RST | VAC2 present mask flag<br>Type : RW<br>POR: 0b<br>0h = VAC2 present status change does produce INT<br>1h = VAC2 present status change does NOT produce INT                      |
| 1   | AC1_PRESENT_MASK | R/W  | 0h    | Reset by:<br>REG_RST | VAC1 present mask flag<br>Type : RW<br>POR: 0b<br>0h = VAC1 present status change does produce INT<br>1h = VAC1 present status change does NOT produce INT                      |

表 8-43. REG28\_Charger\_Mask\_0 Register Field Descriptions (continued)

| Bit | Field             | Type | Reset | Notes                | Description  |
|-----|-------------------|------|-------|----------------------|--|
| 0   | VBUS_PRESENT_MASK | R/W  | 0h    | Reset by:<br>REG_RST | VBUS present mask flag<br>Type : RW<br>POR: 0b<br>0h = VBUS present status change does produce INT<br>1h = VBUS present status change does NOT produce INT |

### 8.5.1.37 REG29\_Charger\_Mask\_1 Register (Offset = 29h) [reset = 0h]

REG29\_Charger\_Mask\_1 is shown in 图 8-59 and described in 表 8-44.

Return to the 表 8-6.

Charger Mask 1

图 8-59. REG29\_Charger\_Mask\_1 Register

| 7        | 6        | 5        | 4         | 3        | 2         | 1                     | 0                   |
|----------|----------|----------|-----------|----------|-----------|-----------------------|---------------------|
| CHG_MASK | ICO_MASK | RESERVED | VBUS_MASK | RESERVED | TREG_MASK | VBAT_PRESEN<br>T_MASK | BC1.2_DONE_<br>MASK |
| R/W-0h   | R/W-0h   | R-0h     | R/W-0h    | R-0h     | R/W-0h    | R/W-0h                | R/W-0h              |

表 8-44. REG29\_Charger\_Mask\_1 Register Field Descriptions

| Bit | Field                 | Type | Reset | Notes                | Description  |
|-----|-----------------------|------|-------|----------------------|--|
| 7   | CHG_MASK              | R/W  | 0h    | Reset by:<br>REG_RST | Charge status mask flag<br>Type : RW<br>POR: 0b<br>0h = Charging status change does produce INT<br>1h = Charging status change does NOT produce INT        |
| 6   | ICO_MASK              | R/W  | 0h    | Reset by:<br>REG_RST | ICO status mask flag<br>Type : RW<br>POR: 0b<br>0h = ICO status change does produce INT<br>1h = ICO status change does NOT produce INT                     |
| 5   | RESERVED              | R    | 0h    |                      | RESERVED   |
| 4   | VBUS_MASK             | R/W  | 0h    | Reset by:<br>REG_RST | VBUS status mask flag<br>Type : RW<br>POR: 0b<br>0h = VBUS status change does produce INT<br>1h = VBUS status change does NOT produce INT                  |
| 3   | RESERVED              | R    | 0h    |                      | RESERVED   |
| 2   | TREG_MASK             | R/W  | 0h    | Reset by:<br>REG_RST | IC thermal regulation mask flag<br>Type : RW<br>POR: 0b<br>0h = entering TREG does produce INT<br>1h = entering TREG does NOT produce INT                  |
| 1   | VBAT_PRESENT_M<br>ASK | R/W  | 0h    | Reset by:<br>REG_RST | VBAT present mask flag<br>Type : RW<br>POR: 0b<br>0h = VBAT present status change does produce INT<br>1h = VBAT present status change does NOT produce INT |
| 0   | BC1.2_DONE_MAS<br>K   | R/W  | 0h    | Reset by:<br>REG_RST | BC1.2 status mask flag<br>Type : RW<br>POR: 0b<br>0h = BC1.2 status change does produce INT<br>1h = BC1.2 status change does NOT produce INT               |

### 8.5.1.38 REG2A\_Charger\_Mask\_2 Register (Offset = 2Ah) [reset = 0h]

REG2A\_Charger\_Mask\_2 is shown in 图 8-60 and described in 表 8-45.

Return to the 表 8-6.

Charger Mask 2

**图 8-60. REG2A\_Charger\_Mask\_2 Register**

| 7        | 6              | 5             | 4         | 3            | 2               | 1               | 0               |
|----------|----------------|---------------|-----------|--------------|-----------------|-----------------|-----------------|
| RESERVED | DPDM_DONE_MASK | ADC_DONE_MASK | VSYS_MASK | CHG_TMR_MASK | TRICHG_TMR_MASK | PRECHG_TMR_MASK | TOPOFF_TMR_MASK |
| R-0h     | R/W-0h         | R/W-0h        | R/W-0h    | R/W-0h       | R/W-0h          | R/W-0h          | R/W-0h          |

**表 8-45. REG2A\_Charger\_Mask\_2 Register Field Descriptions**

| Bit | Field           | Type | Reset | Notes                | Description   |
|-----|-----------------|------|-------|----------------------|---|
| 7   | RESERVED        | R    | 0h    |                      | RESERVED  |
| 6   | DPDM_DONE_MASK  | R/W  | 0h    | Reset by:<br>REG_RST | D+/D- detection is done mask flag<br>Type : RW<br>POR: 0b<br>0h = D+/D- detection done does produce INT pulse<br>1h = D+/D- detection done does NOT produce INT pulse                     |
| 5   | ADC_DONE_MASK   | R/W  | 0h    | Reset by:<br>REG_RST | ADC conversion mask flag (only in one-shot mode)<br>Type : RW<br>POR: 0b<br>0h = ADC conversion done does produce INT pulse<br>1h = ADC conversion done does NOT produce INT pulse        |
| 4   | VSYS_MASK       | R/W  | 0h    | Reset by:<br>REG_RST | VSYS min regulation mask flag<br>Type : RW<br>POR: 0b<br>0h = enter or exit VSYSMIN regulation does produce INT pulse<br>1h = enter or exit VSYSMIN regulation does NOT produce INT pulse |
| 3   | CHG_TMR_MASK    | R/W  | 0h    | Reset by:<br>REG_RST | Fast charge timer mask flag<br>Type : RW<br>POR: 0b<br>0h = Fast charge timer expire does produce INT<br>1h = Fast charge timer expire does NOT produce INT                               |
| 2   | TRICHG_TMR_MASK | R/W  | 0h    | Reset by:<br>REG_RST | Trickle charge timer mask flag<br>Type : RW<br>POR: 0b<br>0h = Trickle charge timer expire does produce INT<br>1h = Trickle charge timer expire does NOT produce INT                      |
| 1   | PRECHG_TMR_MASK | R/W  | 0h    | Reset by:<br>REG_RST | Pre-charge timer mask flag<br>Type : RW<br>POR: 0b<br>0h = Pre-charge timer expire does produce INT<br>1h = Pre-charge timer expire does NOT produce INT                                  |
| 0   | TOPOFF_TMR_MASK | R/W  | 0h    | Reset by:<br>REG_RST | Top off timer mask flag<br>Type : RW<br>POR: 0b<br>0h = Top off timer expire does produce INT<br>1h = Top off timer expire does NOT produce INT   |

### 8.5.1.39 REG2B\_Charger\_Mask\_3 Register (Offset = 2Bh) [reset = 0h]

REG2B\_Charger\_Mask\_3 is shown in 图 8-61 and described in 表 8-46.

Return to the 表 8-6.

Charger Mask 3

图 8-61. REG2B\_Charger\_Mask\_3 Register

| 7        | 6 | 5 | 4        | 3            | 2            | 1            | 0           |
|----------|---|---|----------|--------------|--------------|--------------|-------------|
| RESERVED |   |   | RESERVED | TS_COLD_MASK | TS_COOL_MASK | TS_WARM_MASK | TS_HOT_MASK |
| R-0h     |   |   | R-0h     | R/W-0h       | R/W-0h       | R/W-0h       | R/W-0h      |

表 8-46. REG2B\_Charger\_Mask\_3 Register Field Descriptions

| Bit | Field        | Type | Reset | Notes                            | Description  |
|-----|--------------|------|-------|----------------------------------|--|
| 7-5 | RESERVED     | R    | 0h    |                                  | RESERVED   |
| 4   | RESERVED     | R/W  | 0h    |                                  |  |
| 3   | TS_COLD_MASK | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | TS cold temperature interrupt mask<br>Type : RW<br>POR: 0b<br>0h = TS across cold temperature (T1) does produce INT<br>1h = TS across cold temperature (T1) does NOT produce INT |
| 2   | TS_COOL_MASK | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | TS cool temperature interrupt mask<br>Type : RW<br>POR: 0b<br>0h = TS across cool temperature (T2) does produce INT<br>1h = TS across cool temperature (T2) does NOT produce INT |
| 1   | TS_WARM_MASK | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | TS warm temperature interrupt mask<br>Type : RW<br>POR: 0b<br>0h = TS across warm temperature (T3) does produce INT<br>1h = TS across warm temperature (T3) does NOT produce INT |
| 0   | TS_HOT_MASK  | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | TS hot temperature interrupt mask<br>Type : RW<br>POR: 0b<br>0h = TS across hot temperature (T5) does produce INT<br>1h = TS across hot temperature (T5) does NOT produce INT    |

### 8.5.1.40 REG2C\_FAULT\_Mask\_0 Register (Offset = 2Ch) [reset = 0h]

REG2C\_FAULT\_Mask\_0 is shown in 图 8-62 and described in 表 8-47.

Return to the 表 8-6.

FAULT Mask 0

图 8-62. REG2C\_FAULT\_Mask\_0 Register

| 7             | 6             | 5             | 4             | 3             | 2             | 1             | 0             |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| IBAT_REG_MASK | VBUS_OVP_MASK | VBAT_OVP_MASK | IBUS_OCP_MASK | IBAT_OCP_MASK | CONV_OCP_MASK | VAC2_OVP_MASK | VAC1_OVP_MASK |
| R/W-0h        | R/W-0h        | R/W-0h        | R/W-0h        | R/W-0h        | R/W-0h        | R/W-0h        | R/W-0h        |

表 8-47. REG2C\_FAULT\_Mask\_0 Register Field Descriptions

| Bit | Field         | Type | Reset | Notes                | Description   |
|-----|---------------|------|-------|----------------------|---|
| 7   | IBAT_REG_MASK | R/W  | 0h    | Reset by:<br>REG_RST | IBAT regulation mask flag<br>Type : RW<br>POR: 0b<br>0h = enter or exit IBAT regulation does produce INT<br>1h = enter or exit IBAT regulation does NOT produce INT |
| 6   | VBUS_OVP_MASK | R/W  | 0h    | Reset by:<br>REG_RST | VBUS over-voltage mask flag<br>Type : RW<br>POR: 0b<br>0h = entering VBUS OVP does produce INT<br>1h = entering VBUS OVP does NOT produce INT                       |
| 5   | VBAT_OVP_MASK | R/W  | 0h    | Reset by:<br>REG_RST | VBAT over-voltage mask flag<br>Type : RW<br>POR: 0b<br>0h = entering VBAT OVP does produce INT<br>1h = entering VBAT OVP does NOT produce INT                       |
| 4   | IBUS_OCP_MASK | R/W  | 0h    | Reset by:<br>REG_RST | IBUS over-current mask flag<br>Type : RW<br>POR: 0b<br>0h = IBUS OCP fault does produce INT<br>1h = IBUS OCP fault does NOT produce INT                             |
| 3   | IBAT_OCP_MASK | R/W  | 0h    | Reset by:<br>REG_RST | IBAT over-current mask flag<br>Type : RW<br>POR: 0b<br>0h = IBAT OCP fault does produce INT<br>1h = IBAT OCP fault does NOT produce INT                             |
| 2   | CONV_OCP_MASK | R/W  | 0h    | Reset by:<br>REG_RST | Converter over-current mask flag<br>Type : RW<br>POR: 0b<br>0h = Converter OCP fault does produce INT<br>1h = Converter OCP fault does NOT produce INT              |
| 1   | VAC2_OVP_MASK | R/W  | 0h    | Reset by:<br>REG_RST | VAC2 over-voltage mask flag<br>Type : RW<br>POR: 0b<br>0h = entering VAC2 OVP does produce INT<br>1h = entering VAC2 OVP does NOT produce INT                       |
| 0   | VAC1_OVP_MASK | R/W  | 0h    | Reset by:<br>REG_RST | VAC1 over-voltage mask flag<br>Type : RW<br>POR: 0b<br>0h = entering VAC1 OVP does produce INT<br>1h = entering VAC1 OVP does NOT produce INT                       |



### 8.5.1.41 REG2D\_FAULT\_Mask\_1 Register (Offset = 2Dh) [reset = 0h]

REG2D\_FAULT\_Mask\_1 is shown in 图 8-63 and described in 表 8-48.

Return to the 表 8-6.

FAULT Mask 1

图 8-63. REG2D\_FAULT\_Mask\_1 Register

| 7               | 6             | 5        | 4 | 3 | 2          | 1        | 0 |
|-----------------|---------------|----------|---|---|------------|----------|---|
| VSYS_SHORT_MASK | VSYS_OVP_MASK | RESERVED |   |   | TSHUT_MASK | RESERVED |   |
| R/W-0h          | R/W-0h        | R-0h     |   |   | R/W-0h     | R-0h     |   |

表 8-48. REG2D\_FAULT\_Mask\_1 Register Field Descriptions

| Bit | Field           | Type | Reset | Notes                | Description   |
|-----|-----------------|------|-------|----------------------|---|
| 7   | VSYS_SHORT_MASK | R/W  | 0h    | Reset by:<br>REG_RST | VSYS short circuit mask flag<br>Type : RW<br>POR: 0b<br>0h = System short fault does produce INT<br>1h = System short fault does NOT produce INT            |
| 6   | VSYS_OVP_MASK   | R/W  | 0h    | Reset by:<br>REG_RST | VSYS over-voltage mask flag<br>Type : RW<br>POR: 0b<br>0h = System overvoltage fault does produce INT<br>1h = System overvoltage fault does NOT produce INT |
| 5-3 | RESERVED        | R/W  | 0h    |                      | RESERVED  |
| 2   | TSHUT_MASK      | R/W  | 0h    | Reset by:<br>REG_RST | IC thermal shutdown mask flag<br>Type : RW<br>POR: 0b<br>0h = TSHUT does produce INT<br>1h = TSHUT does NOT produce INT                                     |
| 1-0 | RESERVED        | R    | 0h    |                      | RESERVED  |

### 8.5.1.42 REG2E\_ADC\_Control Register (Offset = 2Eh) [reset = 30h]

REG2E\_ADC\_Control is shown in 图 8-64 and described in 表 8-49.

Return to the 表 8-6.

ADC Control

**图 8-64. REG2E\_ADC\_Control Register**

| 7      | 6        | 5              | 4       | 3            | 2        | 1 | 0 |
|--------|----------|----------------|---------|--------------|----------|---|---|
| ADC_EN | ADC_RATE | ADC_SAMPLE_1:0 | ADC_AVG | ADC_AVG_INIT | RESERVED |   |   |
| R/W-0h | R/W-0h   | R/W-3h         | R/W-0h  | R/W-0h       | R/W-0h   |   |   |

**表 8-49. REG2E\_ADC\_Control Register Field Descriptions**

| Bit | Field          | Type | Reset | Notes                            | Description   |
|-----|----------------|------|-------|----------------------------------|---|
| 7   | ADC_EN         | R/W  | 0h    | Reset by:<br>WATCHDOG<br>REG_RST | ADC Control<br>Type : RW<br>POR: 0b<br>0h = Disable<br>1h = Enable  |
| 6   | ADC_RATE       | R/W  | 0h    | Reset by:<br>REG_RST             | ADC conversion rate control<br>Type : RW<br>POR: 0b<br>0h = Continuous conversion<br>1h = One shot conversion   |
| 5-4 | ADC_SAMPLE_1:0 | R/W  | 3h    | Reset by:<br>REG_RST             | ADC sample speed<br>Type : RW<br>POR: 11b<br>0h = 15-bit effective resolution<br>1h = 14-bit effective resolution<br>2h = 13-bit effective resolution<br>3h = 12-bit effective resolution |
| 3   | ADC_AVG        | R/W  | 0h    | Reset by:<br>REG_RST             | ADC average control<br>Type : RW<br>POR: 0b<br>0h = Single value<br>1h = Running average  |
| 2   | ADC_AVG_INIT   | R/W  | 0h    | Reset by:<br>REG_RST             | ADC average initial value control<br>Type : RW<br>POR: 0b<br>0h = Start average using the existing register value<br>1h = Start average using a new ADC conversion                        |
| 1-0 | RESERVED       | R/W  | 0h    |                                  | RESERVED  |

### 8.5.1.43 REG2F\_ADC\_Function\_Disable\_0 Register (Offset = 2Fh) [reset = 0h]

REG2F\_ADC\_Function\_Disable\_0 is shown in 图 8-65 and described in 表 8-50.

Return to the 表 8-6.

ADC Function Disable 0

图 8-65. REG2F\_ADC\_Function\_Disable\_0 Register

| 7            | 6            | 5            | 4            | 3            | 2          | 1            | 0        |
|--------------|--------------|--------------|--------------|--------------|------------|--------------|----------|
| IBUS_ADC_DIS | IBAT_ADC_DIS | VBUS_ADC_DIS | VBAT_ADC_DIS | VSYS_ADC_DIS | TS_ADC_DIS | TDIE_ADC_DIS | RESERVED |
| R/W-0h       | R/W-0h       | R/W-0h       | R/W-0h       | R/W-0h       | R/W-0h     | R/W-0h       | R-0h     |

表 8-50. REG2F\_ADC\_Function\_Disable\_0 Register Field Descriptions

| Bit | Field        | Type | Reset | Notes                | Description   |
|-----|--------------|------|-------|----------------------|---|
| 7   | IBUS_ADC_DIS | R/W  | 0h    | Reset by:<br>REG_RST | IBUS ADC control<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable |
| 6   | IBAT_ADC_DIS | R/W  | 0h    | Reset by:<br>REG_RST | IBAT ADC control<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable |
| 5   | VBUS_ADC_DIS | R/W  | 0h    | Reset by:<br>REG_RST | VBUS ADC control<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable |
| 4   | VBAT_ADC_DIS | R/W  | 0h    | Reset by:<br>REG_RST | VBAT ADC control<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable |
| 3   | VSYS_ADC_DIS | R/W  | 0h    | Reset by:<br>REG_RST | VSYS ADC control<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable |
| 2   | TS_ADC_DIS   | R/W  | 0h    | Reset by:<br>REG_RST | TS ADC control<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable   |
| 1   | TDIE_ADC_DIS | R/W  | 0h    | Reset by:<br>REG_RST | TDIE ADC control<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable |
| 0   | RESERVED     | R    | 0h    |                      | RESERVED  |

#### 8.5.1.44 REG30\_ADC\_Function\_Disable\_1 Register (Offset = 30h) [reset = 0h]

REG30\_ADC\_Function\_Disable\_1 is shown in 图 8-66 and described in 表 8-51.

Return to the 表 8-6.

ADC Function Disable 1

**图 8-66. REG30\_ADC\_Function\_Disable\_1 Register**

| 7          | 6          | 5            | 4            | 3        | 2 | 1 | 0 |
|------------|------------|--------------|--------------|----------|---|---|---|
| DP_ADC_DIS | DM_ADC_DIS | VAC2_ADC_DIS | VAC1_ADC_DIS | RESERVED |   |   |   |
| R/W-0h     | R/W-0h     | R/W-0h       | R/W-0h       | R-0h     |   |   |   |

**表 8-51. REG30\_ADC\_Function\_Disable\_1 Register Field Descriptions**

| Bit | Field        | Type | Reset | Notes                | Description   |
|-----|--------------|------|-------|----------------------|---|
| 7   | DP_ADC_DIS   | R/W  | 0h    | Reset by:<br>REG_RST | D+ ADC Control<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable   |
| 6   | DM_ADC_DIS   | R/W  | 0h    | Reset by:<br>REG_RST | D- ADC Control<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable   |
| 5   | VAC2_ADC_DIS | R/W  | 0h    | Reset by:<br>REG_RST | VAC2 ADC Control<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable |
| 4   | VAC1_ADC_DIS | R/W  | 0h    | Reset by:<br>REG_RST | VAC1 ADC Control<br>Type : RW<br>POR: 0b<br>0h = Enable (Default)<br>1h = Disable |
| 3-0 | RESERVED     | R    | 0h    |                      | RESERVED  |

### 8.5.1.45 REG31\_IBUS\_ADC Register (Offset = 31h) [reset = 0h]

REG31\_IBUS\_ADC is shown in 图 8-67 and described in 表 8-52.

Return to the 表 8-6.

IBUS ADC

图 8-67. REG31\_IBUS\_ADC Register

|               |    |    |    |    |    |   |   |
|---------------|----|----|----|----|----|---|---|
| 15            | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| IBUS_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |
| 7             | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| IBUS_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |

表 8-52. REG31\_IBUS\_ADC Register Field Descriptions

| Bit  | Field         | Type | Reset | Description  |
|------|---------------|------|-------|--|
| 15-0 | IBUS_ADC_15:0 | R    | 0h    | IBUS ADC reading<br>Reported in 2's Complement.<br>When the current is flowing from VBUS to PMID, IBUS ADC reports positive value, and when the current is flowing from PMID to VBUS, IBUS ADC reports negative value.<br>Type : R<br>POR: 0 mA (0h)<br>Range : 0 mA-5000 mA<br>Fixed Offset : 0 mA<br>Bit Step Size : 1mA |

### 8.5.1.46 REG33\_IBAT\_ADC Register (Offset = 33h) [reset = 0h]

REG33\_IBAT\_ADC is shown in 图 8-68 and described in 表 8-53.

Return to the 表 8-6.

IBAT ADC

图 8-68. REG33\_IBAT\_ADC Register

|               |    |    |    |    |    |   |   |
|---------------|----|----|----|----|----|---|---|
| 15            | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| IBAT_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |
| 7             | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| IBAT_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |

表 8-53. REG33\_IBAT\_ADC Register Field Descriptions

| Bit  | Field         | Type | Reset | Description   |
|------|---------------|------|-------|---|
| 15-0 | IBAT_ADC_15:0 | R    | 0h    | IBAT ADC reading<br>Reported in 2 's Complement.<br>The IBAT ADC reports positive value for the battery charging current,<br>and negative value for the battery discharging current.<br>Type : R<br>POR: 0 mA (0h)<br>Range : 0 mA-8000 mA<br>Fixed Offset : 0 mA<br>Bit Step Size : 1 mA |

### 8.5.1.47 REG35\_VBUS\_ADC Register (Offset = 35h) [reset = 0h]

REG35\_VBUS\_ADC is shown in 图 8-69 and described in 表 8-54.

Return to the 表 8-6.

VBUS ADC

图 8-69. REG35\_VBUS\_ADC Register

|               |    |    |    |    |    |   |   |
|---------------|----|----|----|----|----|---|---|
| 15            | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| VBUS_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |
| 7             | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| VBUS_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |

表 8-54. REG35\_VBUS\_ADC Register Field Descriptions

| Bit  | Field         | Type | Reset | Description  |
|------|---------------|------|-------|--|
| 15-0 | VBUS_ADC_15:0 | R    | 0h    | VBUS ADC reading<br>Reported in 2 's Complement.<br>Type : R<br>POR: 0 mV (0h)<br>Range : 0 mV-30000 mV<br>Fixed Offset : 0 mV<br>Bit Step Size : 1 mV |

### 8.5.1.48 REG37\_VAC1\_ADC Register (Offset = 37h) [reset = 0h]

REG37\_VAC1\_ADC is shown in 图 8-70 and described in 表 8-55.

Return to the 表 8-6.

VAC1 ADC

图 8-70. REG37\_VAC1\_ADC Register

|               |    |    |    |    |    |   |   |
|---------------|----|----|----|----|----|---|---|
| 15            | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| VAC1_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |
| 7             | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| VAC1_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |

表 8-55. REG37\_VAC1\_ADC Register Field Descriptions

| Bit  | Field         | Type | Reset | Description  |
|------|---------------|------|-------|--|
| 15-0 | VAC1_ADC_15:0 | R    | 0h    | VAC1 ADC reading<br>Reported in 2 's Complement.<br>Type : R<br>POR: 0 mV (0h)<br>Range : 0 mV-30000 mV<br>Fixed Offset : 0 mV<br>Bit Step Size : 1 mV |



### 8.5.1.49 REG39\_VAC2\_ADC Register (Offset = 39h) [reset = 0h]

REG39\_VAC2\_ADC is shown in 图 8-71 and described in 表 8-56.

Return to the 表 8-6.

VAC2 ADC

图 8-71. REG39\_VAC2\_ADC Register

|               |    |    |    |    |    |   |   |
|---------------|----|----|----|----|----|---|---|
| 15            | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| VAC2_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |
| 7             | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| VAC2_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |

表 8-56. REG39\_VAC2\_ADC Register Field Descriptions

| Bit  | Field         | Type | Reset | Description  |
|------|---------------|------|-------|--|
| 15-0 | VAC2_ADC_15:0 | R    | 0h    | VAC2 ADC reading<br>Reported in 2 's Complement.<br>Type : R<br>POR: 0 mV (0h)<br>Range : 0 mV-30000 mV<br>Fixed Offset : 0 mV<br>Bit Step Size : 1 mV |

### 8.5.1.50 REG3B\_VBAT\_ADC Register (Offset = 3Bh) [reset = 0h]

REG3B\_VBAT\_ADC is shown in 图 8-72 and described in 表 8-57.

Return to the 表 8-6.

VBAT ADC

图 8-72. REG3B\_VBAT\_ADC Register

|               |    |    |    |    |    |   |   |
|---------------|----|----|----|----|----|---|---|
| 15            | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| VBAT_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |
| 7             | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| VBAT_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |

表 8-57. REG3B\_VBAT\_ADC Register Field Descriptions

| Bit  | Field         | Type | Reset | Description   |
|------|---------------|------|-------|---|
| 15-0 | VBAT_ADC_15:0 | R    | 0h    | The battery differential voltage (VBATP - VBATN) ADC reading<br>Reported in 2's Complement.<br>Type : R<br>POR: 0 mV (0h)<br>Range : 0 mV-20000 mV<br>Fixed Offset : 0 mV<br>Bit Step Size : 1 mV |

### 8.5.1.51 REG3D\_VSYS\_ADC Register (Offset = 3Dh) [reset = 0h]

REG3D\_VSYS\_ADC is shown in 图 8-73 and described in 表 8-58.

Return to the 表 8-6.

VSYS ADC

图 8-73. REG3D\_VSYS\_ADC Register

|               |    |    |    |    |    |   |   |
|---------------|----|----|----|----|----|---|---|
| 15            | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| VSYS_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |
| 7             | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| VSYS_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |

表 8-58. REG3D\_VSYS\_ADC Register Field Descriptions

| Bit  | Field         | Type | Reset | Description  |
|------|---------------|------|-------|--|
| 15-0 | VSYS_ADC_15:0 | R    | 0h    | VSYS ADC reading<br>Reported in 2 's Complement.<br>Type : R<br>POR: 0 mV (0h)<br>Range : 0 mV-24000 mV<br>Fixed Offset : 0 mV<br>Bit Step Size : 1 mV |

### 8.5.1.52 REG3F\_TS\_ADC Register (Offset = 3Fh) [reset = 0h]

REG3F\_TS\_ADC is shown in 图 8-74 and described in 表 8-59.

Return to the 表 8-6.

TS ADC

图 8-74. REG3F\_TS\_ADC Register

|             |    |    |    |    |    |   |   |
|-------------|----|----|----|----|----|---|---|
| 15          | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TS_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h        |    |    |    |    |    |   |   |
| 7           | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| TS_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h        |    |    |    |    |    |   |   |

表 8-59. REG3F\_TS\_ADC Register Field Descriptions

| Bit  | Field       | Type | Reset | Description  |
|------|-------------|------|-------|--|
| 15-0 | TS_ADC_15:0 | R    | 0h    | TS ADC reading<br>Type : R<br>POR: 0% (0h)<br>Range : 0%-99.9023%<br>Fixed Offset : 0%<br>Bit Step Size : 0.0976563% |

### 8.5.1.53 REG41\_TDIE\_ADC Register (Offset = 41h) [reset = 0h]

REG41\_TDIE\_ADC is shown in 图 8-75 and described in 表 8-60.

Return to the 表 8-6.

TDIE\_ADC

图 8-75. REG41\_TDIE\_ADC Register

|               |    |    |    |    |    |   |   |
|---------------|----|----|----|----|----|---|---|
| 15            | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TDIE_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |
| 7             | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| TDIE_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h          |    |    |    |    |    |   |   |

表 8-60. REG41\_TDIE\_ADC Register Field Descriptions

| Bit  | Field         | Type | Reset | Description  |
|------|---------------|------|-------|--|
| 15-0 | TDIE_ADC_15:0 | R    | 0h    | TDIE ADC reading<br>Reported in 2's Complement.<br>Type : R<br>POR: 0°C (0h)<br>Range : -40°C-150°C<br>Fixed Offset : 0°C<br>Bit Step Size : 0.5°C |

### 8.5.1.54 REG43\_D+\_ADC Register (Offset = 43h) [reset = 0h]

REG43\_D+\_ADC is shown in 图 8-76 and described in 表 8-61.

Return to the 表 8-6.

D+ ADC

图 8-76. REG43\_D+\_ADC Register

|             |    |    |    |    |    |   |   |
|-------------|----|----|----|----|----|---|---|
| 15          | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| D+_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h        |    |    |    |    |    |   |   |
| 7           | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| D+_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h        |    |    |    |    |    |   |   |

表 8-61. REG43\_D+\_ADC Register Field Descriptions

| Bit  | Field       | Type | Reset | Description   |
|------|-------------|------|-------|---|
| 15-0 | D+_ADC_15:0 | R    | 0h    | D+ ADC reading<br>Type : R<br>POR: 0 mV (0h)<br>Range : 0 mV-3600 mV<br>Fixed Offset : 0 mV<br>Bit Step Size : 1 mV |

### 8.5.1.55 REG45\_D-\_ADC Register (Offset = 45h) [reset = 0h]

REG45\_D-\_ADC is shown in 图 8-77 and described in 表 8-62.

Return to the 表 8-6.

D- ADC

图 8-77. REG45\_D-\_ADC Register

|             |    |    |    |    |    |   |   |
|-------------|----|----|----|----|----|---|---|
| 15          | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| D-_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h        |    |    |    |    |    |   |   |
| 7           | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| D-_ADC_15:0 |    |    |    |    |    |   |   |
| R-0h        |    |    |    |    |    |   |   |

表 8-62. REG45\_D-\_ADC Register Field Descriptions

| Bit  | Field       | Type | Reset | Description   |
|------|-------------|------|-------|---|
| 15-0 | D-_ADC_15:0 | R    | 0h    | D- ADC reading<br>Type : R<br>POR: 0 mV (0h)<br>Range : 0 mV-3600 mV<br>Fixed Offset : 0 mV<br>Bit Step Size : 1 mV |

### 8.5.1.56 REG47\_DPDM\_Driver Register (Offset = 47h) [reset = 0h]

REG47\_DPDM\_Driver is shown in 图 8-78 and described in 表 8-63.

Return to the 表 8-6.

DPDM Driver

图 8-78. REG47\_DPDM\_Driver Register

| 7             | 6 | 5 | 4              | 3 | 2 | 1        | 0 |
|---------------|---|---|----------------|---|---|----------|---|
| DPLUS_DAC_2:0 |   |   | DMINUS_DAC_2:0 |   |   | RESERVED |   |
| R/W-0h        |   |   | R/W-0h         |   |   | R/W-0h   |   |

表 8-63. REG47\_DPDM\_Driver Register Field Descriptions

| Bit | Field          | Type | Reset | Description  |
|-----|----------------|------|-------|--|
| 7-5 | DPLUS_DAC_2:0  | R/W  | 0h    | D+ Output Driver<br>Type : RW<br>POR: 000b<br><br>0h = HIZ<br>1h = 0<br>2h = 0.6 V<br>3h = 1.2 V<br>4h = 2.0 V<br>5h = 2.7 V<br>6h = 3.3 V<br>7h = D+/D- Short |
| 4-2 | DMINUS_DAC_2:0 | R/W  | 0h    | D- Output Driver<br>Type : RW<br>POR: 000b<br><br>0h = HIZ<br>1h = 0<br>2h = 0.6 V<br>3h = 1.2 V<br>4h = 2.0 V<br>5h = 2.7 V<br>6h = 3.3 V<br>7h = Reserved    |
| 1-0 | RESERVED       | R/W  | 0h    | RESERVED   |



### 8.5.1.57 REG48\_Part\_Information Register (Offset = 48h) [reset = 0h]

REG48\_Part\_Information is shown in [图 8-79](#) and described in [表 8-64](#).

Return to the [表 8-6](#).

Part Information

**图 8-79. REG48\_Part\_Information Register**

| 7        | 6 | 5      | 4 | 3 | 2           | 1 | 0 |
|----------|---|--------|---|---|-------------|---|---|
| RESERVED |   | PN_2:0 |   |   | DEV_REV_2:0 |   |   |
| R-0h     |   | R-0h   |   |   | R-0h        |   |   |

**表 8-64. REG48\_Part\_Information Register Field Descriptions**

| Bit | Field       | Type | Reset | Description  |
|-----|-------------|------|-------|--|
| 7-6 | RESERVED    | R    | 0h    | RESERVED   |
| 5-3 | PN_2:0      | R    | 0h    | Device Part number 0h = BQ24179. All the other options are reserved<br>Type : R<br>POR: 000b |
| 2-0 | DEV_REV_2:0 | R    | 0h    | Device Revision<br>Type : R<br>POR: 001b   |

## 9 Application and Implementation

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### Note

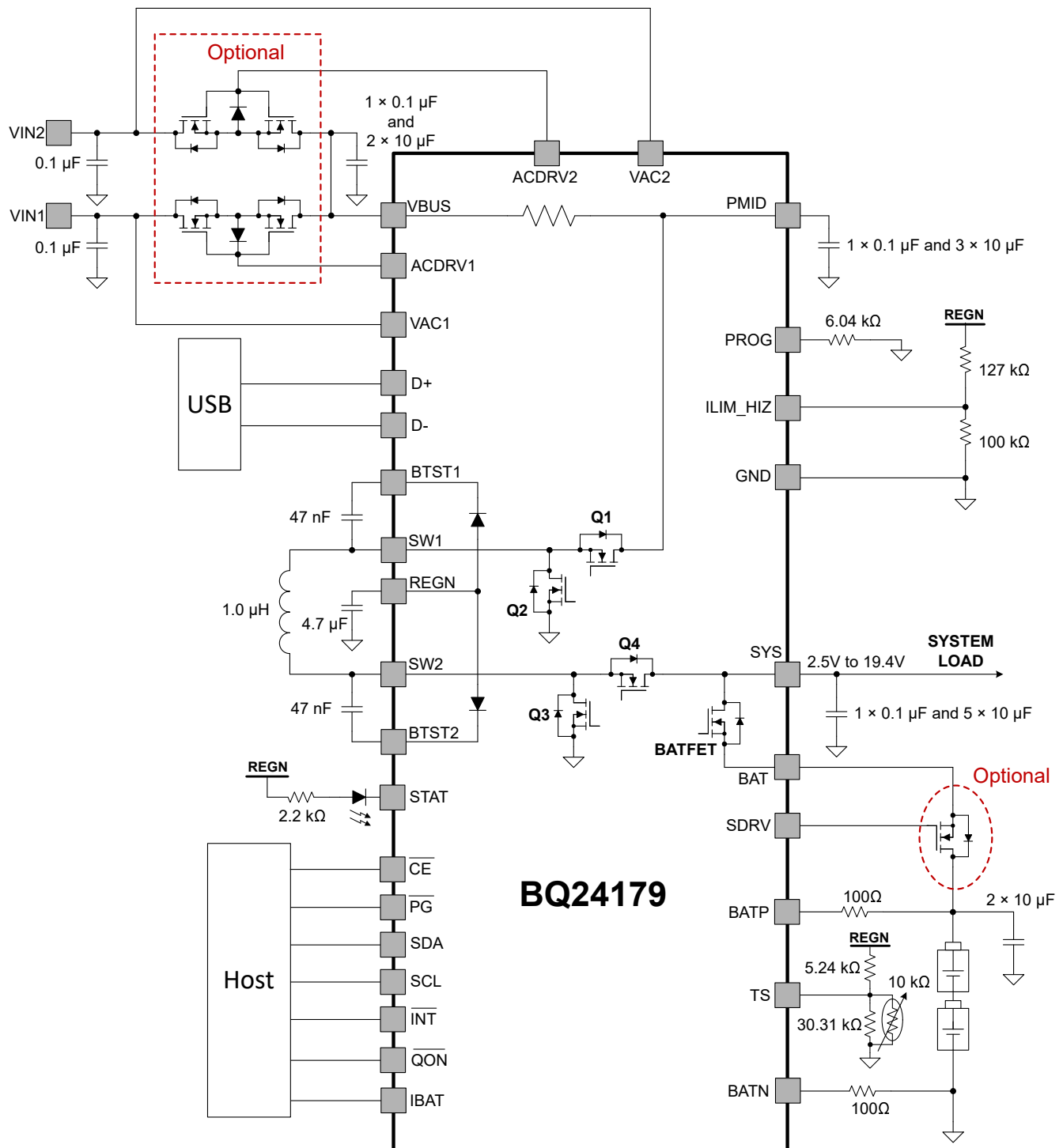
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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### 9.1 Application Information

A typical application consists of the device configured as an I<sup>2</sup>C controlled device and a multi-cell battery charger for Li-Ion and Li-polymer batteries. It integrates the four switching MOSFETs (Q<sub>1</sub> to Q<sub>4</sub>) for the buck-boost converter, and the battery FET (BATFET) between system and battery. The device also integrates the input current sensing and charging current sensing circuitries, the bootstrap diode for the high-side gate driving and the dual-input power mux for the power sources selection.

## 9.2 Typical Application



**图 9-1. BQ24179 Application Diagram with Two Input Sources and Ship FET**

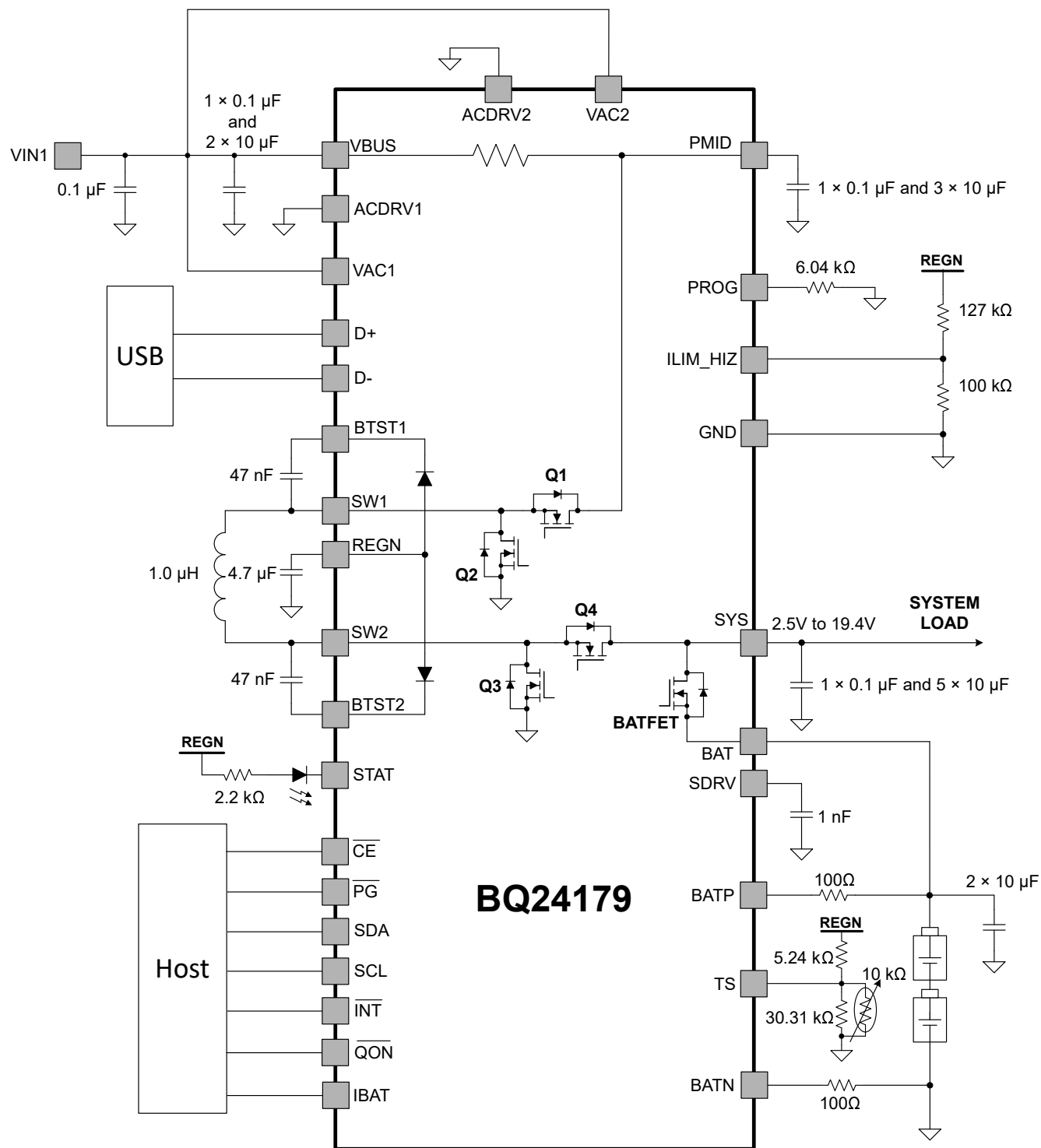


图 9-2. BQ24179 Application Diagram with Single Input Source and No Ship FET

## 9.2.1 Design Requirements

For this design example, use the parameters shown in the table below.

表 9-1. Design Parameters

| PARAMETER  | VALUE       |
|--|-------------|
| V <sub>BUS</sub> voltage range                       | 5 V to 20 V |
| Input current limit (I <sub>INDPM</sub> [8:0])       | 3.0 A       |
| Fast charge current limit (I <sub>CHG</sub> [8:0])   | 3.0 A       |
| Battery regulation voltage (V <sub>REG</sub> [10:0]) | 8.4 V       |

## 9.2.2 Detailed Design Procedure

### 9.2.2.1 Inductor Selection

The device has 1.5-MHz switching frequency to allow the use of small inductor (1  $\mu$ H) and capacitor values. It also provide the 750-kHz switching frequency to achieve higher efficiency for the applications which have enough design space to accommodate the larger inductor (2.2  $\mu$ H) and capacitors. Please note that the 1.5-MHz switching frequency only works with the 1- $\mu$ H inductor and the 750-kHz switching frequency only works with the 2.2- $\mu$ H inductor.

Because the converter might be either operated in the buck mode or the boost mode, so the inductor current is equal to either the charging current or the input current. The inductor saturation current should be higher than the larger value of the input current (I<sub>IN</sub>) or the charging current (I<sub>CHG</sub>) plus half the ripple current (I<sub>RIPPLE</sub>):

$$I_{SAT} \geq \max \left[ \left( I_{IN} + \frac{I_{RIPPLE}}{2} \right), \left( I_{CHG} + \frac{I_{RIPPLE}}{2} \right) \right] \quad (3)$$

The inductor ripple current (I<sub>RIPPLE</sub>) depends on the input voltage (V<sub>BUS</sub>), the output voltage (V<sub>SYS</sub>), the switching frequency (F<sub>SW</sub>) and the inductance (L). The inductor current ripples for buck mode and boost mode are calculated with equations (4) and (5), respectively:

$$I_{RIPPLE\_BUCK} = \frac{V_{SYS} \times (V_{BUS} - V_{SYS})}{V_{BUS} \times F_{SW} \times L} \quad (4)$$

$$I_{RIPPLE\_BOOST} = \frac{V_{BUS} \times (V_{SYS} - V_{BUS})}{V_{SYS} \times F_{SW} \times L} \quad (5)$$

The inductor current ripple in the buck mode is usually larger than that in the boost mode, since the voltage-second applied on the inductor is larger. The maximum inductor current ripple in the buck mode happens in the vicinity of  $D = V_{SYS} / V_{BUS} = 0.5$ . The SYS voltage is approximately 8 V for the 2s battery configuration, so the worst case for the inductor ripples is with the 15-V or 20-V input voltage.

### 9.2.2.2 Input (V<sub>BUS</sub> / P<sub>MID</sub>) Capacitor

In the buck mode operation, the input current is discontinuous, which dominates the input RMS ripple current and input voltage ripple. The input capacitors should have enough ripple current rating to absorb the input AC current and have large enough capacitance to maintain the small input voltage ripple. For the buck mode operation, the input RMS ripple current is calculated by the equation (6) and the input voltage ripple is calculated by the equation (7), where  $D = V_{SYS} / V_{BUS}$ .

$$I_{CIN\_BUCK} = I_{CHG} \times \sqrt{D \times (1 - D)} \quad (6)$$

$$\Delta V_{IN\_BUCK} = \frac{D \times (1 - D) \times I_{CHG}}{C_{IN} \times F_{SW}} \quad (7)$$

The worst case input RMS ripple current and input voltage ripple both occur at 0.5 duty cycle condition. The SYS voltage is approximately 8V for the 2s battery configuration, so the worst case is when 15-V to 20-V VBUS condition. Low ESR ceramic capacitor such as X7R or X5R is preferred for the input decoupling capacitor and should be placed close to the PMID and GND pins of the IC. The voltage rating of the capacitor must be higher than the normal input voltage level. The capacitor with 25-V or higher voltage rating is preferred for up to 20-V input voltage. 1\*0.1-μF + 3\*10-μF ceramic capacitors are suggested for up to 3.3-A input current limit to support the converter in forward mode.

### 9.2.2.3 Output (VSYS) Capacitor

In the boost mode operation, the output current is discontinuous, which dominates the output RMS ripple current and output voltage ripple. The output capacitors should have enough ripple current rating to absorb the output AC current and have large enough capacitance to maintain the small output voltage ripple. For the boost mode operation, the output RMS ripple current is calculated by the equation (8) and the output voltage ripple is calculated by the equation (9), where  $D = (1 - V_{BUS} / V_{SYS})$ .

$$I_{COUT\_BOOST} = I_{CHG} \times \sqrt{\frac{D}{(1-D)}} \quad (8)$$

$$\Delta V_{OUT\_BOOST} = \frac{I_{CHG} \times D}{C_{OUT} \times F_{SW}} \quad (9)$$

The worst case output RMS ripple current and output voltage ripple both occur at the lowest VBUS input voltage. The SYS voltage is approximately 8 V for the 2s battery configuration, so the worst case is 5-V VBUS condition. Low ESR ceramic capacitor such as X7R or X5R is preferred for the output decoupling capacitor and should be placed close to the SYS and GND pins of the IC. The voltage rating of the capacitor must be higher than the normal input voltage level. The capacitor with 16-V or higher voltage rating is preferred for the 2s battery configuration. 1\*0.1-μF + 5\*10-μF capacitors are suggested for up to 5-A charging current.

### 9.2.3 Application Curves

$C_{VBUS} = 2 \times 10 \mu\text{F}$ ,  $C_{PMID} = 3 \times 10 \mu\text{F}$ ,  $C_{SYS} = 5 \times 10 \mu\text{F}$ ,  $C_{BAT} = 2 \times 10 \mu\text{F}$ ,  $L1 = 1 \mu\text{H}$  (SPM6530T-1R0M120),  $F_{sw} = 1.5 \text{ MHz}$ .

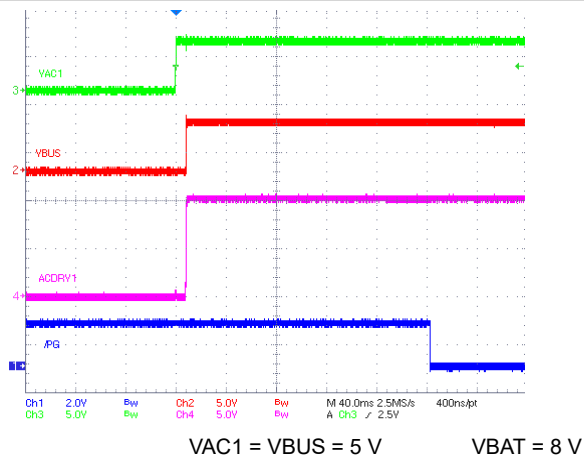


图 9-3. ACFET1-RBFET1 Turns on at Power Up

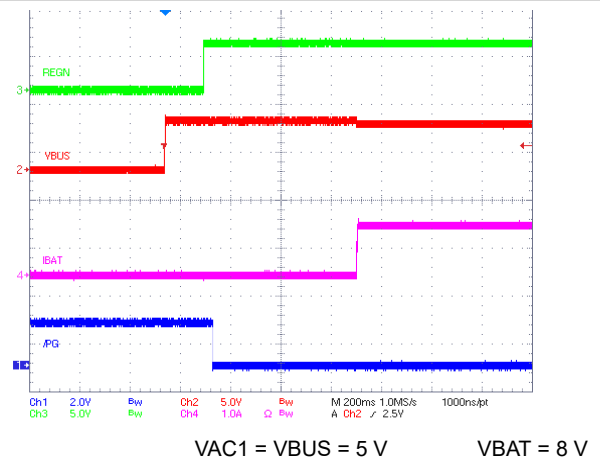


图 9-4. Power Up from VAC1 with Charge Enabled

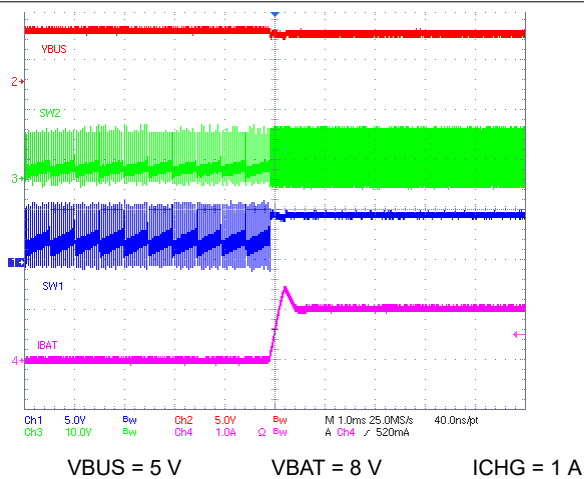


图 9-5. Charge Enable

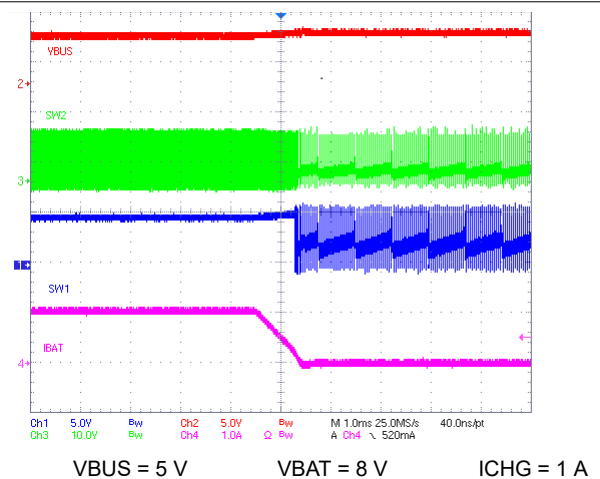


图 9-6. Charge Disable

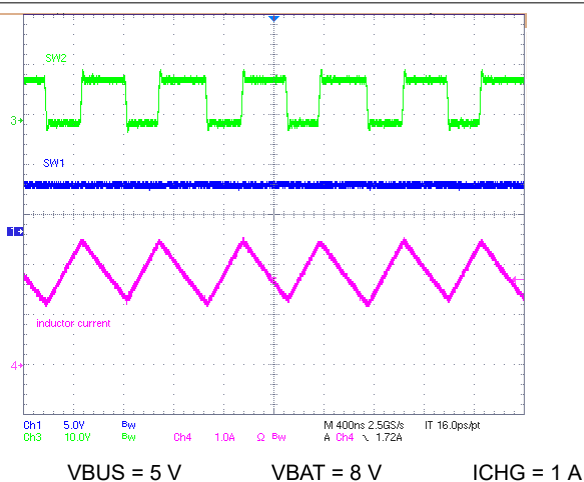


图 9-7. Boost Charging Mode PWM Operation

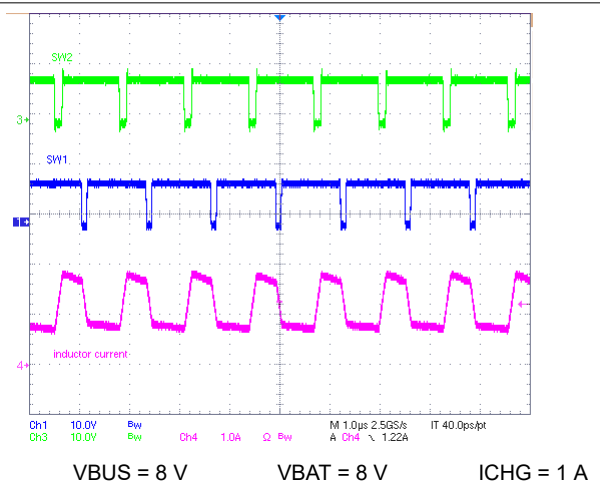


图 9-8. Buck-Boost Charging Mode PWM Operation



VBUS = 15 V      VBAT = 8 V      ICHG = 0 A

VBUS = 15 V      VBAT = 8 V      ICHG = 0 A

VBUS = 15 V      VBAT = 8 V      Charge disabled

VBUS = 5 V                      VBAT = 8 V



## 10 Power Supply Recommendations

In order to provide an output voltage on SYS, the device requires a power supply between 3.6-V and 24-V input with recommended > 500-mA current rating connected to VBUS or a 1s to 4s Li-Ion battery with voltage higher than  $V_{BAT\_UVLO}$  connected to BAT. The source current rating needs to be at least 3 A for the buck-boost converter of the charger to provide maximum output power to SYS.

The charger does not support the testing condition when the battery connection is floating. The BAT pin has to be connected to a real battery or some devices which can emulate the battery, like the battery emulator or bulk capacitors. When the BAT pin is floating, please disable charge by setting EN\_CHG to 0 or pulling low the  $\overline{EC}$  pin. Otherwise, the voltage overshoot at SYS might trigger the SYSOVP protection periodically.

## 11 Layout

### 11.1 Layout Guidelines

The switching nodes rising and falling times should be minimized for minimum switching loss. Proper layout of the components to minimize the high frequency current path loops (shown in the figure below) is important to prevent the electrical and magnetic field radiation and the high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Place the SYS output capacitors as close to SYS and GND as possible. Place a 0.1- $\mu$ F small size (such as 0402 or 0201) capacitor closer than the other 10- $\mu$ F capacitors. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
2. Place the PMID input capacitors as close to PMID and GND as possible. Place a 0.1- $\mu$ F small size (such as 0402 or 0201) capacitor closer than the other 10- $\mu$ F capacitors. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
3. Place the VBUS input capacitors as close to VBUS and GND as possible. Place a 0.1- $\mu$ F small size (such as 0402 or 0201) capacitor closer than the other 10- $\mu$ F capacitors. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
4. The connection from SYS/PMID/VBUS to the 0.1  $\mu$ F has to be routed on the top layer of the PCB, the returning back to GND also has to be in the top layer. Keep the whole routing loop as small as possible.
5. Place the inductor input terminal to SW1 and the inductor output terminal to SW2 as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the inductor current. Minimize parasitic capacitance from this area to any other trace or plane.
6. Place the BAT capacitors close to BAT and GND, place the VBUS capacitors close to VBUS and GND.
7. The REGN decoupling capacitor and the bootstrap capacitors should be placed next to the IC and make trace connection as short as possible.
8. Ensure that there are sufficient thermal vias directly under the power MOSFETs, connecting to copper on other layers.
9. Via size and number should be enough for a given current path.
10. Route BATP and BATN away from switching nodes such as SW1 and SW2.

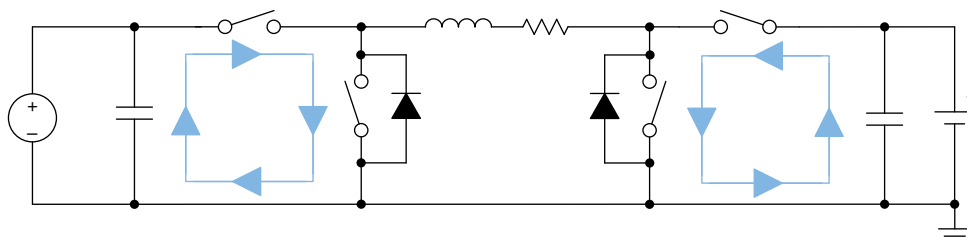


图 11-1. Buck-Boost Converter High Frequency Current Path

## 11.2 Layout Example

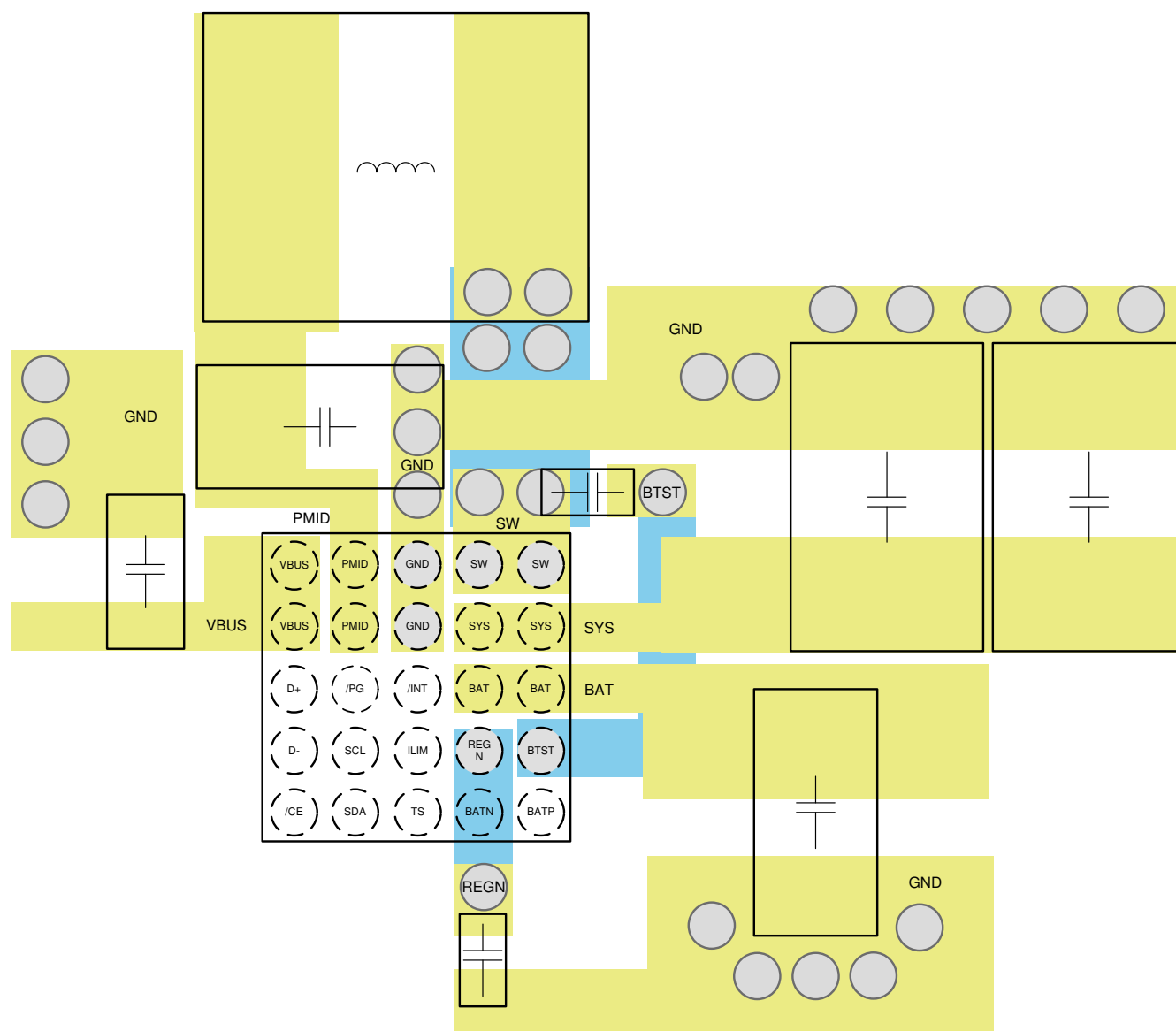


图 11-2. PCB Layout Example

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 第三方产品免责声明

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### 12.2 Documentation Support

#### 12.2.1 Related Documentation

For related documentation see the following:

- [BQ25790EVM \(BMS027\) Evaluation Module User's Guide](#)

### 12.3 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](#) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 12.4 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

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### 12.6 静电放电警告



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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 12.7 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number       | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">BQ24179YBGR</a> | Active        | Production           | DSBGA (YBG)   56 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 85    | BQ24179             |
| BQ24179YBGR.A               | Active        | Production           | DSBGA (YBG)   56 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 85    | BQ24179             |
| BQ24179YBGR.B               | Active        | Production           | DSBGA (YBG)   56 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 85    | BQ24179             |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## DSBGA - 0.5 mm max height

[illegible]

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

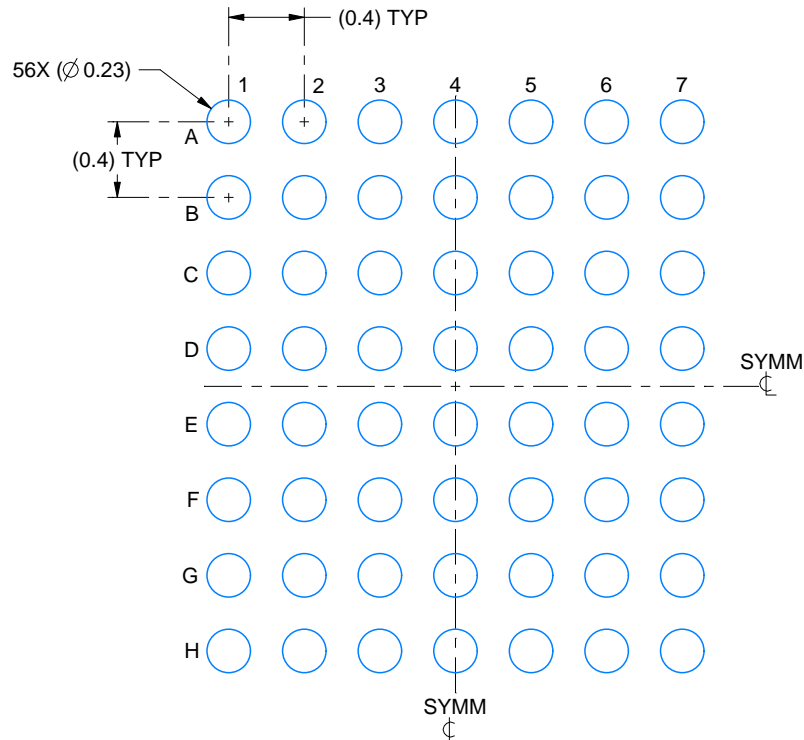
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

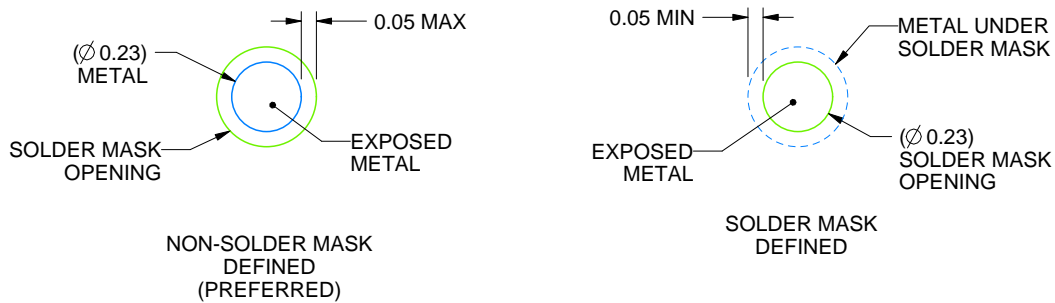
YBG0056

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



SOLDER MASK DETAILS  
NOT TO SCALE

4225513/A 11/2019

NOTES: (continued)

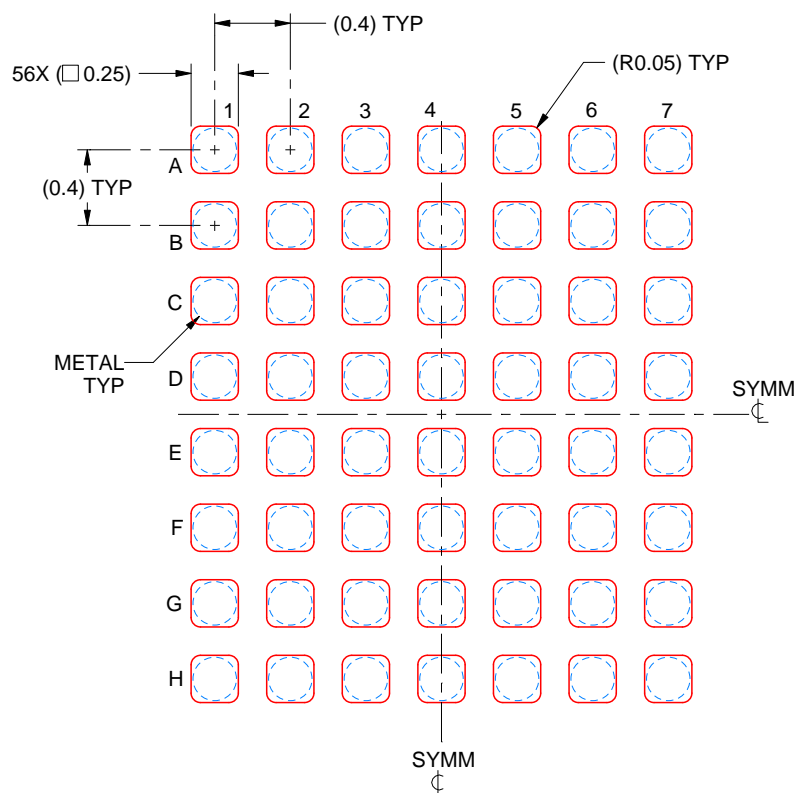
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).



**YBG0056**

## DSBGA - 0.5 mm max height

## DIE SIZE BALL GRID ARRAY



**SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE: 25X**

4225513/A 11/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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