AMC1336-Q1 Small, High-Precision, Reinforced Isolated Delta-Sigma Modulator for Voltage Sensing Applications

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to 125°C, T_A
- Input structure optimized for voltage measurements:
  - Input voltage range: ±1 V
  - Input resistance: 1.5 GΩ (typ)
- Excellent DC performance:
  - Offset error: ±0.5 mV (max)
  - Offset drift: ±4 µV/°C (max)
  - Gain error: ±0.2% (max)
  - Gain drift: ±40 ppm/°C (max)
- Transient immunity: 115 kV/µs (typ)
- Missing high-side supply detection
- Safety-related certifications:
  - 8000-V_{PEAK} reinforced isolation per DIN VDE V 0884-11: 2017-01
  - 5700-V_{RMS} isolation for 1 minute per UL1577
  - IEC 62368-1 end equipment standard

2 Applications

- Isolated AC and DC voltage measurement in:
  - HEV/EV on-board chargers (OBC)
  - HEV/EV DC/DC converters
  - HEV/EV traction inverters

3 Description

The AMC1336-Q1 is a precision, delta-sigma (ΔΣ) modulator with the output separated from the input circuitry by a capacitive double isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced isolation of up to 8000 V_{PEAK} according to the DIN VDE V 0884-11 and UL1577 standards. Used in conjunction with isolated power supplies, this isolated modulator separates parts of the system that operate on different common-mode voltage levels and protects lower-voltage parts from damage.

The unique wide, bipolar. ±1-V input voltage range of theAMC1336-Q1 and its high input resistance support direct connection of the device to resistive dividers in high-voltage applications. When used with a digital filter (for instance, as integrated in the TMS320F28004x, TMS320F2807x, or TMS320F2837x microcontroller families) to decimate the output bitstream, the device can achieve 16 bits of resolution with a dynamic range of 87 dB at a data rate of 82 kSPS.

On the high-side, the AMC1336-Q1 is supplied by a 3.3-V or 5-V power supply. The isolated digital interface operates from a 3.0-V, 3.3-V or 5-V power supply.

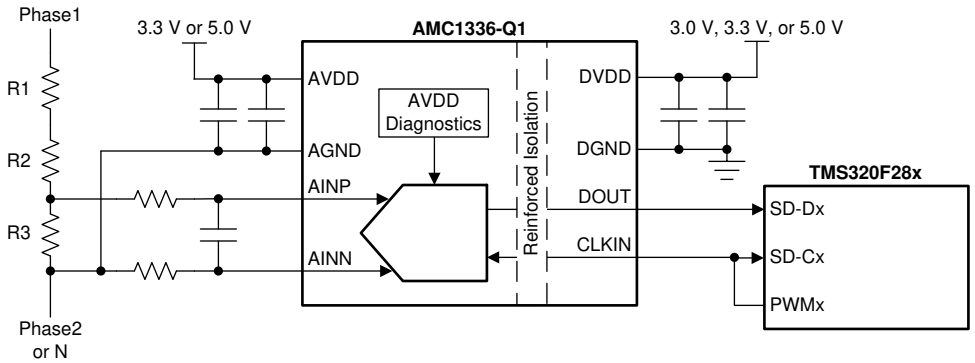
The AMC1336-Q1 performance is specified over the extended industrial temperature range of –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AMC1336-Q1	SOIC (8)	5.85 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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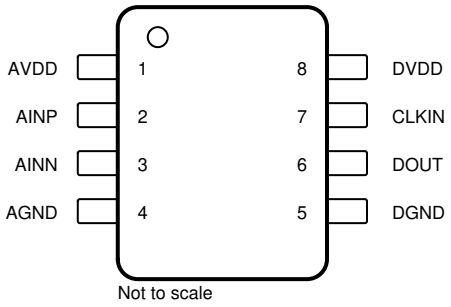
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2020	*	Initial release.

5 Pin Configuration and Functions

DWV Package
8-Pin SOIC
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	AVDD	—	Analog (high-side) power supply, 3.0 V to 5.5 V. See the *Power Supply Recommendations* section for decoupling recommendations.
2	AINP	I	Noninverting analog input
3	AINN	I	Inverting analog input
4	AGND	—	Analog (high-side) ground reference
5	DGND	—	Digital (controller-side) ground reference
6	DOUT	O	Modulator bitstream output, updated with the rising edge of the clock signal present on CLKIN. Use the rising edge of the clock to latch the modulator bitstream at the input of the digital filter device.
7	CLKIN	I	Modulator clock input with internal pulldown resistor (typical value: 1 MΩ). The clock signal must be applied continuously for proper device operation; see the *Clock Input* section for additional details.
8	DVDD	—	Digital (controller-side) power supply, 2.7 V to 5.5 V. See the *Power Supply Recommendations* section for decoupling recommendations.

6 Specifications

6.1 Absolute Maximum Ratings

see(1)

		MIN	MAX	UNIT
Power-supply voltage	AVDD to AGND	–0.3	6.5	V
	DVDD to DGND	–0.3	6.5	
Analog input voltage	On the AINP and AINN pins	AGND – 5	AVDD + 0.5	V
Digital input voltage	On the CLKIN pin	DGND – 0.5	DVDD + 0.5	V
Digital output voltage	On the DOUT pin	DGND – 0.5	DVDD + 0.5	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1), HBM ESD classification Level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011, CDM ESD classification Level C6	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
AVDD	High-side supply voltage	AVDD to AGND	3.0	5.0	5.5	V
DVDD	Controller-side	DVDD to DGND	2.7	3.3	5.5	V
ANALOG INPUT						
$V_{Clipping}$	Differential input voltage before clipping output	$V_{IN} = V_{AINP} – V_{AINN}$		±1.25		V
V_{FSR}	Specified linear differential full-scale voltage	$V_{IN} = V_{AINP} – V_{AINN}$	–1		1	V
	Absolute common-mode input voltage(1)	$(V_{AINP} + V_{AINN}) / 2$ to AGND	–2		AVDD	V
V_{CM}	Operating common-mode input voltage(2)	$(V_{AINP} + V_{AINN}) / 2$ to AGND, 3.0 V ≤ AVDD < 4 V, $V_{AINP} = V_{AINN}$	–1.4		AVDD – 1.4	V
		$(V_{AINP} + V_{AINN}) / 2$ to AGND, 3.0 V ≤ AVDD < 4.5 V, $\lvert V_{AINP} – V_{AINN} \rvert$ = 1.25 V	–0.8		AVDD – 2.4	
		$(V_{AINP} + V_{AINN}) / 2$ to AGND, 4 V ≤ AVDD ≤ 5.5 V, $V_{AINP} = V_{AINN}$	–1.4		2.7	
		$(V_{AINP} + V_{AINN}) / 2$ to AGND, 4.5 V ≤ AVDD ≤ 5.5 V, $\lvert V_{AINP} – V_{AINN} \rvert$ = 1.25 V	–0.8		2.1	
DIGITAL INPUT						
	Input voltage	V_{CLKIN} to DGND	DGND		DVDD	V
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–40	25	125	°C

(1) Steady-state voltage supported by the device in case of a system failure. See specified common-mode input voltage V_{CM} for normal operation. Observe analog input voltage range as specified in the *Absolute Maximum Ratings* table.
(2) See the Analog Input section for more details.

6.4 Thermal Information

THERMAL METRIC(1)		AMC1336-Q1 DWV (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	94	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	44.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	AVDD = DVDD = 5.5 V	90.75	mW
		AVDD = DVDD = 3.6 V	50.4	
P_{D1}	Maximum power dissipation (high-side supply)	AVDD = 5.5 V	57.75	mW
		AVDD = 3.6 V	32.4	
P_{D2}	Maximum power dissipation (controller-side supply)	DVDD = 5.5 V	33	mW
		DVDD = 3.6 V	18	

6.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 8.5	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 8.5	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation	≥ 0.021	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN VDE V 0884-11: 2017-01(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	2121	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave); see Figure 5	1500	V_{RMS}
		At DC voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification test)	8000	V_{PK}
		$V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production test)	9600	
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 60065, 1.2/50-µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 12800\ V_{PK}$ (qualification)	8000	V_{PK}
q_{pd}	Apparent charge(4)	Method a, after input/output safety test subgroups 2 & 3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.5 V_{PP} at 1 MHz	~1	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500 V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^{9}	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ = 5700 V_{RMS}, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$ = 6840 V_{RMS}, t = 1 s (100% production test)	5700	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier are tied together, creating a two-pin device.

6.7 Safety-Related Certifications

VDE	UL
Certified according to DIN VDE V 0884-11: 2017-01, DIN EN 62368-1: 2016-05, EN 62368-1: 2014, and IEC 62368-1: 2014	Recognized under 1577 component recognition
Reinforced insulation	Single protection
Certificate number: 40040142	File number: pending

6.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 94°C/W, T_J = 150°C, T_A = 25°C, AVDD = DVDD = 5.5 V, see Figure 3			241	mA
		$R_{\theta JA}$ = 94°C/W, T_J = 150°C, T_A = 25°C, AVDD = DVDD = 3.6 V, see Figure 3			369	
P_S	Safety input, output, or total power(1)	$R_{\theta JA}$ = 94°C/W, T_J = 150°C, T_A = 25°C, see Figure 4			1329	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times AVDD_{max} + I_S \times DVDD_{max}$, where $AVDD_{max}$ is the maximum high-side voltage and $DVDD_{max}$ is the maximum controller-side supply voltage.

6.9 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C, AVDD = 3.0 V to 5.5 V, DVDD = 2.7 V to 5.5 V, AINP = –1 V to +1 V, and AINN = AGND = 0 V; typical specifications are at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, and f_{CLKIN} = 20 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
R_{IN}	Single-ended input resistance	AINN = AGND	0.1	1.5		GΩ
R_{IND}	Differential input resistance		0.16	1.5		GΩ
C_{IN}	Single-ended input capacitance	AINN = AGND, f_{CLKIN} = 20 MHz		2		pF
C_{IND}	Differential input capacitance	f_{CLKIN} = 20 MHz		2		pF
I_{IB}	Input bias current	AINP = AINN = AGND; $I_{IB} = (I_{AINP} + I_{AINN}) / 2$	–10	±3	10	nA
TCI_{IB}	Input bias current drift	AINP = AINN = AGND; $I_{IB} = (I_{AINP} + I_{AINN}) / 2$		–14		pA/°C
I_{IO}	Input offset current	$I_{IO} = I_{AINP} – I_{AINN}$	–5	±1	5	nA
CMTI	Common-mode transient immunity	|AGND – DGND| = 1 kV	80	115		kV/µs

Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C, AVDD = 3.0 V to 5.5 V, DVDD = 2.7 V to 5.5 V, AINP = –1 V to +1 V, and AINN = AGND = 0 V; typical specifications are at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, and f_{CLKIN} = 20 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC ACCURACY						
	Resolution	Decimation filter output set to 16 bits	16			Bit
INL	Integral nonlinearity(1)	Resolution: 16 bits	–4	±1.6	4	LSB
E_O	Offset error	Initial, at T_A = 25°C, AINP = AINN = AGND	–0.5	±0.03	0.5	mV
TCE_O	Offset error drift(2)		–4	±0.6	4	µV/°C
E_G	Gain error(3)	Initial, at T_A = 25°C, V_{AINP} = 1 V or V_{AINN} = –1 V, AINN = AGND	–0.2	±0.02	0.2	%
TCE_G	Gain error drift(4)		–40	±20	40	ppm/°C
CMRR	Common-mode rejection ratio	AINP = AINN, f_{IN} = 0 Hz, $V_{CM\ min} \le V_{CM} \le V_{CM\ max}$		–104		dB
		AINP = AINN, f_{IN} = 10 kHz, –0.5 V ≤ V_{IN} ≤ 0.5 V		–96		
PSRR	Power-supply rejection ratio	PSRR vs AVDD, at DC		–83		dB
		PSRR vs AVDD, 100-mV and 10-kHz ripple		–83		
AC ACCURACY						
SNR	Signal-to-noise ratio	V_{IN} = 2 V_{PP}, f_{IN} = 1 kHz	82	87		dB
SINAD	Signal-to-noise + distortion	V_{IN} = 2 V_{PP}, f_{IN} = 1 kHz	79	85		dB
THD	Total harmonic distortion	V_{IN} = 2 V_{PP}, f_{IN} = 1 kHz; single-ended input (AINN = AGND = 0V)		-91	-80	dB
		V_{IN} = 2 V_{PP}, f_{IN} = 1 kHz; Differential input over full CM range		-92	-78	dB
SFDR	Spurious-free dynamic range	V_{IN} = 2 V_{PP}, f_{IN} = 1 kHz	80	92		dB
DIGITAL INPUT (CMOS Logic With Schmitt-Trigger)						
I_{IN}	Input current	DGND ≤ V_{IN} ≤ DVDD			7	µA
C_{IN}	Input capacitance			4		pF
V_{IH}	High-level input voltage		0.7 x DVDD		DVDD + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.3 x DVDD	V
DIGITAL OUTPUT (CMOS)						
C_{LOAD}	Output load capacitance	f_{CLKIN} = 21 MHz		15	30	pF
V_{OH}	High-level output voltage	I_{OH} = –20 µA	DVDD – 0.1			V
		I_{OH} = –4 mA	DVDD – 0.4			
V_{OL}	Low-level output voltage	I_{OL} = 20 µA			0.1	V
		I_{OL} = 4 mA			0.4	
POWER SUPPLY						
$AVDD_{POR}$	AVDD power-on reset threshold voltage	AVDD falling	2.4	2.6	2.8	V
I_{AVDD}	High-side supply current	3 V ≤ AVDD ≤ 3.6 V		6.8	9	mA
		4.5 V ≤ AVDD ≤ 5.5 V		7.8	10.5	
I_{DVDD}	Controller-side supply current	2.7 V ≤ DVDD ≤ 3.6 V, C_{LOAD} = 15 pF		3.4	5	mA
		4.5 V ≤ DVDD ≤ 5.5 V, C_{LOAD} = 15 pF		3.7	6	

(1) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as number of LSBs or as a percent of the specified linear full-scale range FSR.
(2) Offset error drift is calculated using the box method, as described by the following equation:
TCE_O = ($value_{MAX}$ - $value_{MIN}$) / TempRange
(3) The typical value includes one sigma statistical variation.
(4) Gain error drift is calculated using the box method, as described by the following equation:
TCE_G (ppm) = (($value_{MAX}$ - $value_{MIN}$) / (value x TempRange)) x 10^6.

6.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{CLKIN}	CLKIN clock frequency	3.0 V ≤ AVDD ≤ 5.5 V	9	20	21	MHz
		4.5 V ≤ AVDD ≤ 5.5 V	5	20	21	
	CLKIN duty cycle		40%	50%	60%	
t_{H1}	DOUT hold time after rising edge of CLKIN	C_{LOAD} = 15 pF	3.5			ns
t_{D1}	Rising edge of CLKIN to DOUT valid delay	C_{LOAD} = 15 pF			15	ns
t_r	DOUT rise time	10% to 90%, 2.7 V ≤ DVDD ≤ 3.6 V, C_{LOAD} = 15 pF		2.5	6	ns
		10% to 90%, 4.5 V ≤ DVDD ≤ 5.5 V, C_{LOAD} = 15 pF		3.2	6	
t_f	DOUT fall time	10% to 90%, 2.7 V ≤ DVDD ≤ 3.6 V, C_{LOAD} = 15 pF		2.2	6	ns
		10% to 90%, 4.5 V ≤ DVDD ≤ 5.5 V, C_{LOAD} = 15 pF		2.9	6	
t_{ASTART}	Analog start-up time	AVDD step to 3.0 V; 0.1%-settling, clock applied		0.25		ms

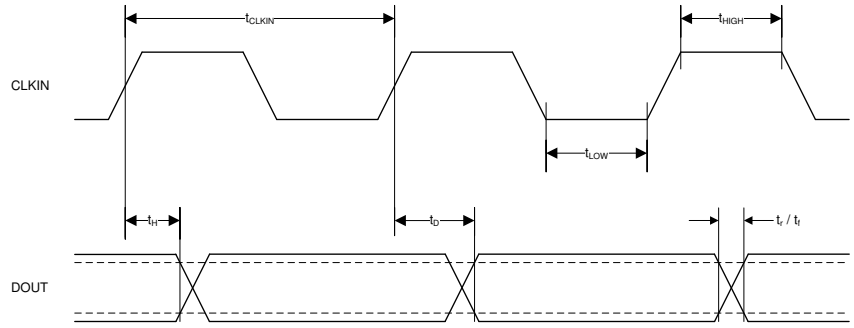


Figure 1. Digital Interface Timing

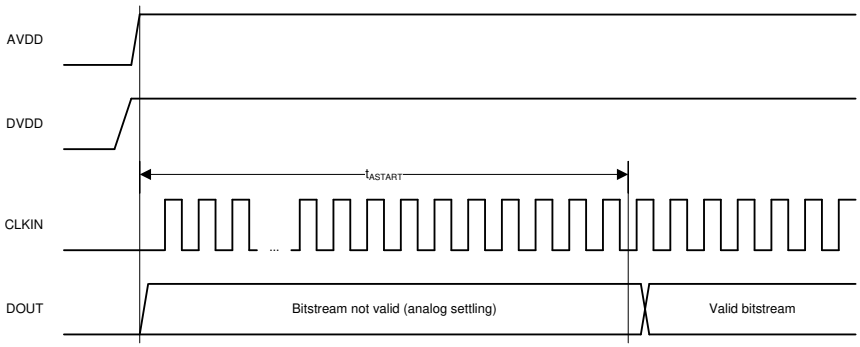


Figure 2. Device Start-Up Timing

6.11 Insulation Characteristics Curves

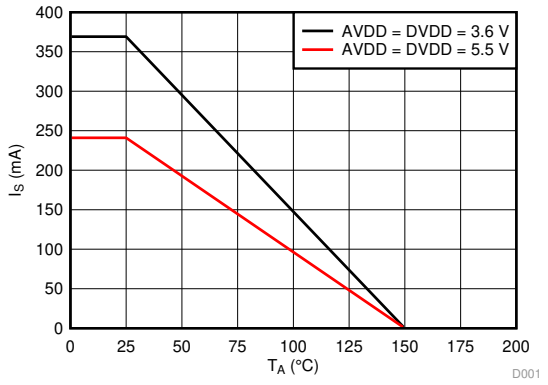


Figure 3. Thermal Derating Curve for Safety-Limiting Current per VDE

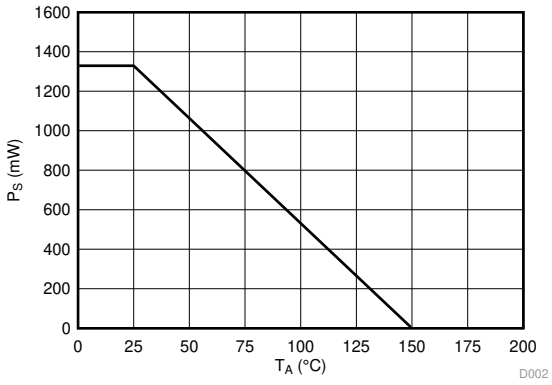
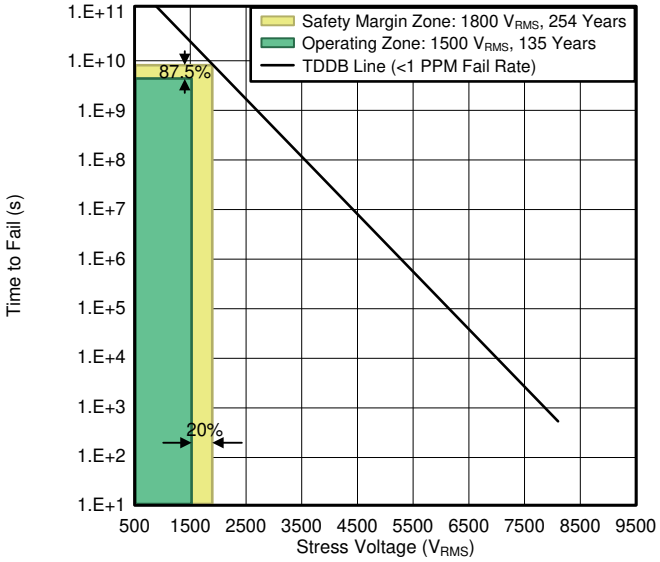


Figure 4. Thermal Derating Curve for Safety-Limiting Power per VDE



T_A up to 150°C, stress-voltage frequency = 60 Hz,
isolation working voltage = 1500 V_{RMS}, operating lifetime = 135 years

Figure 5. Reinforced Isolation Capacitor Lifetime Projection

6.12 Typical Characteristics

at AVDD = 5 V, DVDD = 3.3 V, AINP = –1 V to 1 V, AINN = AGND, f_{CLKIN} = 20 MHz, and sinc^3 filter with OSR = 256 (unless otherwise noted)

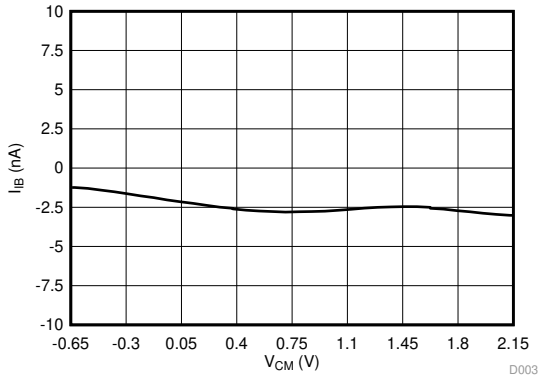


Figure 6. Input Bias Current vs Common-Mode Input Voltage

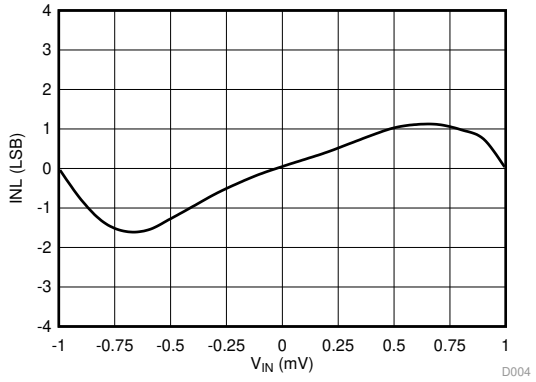


Figure 7. Integral Nonlinearity vs Input Voltage

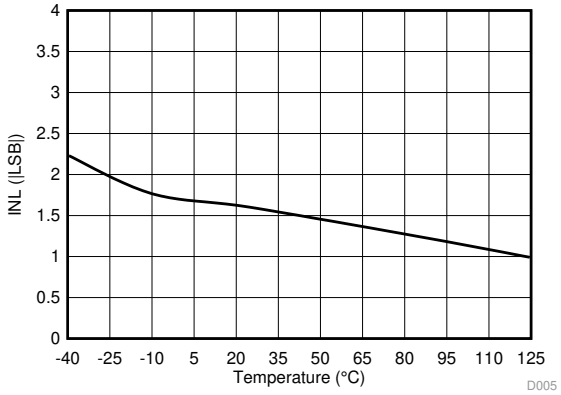


Figure 8. Integral Nonlinearity vs Temperature

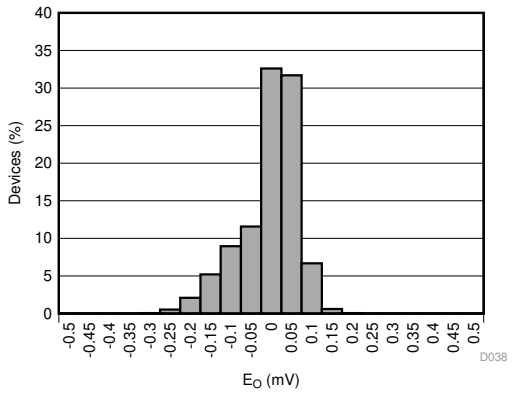


Figure 9. Offset Error Histogram

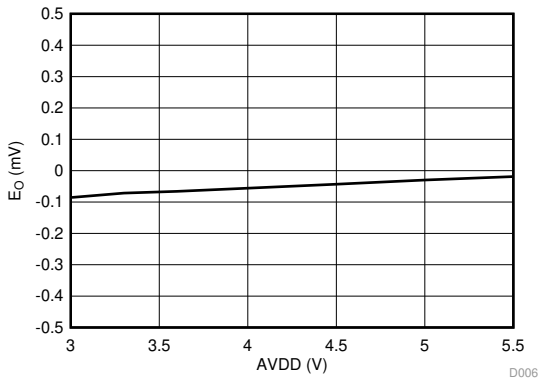


Figure 10. Offset Error vs High-Side Supply Voltage

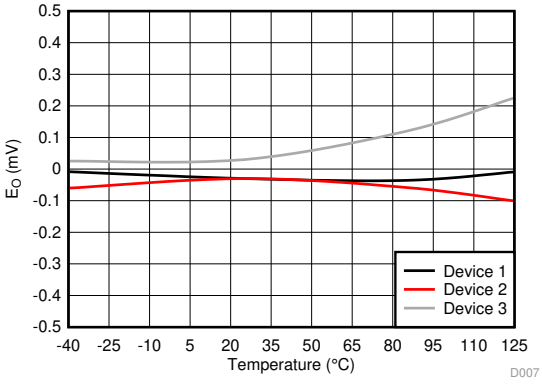
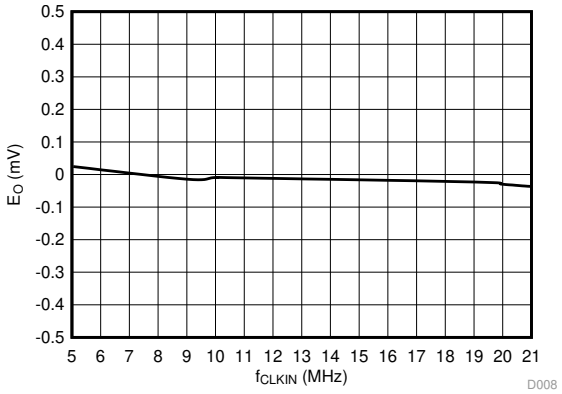


Figure 11. Offset Error vs Temperature

Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, AINP = –1 V to 1 V, AINN = AGND, f_{CLKIN} = 20 MHz, and $sinc^3$ filter with OSR = 256 (unless otherwise noted)



f_{CLKIN} < 9 MHz with AVDD ≥ 4.5 V only

Figure 12. Offset Error vs Clock Frequency

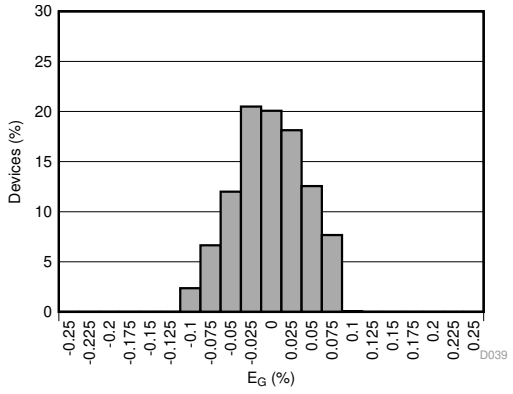


Figure 13. Gain Error Histogram

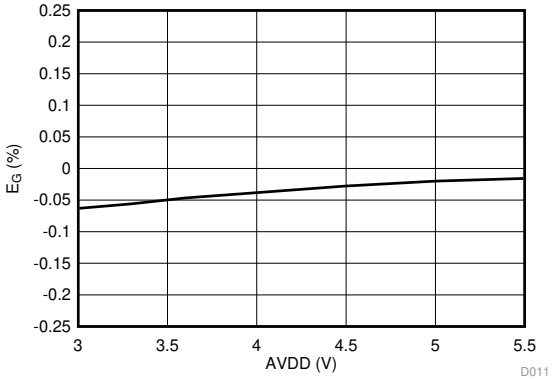


Figure 14. Gain Error vs High-Side Supply Voltage

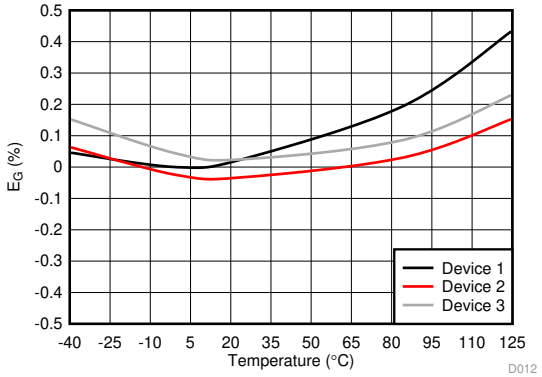
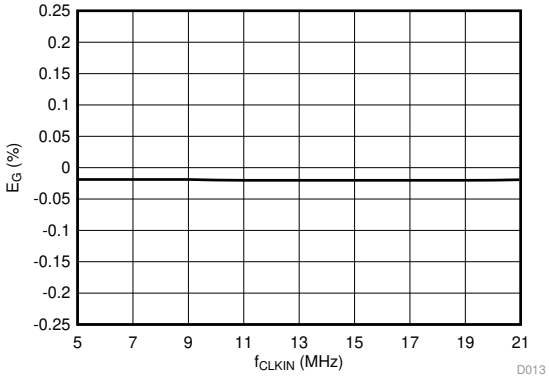


Figure 15. Gain Error vs Temperature



f_{CLKIN} < 9 MHz with AVDD ≥ 4.5 V only

Figure 16. Gain Error vs Clock Frequency

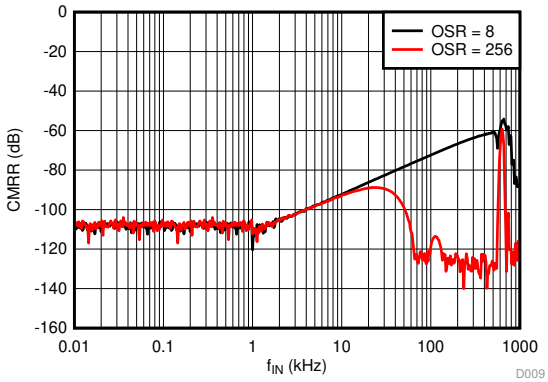


Figure 17. Common-Mode Rejection Ratio vs Input Signal Frequency

Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, AINP = –1 V to 1 V, AINN = AGND, f_{CLKIN} = 20 MHz, and sinc^3 filter with OSR = 256 (unless otherwise noted)

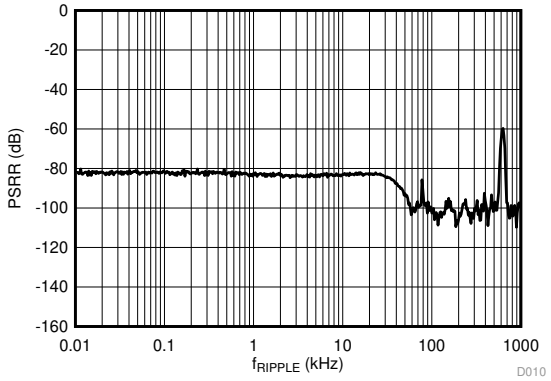


Figure 18. Power-Supply Rejection Ratio vs Ripple Frequency

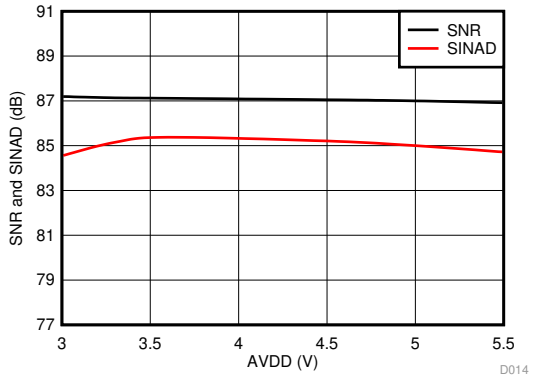


Figure 19. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs High-Side Supply Voltage

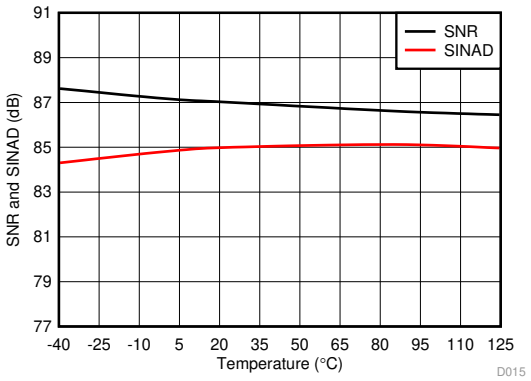
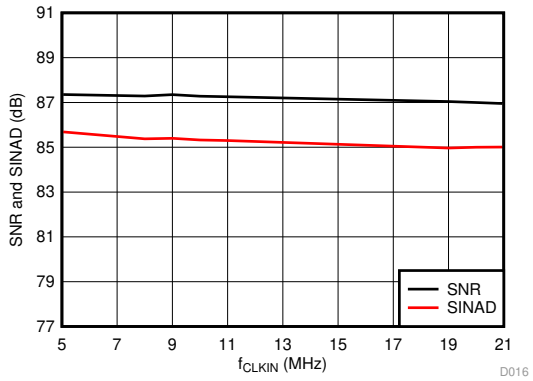


Figure 20. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Temperature



f_{CLKIN} < 9 MHz with AVDD ≥ 4.5 V only

Figure 21. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Clock Frequency

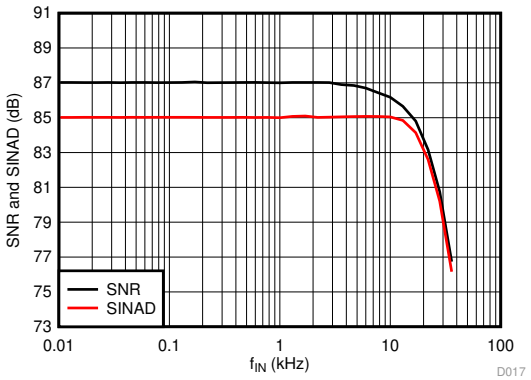


Figure 22. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Input Signal Frequency

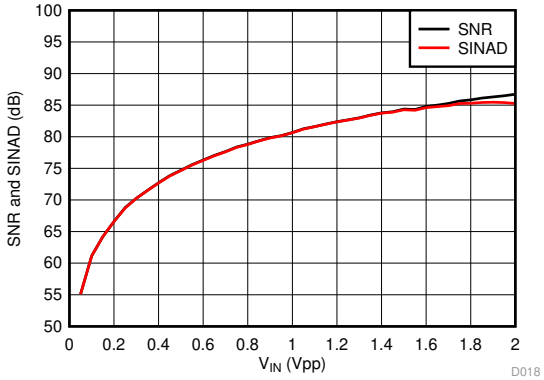


Figure 23. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Input Signal Amplitude

Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, AINP = –1 V to 1 V, AINN = AGND, f_{CLKIN} = 20 MHz, and $sinc^3$ filter with OSR = 256 (unless otherwise noted)

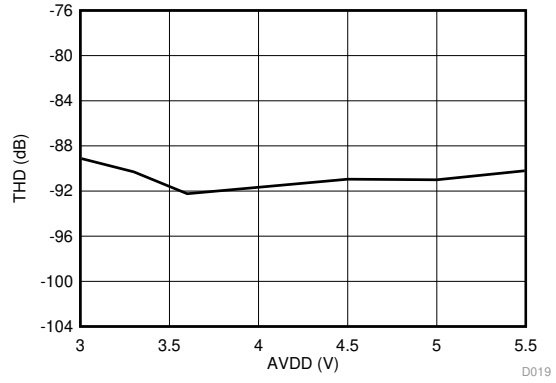


Figure 24. Total Harmonic Distortion vs High-Side Supply Voltage

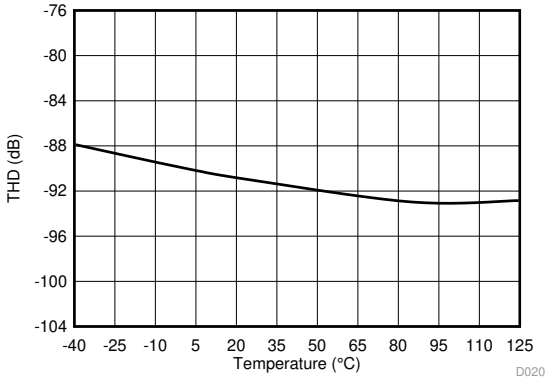
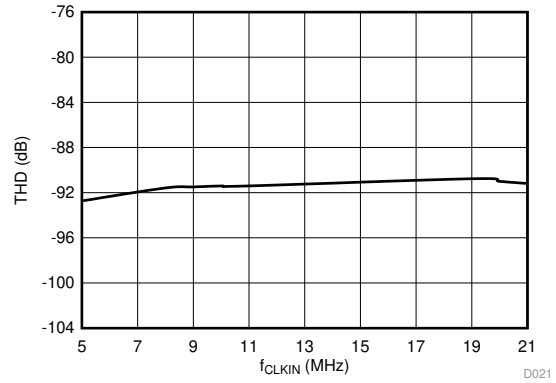


Figure 25. Total Harmonic Distortion vs Temperature



f_{CLKIN} < 9 MHz with AVDD ≥ 4.5 V only

Figure 26. Total Harmonic Distortion vs Clock Frequency

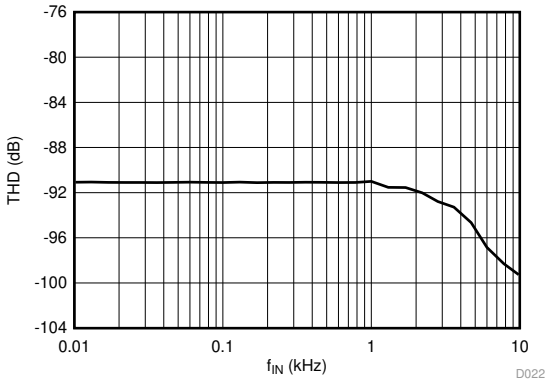


Figure 27. Total Harmonic Distortion vs Input Signal Frequency

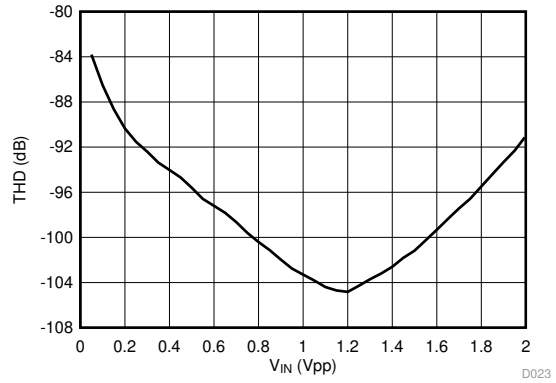


Figure 28. Total Harmonic Distortion vs Input Signal Amplitude

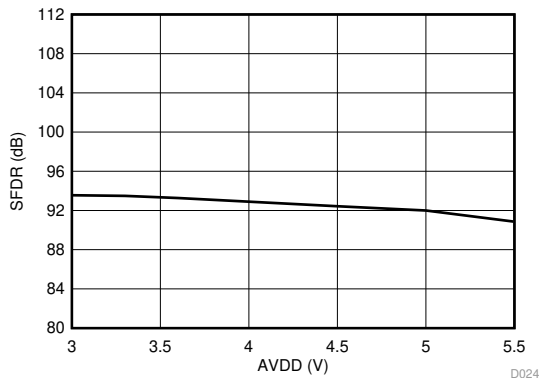


Figure 29. Spurious-Free Dynamic Range vs High-Side Supply Voltage

Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, AINP = –1 V to 1 V, AINN = AGND, f_{CLKIN} = 20 MHz, and sinc^3 filter with OSR = 256 (unless otherwise noted)

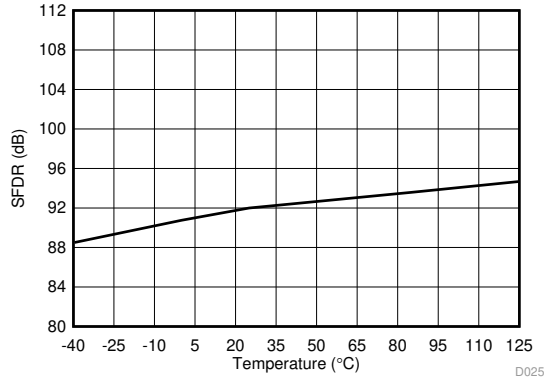
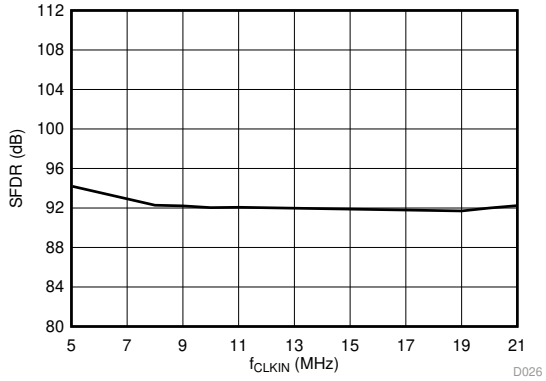


Figure 30. Spurious-Free Dynamic Range vs Temperature



f_{CLKIN} < 9 MHz with AVDD ≥ 4.5 V only

Figure 31. Spurious-Free Dynamic Range vs Clock Frequency

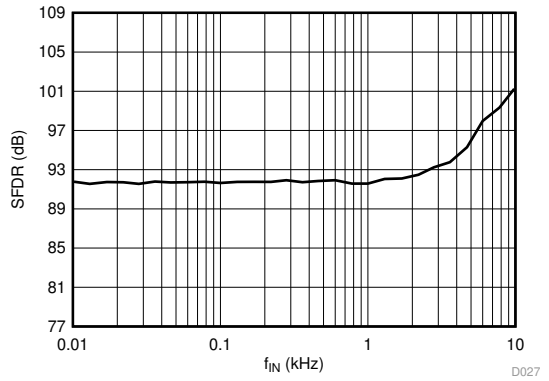


Figure 32. Spurious-Free Dynamic Range vs Input Signal Frequency

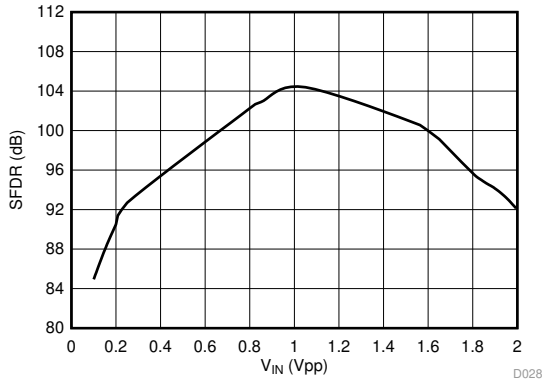
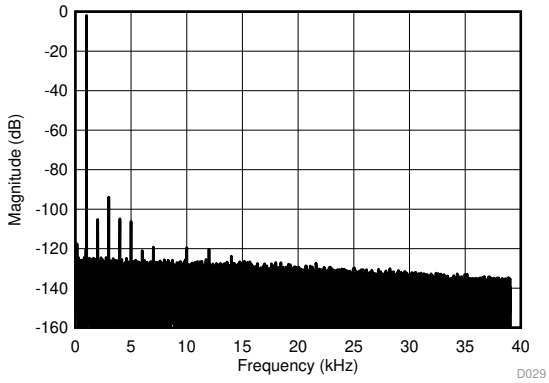
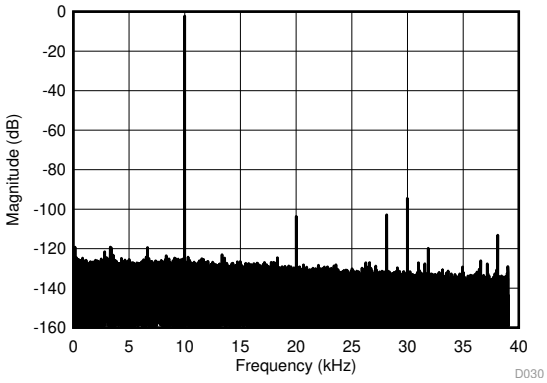


Figure 33. Spurious-Free Dynamic Range vs Input Signal Amplitude



156,250-point DFT, V_{IN} = 2 V_{PP}

Figure 34. Frequency Spectrum with 1-kHz Input Signal



156,250-point DFT, V_{IN} = 2 V_{PP}

Figure 35. Frequency Spectrum with 10-kHz Input Signal

Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, AINP = –1 V to 1 V, AINN = AGND, f_{CLKIN} = 20 MHz, and sinc^3 filter with OSR = 256 (unless otherwise noted)

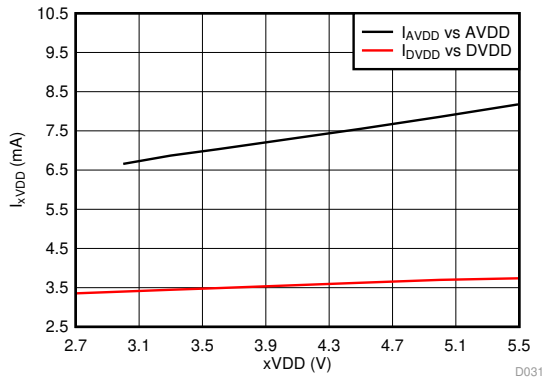


Figure 36. Supply Current vs Supply Voltage

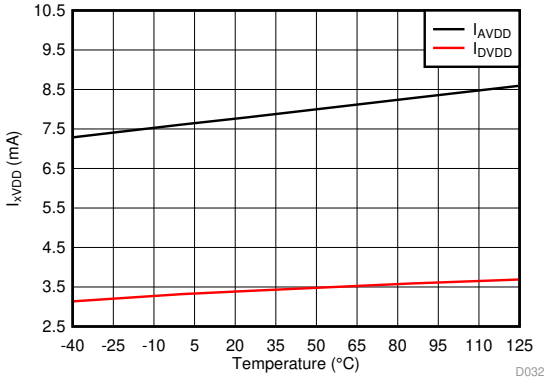
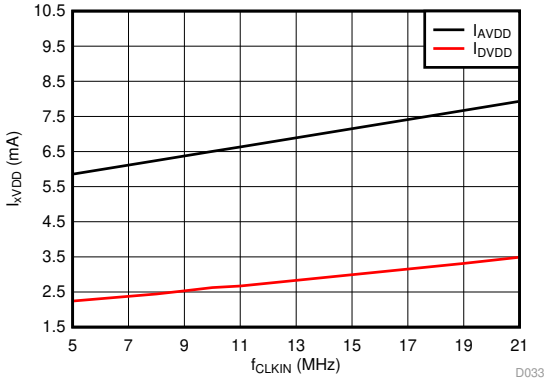


Figure 37. Supply Current vs Temperature



f_{CLKIN} < 9 MHz with AVDD ≥ 4.5 V only

Figure 38. Supply Current vs Clock Frequency

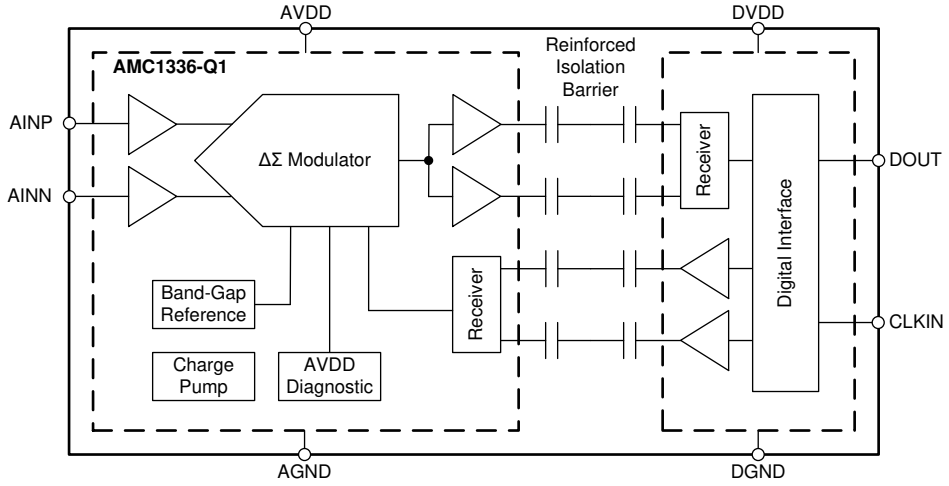
7 Detailed Description

7.1 Overview

The differential analog input (comprised of input signals AINP and AINN) of the AMC1336-Q1 is a chopper-stabilized instrumentation amplifier, followed by the switched-capacitor input of a second-order, delta-sigma (ΔΣ) modulator stage that digitizes the input signal into a 1-bit output stream. The data output DOUT of the converter provides a stream of digital ones and zeros that is synchronous to the externally provided clock source at the CLKIN pin with a frequency in the range of 5 MHz to 21 MHz. The time average of this serial bitstream output is proportional to the analog input voltage. The *Functional Block Diagram* section shows a detailed block diagram of the AMC1336-Q1. The 1.6-GΩ differential input resistance of the analog input stage supports low gain-error signal sensing in high-voltage applications using resistive dividers. The external clock input simplifies the synchronization of multiple current-sensing channels on the system level.

The silicon-dioxide (SiO_2)-based capacitive isolation barrier supports a high level of magnetic field immunity, as described in the *ISO72x Digital Isolator Magnetic-Field Immunity* application report, available for download at www.ti.com.

7.2 Functional Block Diagram

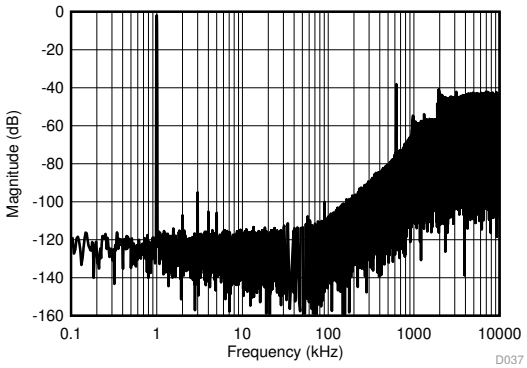


7.3 Feature Description

7.3.1 Analog Input

The AMC1336-Q1 incorporates front-end circuitry that contains an instrumentation amplifier, followed by a ΔΣ modulator. To support a bipolar input range with a unipolar high-side supply AVDD, the device uses a charge pump to simplify the overall system design and minimize circuit cost. For reduced offset and offset drift, the input buffer is chopper-stabilized with the switching frequency set at f_{CLKIN} / 32. Figure 39 illustrates the spur created by the switching frequency.

Feature Description (continued)



$sinc^3$ filter, OSR = 1, f_{CLKIN} = 20 MHz, f_{IN} = 1 kHz

Figure 39. Quantization Noise Shaping

The linearity and noise performance of the device are ensured only when the differential analog input voltage remains within the specified linear full-scale range (FSR), that is ±1 V, and within the specified input common-mode range.

Figure 40 shows the specified common-mode input voltage that applies for the full-scale input voltage range as specified in this document.

If smaller input signals are used, the operational common-mode input voltage range widens. Figure 41 shows the common-mode input voltage that applies with no differential input signal; that is, when the voltage applied on AINP is equal to the voltage applied on AINN. The common-mode input voltage range scales with the actual differential input voltage between this range and the range in Figure 40.

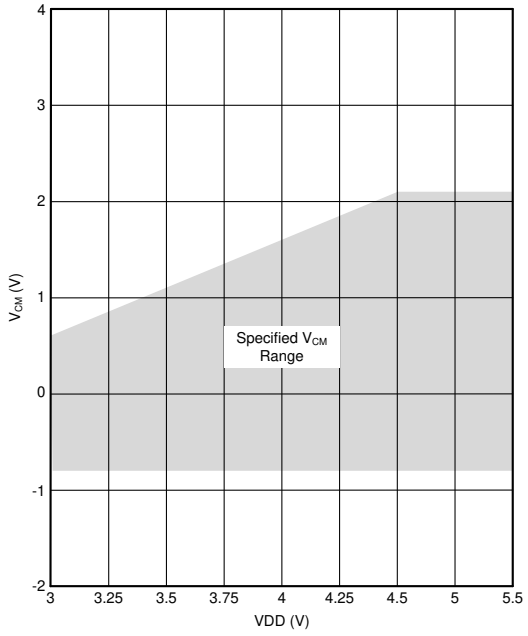


Figure 40. Common-Mode Input Voltage Range With a Clipping Differential Input Signal of ±1.25 V

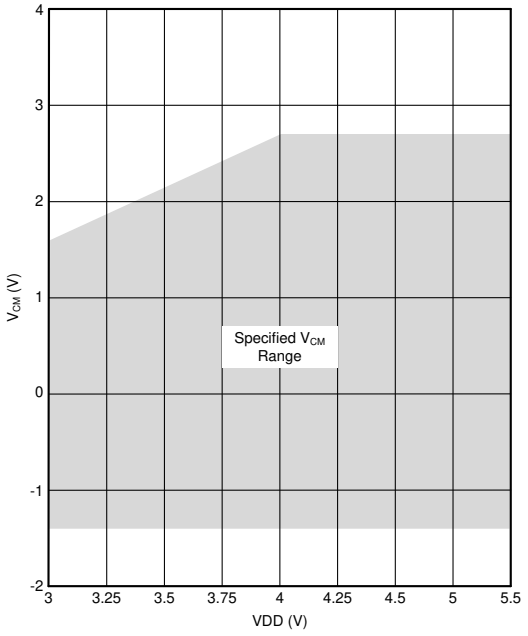


Figure 41. Common-Mode Input Voltage Range With a Zero Differential Input Signal

Feature Description (continued)

There are two restrictions on the analog input signals (AINP and AINN). First, if the input voltage exceeds the range AGND – 5 V to AVDD + 0.5 V, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on. In addition, the linearity and noise performance of the device are ensured only when the differential analog input voltage remains within the specified linear full-scale range (FSR) and within the specified input common-mode range.

7.3.2 Modulator

The modulator implemented in the AMC1336-Q1, as conceptualized in Figure 42, is a second-order, switched-capacitor, feed-forward ΔΣ modulator. The analog input voltage V_{IN} and the output V_5 of the 1-bit digital-to-analog converter (DAC) are subtracted, providing an analog voltage V_1 at the input of the first integrator stage. The output of the first integrator feeds the input of the second integrator stage, resulting in an output voltage V_3 that is differentiated with the input signal V_{IN} and the output of the first integrator V_2. Depending on the polarity of the resulting voltage V_4, the output of the comparator is changed. In this case, the 1-bit DAC responds on the next clock pulse by changing the associated analog output voltage V_5, causing the integrators to progress in the opposite direction and forcing the value of the integrator output to track the average value of the input.

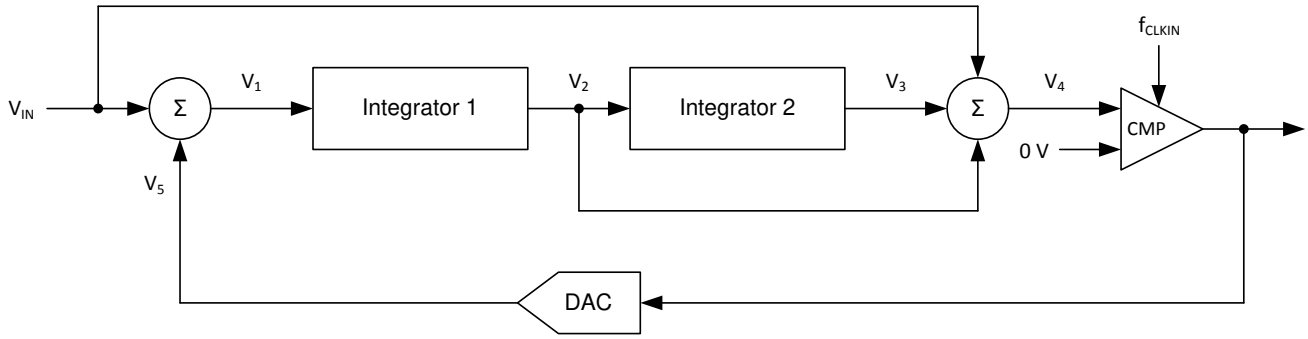


Figure 42. Block Diagram of a Second-Order Modulator

As depicted in Figure 39, the modulator shifts the quantization noise to high frequencies. Therefore, use a low-pass digital filter at the output of the device to increase the overall performance. This filter is also used to convert from the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation). TI's microcontroller families TMS320F2807x and TMS320F2837x offer a suitable programmable, hardwired filter structure termed a *sigma-delta filter module* (SDFM) optimized for usage with the AMC1336-Q1. Furthermore, the SD24_B converters on the MSP430F677x microcontrollers offer a path to directly access the integrated sinc filters for a simple system-level solution for multichannel, isolated current sensing. Alternatively, a field-programmable gate array (FPGA) can be used to implement the filter.

Feature Description (continued)

7.3.3 Isolation Channel Signal Transmission

The AMC1336-Q1 uses an on-off keying (OOK) modulation scheme to transmit the modulator output bitstream across the capacitive SiO_2-based isolation barrier. The transmitter modulates the bitstream at TX IN in Figure 43 with an internally-generated, 480-MHz carrier across the isolation barrier to represent a digital *one* and sends a *no signal* to represent the digital *zero*. The receiver demodulates the signal after advanced signal conditioning and produces the output. The symmetrical design of each isolation channel improves the common-mode transient immunity (CMTI) performance and reduces the radiated emissions caused by the high-frequency carrier. Figure 43 shows the block diagram of an isolation channel integrated in the AMC1336-Q1.

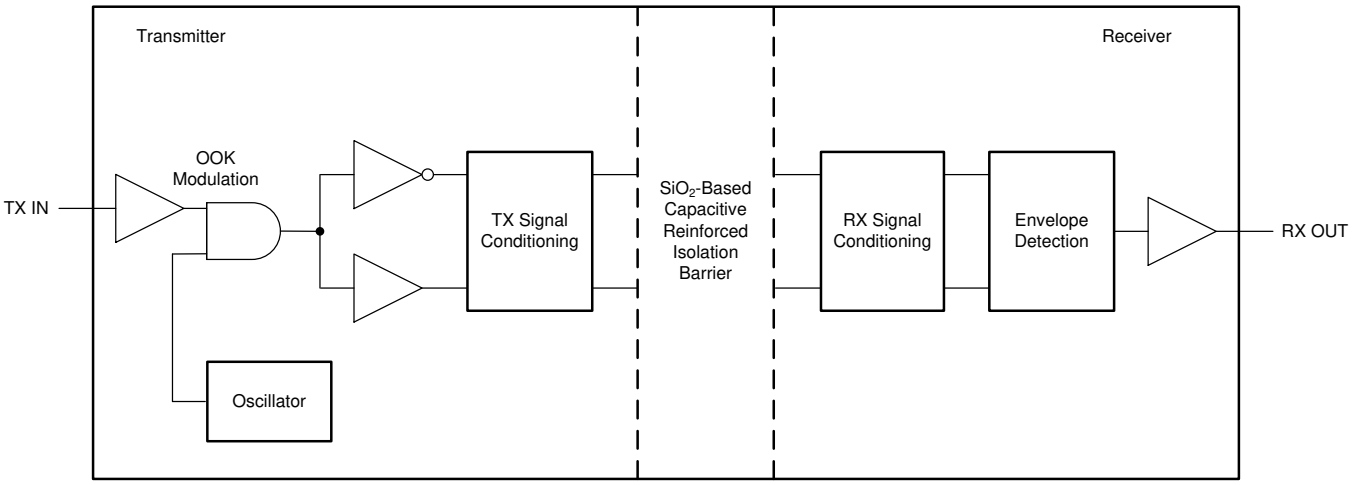


Figure 43. Block Diagram of an Isolation Channel

Figure 44 shows the concept of the on-off keying scheme.

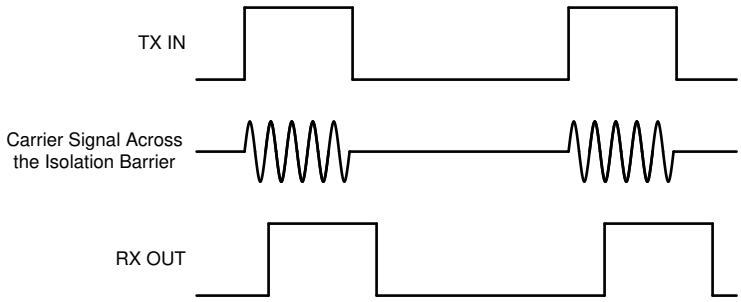


Figure 44. OOK-Based Modulation Scheme

Feature Description (continued)

7.3.4 Clock Input

The AMC1336-Q1 system clock is provided externally at the CLKIN pin. The clock signal must be applied continuously for proper device operation.

To support the bipolar input voltage range with a unipolar high-side supply AVDD, the AMC1336-Q1 includes a charge pump. This charge pump stops operating if the clock signal is below the specified frequency range or if the signal is paused or missing. In that case, the input bias current increases beyond the specified range and significantly reduces the input resistance of the device. When the clock signal is paused or missing, the modulator stops the analog signal conversion and the digital output signal remains frozen in the last logic state. When the clock signal is applied again after a pause, the internal analog circuitry biasing must settle for proper device performance. In this case, consider the t_{ASTART} specification in the *Switching Characteristics* table.

7.3.5 Digital Output

A differential input signal of 0 V ideally produces a stream of ones and zeros that are high 50% of the time. A differential input of 1 V produces a stream of ones and zeros that are high 90% of the time. With 16 bits of resolution, that percentage ideally corresponds to code 58982 (an unsigned code). A differential input of –1 V produces a stream of ones and zeros that are high 10% of the time and ideally results in code 6553 with 16-bit resolution. These input voltages are also the specified linear range of the AMC1336-Q1 with performance as specified in this document. If the input voltage value exceeds this range, the output of the modulator shows nonlinear behavior when the quantization noise increases. The output of the modulator clips with a stream of only zeros with an input less than or equal to –1.25 V or with a stream of only ones with an input greater than or equal to 1.25 V. In this case, however, the AMC1336-Q1 generates a single 1 (if the input is at negative full-scale) or 0 every 128 clock cycles to indicate proper device function (see the *AVDD Diagnostics and Fail-Safe Output* section for more details). Figure 45 shows the input voltage versus the output modulator signal.

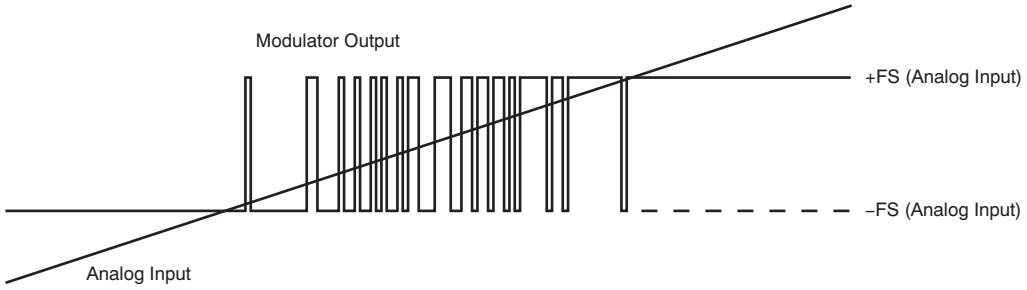


Figure 45. Analog Input versus the AMC1336-Q1 Modulator Output

Equation 1 calculates the density of ones in the output bitstream for any input voltage value (with the exception of a full-scale input signal, as described in the *Output Behavior in Case of a Full-Scale Input* section):

$$\frac{V_{IN} + V_{Clipping}}{2 \times V_{Clipping}} \quad (1)$$

The modulator bitstream on the DOUT pin changes with the rising edge of the clock signal applied on the CLKIN pin. Use the rising edge of the clock to latch the modulator bitstream at the input of the digital filter device.

Feature Description (continued)

The AMC1336-Q1 features a slew-rate-controlled output stage that reduces the over- and undershoots of the output amplitude and radiated emissions of the DOUT line in the system. Figure 46 and Figure 47 show examples of rising and falling edges of DOUT with different capacitive loads.

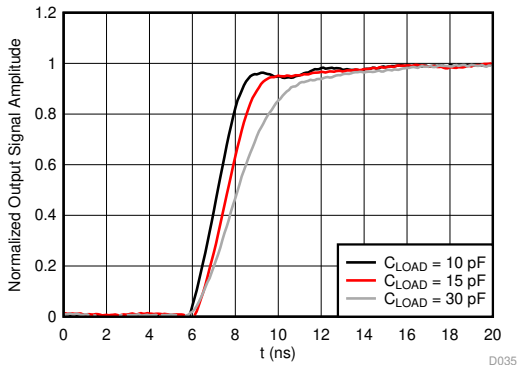


Figure 46. DOUT Rising Edge With Different Capacitive Loads

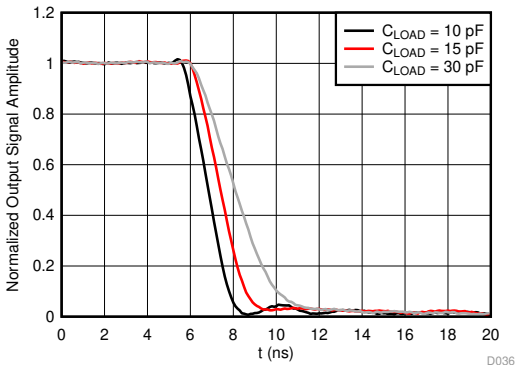


Figure 47. DOUT Falling Edge With Different Capacitive Loads

7.4 Device Functional Modes

The AMC1336-Q1 is operational when the power supplies AVDD and DVDD, and the clock signal CLKIN are applied, as specified in the *Recommended Operating Conditions* and *Switching Characteristics* tables.

7.4.1 Output Behavior in Case of a Full-Scale Input

Figure 48 shows that if a full-scale input signal is applied to the AMC1336-Q1 (that is, $V_{IN} \geq V_{Clipping}$), the device generates a single one or zero every 128 bits at DOUT, depending on the actual polarity of the signal being sensed. This feature can be used for advanced system-level diagnostics to differentiate between system failures caused by missing high-side supply AVDD or input overvoltage events.

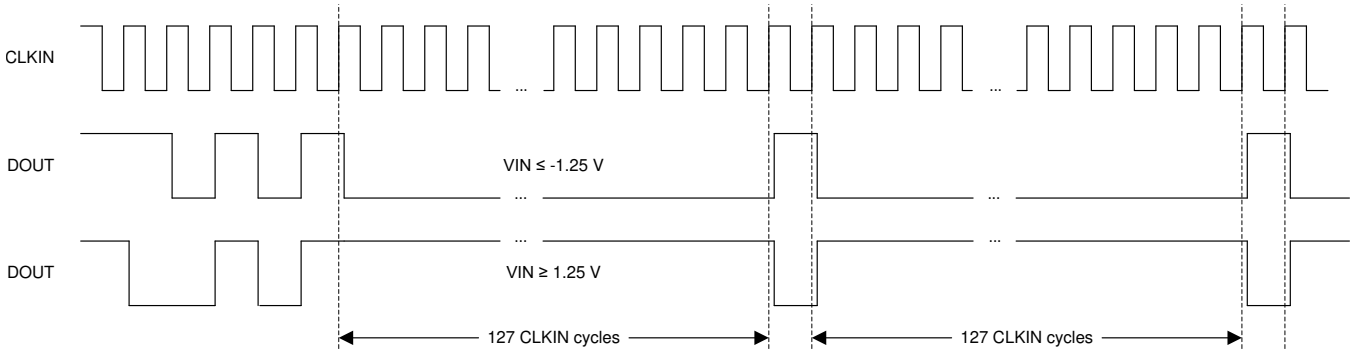


Figure 48. Out-of-Range Output of the AMC1336-Q1

7.4.2 AVDD Diagnostics and Fail-Safe Output

In the case of a missing high-side supply voltage AVDD, the output of a ΔΣ modulator is not defined and can cause a system malfunction. In systems with high safety requirements, this behavior is not acceptable. As shown in Figure 49, the AMC1336-Q1 implements an AVDD diagnostics and fail-safe output function that ensures that the output DOUT of the device offers a steady-state bitstream of logic 0's in case of a missing AVDD. Sample at least 128 CLKIN cycles in order to distinguish a missing AVDD condition from an input underrange condition.

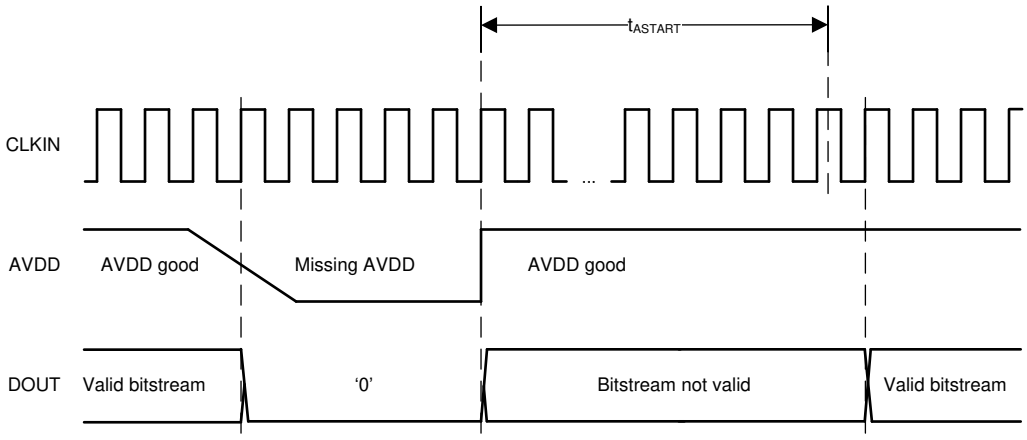


Figure 49. Fail-Safe Output of the AMC1336-Q1

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Digital Filter Usage

The modulator generates a bitstream that is processed by a digital filter to obtain a digital word similar to a conversion result of a conventional analog-to-digital converter (ADC). Equation 2 shows a $sinc^3$-type filter, which is a very simple filter that is built with minimal effort and hardware:

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}} \right)^3 \tag{2}$$

This filter provides the best output performance at the lowest hardware size (count of digital gates) for a second-order modulator. All the characterization in this document is also done with a $sinc^3$ filter with an oversampling ratio (OSR) of 256 and an output word width of 16 bits.

An example code for implementing a $sinc^3$ filter in an FPGA is discussed in the *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications* application note, available for download at www.ti.com.

8.2 Typical Application

Isolated ΔΣ modulators are widely used in onboard charger (OBC) and traction inverter designs because of their high AC and DC performance. The input structure of the AMC1336-Q1 is optimized for use with high-impedance resistor dividers. The ±1-V, differential input enables sensing of positive and negative voltages in the system.

Figure 50 shows a simplified schematic of a traction inverter application with the AMC1336-Q1 used for output phase voltage sensing. In this example, the ground reference point for the microcontroller is not connected by any means to the power stage. This configuration is usually the case in systems with the microcontroller located on a dedicated control card or PCB.

Current feedback is performed with shunt resistors (R_{SHUNT}) and TI's AMC1305M05-Q1 isolated modulators. Depending on the system design, either all three or only two motor phase currents are sensed.

Depending on the overall digital processing power requirements and with a total of eight ΔΣ modulator bitstreams to be processed by the microcontroller (MCU), a derivate from either the low-cost single-core TMS320F2807x or the dual-core TMS320F2837x families can be used in this application.

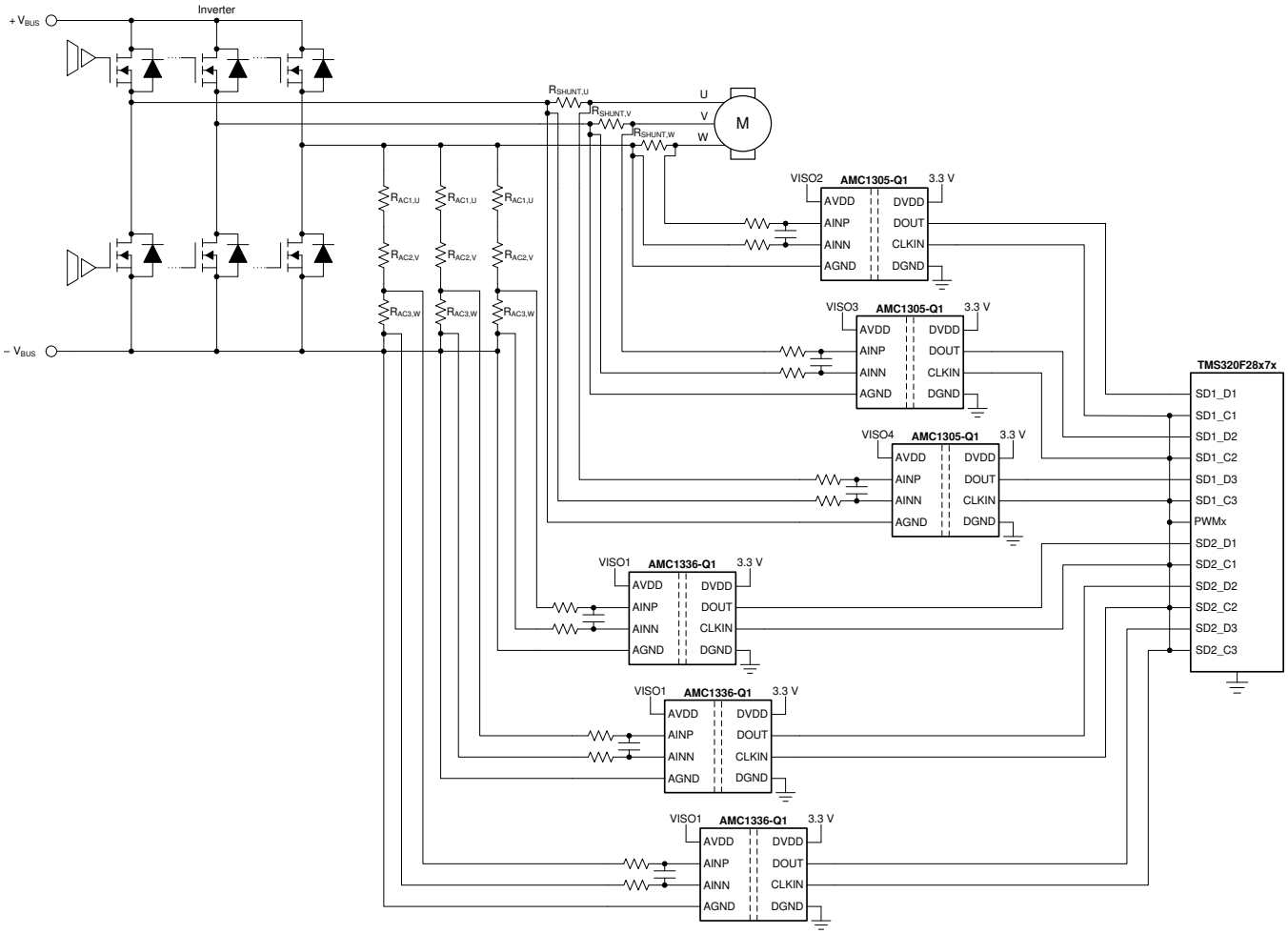


Figure 50. The AMC1336-Q1 in a Frequency Inverter Application

Typical Application (continued)

Figure 51 shows an additional example of the AMC1336-Q1 used for DC-link and V_{BUS} voltage sensing in an onboard charger. Also in this case, the microcontroller is located on a dedicated control card and the AMC1305M05-Q1 is used for shunt-based current sensing.

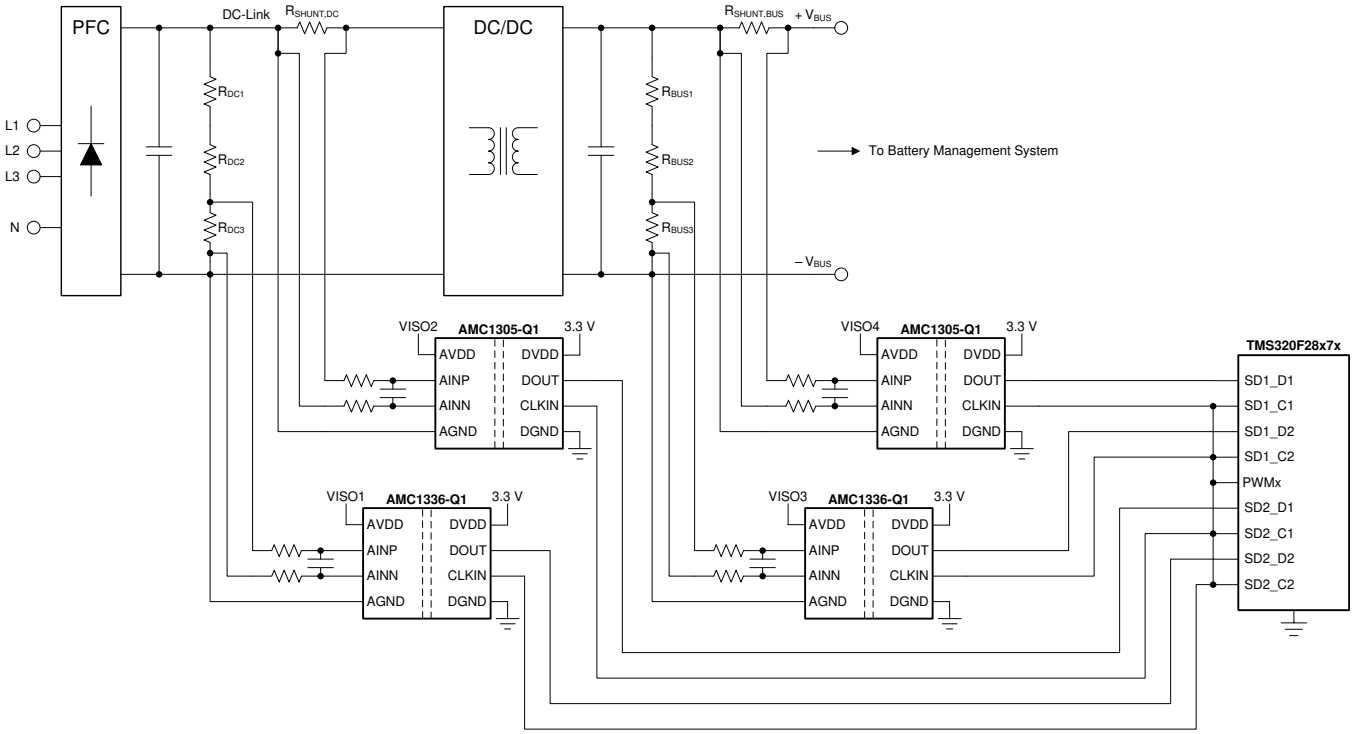


Figure 51. The in an On-Board Charger Application

Typical Application (continued)

8.2.1 Design Requirements

Table 1 lists the parameters for this typical application.

Table 1. Design Requirements

PARAMETER	VALUE
Supply voltage	3.3 V
Voltage drop across the sensing resistor R_{DC1} for a linear response	1 V (maximum)
Voltage drop across the sensing resistors R_{AC3} for a linear response	±1 V (maximum)
Current through the sensing resistors R_{ACx}	±100 µA (maximum)

8.2.2 Detailed Design Procedure

Use Ohm's Law to calculate the minimum total resistance of the resistive dividers to limit the cross current to the desired values:

- For the voltage sensing on the DC bus: $R_{DC1} + R_{DC2} + R_{DC3} = V_{BUS} / I_{DC}$
- For the voltage sensing on the output phases U, V, and W: $R_{AC1} + R_{AC2} + R_{AC3} = V_{PHASE\ (max)} / I_{AC}$

Consider the following two restrictions to choose the proper value of the resistors R_{DC3} and R_{AC3}:

- The voltage drop caused by the nominal voltage range of the system must not exceed the recommended input voltage range for a linear response of the AMC1336-Q1: $V_{xC3} \leq V_{FSR}$
- The voltage drop caused by the maximum allowed system overvoltage must not exceed the input voltage that causes a clipping output: $V_{xC3} \leq V_{Clipping}$

Use similar approach for calculation of the shunt resistor values R_{SHUNT} and see the AMC1305M05-Q1 for further details.

Table 2 lists examples of nominal E96-series (1% accuracy) resistor values for systems using 600 V and 800 V on the DC bus.

Table 2. Resistor Value Examples for DC Bus Sensing

PARAMETER	600-V DC BUS	800-V DC BUS
Resistive divider resistor R_{DC1}	3.01 MΩ	4.22 MΩ
Resistive divider resistor R_{DC2}	3.01 MΩ	4.22 MΩ
Sense resistor R_{DC3}	10 kΩ	10.5 kΩ
Resulting current through resistive divider I_{DC}	99.5 µA	94.7 µA
Resulting voltage drop on sense resistor V_{RDC3}	0.995 V	0.994 V

Table 3 lists examples of nominal E96-series (1% accuracy) resistor values for systems using 230 V and 690 V on the input or output phases.

Table 3. Resistor Value Examples for Phase Voltage Sensing

PARAMETER	±400-V_{AC} PHASE	±690-V_{AC} PHASE
Resistive divider resistor R_{AC1}	2.0 MΩ	3.48 MΩ
Resistive divider resistor R_{AC2}	2.0 MΩ	3.48 MΩ
Sense resistor R_{AC3}	10.0 kΩ	10.0 kΩ
Resulting current through resistive divider I_{AC}	99.8 µA	99.0 µA
Resulting voltage drop on sense resistor V_{RAC3}	±0.998 V	±0.990 V

Use a power supply with a nominal voltage of 3.3 V for DVDD to directly connect all modulators to the microcontroller.

For modulator output bitstream filtering, a device from TI's TMS320F2807x family of low-cost microcontrollers (MCUs) or TMS320F2837x family of dual-core MCUs is recommended. These MCU families support up to eight channels of dedicated hardwired filter structures called sigma-delta filter modules (SDFMs) that significantly simplify system level design by offering two filtering paths per channel: one providing high accuracy results for the control loop and one that offers a fast response path for overcurrent detection. Use one of the pulse-width modulation (PWM) sources inside the MCU to generate the clock for the modulators and for easy synchronization of all feedback signals and the switching control of the gate drivers.

8.2.3 Input Filter Design

TI recommends placing an RC filter in front of a ΔΣ modulator to improve signal-to-noise performance of the signal path. Design the input filter such that:

- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency of the ΔΣ modulator
- The DC impedance of the filter does not generate significant voltage drop in the analog input lines
- The source impedance of the analog inputs are equal

For most applications, the structure shown in Figure 52 achieves excellent performance.

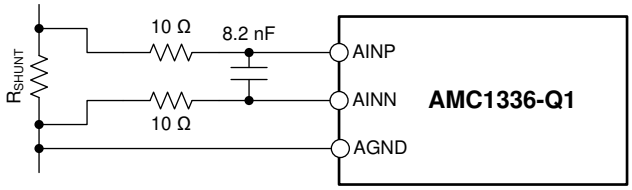


Figure 52. Differential Input Filter

8.2.4 Application Curve

The effective number of bits (ENOB) is often used to compare the performance of ADCs and ΔΣ modulators. Figure 53 shows the ENOB of the AMC1336-Q1 with different oversampling ratios. In this document, this number is calculated from the SINAD by using following equation: SINAD = 1.76 dB + 6.02 × ENOB.

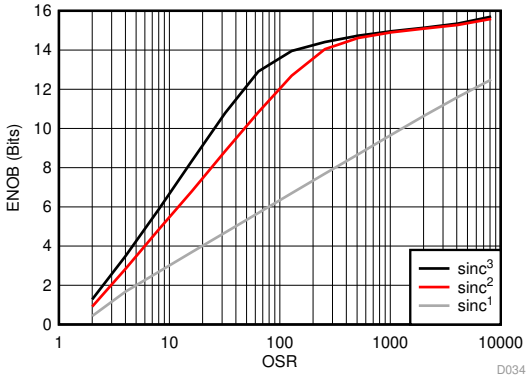


Figure 53. Measured Effective Number of Bits versus Oversampling Ratio

8.2.5 What to Do and What Not to Do

Do not leave the inputs of the AMC1336-Q1 unconnected (floating) when the device is powered up. If either modulator input is left floating, the input bias current can drive this input beyond the specified common-mode input voltage range. If both inputs are beyond that range, the gain of the front-end diminishes and the output bitstream is not valid.

9 Power Supply Recommendations

In a typical frequency-inverter application, the high-side power supply (AVDD) for the AMC1336-Q1 is generated from the controller-side supply (DVDD) of the device by an isolated dc/dc converter circuit. Figure 54 shows a low-cost solution based on the push-pull driver SN6501 and a transformer that supports the desired isolation voltage ratings. TI recommends using a low-ESR decoupling capacitor of 0.1 µF and an additional capacitor of minimum 1 µF for both supplies of the AMC1336-Q1. Place these decoupling capacitors as close as possible to the device power-supply pins to minimize supply current loops and electromagnetic emissions.

The AMC1336-Q1 does not require any specific power up sequencing. Consider the analog settling time t_{ASTART} as specified in the *Switching Characteristics* table after ramp up of the AVDD high-side supply.

Connect the high-side ground pin AGND of the AMC1336-Q1 to one of the analog inputs AINx to avoid common-mode input voltage range violations.

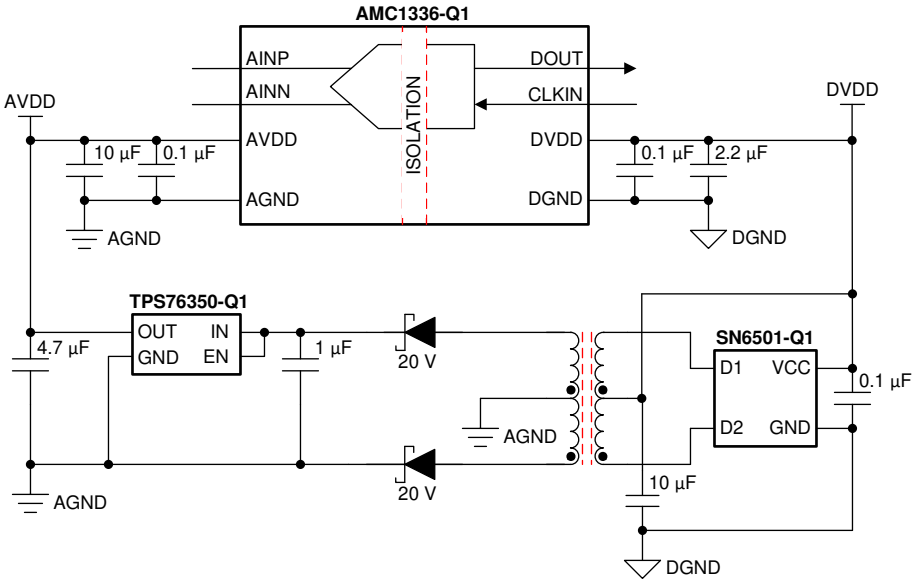


Figure 54. Decoupling the AMC1336-Q1

10 Layout

10.1 Layout Guidelines

Figure 55 shows an example layout that is used on the AMC1336-Q1 evaluation module. For best performance, place the smaller 0.1-µF decoupling capacitors (C7 and C9) as close as possible to the AMC1336-Q1 power-supply pins, followed by the additional C1 and C11 capacitors with a minimum value of 1 µF. The resistors and capacitors used for the analog input filter (R1, R2, C4, C5, and C8) are placed next to the decoupling capacitors. Use 1206-size, SMD-type, ceramic decoupling capacitors and route the traces to the AINx pins underneath. Connect the supply voltage sources in a way that allows the supply current to flow through the pads of the decoupling capacitors before powering the device.

Consider use of RC filters on the digital clock and data lines to reduce reflections and slew rate that cause radiated emissions. The AMC1336-Q1 evaluation module offers placeholders for RC filters (termed R8 and C13 in Figure 55) for the CLKIN line, and R7 and C12 for the DOUT line.

10.2 Layout Example

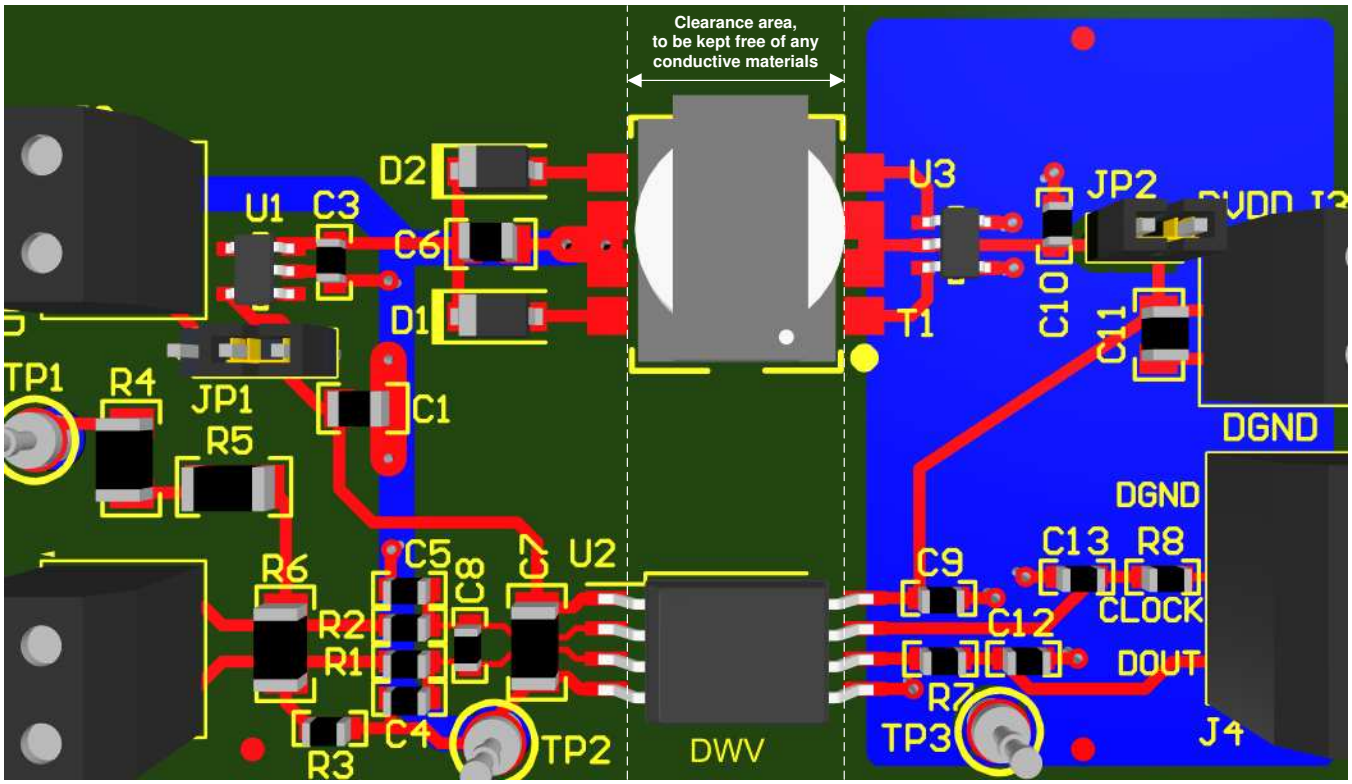


Figure 55. Recommended Layout of the AMC1336-Q1

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

11.1.1.1 Isolation Glossary

See the *Isolation Glossary*

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TMS320F28004x Piccolo™ Microcontrollers* data sheet
- Texas Instruments, *TMS320F2807x Piccolo™ Microcontrollers* data sheet
- Texas Instruments, *TMS320F2837xD Dual-Core Delfino™ Microcontrollers* data sheet
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity*
- Texas Instruments, *MSP430F677x Polyphase Metering SoCs* data sheet
- Texas Instruments, *AMC1210 Quad Digital Filter for 2nd-Order Delta-Sigma Modulator* data sheet
- Texas Instruments, *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications* application report
- Texas Instruments, *AMC1306x Small, High-Precision, Reinforced Isolated Delta-Sigma Modulators With High CMTI* data sheet
- Texas Instruments, *CDCLVC11xx 3.3-V and 2.5-V LVCMOS High-Performance Clock Buffer Family* data sheet
- Texas Instruments, *SN6501 ransformer Driver for Isolated Power Supplies* data sheet
- Texas Instruments, *AMC1303, AMC1306, and AMC1336 Evaluation Module* user's guide

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.5 Trademarks

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AMC1336QDWVRQ1	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1336Q
AMC1336QDWVRQ1.A	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1336Q
AMC1336QDWVRQ1.B	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1336Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF AMC1336-Q1 :

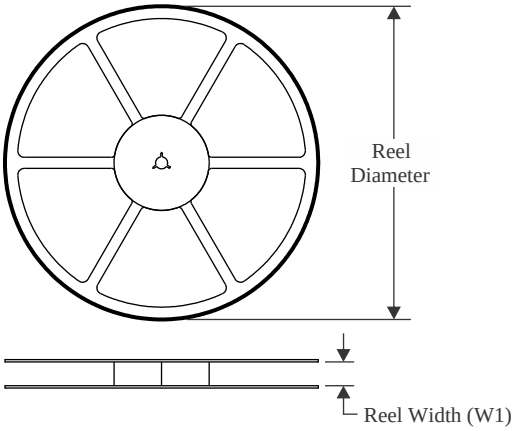
- Catalog : AMC1336

NOTE: Qualified Version Definitions:

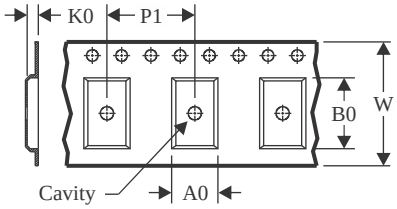
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

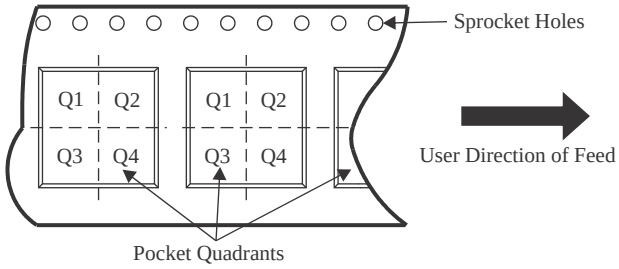


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

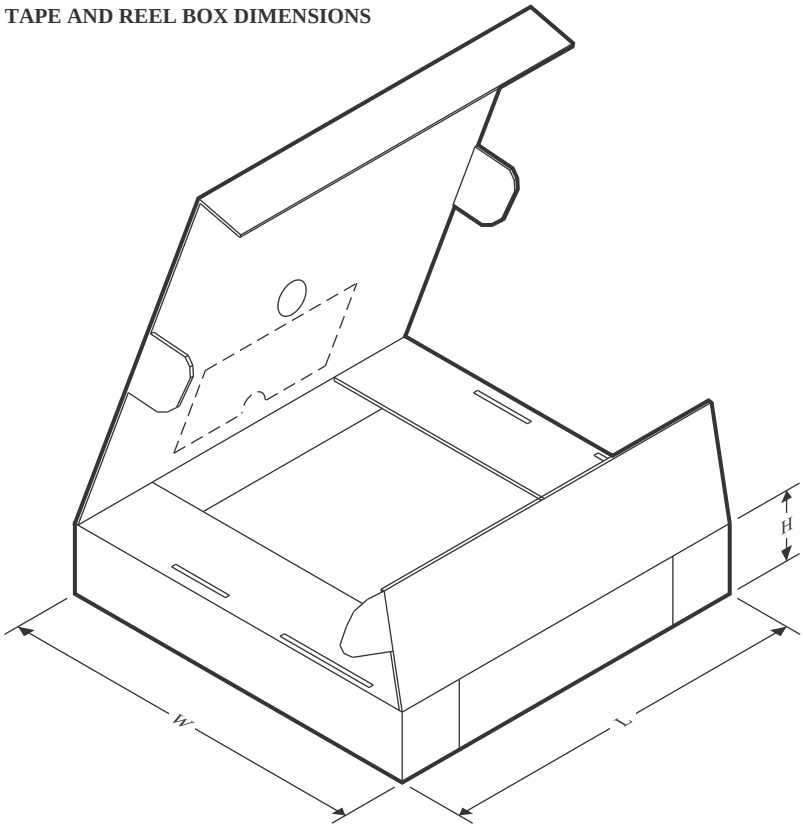
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

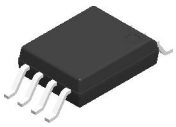
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1336QDWVRQ1	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

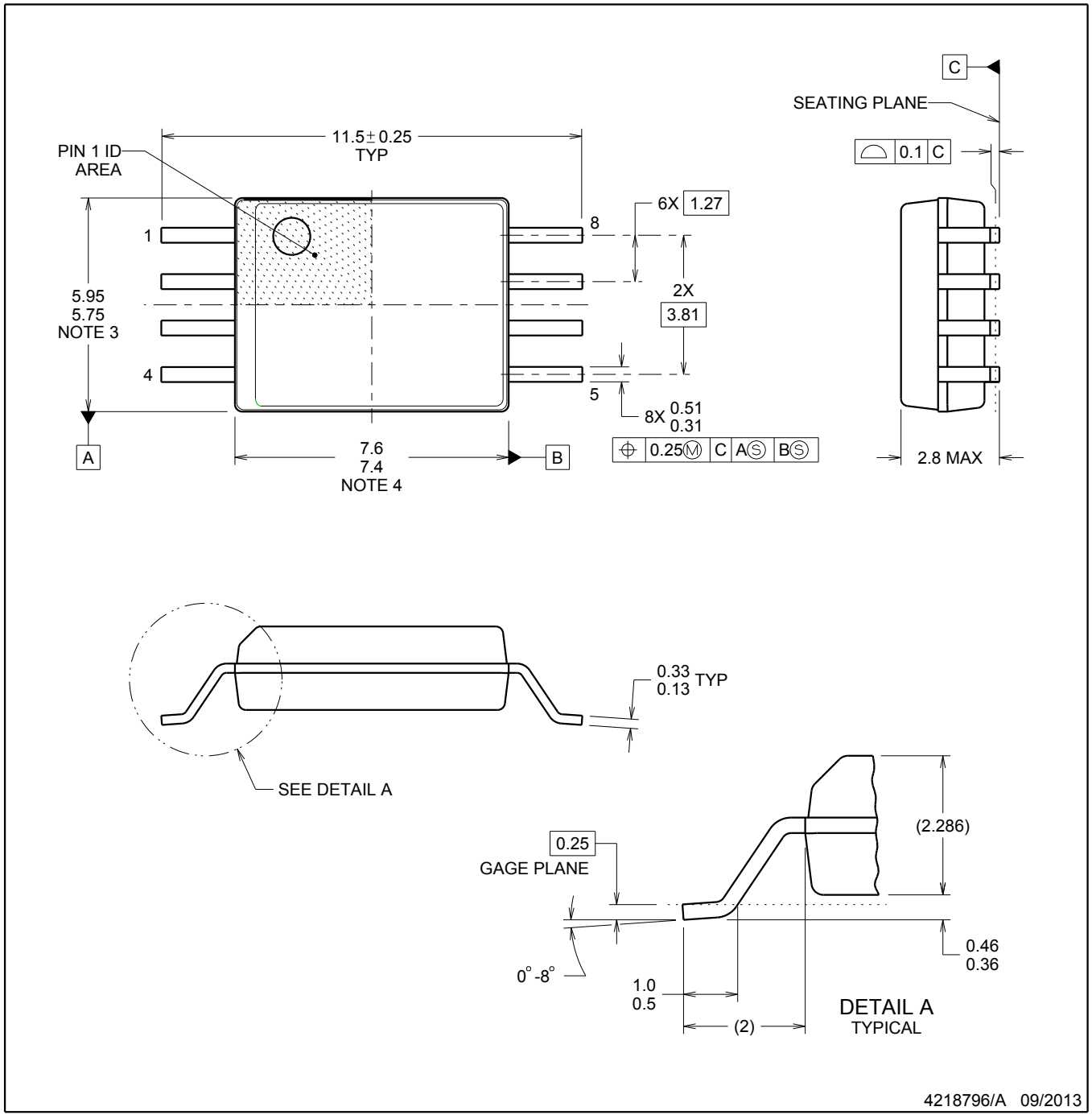
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1336QDWVRQ1	SOIC	DWV	8	1000	350.0	350.0	43.0



DWV0008A

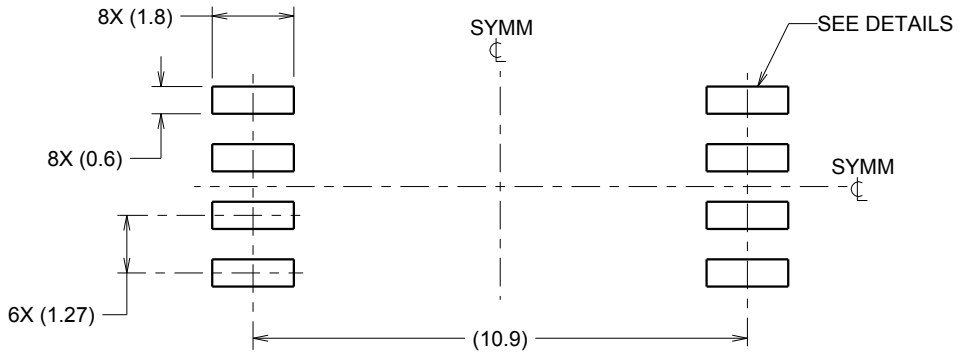
SOIC - 2.8 mm max height

SOIC

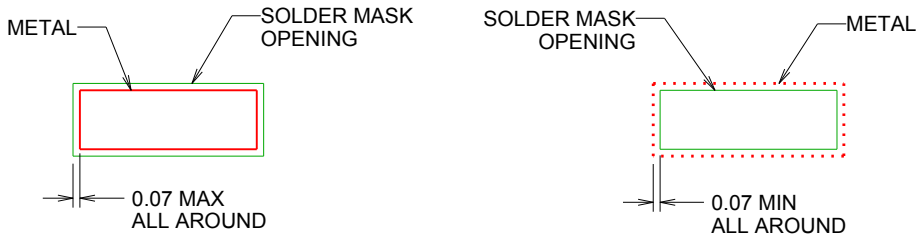


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



SOLDER MASK DETAILS

4218796/A 09/2013

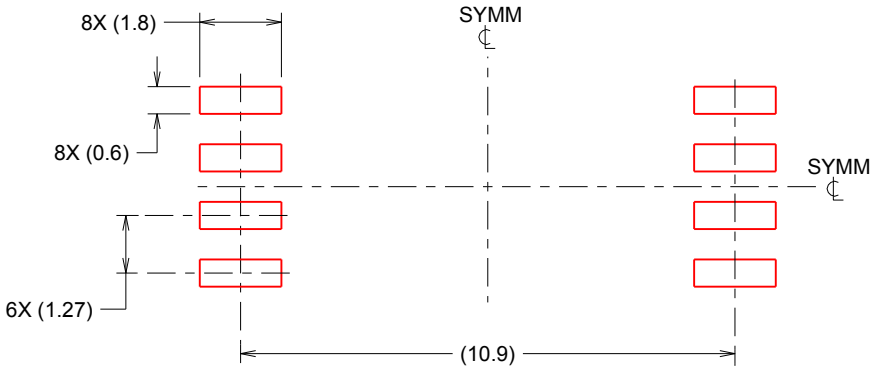
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DWV0008A

SOIC - 2.8 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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