LOW-VOLTAGE HIGH-SPEED QUADRUPLE DIFFERENTIAL LINE RECEIVER WITH ±15-kV IEC ESD PROTECTION

Check for Samples: AM26LV32E-EP

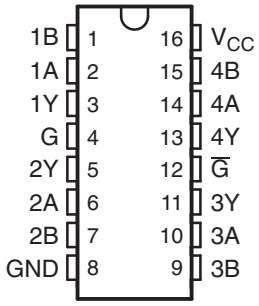
FEATURES

- **Meets or Exceeds Standard TIA/EIA-422-B and ITU Recommendation V.11**
- **Operates From a Single 3.3-V Power Supply**
- **ESD Protection for RS422 Bus Pins**
  - **±15-kV Human-Body Model (HBM)**
  - **±8-kV IEC61000-4-2, Contact Discharge**
  - **±15-kV IEC61000-4-2, Air-Gap Discharge**
- **Switching Rates up to 32 MHz**
- **Low Power Dissipation: 27 mW Typ**
- **Open-Circuit, Short-Circuit, and Terminated Fail-Safe**
- **±7-V Common-Mode Input Voltage Range With ±200-mV Sensitivity**
- **Accepts 5-V Logic Inputs With 3.3-V Supply (Enable Inputs)**
- **Input Hysteresis: 35 mV Typ**
- **Pin-to-Pin Compatible With AM26C32, AM26LS32**
- **I_{off} Supports Partial-Power-Down Mode Operation**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C/125°C) Temperature Range** (1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

D PACKAGE
(TOP VIEW)



(1) Additional temperature ranges are available – contact factory

DESCRIPTION/ORDERING INFORMATION

The AM26LV32E consists of quadruple differential line receivers with 3-state outputs. These differential receivers have ±15-kV ESD (HBM and IEC61000-4-2, Air-Gap Discharge) and ±8-kV ESD (IEC61000-4-2, Contact Discharge) protection for RS422 bus pins.

This device is designed to meet TIA/EIA-422-B and ITU recommendation V.11 drivers with reduced supply voltage. The device is optimized for balanced bus transmission at switching rates up to 32 MHz. The 3-state outputs permit connection directly to a bus-organized system.

The AM26LV32E has an internal fail-safe circuitry that prevents the device from putting an unknown voltage signal at the receiver outputs. In the open fail-safe, shorted fail-safe, and terminated fail-safe, a high state is produced at the respective output.

This device is supported for partial-power-down applications using I_{off}. I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The AM26LV32EM is characterized for operation from –55°C to 125°C.

Table 1. ORDERING INFORMATION

T_A	PACKAGE(1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOIC – D	Tape and reel	AM26LV32EMDREP	A26LV32EMP

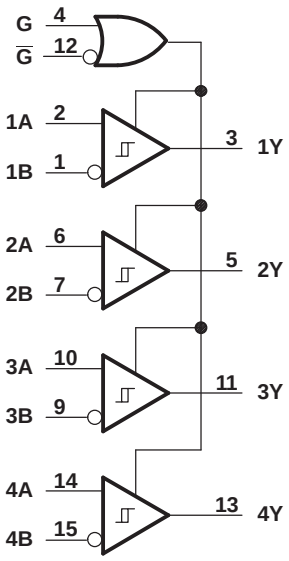
(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLE(1) (each receiver)

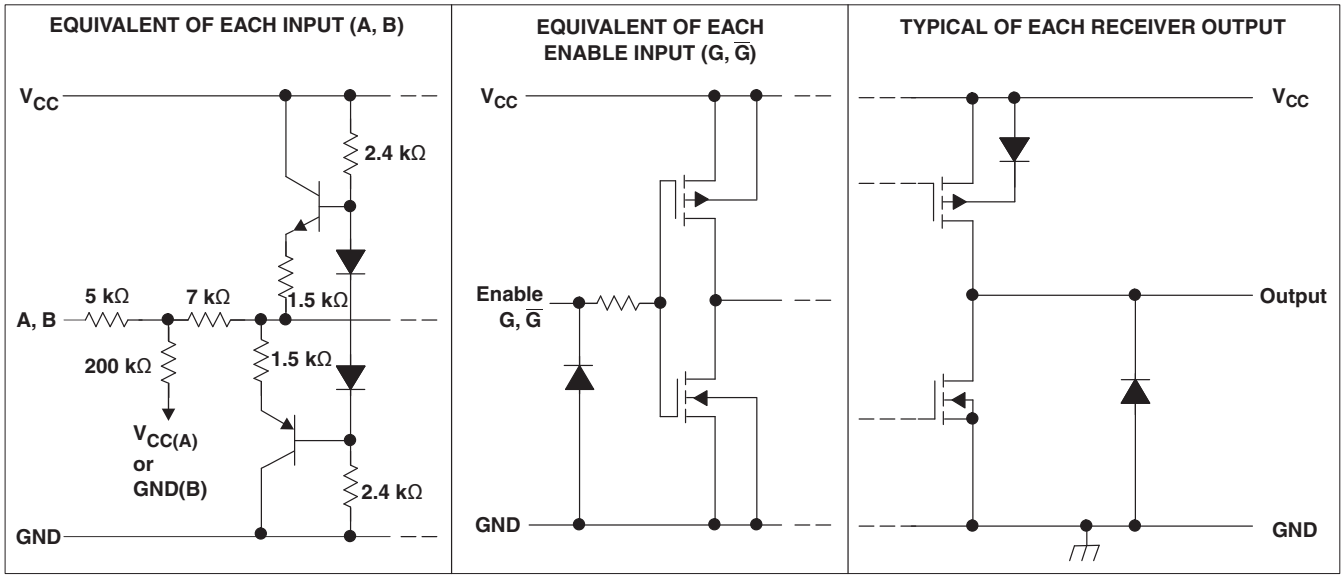
DIFFERENTIAL INPUT	ENABLES		OUTPUT
	G	$\overline{G}$	
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
–0.2 V < V_{ID} < 0.2 V	H	X	?
	X	L	?
$V_{ID} \leq$ –0.2 V	H	X	L
	X	L	L
Open, shorted, or terminated	H	X	H
	X	L	H
X	L	H	Z

(1) H = high level, L = low level, X = irrelevant,
Z = high impedance (off), ? = indeterminate

LOGIC DIAGRAM (POSITIVE LOGIC)



SCHEMATIC



All resistor values are nominal.

ABSOLUTE MAXIMUM RATINGS(1) (2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(3)		–0.5	6	V
V_I	Input voltage range	A or B inputs	–14	14	V
		Enable Inputs	–0.5	6	V
V_{ID}	Differential input voltage(4)		–14	14	V
V_O	Output voltage range		–0.5	6	V
I_{IK}	Input clamp current range	$V_I < 0$		–20	mA
I_{OK}	Output clamp current range	$V_O < 0$		–20	mA
I_O	Maximum output current			±20	mA
T_J	Operating virtual junction temperature			150	°C
θ_{JA}	Package thermal impedance(5) (6)			73	°C/W
T_A	Operating free-air temperature range		–55	125	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This device is designed to meet TIA/EIA-422-B and ITU.
(3) All voltage values except differential input voltage are with respect to the network GND.
(4) Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.
(5) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_A)/\theta_{JA}$. Selecting the maximum of 150°C can affect reliability.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	Enable high-level input voltage	2		5.5	V
V_{IL}	Enable low-level input voltage	0		0.8	V
V_{IC}	Common-mode input voltage	–7		7	V
V_{ID}	Differential input voltage	–7		7	V
I_{OH}	High-level output current			–5	mA
I_{OL}	Low-level output current			5	mA
T_A	Operating free-air temperature	–55		125	°C

ELECTRICAL CHARACTERISTICS

over recommended ranges of common-mode input, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage, differential input					0.2	V
V_{IT-}	Negative-going input threshold voltage, differential input			–0.2			V
V_{hys}	Input hysteresis ($V_{IT+} – V_{IT-}$)				35		mV
V_{IK}	Input clamp voltage, G and $\overline{G}$	I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = –5 mA		2.4	3.2		V
		V_{ID} = 200 mV, I_{OH} = –100 µA		V_{CC} – 0.1			
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, I_{OL} = 5 mA			0.17	0.5	V
		V_{ID} = –200 mV, I_{OL} = 100 µA				0.1	
I_{OZ}	High-impedance state output current	$V_O = V_{CC}$ or GND				±50	µA
I_{off}	Output current with power off	V_{CC} = 0 V, V_O = 0 or 5.5 V				±100	µA
I_I	Line input current	Other input at 0 V	V_I = 10 V			1.5	mA
			V_I = –10 V			–2.5	
I_I	Enable input current, G and $\overline{G}$	$V_I = V_{CC}$ or GND				±1	µA
r_i	Input resistance	V_{IC} = –7 V to 7 V, Other input at 0 V		4	17		kΩ
I_{CC}	Supply current (total package)	G, $\overline{G} = V_{CC}$ or GND, No load, Line inputs open			8	17	mA
C_{pd}	Power dissipation capacitance(2)	One channel			150		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) C_{pd} determines the no-load dynamic current consumption: $I_S = C_{pd} \times V_{CC} \times f + I_{CC}$

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 1	8	16	26	ns
t_{PHL}	Propagation delay time, high- to low-level output		8	16	26	ns
t_t	Transition time	See Figure 1		5		ns
t_{PZH}	Output-enable time to high level	See Figure 2		17	40	ns
t_{PZL}	Output-enable time to low level	See Figure 3		10	40	ns
t_{PHZ}	Output-disable time from high level	See Figure 2		20	40	ns
t_{PLZ}	Output-disable time from low level	See Figure 3		16	40	ns
$t_{sk(p)}$	Pulse skew	See Figure 1 (2)		4	6	ns
$t_{sk(o)}$	Pulse skew	See Figure 1 (3)		4	6	ns
$t_{sk(pp)}$	Pulse skew (device to device)	See Figure 1 (4)		6	9	ns
$f_{(max)}$	Maximum operating frequency	See Figure 1		32		MHz

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) $t_{sk(p)}$ is $|t_{pLH} - t_{pHL}|$ of each channel of same device.
(3) $t_{sk(o)}$ is the maximum difference in propagation delay times between any two channels of same device switching in the same direction.
(4) $t_{sk(pp)}$ is the maximum difference in propagation delay times between any two channels of any two devices switching in the same direction.

ESD PROTECTION

PARAMETER	TEST CONDITIONS	TYP	UNIT
Receiver input	HBM	±15	kV
	IEC61000-4-2, Air-Gap Discharge	±15	
	IEC61000-4-2, Contact Discharge	±8	

PARAMETER MEASUREMENT INFORMATION

A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 10 MHz, duty cycle = 50%, $t_r = t_f \leq 2$ns.

C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform $\overline{G}$.

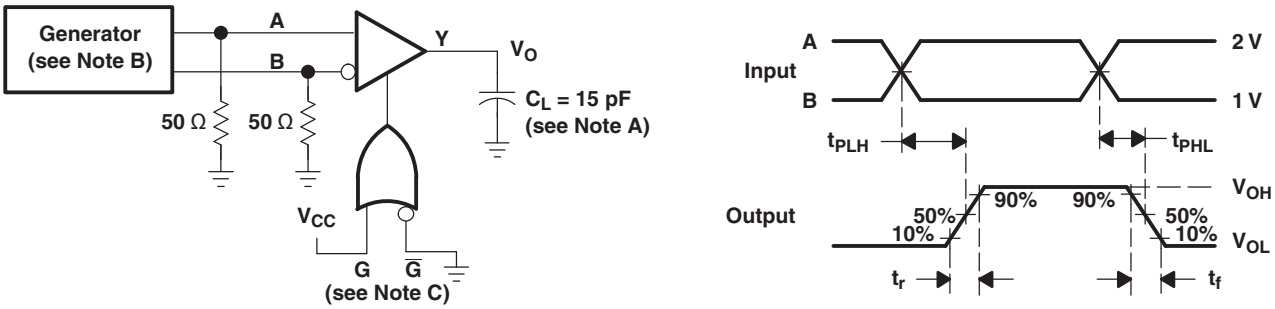


Figure 1. Test Circuit and Voltage Waveforms, t_{PLH} and t_{PHL}

A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 10 MHz, duty cycle = 50%, $t_r = t_f \leq 2$ns.

C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform $\overline{G}$.

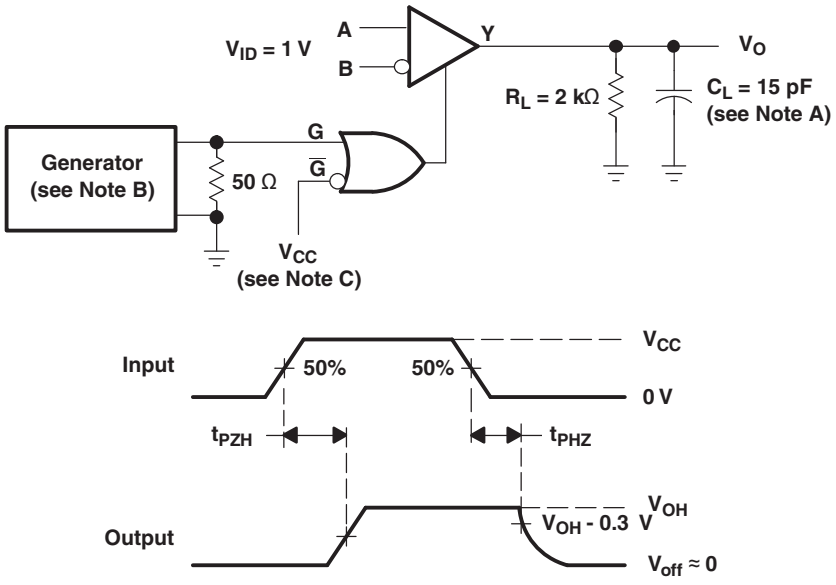


Figure 2. Test Circuit and Voltage Waveforms, t_{PZH} and t_{PHZ}

A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 10 MHz, duty cycle = 50%, $t_r = t_f \leq 2$ns.

C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform $\overline{G}$.

PARAMETER MEASUREMENT INFORMATION (continued)

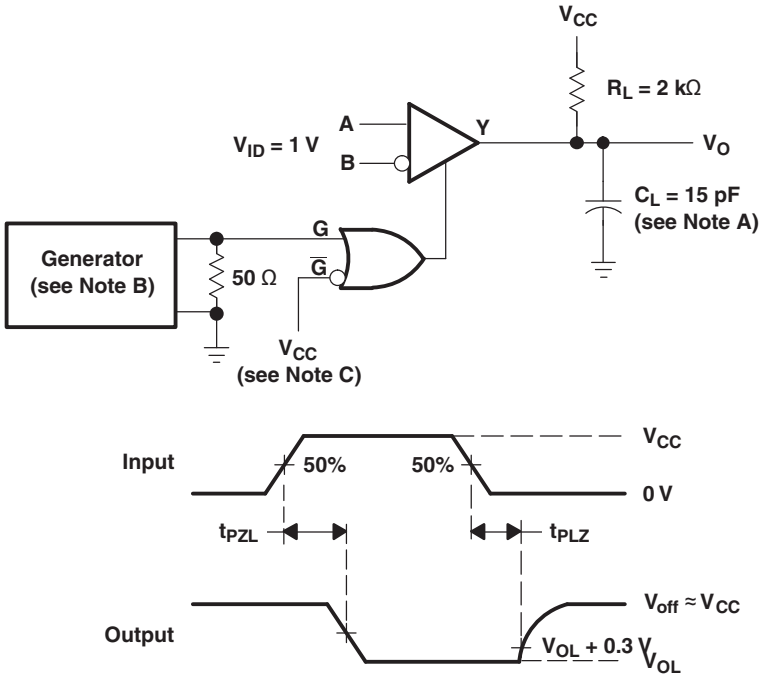


Figure 3. Test Circuit and Voltage Waveforms, t_{PZL} and t_{PLZ}

REVISION HISTORY

Changes from Original (November 2008) to Revision A	Page
• Changed units for V_{IC} and V_{ID} recommended operating conditions from mA to V	4

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AM26LV32EMDREP	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	A26LV32EMP
AM26LV32EMDREP.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	A26LV32EMP
V62/09602-01XE	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	A26LV32EMP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF AM26LV32E-EP :

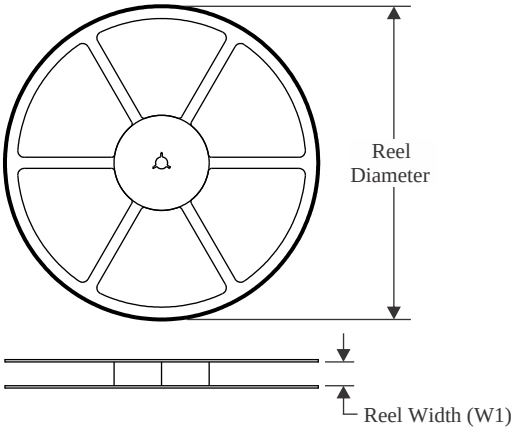
- Catalog : AM26LV32E

NOTE: Qualified Version Definitions:

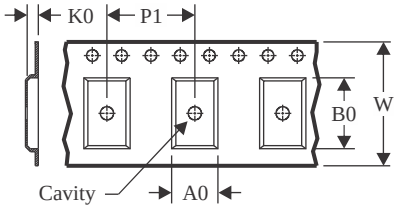
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

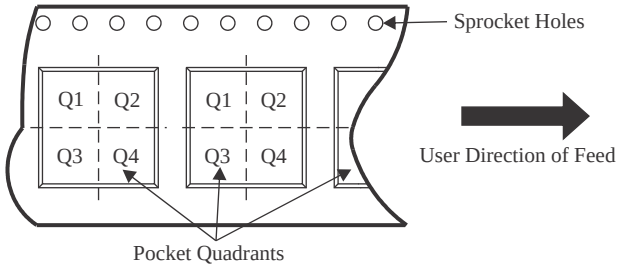


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

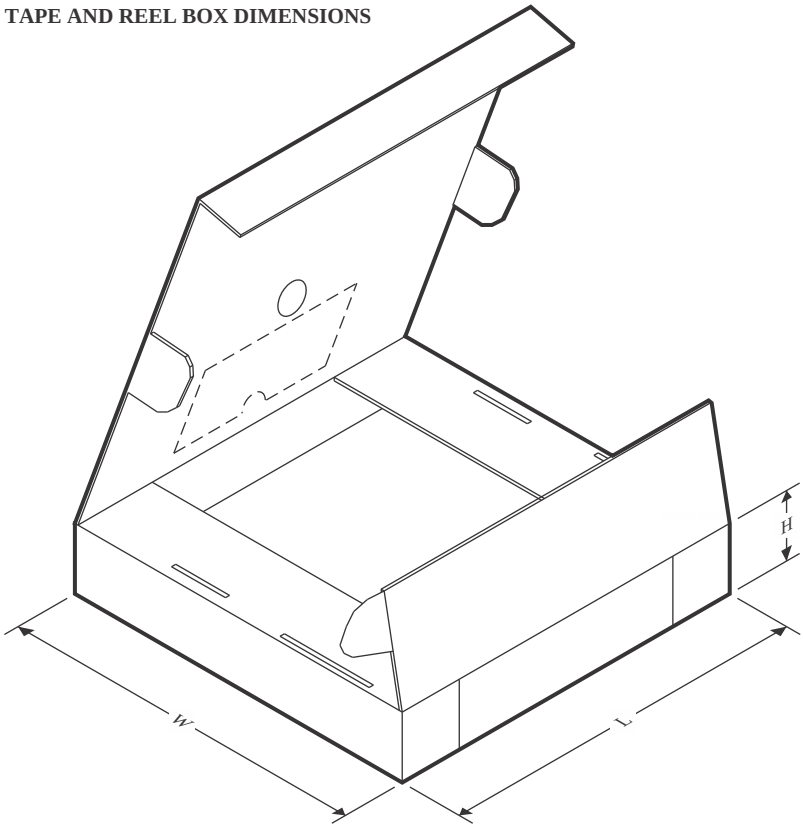
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM26LV32EMDREP	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

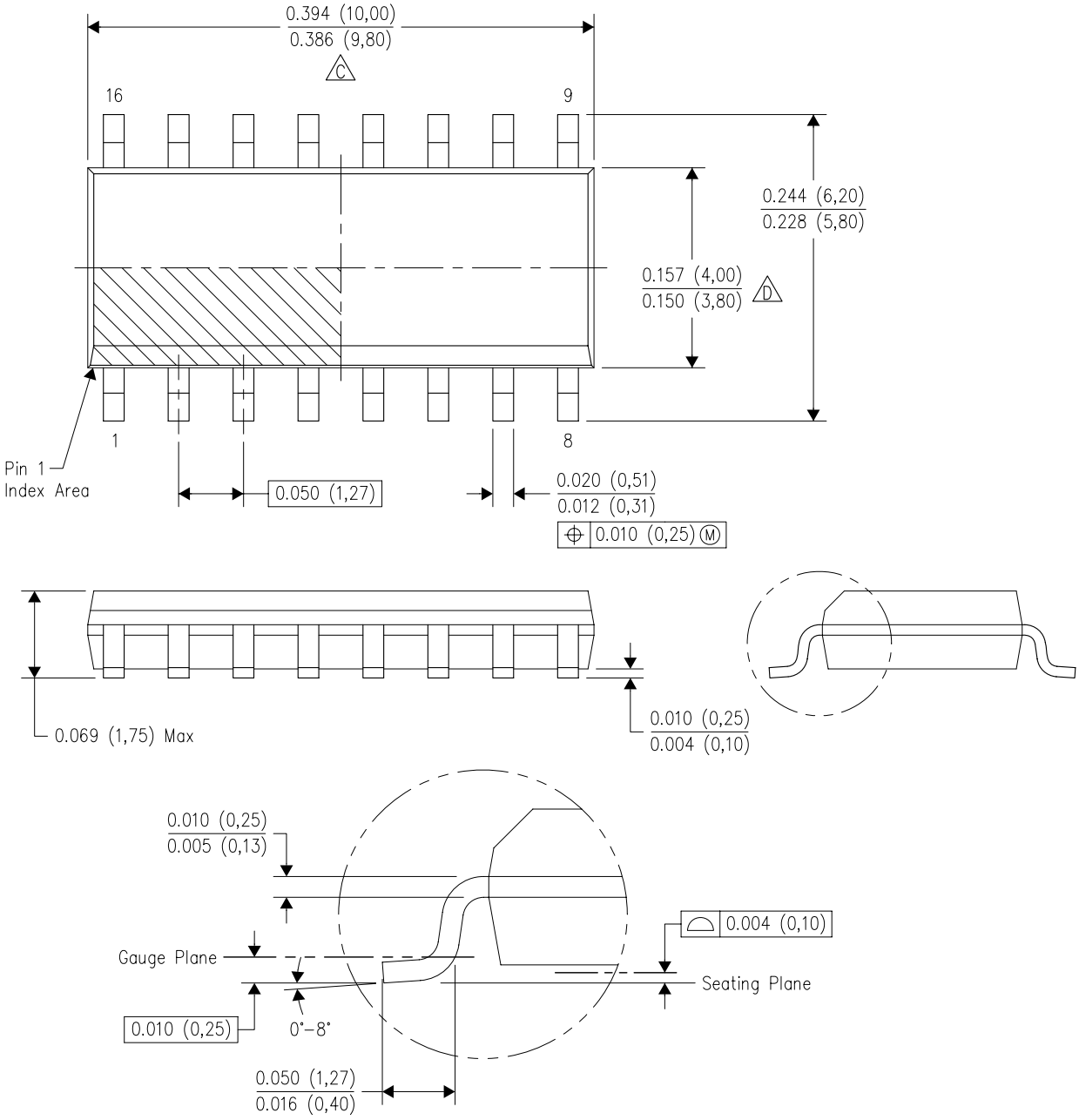
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM26LV32EMDREP	SOIC	D	16	2500	353.0	353.0	32.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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