完全集成，8通道超声波模拟前端，0.75 nV/rtHz，14/12位，65MSPS，158 mW/CH

查询样品: AFE5803

特性

- **8** 通道完全模拟前端
  - **LNA, VCAT, PGA, LPF, ADC**
- 可编程增益低噪音放大器 **(LNA)**
  - **24/18/12dB** 增益
  - **0.25/0.5/1 V_{PP}**线性输入范围
  - **0.63/0.7/0.9 nV/rtHz** 输入参考噪音
  - 可编主动终止
- **40dB** 低噪音电压控制衰减器 **(VACT)**
- **24/30dB** 可编程增益放大器 **(PGA)**
- **3rd**次序线性相位低通滤波器 **(LPF)**
  - **10, 15, 20, 30MHz**
- **14**位模数转换器 **(ADC)**
  - **65MSPS** 时为 **77dBFS** 信噪比 **(SNR)**
  - **LVDS** 输出
- 噪音**/**功率优化（完全链路）
  - **0.75nV/rtHz**，**65MSPS**时为**158mW/CH**
  - **1.1nV/rtHz**，**40MSPS**时为**101mW/CH**
- 出色的器件到器件增益匹配
  - **±0.5dB** （典型值）和 **±0.9dB** （最大值）
- 低谐波失真
- 快速且持续的过载恢复
- 小型封装：**15mm x 9mm**，**135-BGA**

应用范围

- 医疗超声波成像
- 非侵入性评估设备

说明

AFE5803是一款高度集成的模拟前端 (AFE) 解决方案，此解决方案设计用于高性能和小型超声波系统。AFE5803 集成了一个完全时间增益控制 (TGC) 成像路径。 它还使得用户可以选择不同的功率/噪音组合来优化系统性能。 因此，AFE5803 适合于用于便携式系统的超声波模拟前端解决方案。

AFE5803 包含8通道电压控制放大器 (VCA)，14/12 位模数转换器 (ADC)。 此 VCA 包括低噪音放大器(LNA)，电压控制衰减器 (VCAT)，可编程增益放大器 (PGA)，和低通滤波器 (LPF)。 LNA增益可编程以支持 250mV_{PP}至 1V $_{PP}$的输入信号。 LNA 还支持可编程主动终止。 此超低噪音 VCAT 提供了一个 40dB 的衰减控制范围并提升了有益于谐波成像和近场成像的总体低增益 SNR。 PGA 提供了 24dB 和 30dB 的增益选项。 在 ADC 之前，一个LPF可被配置为 10MHz，15MHz，20MHz 或者 30MHz 以支持不同频率下的超声波应用。 AFE5803 中的高性能 14 位/65MSPS ADC 可实现7 7dBFS SNR。 它确保了低链路增益下的出色SNR。 ADC 的 LVDS 输出可实现小型化系统所需的灵活系统集成。

AFE5803 采用 15mm × 9mm，135 引脚球状引脚栅格 (BGA) 封装并且其额定运行温度为 0°C 至 85°C。 此器件与 AFE5807，AFE5808 和 AFE5808A 引脚至引脚兼容。

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

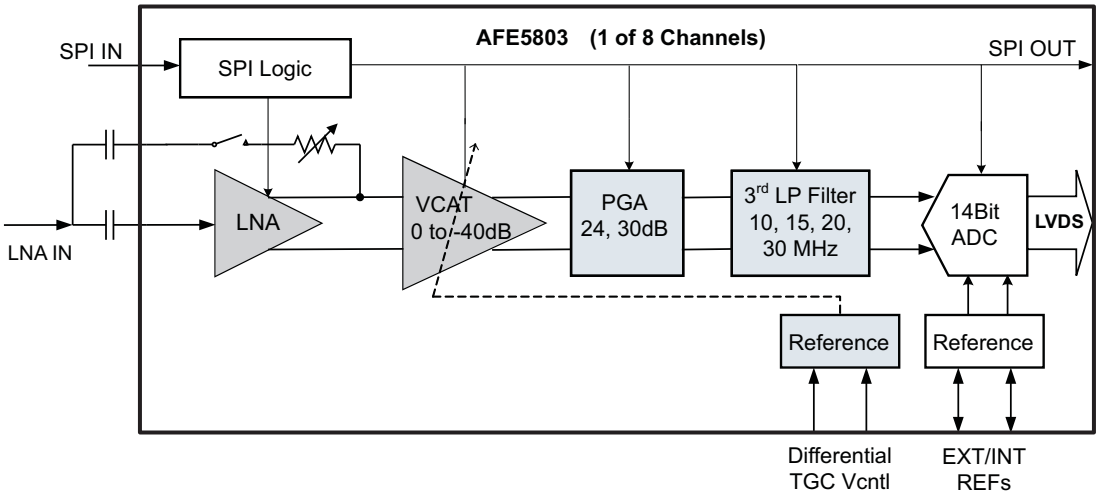


Figure 1. Block Diagram

PACKAGING/ORDERING INFORMATION(1)

PRODUCT	PACKAGE TYPE	OPERATING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
AFE5803	ZCF	0°C to 85°C	AFE5803ZCF	Tray, 160

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE		UNIT
		MIN	MAX	
Supply voltage range	AVDD	–0.3	3.9	V
	AVDD_ADC	–0.3	2.2	V
	AVDD_5V	–0.3	6	V
	DVDD	–0.3	2.2	V
Voltage between AVSS and LVSS		–0.3	0.3	V
Voltage at analog inputs and digital inputs		–0.3	min [3.6,AVDD+0.3]	V
Peak solder temperature(2)			260	°C
Maximum junction temperature (T_J), any condition			105	°C
Storage temperature range		–55	150	°C
Operating temperature range		0	85	°C
ESD Ratings	Human Body Model (HBM)		2000	V
	Charged Device Model (CDM)		500	V

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied Exposure to absolute maximum rated conditions for extended periods may degrade device reliability.
(2) Device complies with JSTD-020D.

THERMAL INFORMATION

THERMAL METRIC(1)		AFE5803 BGA 135 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	34.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	5	
θ_{JB}	Junction-to-board thermal resistance	11.5	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	10.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) 有关传统和新的热度量的更多信息，请参阅 *IC* 封装热度量 应用报告 SPRA953。

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	MAX	UNIT
AVDD	3.15	3.6	V
AVDD_ADC	1.7	1.9	V
DVDD	1.7	1.9	V
AVDD_5V	4.75	5.5	V
Ambient Temperature, T_A	0	85	°C

DEVICE INFORMATION

PIN CONFIGURATION
Top View
ZCF (BGA-135)

	1	2	3	4	5	6	7	8	9
A	AVDD	INP8	INP7	INP6	INP5	INP4	INP3	INP2	INP1
B	CM_BYP	ACT8	ACT7	ACT6	ACT5	ACT4	ACT3	ACT2	ACT1
C	AVSS	INM8	INM7	INM6	INM5	INM4	INM3	INM2	INM1
D	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVDD	AVDD
E	CH7_TEST_OUTP	CH7_TEST_OUTM	AVSS	AVSS	AVSS	AVSS	AVSS	AVDD	AVDD
F	CH7_BUFFER_OUTM	CH7_BUFFER_OUTP	AVSS	AVSS	AVSS	AVSS	AVSS	DNC	DNC
G	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	DNC	DNC
H	CH8_BUFFER_OUTM	CH8_BUFFER_OUTP	AVSS	AVSS	AVSS	AVSS	AVSS	PDN_GLOBAL	RESET
J	CH8_TEST_OUTP	CH8_TEST_OUTM	AVSS	AVSS	AVSS	AVDD_ADC	AVDD_ADC	PDN_VCA	SCLK
K	AVDD	AVDD_5V	VCNTLP	VCNTLM	VHIGH	AVSS	DNC	AVDD_ADC	SDATA
L	CLKP_ADC	CLKM_ADC	AVDD_ADC	REFM	DNC	DNC	DNC	PDN_ADC	SEN
M	AVDD_ADC	AVDD_ADC	VREF_IN	REFP	DNC	DNC	DNC	DNC	SDOUT
N	D8P	D8M	DVDD	DNC	DVSS	DNC	DVDD	D1M	D1P
P	D7M	D6M	D5M	FCLKM	DVSS	DCLKM	D4M	D3M	D2M
R	D7P	D6P	D5P	FCLKP	DVSS	DCLKP	D4P	D3P	D2P

PIN FUNCTIONS

PIN		DESCRIPTION
NO.	NAME	
B9~ B2	ACT1...ACT8	Active termination input pins for CH1~8. 1 µF capacitors are recommended. See the Applicaiton Information section.
A1, D8, D9, E8, E9, K1	AVDD	3.3 V Analog supply for LNA, VCAT, PGA, LPF blocks.
K2	AVDD_5V	5 V Analog supply for LNA, VCAT, PGA, LPF blocks.
J6, J7, K8, L3, M1, M2	AVDD_ADC	1.8 V Analog power supply for ADC.
C1, D1~D7, E3~E7, F3~F7, G1~G7, H3~H7,J3~J5, K6	AVSS	Analog ground.
L2	CLKM_ADC	Negative input of differential ADC clock. In the single-end clock mode, it can be tied to GND directly or through a 0.1 µF capacitor.
L1	CLKP_ADC	Positive input of differential ADC clock. In the single-end clock mode, it can be tied to clock signal directly or through a 0.1 µF capacitor.
B1	CM_BYP	Bias voltage and bypass to ground. ≥1µF is recommended. To suppress the ultra low frequency noise, 10µF can be used.
E2	CH7_TEST_OUTM	CH7 PGA negative output when PGA test mode is enabled. Can be floated if not used.
E1	CH7_TEST_OUTP	CH7 PGA positive output when PGA test mode is enabled. Can be floated if not used.
F1	CH7_BUFFER_OUTM	Negative differential output for the buffer amplifier when PGA test mode is enabled. Can be floated if not used. See the *TEST MODES* in the application information section.
F2	CH7_BUFFER_OUTP	Positive differential output for the buffer amplifier when PGA test mode is enabled. Can be floated if not used. See the *TEST MODES* in the application information section.
J2	CH8_TEST_OUTM	CH8 PGA negative output when PGA test mode is enabled. Can be floated if not used.
J1	CH8_TEST_OUTP	CH8 PGA positive output when PGA test mode is enabled. Can be floated if not used.
H1	CH8_BUFFER_OUTM	Negative differential output for the buffer amplifier when PGA test mode is enabled. Can be floated if not used. See the *TEST MODES* in the application information section.
H2	CH8_BUFFER_OUTP	Positive differential output for the buffer amplifier when PGA test mode is enabled. Can be floated if not used. See the *TEST MODES* in the application information section.
N8, P9~P7, P3~P1, N2	D1M~D8M	ADC CH1~8 LVDS negative outputs
N9, R9~R7, R3~R1, N1	D1P~D8P	ADC CH1~8 LVDS positive outputs
P6	DCLKM	LVDS bit clock (7x) negative output

PIN FUNCTIONS (continued)

PIN		DESCRIPTION
NO.	NAME	
R6	DCLKP	LVDS bit clock (7x) positive output
F8, F9, G8, G9, K7, L5~L7,M5~M8, N4, N6	DNC	Do not connect. Must leave floated
N3, N7	DVDD	ADC digital and I/O power supply, 1.8 V
N5, P5, R5	DVSS	ADC digital ground
P4	FCLKM	LVDS frame clock (1X) negative output
R4	FCLKP	LVDS frame clock (1X) positive output
C9~C2	INM1…INM8	CH1~8 complimentary analog inputs. Bypass to ground with ≥ 0.015 µF capacitors. The HPF response of the LNA depends on the capacitors.
A9~A2	INP1...INP8	CH1~8 analog inputs. AC couple to inputs with ≥ 0.1µF capacitors.
L8	PDN_ADC	ADC partial (fast) power down control pin with an internal pull down resistor of 100 kΩ. Active High.
J8	PDN_VCA	VCA partial (fast) power down control pin with an internal pull down resistor of 20 kΩ. Active High.
H8	PDN_GLOBAL	Global (complete) power-down control pin for the entire chip with an internal pull down resistor of 20kΩ. Active High.
L4	REFM	0.5 V reference output in the internal reference mode. Must leave floated in the internal reference mode. Adding test point on PCB is recommended for monitoring the reference output.
M4	REFP	1.5 V reference output in the internal reference mode. Must leave floated in the internal reference mode. Adding test point on PCB is recommended for monitoring the reference output.
H9	RESET	Hardware reset pin with an internal pull-down resistor of 20 kΩ. Active high.
J9	SCLK	Serial interface clock input with an internal pull-down resistor of 2 0kΩ
K9	SDATA	Serial interface data input with an internal pull-down resistor of 20 kΩ
M9	SDOUT	Serial interface data readout. High impedance when readout is disabled.
L9	SEN	Serial interface enable with an internal pull up resistor of 20 kΩ. Active low.
K4	VCNTLM	Negative differential attenuation control pin.
K3	VCNTLP	Positive differential attenuation control pin
K5	VHIGH	Bias voltage; bypass to ground with ≥1µF.
M3	VREF_IN	ADC 1.4 V reference input in the external reference mode; bypass to ground with 0. 1 µF.
F8, F9, G8, G9, K7, L5~L7, M5~M8, N4, N6	DNC	Do not connect. Must leave floated

ELECTRICAL CHARACTERISTICS

AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, AC-coupled with 0.1µF at INP and bypassed to ground with 15nF at INM, No active termination, V_{CNTL} = 0 V, f_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14Bit, sample rate = 65 MSPS, LPF Filter = 15 MHz, low noise mode, V_{OUT} = –1 dBFS, ADC configured in internal reference mode, single-ended VCNTL mode, VCNTLM = GND, at ambient temperature T_A = 25°C, unless otherwise noted. Min and max values are specified across full-temperature range with AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
TGC FULL SIGNAL CHANNEL (LNA+VCAT+LPF+ADC)						
en (RTI)	Input voltage noise over LNA Gain(low noise mode)	Rs = 0 Ω, f = 2 MHz, LNA =24/18/12 dB, PGA = 2 4dB		0.76/0.83/1.16		nV/rtHz
		Rs = 0 Ω, f = 2 MHz,LNA =24/18/12 dB, PGA = 30 dB		0.75/0.86/1.12		
	Input voltage noise over LNA Gain(low power mode)	Rs = 0 Ω, f = 2 MHz,LNA =24/18/12 dB, PGA = 24 dB		1.1/1.2/1.45		nV/rtHz
		Rs = 0 Ω, f = 2 MHz, LNA =24/18/12 dB, PGA = 30 dB		1.1/1.2/1.45		
	Input Voltage Noise over LNA Gain(Medium Power Mode)	Rs = 0 Ω, f = 2 MHz,LNA = 24/18/12 dB, PGA = 24 dB		1/1.05/1.25		nV/rtHz
		Rs = 0 Ω, f = 2 MHz, LNA = 24/18/12 dB, PGA = 30 dB		0.95/1.0/1.2		
	Input referred current noise	Low Noise Mode/Medium Power Mode/Low Power Mode		2.7/2.1/2		pA/rtHz
NF	Noise figure	Rs = 200 Ω, 200 Ω active termination, PGA = 24dB,LNA = 12/18/24 dB		3.85/2.4/1.8		dB
		Rs = 100 Ω, 100 Ω active termination, PGA = 24dB,LNA = 12/18/24 dB		5.3/3.1/2.3		dB
V_{MAX}	Maximum Linear Input Voltage	LNA gain = 24/18/12 dB		250/500/1000		mV_{PP}
V_{CLAMP}	Clamp Voltage	Reg52[10:9] = 0, LNA = 24/18/12 dB		350/600/1150		
	PGA Gain	Low noise mode		24/30		dB
		Medium/Low power mode		24/28.5		
	Total gain	LNA = 24 dB, PGA = 30 dB, Low noise mode		54		dB
		LNA = 2 4dB, PGA = 30 dB, Med power mode		52.5		
		LNA = 24 dB, PGA = 30 dB, Low power mode		52.5		
	Ch-CH Noise Correlation Factor without Signal (1)	Summing of 8 channels		0		
	Ch-CH Noise Correlation Factor with Signal (1)	Full band (VCNTL = 0/0.8)		0.15/0.17		
		1MHz band over carrier (VCNTL= 0/0.8)		0.18/0.75		
	Signal to Noise Ratio (SNR)	VCNTL = 0.6V(22 dB total channel gain)	68	70		dBFS
		VCNTL = 0, LNA = 18 dB, PGA =24 dB	59.3	63		
		VCNTL = 0, LNA = 24 dB, PGA = 24 dB		58		
	Narrow Band SNR	SNR over 2 MHz band around carrier at VCNTL = 0.6 V (22 dB total gain)	75	77		dBFS
	Input Common-mode Voltage	At INP and INM pins		2.4		V
	Input resistance			8		kΩ
		Preset active termination enabled		50/100/200/400		Ω
	Input capacitance			20		pF
	Input Control Voltage	V_{CNTLP} - V_{CNTLM}	0		1.5	V
	Common-mode voltage	V_{CNTLP} and V_{CNTLM}		0.75		V
	Gain Range			-40		dB
	Gain Slope	V_{CNTL}= 0.1 V to 1.1 V		35		dB/V
	Input Resistance	Between V_{CNTLP} and V_{CNTLM}		200		KΩ
	Input Capacitance	Between V_{CNTLP} and V_{CNTLM}		1		pF
	TGC Response Time	VCNT L= 0 V to 1.5 V step function		1.5		µs
	3rd order-Low-pass Filter			10, 15, 20, 30		MHz
	Settling time for change in LNA gain			14		µs
	Settling time for change in active termination setting			1		µs

(1) Noise correlation factor is defined as Nc/(Nu+Nc), where Nc is the correlated noise power in single channel; and Nu is the uncorrelated noise power in single channel. Its measurement follows the below equation, in which the SNR of single channel signal and the SNR of summed eight channel signal are measured.

$$\frac{N_C}{N_U + N_C} = \frac{10^{-\frac{8CH\_SNR}{10}}}{10^{-\frac{1CH\_SNR}{10}}} \times \frac{1}{56} - \frac{1}{7}$$

ELECTRICAL CHARACTERISTICS (continued)

AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, AC-coupled with 0.1µF at INP and bypassed to ground with 15nF at INM, No active termination, V_{CNTL} = 0 V, f_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14Bit, sample rate = 65 MSPS, LPF Filter = 15 MHz, low noise mode, V_{OUT} = –1 dBFS, ADC configured in internal reference mode, single-ended VCNTL mode, VCNTLM = GND, at ambient temperature T_A = 25°C, unless otherwise noted. Min and max values are specified across full-temperature range with AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
AC ACCURACY						
	LPF Bandwidth tolerance			±5%		
	CH-CH group delay variation	2 MHz to 15 MHz		2		ns
	CH-CH Phase variation	15 MHz signal		11		Degree
	Gain matching	0 V < VCNTL < 0.1 V (Dev-to-Dev)		±0.5		dB
		0.1 V < VCNTL < 1.1 V(Dev-to-Dev)	–0.9	±0.5	0.9	
		0.1 V < VCNTL < 1.1 V(Dev-to-Dev) Temp = 0°C and 85°C	–1.1	±0.5	1.1	
		1.1 V < VCNTL < 1.5 V(Dev-to-Dev)		±0.5		
	Gain matching	Channel-to-Channel		±0.25		dB
	Output offset	V_{cntl}= 0, PGA = 30 dB, LNA = 24 dB	–75		75	LSB
AC PERFORMANCE						
HD2	Second-Harmonic Distortion	Fin = 2 MHz; V_{OUT} = -1 dBFS		–60		dBc
		Fin = 5 MHz; V_{OUT} = -1 dBFS		–60		
		Fin = 5 MHz; V_{IN}= 500 mVpp, V_{OUT} = –1dBFS, LNA = 18dB, V_{CNTL}=0.88 V		–55		
		Fin = 5 MHz; Vin = 250 mVpp, V_{OUT} =–1 dBFS, LNA = 24dB, V_{CNTL}= 0.88 V		–55		
HD3	Third-Harmonic Distortion	Fin = 2 MHz; V_{OUT} = –1dBFS		–55		dBc
		Fin = 5 MHz; V_{OUT} = –1dBFS		–55		
		Fin = 5 MHz; VIN = 500 mVpp, V_{OUT} = –1 dBFS, LNA = 18 dB, V_{CNTL}= 0.88 V		–55		
		Fin = 5 MHz; VIN = 2 50 mVpp, V_{OUT} = –1 dBFS, LNA = 24 dB, V_{CNTL}= 0.88 V		–55		
THD	Total Harmonic Distortion	Fin = 2 MHz; V_{OUT}=–1 dBFS		–55		dBc
		Fin = 5 MHz; V_{OUT}=–1 dBFS		–55		
IMD3	Intermodulation distortion	f1 = 5 MHz at –1dBFS, f2 = 5.01 MHz at –27 dBFS		–60		dBc
XTALK	Cross-talk	Fin = 5 MHz; V_{OUT}= –1 dBFS		–65		dB
	Phase Noise	1 kHz off 5 MHz (V_{CNTL}=0V)		–132		dBc/Hz
LNA						
	Input Referred Voltage Noise	Rs = 0 Ω, f = 2MHz, Rin = High Z, Gain = 24/18/12 dB		0.63/0.70/0.9		nV/rtHz
	High-Pass Filter	-3 dB Cut-off Frequency		50/100/150/200		KHz
	LNA linear output			4		V_{PP}
VCAT+ PGA						
	VCAT Input Noise	0dB/-40 dB Attenuation		2/10.5		nV/rtHz
	PGA Input Noise	24 dB/30 dB		1.75		nV/rtHz
	-3dB HPF cut-off Frequency			80		KHz
ADC SPECIFICATIONS						
	Sample rate		10		65	MSPS
SNR	Signal-to-noise ratio	Idle channel SNR of ADC 14b		77		dBFS
	Internal reference mode	REFP		1.5		V
		REFM		0.5		V
	External reference mode	VREF_IN Voltage		1.4		V
		VREF_IN Current		50		µA
	ADC input full-scale range			2		Vpp
	LVDS Rate	65MSPS at 14 bit		910		Mbps

ELECTRICAL CHARACTERISTICS (continued)

AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, AC-coupled with 0.1µF at INP and bypassed to ground with 15nF at INM, No active termination, V_{CNTL} = 0 V, f_{IN} = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14Bit, sample rate = 65 MSPS, LPF Filter = 15 MHz, low noise mode, V_{OUT} = –1 dBFS, ADC configured in internal reference mode, single-ended VCNTL mode, VCNTLM = GND, at ambient temperature T_A = 25°C, unless otherwise noted. Min and max values are specified across full-temperature range with AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
POWER DISSIPATION					
AVDD Voltage		3.15	3.3	3.6	V
AVDD_ADC Voltage		1.7	1.8	1.9	V
AVDD_5V Voltage		4.75	5	5.5	V
DVDD Voltage		1.7	1.8	1.9	V
Total power dissipation per channel	TGC low noise mode, 65 MSPS		158	190	mW/CH
	TGC low noise mode, 40 MSPS		145		
	TGC medium power mode, 40 MSPS		114		
	TGC low power mode, 40 MSPS		101.5		
AVDD (3.3V) Current	TGC low noise mode, no signal		202	240	mA
	TGC medium power mode, no signal		126		
	TGC low power mode, no signal		99		
	TGC low noise mode, 500 mV_{PP} Input,1% duty cycle		210		
	TGC medium power mode, 500 mV_{PP} Input, 1% duty cycle		133		
	TGC low power, 500 mV_{PP} Input, 1% duty cycle		105		
AVDD_5V Current	TGC mode no signal		25.5	35	mA
	TGC mode, 500 mV_{PP} Input,1% duty cycle		16.5		
VCA Power dissipation	TGC low noise mode, no signal		99	121	mW/CH
	TGC medium power mode, no signal		68		
	TGC low power mode, no signal		55.5		
	TGC low noise mode, 500 mV_{PP} input,1% duty cycle		102.5		
	TGC medium power mode, 500 mV_{PP} Input, 1% duty cycle		71		
	TGC low power mode, 500 mV_{PP} input,1% duty cycle		59.5		
AVDD_ADC(1.8V) Current	65 MSPS		187	205	mA
DVDD(1.8V) Current	65 MSPS		77	110	mA
ADC Power dissipation/CH	65 MSPS		59	69	mW/CH
	50 MSPS		51		
	40 MSPS		46		
	20 MSPS		35		
Power dissipation in power down mode	PDN_VCA = High, PDN_ADC = High		25		mW/CH
	Complete power-down PDN_Global=High		0.6		
Power-down response time	Time taken to enter power down		1		µs
Power-up response time	VCA power down		2µs+1% of PDN time		µs
	ADC power down		1		
	Complete power down		2.5		ms
Power supply modulation ratio, AVDD and AVDD_5V	fin = 5 MHz, at 50 mVpp noise at 1 KHz on supply(2)		–65		dBc
	fin = 5 MHz, at 50 mVpp noise at 50 KHz on supply(2)		–65		dBc
Power supply rejection ratio	f = 10 kHz,VCNTL = 0 V (high gain), AVDD		–40		dBc
	f = 10 kHz,VCNTL = 0 V(high gain), AVDD_5V		–55		dBc
	f = 10 kHz,VCNTL = 1 V (low gain), AVDD		–50		dBc

(2) PSMR specification is with respect to input signal amplitude.

DIGITAL CHARACTERISTICS

Typical values are at 25°C, AVDD = 3.3 V, AVDD_5 = 5 V and AVDD_ADC = 1.8 V, DVDD = 1.8 V, 14 bit sample rate = 65 MSPS, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = 0°C to T_{MAX} = +85°C

PARAMETER		CONDITION	MIN	TYP	MAX	UNITS (1)
DIGITAL INPUTS/OUTPUTS						
V_{IH}	Logic high input voltage		2		3.3	V
V_{IL}	Logic low input voltage		0		0.3	V
	Logic high input current			200		µA
	Logic low input current			200		µA
	Input capacitance			5		pF
V_{OH}	Logic high output voltage	SDOUT pin		DVDD		V
V_{OL}	Logic low output voltage	SDOUT pin		0		V
LVDS OUTPUTS						
	Output differential voltage	with 100 ohms external differential termination		400		mV
	Output offset voltage	Common-mode voltage		1100		mV
	FCLKP and FCLKM	1X clock rate	10		65	MHz
	DCLKP and DCLKM	7X clock rate	70		455	MHz
		6X clock rate	60		390	MHz
t_{su}	Data setup time (2)			350		ps
t_h	Data hold time (2)			350		ps
ADC INPUT CLOCK						
	CLOCK frequency		10		65	MSPS
	Clock duty cycle		45%	50%	55%	
	Clock input amplitude, differential(V_{CLKP_ADC}–V_{CLKM_ADC})	Sine-wave, ac-coupled	0.5			Vpp
		LVPECL, ac-coupled		1.6		Vpp
		LVDS, ac-coupled		0.7		Vpp
	Common-mode voltage	biased internally		1		V
	Clock input amplitude V_{CLKP_ADC} (single-ended)	CMOS CLOCK		1.8		Vpp

(1) The DC specifications refer to the condition where the LVDS outputs are not switching, but are permanently at a valid logic level 0 or 1 with 100Ω external termination.

(2) Setup and hold time specifications take into account the effect of jitter on the output data and clock. These specifications also assume that the data and clock paths are perfectly matched within the receiver. Any mismatch in these paths within the receiver would appear as reduced timing margins

TYPICAL CHARACTERISTICS

AVDD_5 V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, ac-coupled with 0.1µF caps at INP and 1 5nF caps at INM, No active termination, VCNTL = 0 V, F*IN* = 5 MHz, LNA = 18 dB, PGA = 24 dB, 14 Bit, sample rate = 65 MSPS, LPF Filter = 15 MHz, low noise mode, V_{OUT} = -1dBFS, ADC is configured in internal reference mode, single-ended VCNTL mode, VCNTLM = GND, at ambient temperature T_A = 25°C, unless otherwise noted.

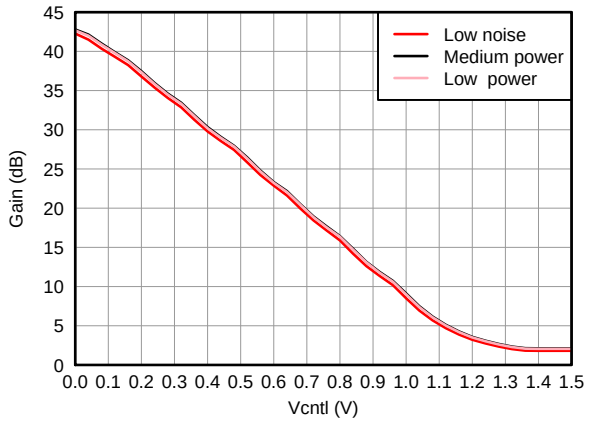


Figure 2. Gain vs. VCNTL, LNA = 18 dB and PGA = 24 dB

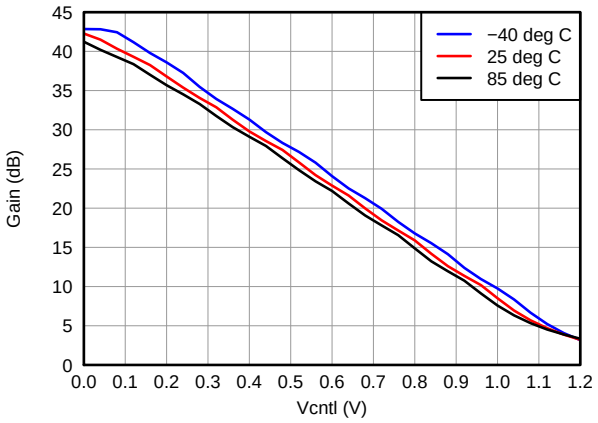


Figure 3. Gain Variation vs. Temperature, LNA = 18 dB and PGA = 24 dB

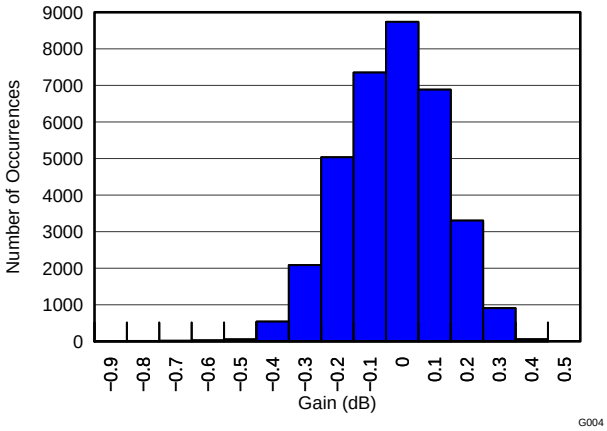


Figure 4. Gain Matching Histogram, VCNTL= 0.3V (34951 channels)

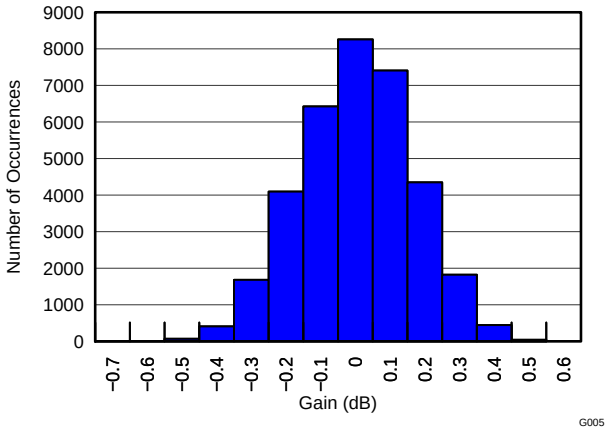


Figure 5. Gain Matching Histogram, VCNTL = 0.6V (34951 channels)

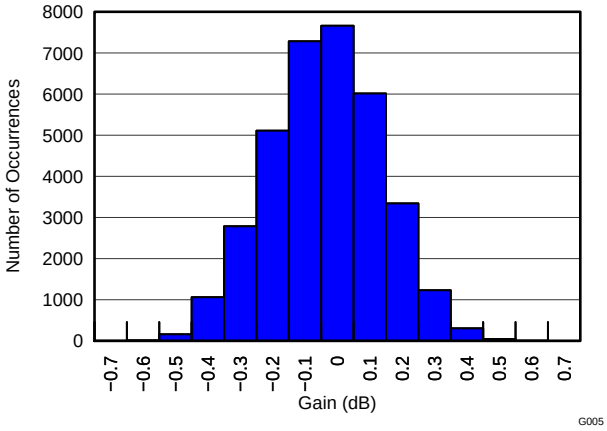


Figure 6. Gain Matching Histogram, VCNTL = 0.9V (34951 channels)

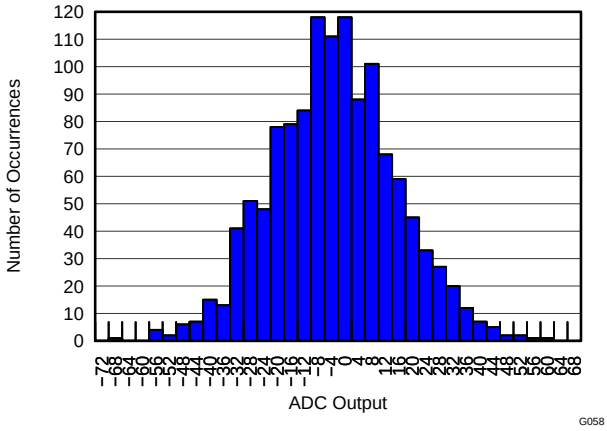


Figure 7. Output Offset Histogram, VCNTL = 0V (1247 channels)

TYPICAL CHARACTERISTICS (continued)

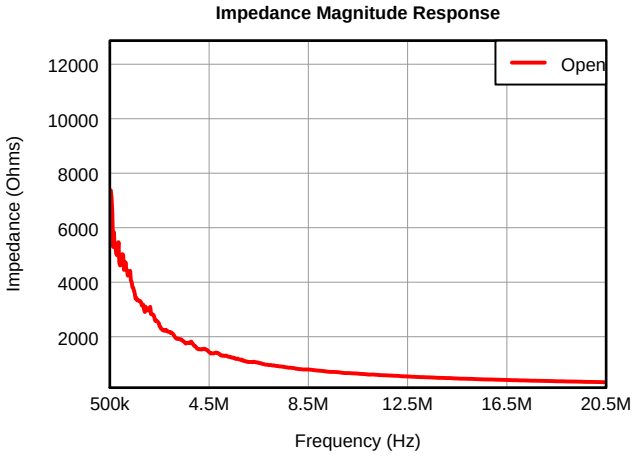


Figure 8. Input Impedance without Active Termination (Magnitude)

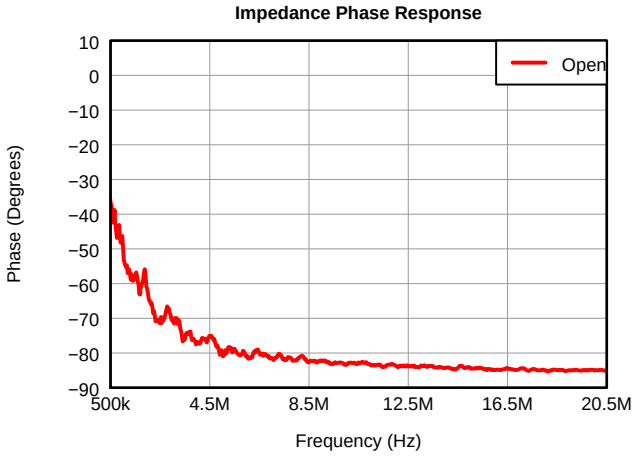


Figure 9. Input Impedance without Active Termination (Phase)

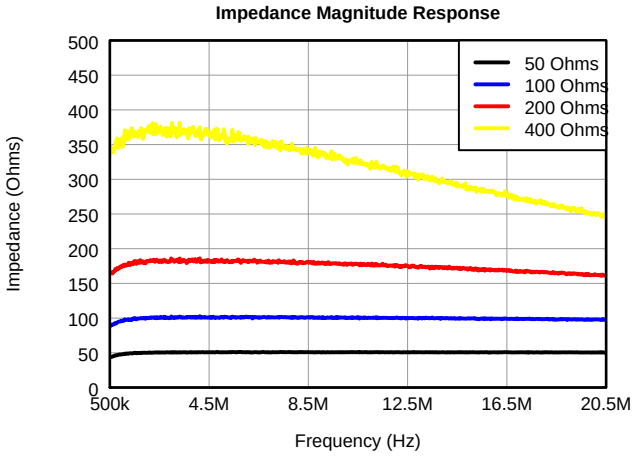


Figure 10. Input Impedance with Active Termination (Magnitude)

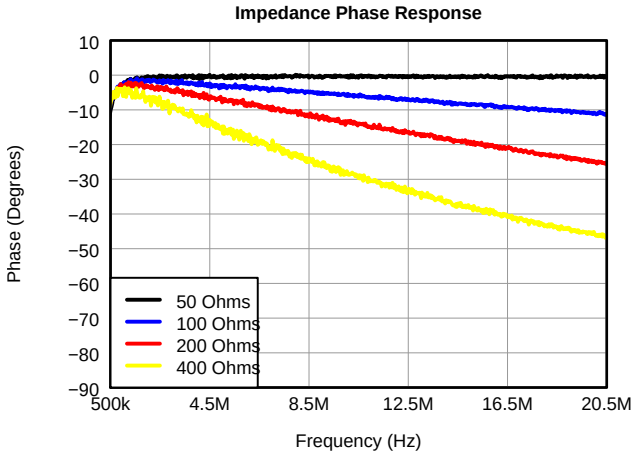


Figure 11. Input Impedance with Active Termination (Phase)

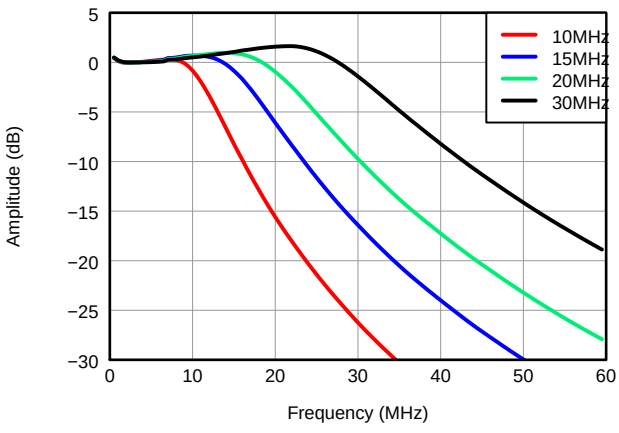


Figure 12. Low-Pass Filter Response

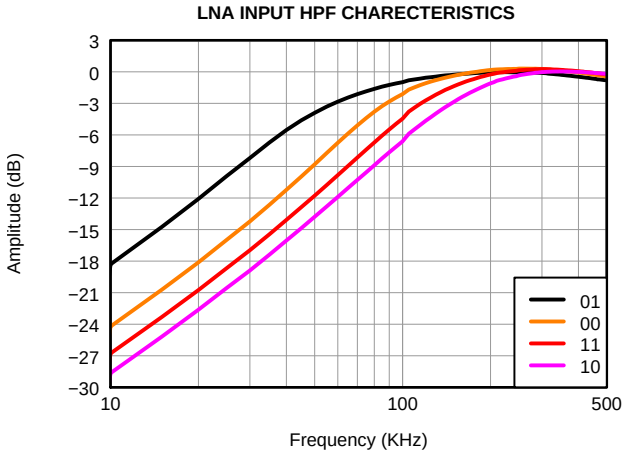


Figure 13. LNA High-Pass Filter Response vs. Reg59[3:2]

TYPICAL CHARACTERISTICS (continued)

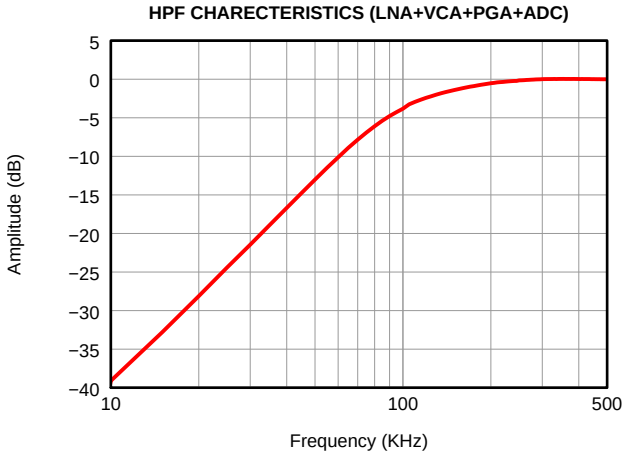


Figure 14. Full Channel High-Pass Filter Response at Default Register Setting

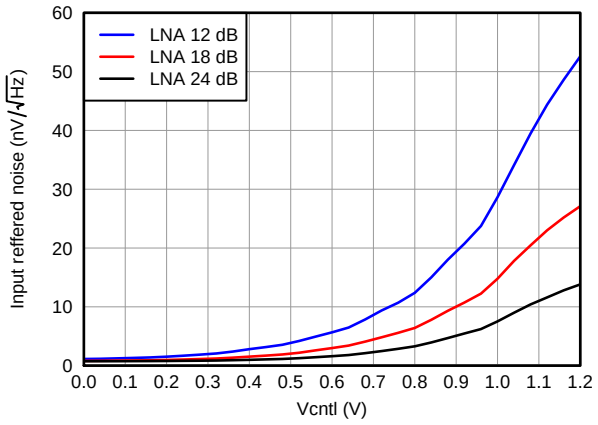


Figure 15. IRN, PGA = 24 dB and Low Noise Mode

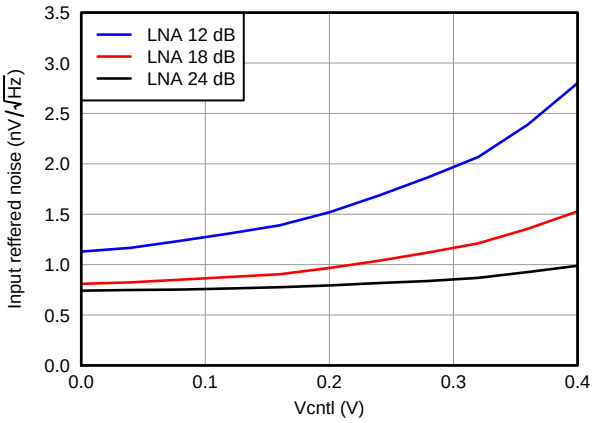


Figure 16. IRN, PGA = 24 dB and Low Noise Mode

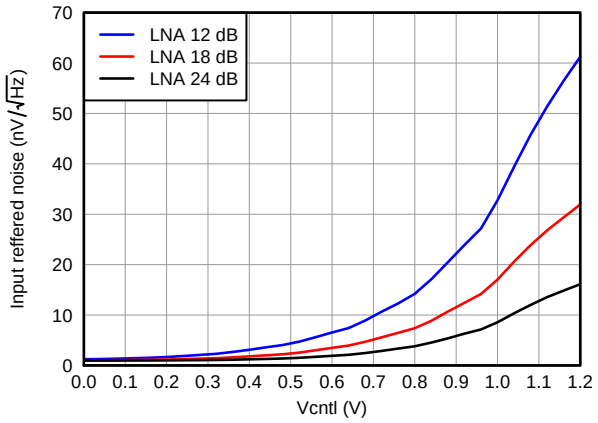


Figure 17. IRN, PGA = 24 dB and Medium Power Mode

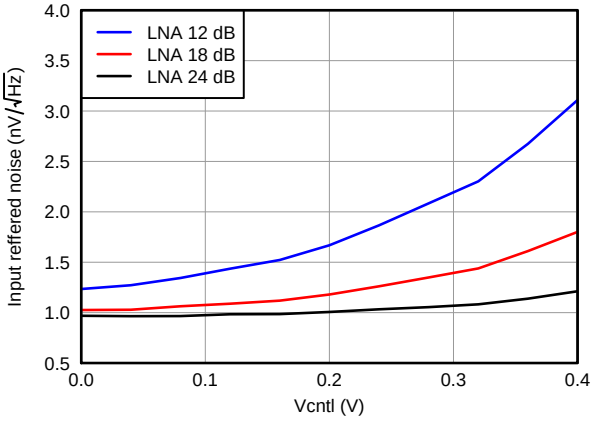


Figure 18. IRN, PGA = 24 dB and Medium Power Mode

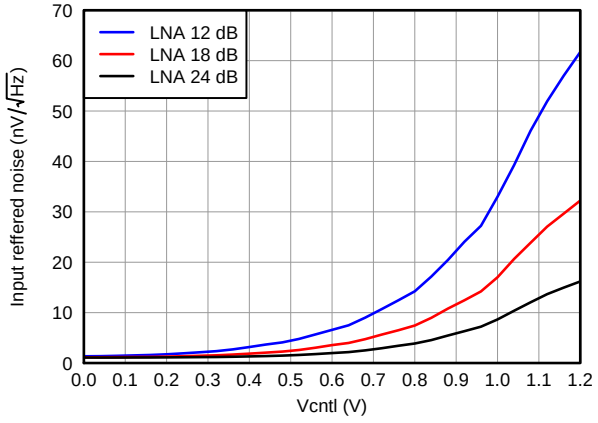


Figure 19. IRN, PGA = 24 dB and Low Power Mode

TYPICAL CHARACTERISTICS (continued)

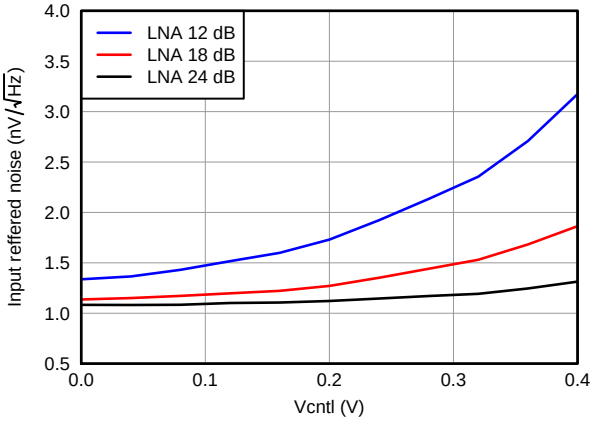


Figure 20. IRN, PGA = 24 dB and Low Power Mode

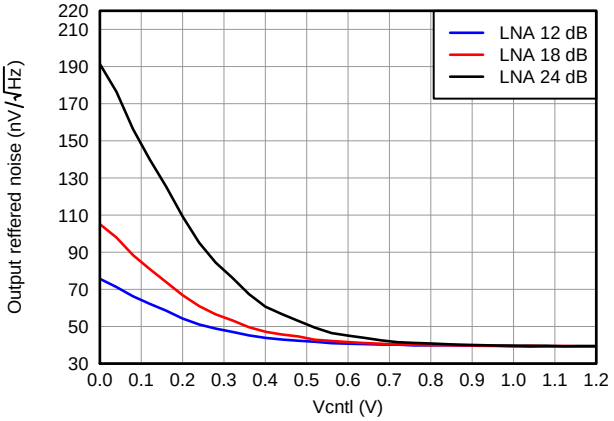


Figure 21. ORN, PGA = 24 dB and Low Noise Mode

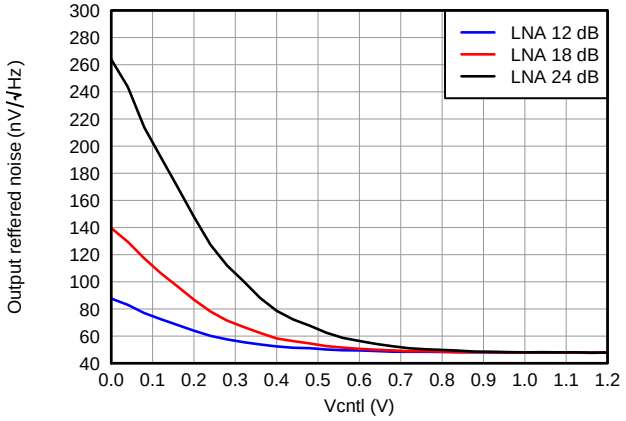


Figure 22. ORN, PGA = 24 dB and Medium Power Mode

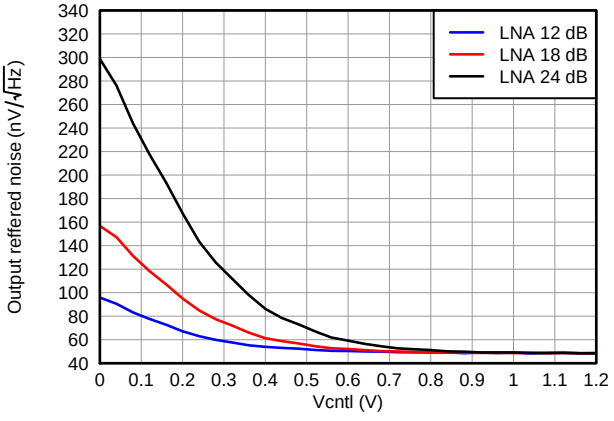


Figure 23. ORN, PGA = 24 dB and Low Power Mode

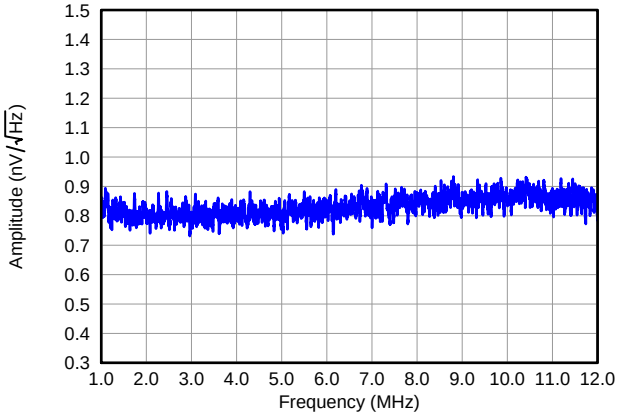


Figure 24. IRN, PGA = 24 dB and Low Noise Mode

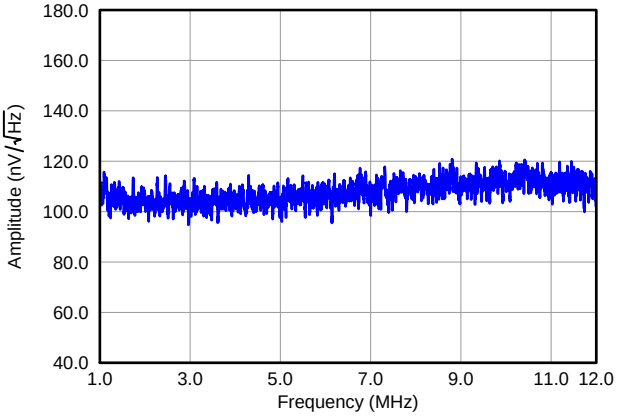


Figure 25. ORN, PGA = 24 dB and Low Noise Mode

TYPICAL CHARACTERISTICS (continued)

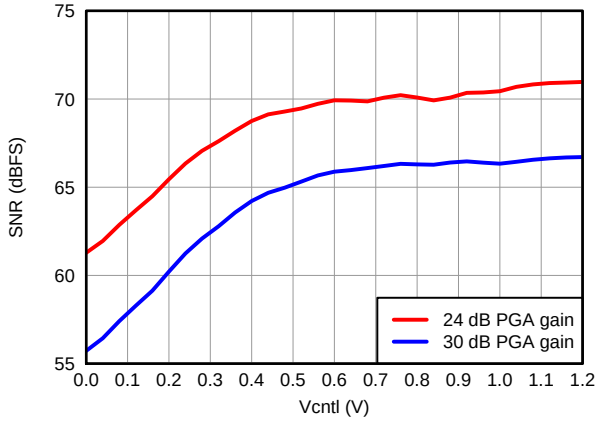


Figure 26. SNR, LNA = 18 dB and Low Noise Mode

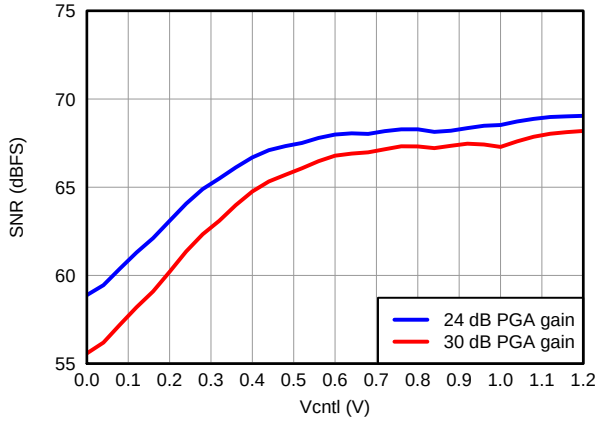


Figure 27. SNR, LNA = 18 dB and Low Power Mode

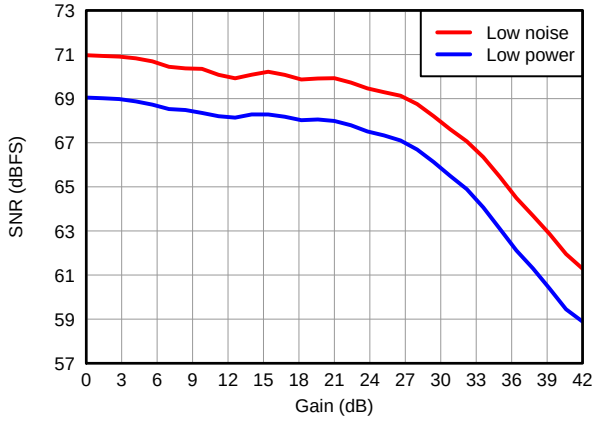


Figure 28. SNR vs. Different Power Modes

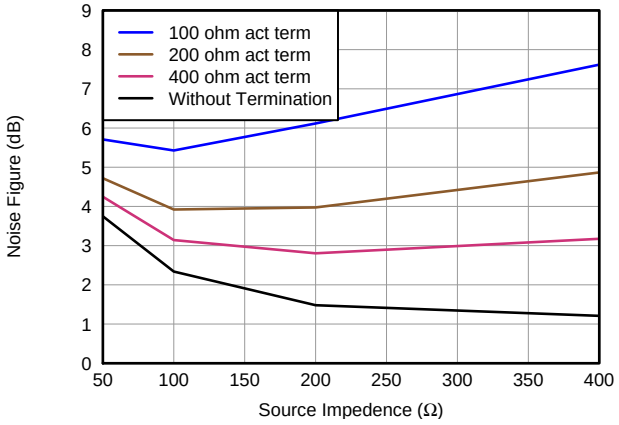


Figure 29. Noise Figure, LNA = 12 dB and Low Noise Mode

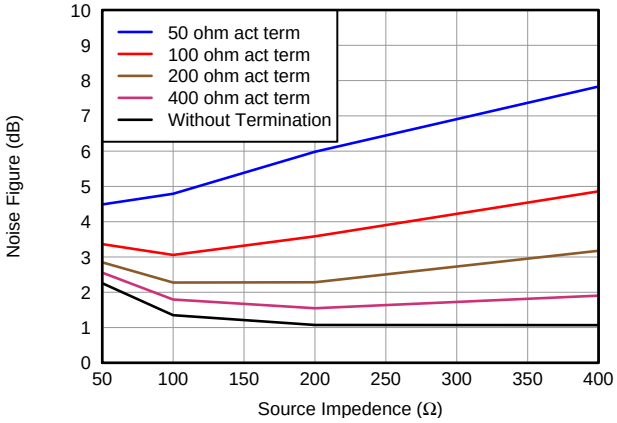


Figure 30. Noise Figure, LNA = 18 dB and Low Noise Mode

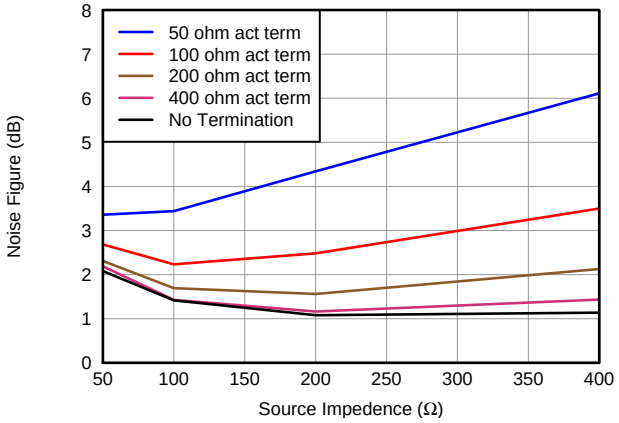


Figure 31. Noise Figure, LNA = 24 dB and Low Noise Mode

TYPICAL CHARACTERISTICS (continued)

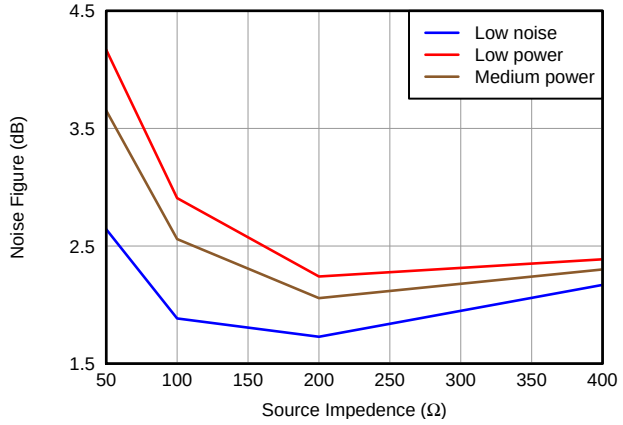


Figure 32. Noise Figure vs. Power Modes with 400 Ω Termination

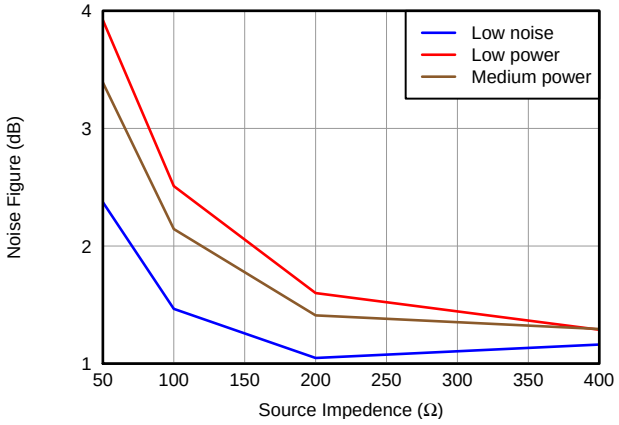


Figure 33. Noise Figure vs. Power Modes without Termination

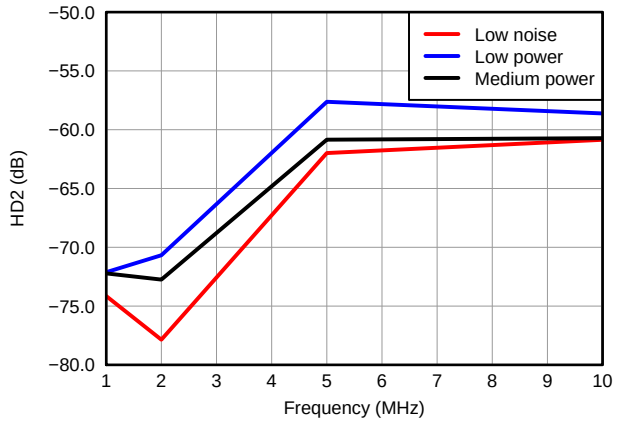


Figure 34. HD2 vs. Frequency, Vin = 500 mV_{PP} and V_{OUT} = -1 dBFS

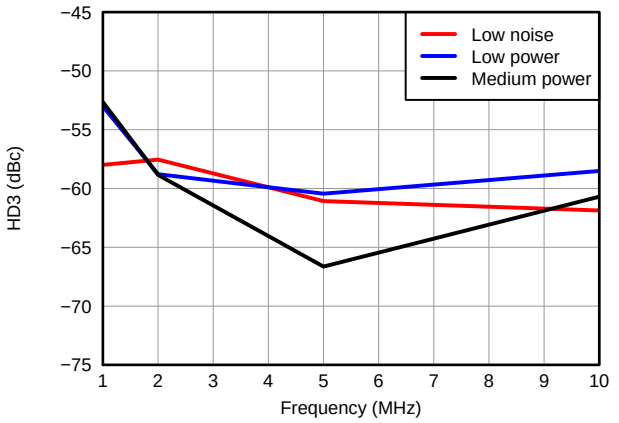


Figure 35. HD3 vs. Frequency, Vin = 500 mVpp and V_{OUT} = -1 dBFS

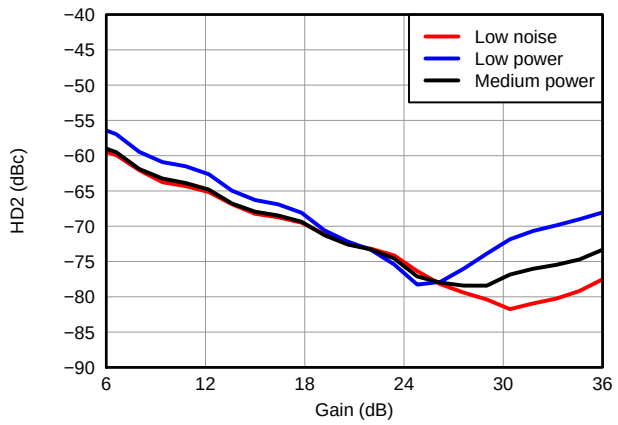


Figure 36. HD2 vs. Gain, LNA = 12 dB and PGA = 24 dB and V_{OUT} = -1 dBFS

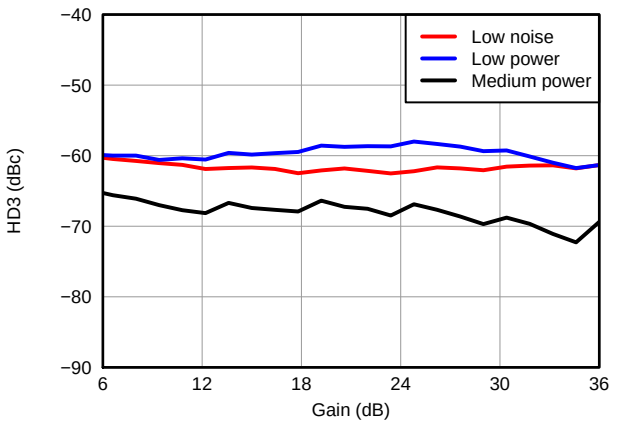


Figure 37. HD3 vs. Gain, LNA = 12 dB and PGA = 24 dB and V_{OUT} = -1 dBFS

TYPICAL CHARACTERISTICS (continued)

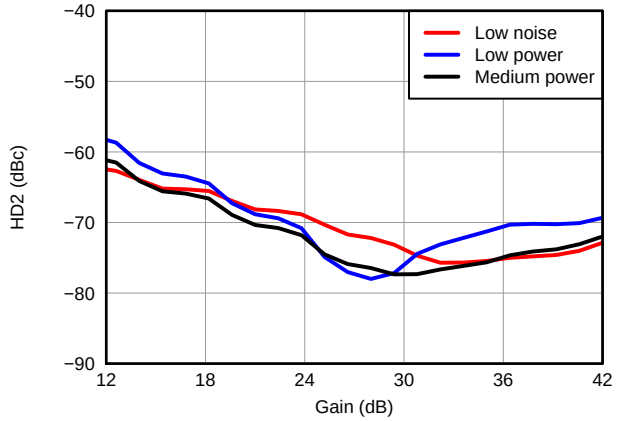


Figure 38. HD2 vs. Gain, LNA = 18 dB and PGA = 24 dB and V_{OUT} = -1 dBFS

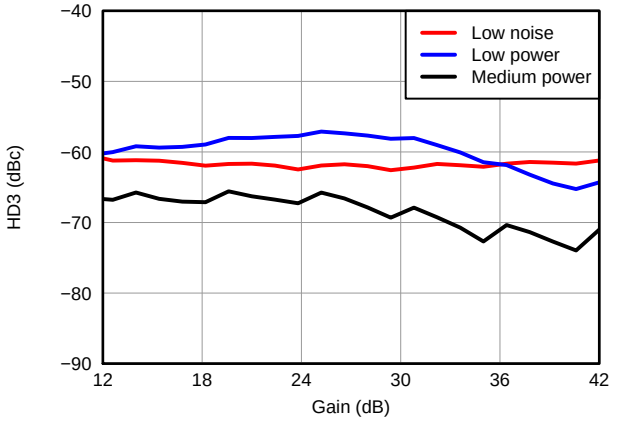


Figure 39. HD3 vs. Gain, LNA = 18 dB and PGA = 24 dB and V_{OUT} = -1 dBFS

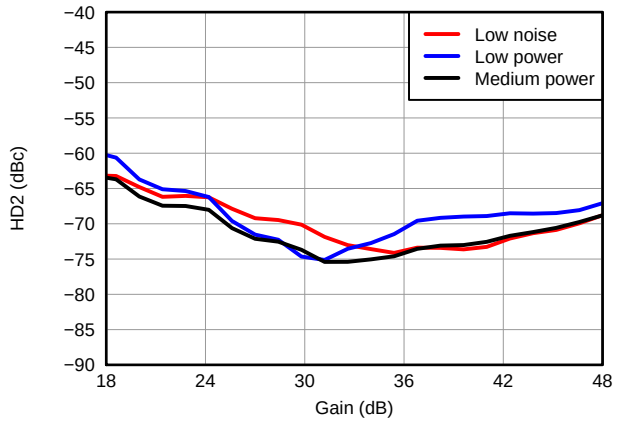


Figure 40. HD2 vs. Gain, LNA = 24 dB and PGA = 24 dB and V_{OUT} = -1 dBFS

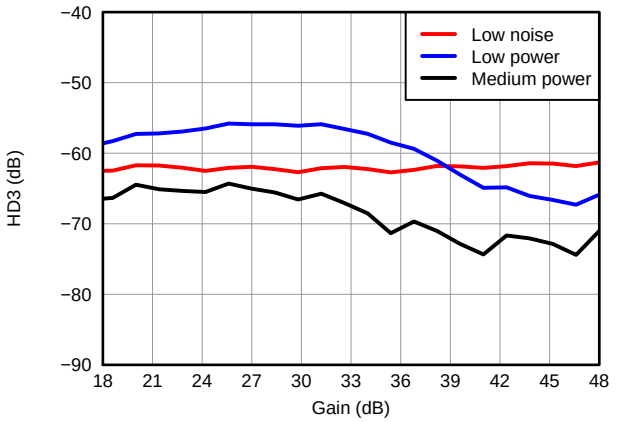


Figure 41. HD3 vs. Gain, LNA = 24 dB and PGA = 24 dB and V_{OUT} = -1 dBFS

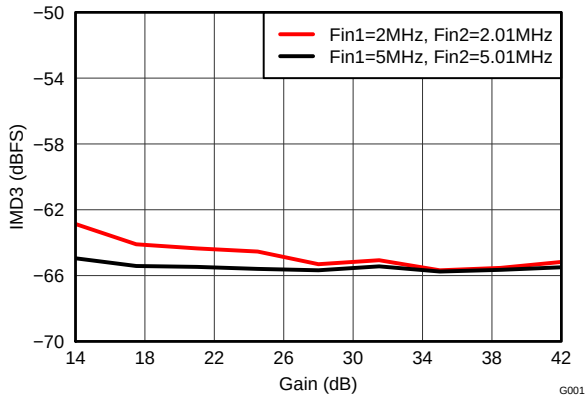


Figure 42. IMD3, Fout1 = -1 dBFS and Fout2 = -21 dBFS

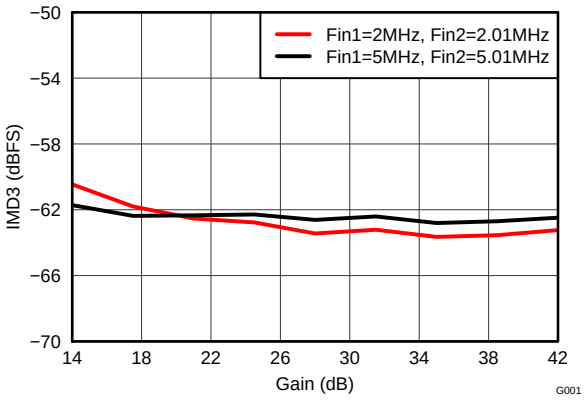


Figure 43. IMD3, Fout1 = -7dBFS and Fout2 = -7dBFS

TYPICAL CHARACTERISTICS (continued)

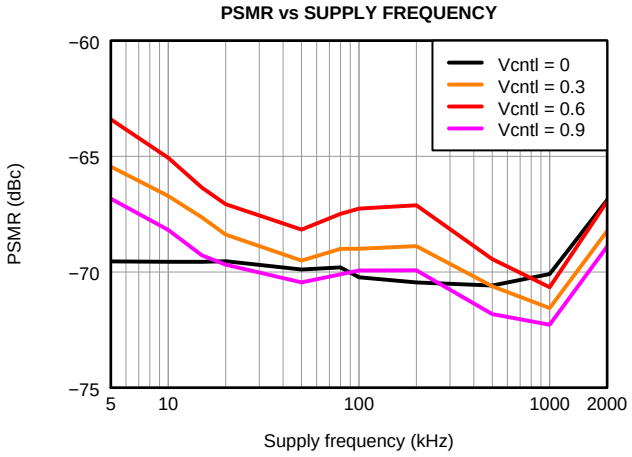


Figure 44. AVDD Power Supply Modulation Ratio, 100 mV_{PP} Supply Noise with Different Frequencies

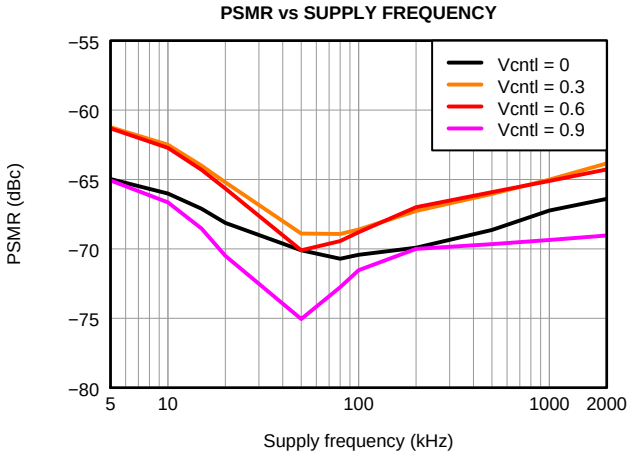


Figure 45. AVDD_5V Power Supply Modulation Ratio, 100mV_{PP} Supply Noise with Different Frequencies

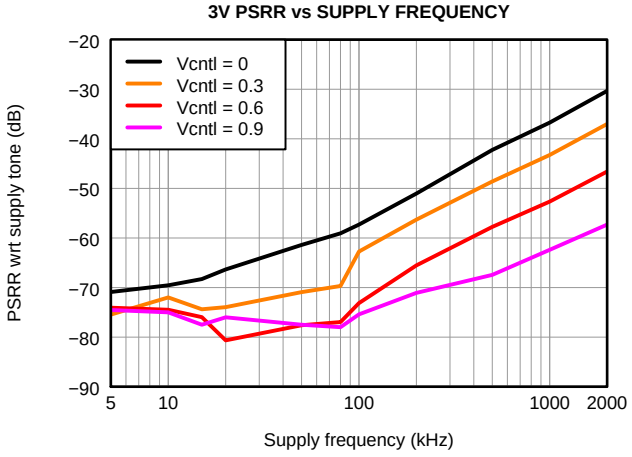


Figure 46. AVDD Power Supply Rejection Ratio, 100mV_{PP} Supply Noise with Different Frequencies

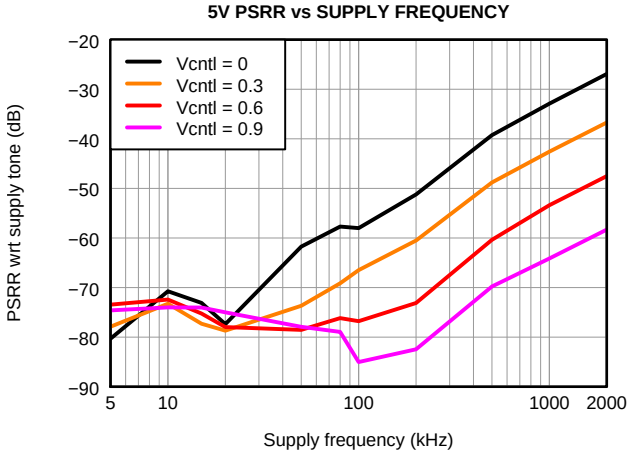


Figure 47. AVDD_5 V Power Supply Rejection Ratio, 100mV_{PP} Supply Noise with Different Frequencies

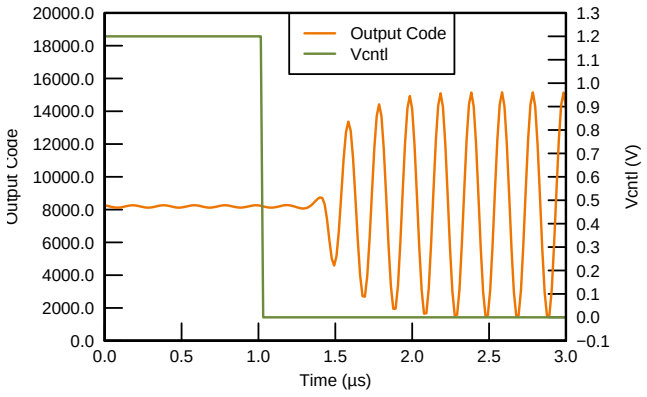


Figure 48. VCNTL Response Time, LNA = 18 dB and PGA = 24 dB

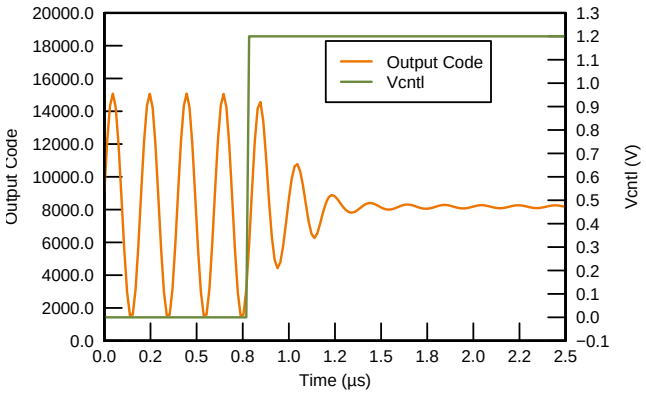


Figure 49. VCNTL Response Time, LNA = 18 dB and PGA = 24 dB

TYPICAL CHARACTERISTICS (continued)

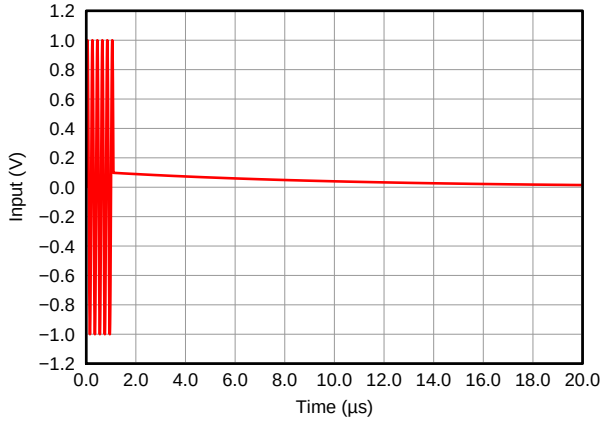


Figure 50. Pulse Inversion Asymmetrical Positive Input

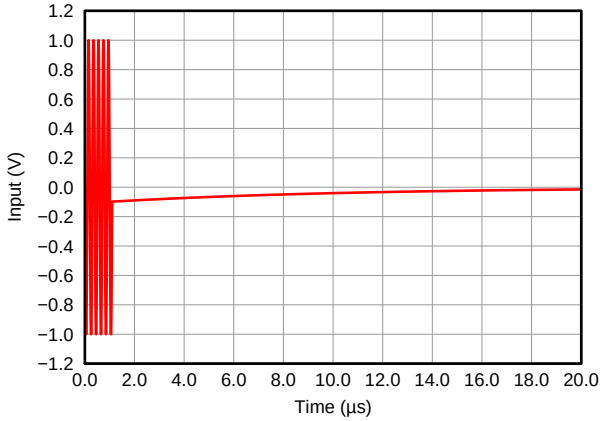


Figure 51. Pulse Inversion Asymmetrical Negative Input

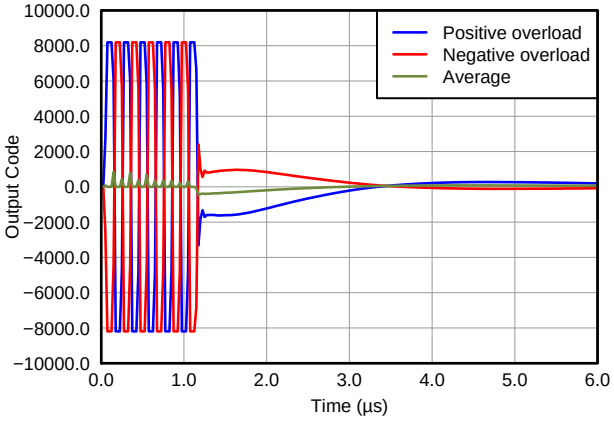


Figure 52. Pulse Inversion, V_{IN} = 2 V_{PP}, PRF = 1 KHz, Gain = 21 dB

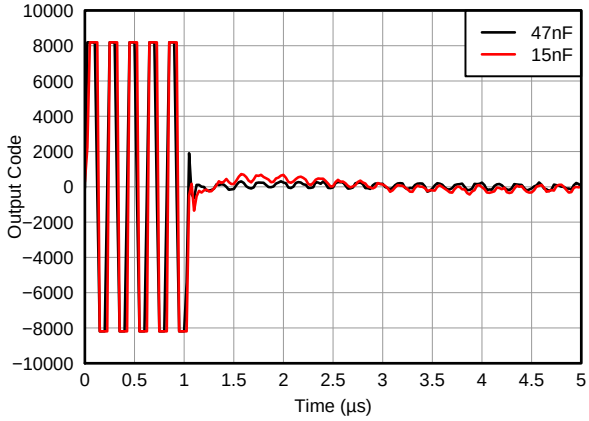


Figure 53. Overload Recovery Response vs. INM Capacitor, V_{IN} = 50 mV_{PP}/100 μV_{PP}, Max Gain

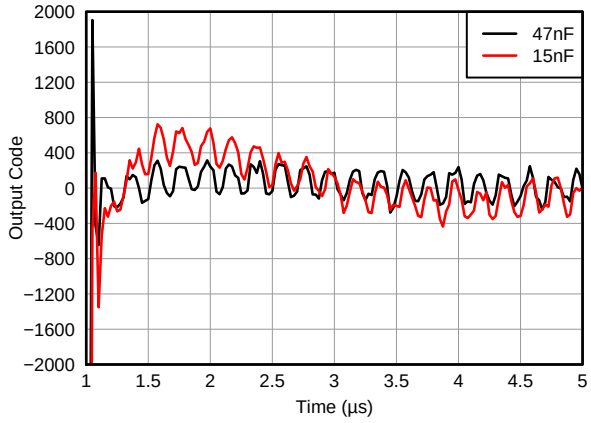


Figure 54. Overload Recovery Response vs. INM Capacitor (Zoomed), V_{IN} = 50 mV_{PP}/100 μV_{PP}, Max Gain

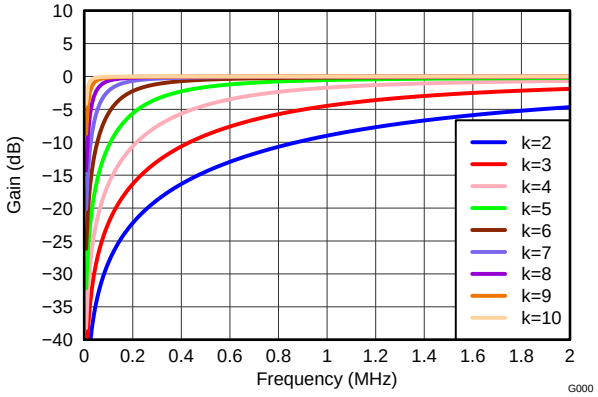


Figure 55. Digital High-Pass Filter Response

TIMING CHARACTERISTICS(1)

Typical values are at 25°C, AVDD_5V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V, Differential clock, C_{LOAD} = 5pF, R_{LOAD} = 100 Ω, 14Bit, sample rate = 65MSPS, unless otherwise noted. Minimum and maximum values are across the full temperature range T_{MIN} = 0°C to T_{MAX} = 85°C with AVDD_5V = 5 V, AVDD = 3.3 V, AVDD_ADC = 1.8 V, DVDD = 1.8 V

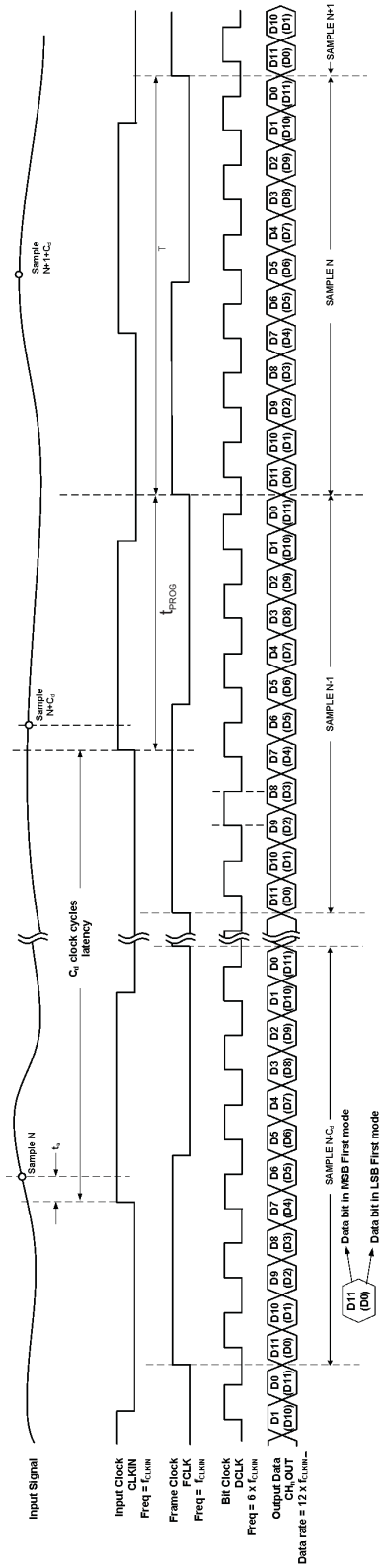
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ta	Aperture delay	The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs	0.7	3		ns
	Aperture delay matching	Across channels within the same device		±150		ps
t_j	Aperture jitter			450		Fs rms
	ADC latency	Default, after reset, or / 0 x 2 [12] = 1, LOW_LATENCY = 1		11/8		Input clock cycles
t_{delay}	Data and frame clock delay	Input clock rising edge (zero cross) to frame clock rising edge (zero cross) minus 3/7 of the input clock period (T).	3	5.4	7	ns
Δt_{delay}	Delay variation	At fixed supply and 20°C T difference. Device to device	–1		1	ns
t_{RISE}	Data rise time Data fall time	Rise time measured from –100 mV to 100 mV Fall time measured from 100 mV to –100 mV 10 MHz < f_{CLKIN} < 65 MHz		0.14		ns
t_{FALL}				0.15		
$t_{FCLKRISE}$	Frame clock rise time Frame clock fall time	Rise time measured from –100mV to 100mV Fall time measured from 100 mV to –100 mV 10 MHz < f_{CLKIN} < 65MHz		0.14		ns
$t_{FCLKFALL}$				0.15		
	Frame clock duty cycle	Zero crossing of the rising edge to zero crossing of the falling edge	48%	50%	52%	
$t_{DCLKRISE}$	Bit clock rise time Bit clock fall time	Rise time measured from –100mV to 100mV Fall time measured from 100 mV to –100 mV 10 MHz < f_{CLKIN} < 65MHz		0.13		ns
$t_{DCLKFALL}$				0.12		
	Bit clock duty cycle	Zero crossing of the rising edge to zero crossing of the falling edge 10 MHz < f_{CLKIN} < 65 MHz	46%		54%	

(1) Timing parameters are ensured by design and characterization; not production tested.

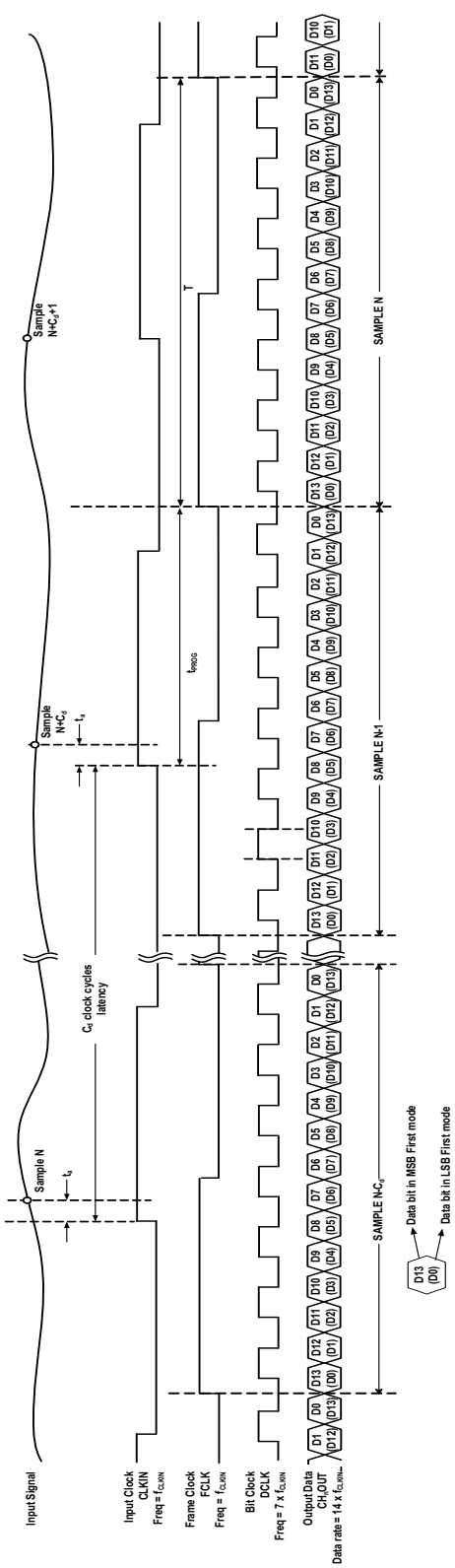
OUTPUT INTERFACE TIMING(1)(2)(3)

f_{CLKIN}, Input Clock Frequency	Setup Time (t_{su}), ns (for output data and frame clock)			Hold Time (t_h), ns (for output data and frame clock)			t_{PROG} = (3/7)x T + t_{delay}, ns		
	Data Valid to Input Clock Zero-Crossing			Input Clock Zero-Crossing to Data Invalid			Input Clock Zero-Cross (rising edge) to Frame Clock Zero-Cross (rising edge)		
MHz	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
65/14bit	0.24	0.37		0.24	0.38		11	12	12.5
50/14bit	0.41	0.54		0.46	0.57		13	13.9	14.4
40/14bit	0.55	0.70		0.61	0.73		15	16	16.7
30/14bit	0.87	1.10		0.94	1.1		18.5	19.5	20.1
20/14bit	1.30	1.56		1.46	1.6		25.7	26.7	27.3

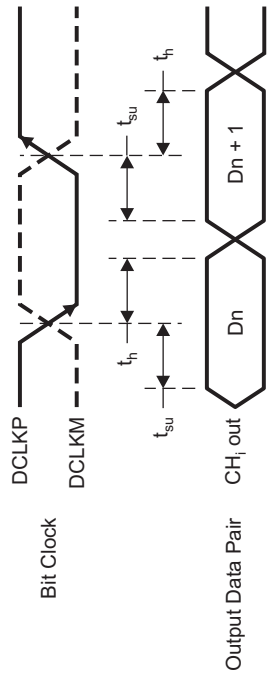
(1) FCLK timing is the same as for the output data lines. It has the same relation to DCLK as the data pins. Setup and hold are the same for the data and the frame clock.
(2) Data valid is logic HIGH = +100mV and logic LOW = -100mV
(3) Timing parameters are ensured by design and characterization; not production tested.



12-Bit 6x serialization mode



14-Bit 7x serialization mode



LVDS Setup and Hold Timing

Figure 56. LVDS Timing Diagrams

LVDS Output Interface Description

AFE5803 has LVDS output interface which supports multiple output formats. The ADC resolutions can be configured as 12bit or 14bit as shown in the LVDS timing diagrams Figure 56. The ADCs in the AFE5803 are running at 14bit; 2 LSBs are removed when 12-bit output is selected; and two 0s are added at LSBs when 16-bit output is selected. Appropriate ADC resolutions can be selected for optimizing system performance-cost effectiveness. When the devices run at 16bit mode, higher end FPGAs are required to process higher rate of LVDS data. Corresponding register settings are listed in Table 1.

Table 1. Corresponding Register Settings

LVDS Rate	12 bit (6X DCLK)	14 bit (7X DCLK)	16 bit (8X DCLK)
Reg 3 [14:13]	11	00	01
Reg 4 [2:0]	010	000	000
Description	2 LSBs removed	N/A	2 0s added at LSBs

SERIAL REGISTER TIMING

Serial Register Write Description

Programming of different modes can be done through the serial interface formed by pins SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface data) and RESET. All these pins have a pull-down resistor to GND of 100kΩ. Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA is latched at every rising edge of SCLK when SEN is active (low). The serial data is loaded into the register at every 24th SCLK rising edge when SEN is low. If the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiple of 24-bit words within a single active SEN pulse (there is an internal counter that counts groups of 24 clocks after the falling edge of SEN). The interface can work with the SCLK frequency from 20 MHz down to low speeds (few Hertz) and even with non-50% duty cycle SCLK. The data is divided into two main portions: a register address (8 bits) and the data itself (16 bits), to load on the addressed register. When writing to a register with unused bits, these should be set to 0. Figure 57 illustrates this process.

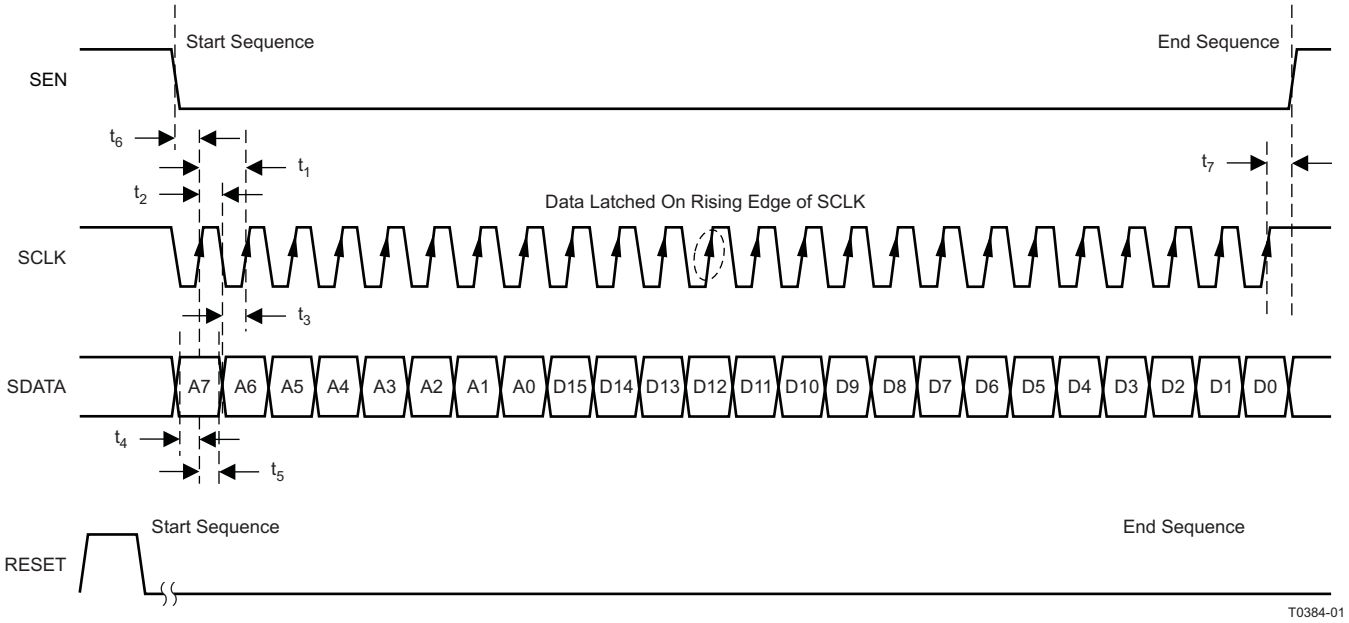


Figure 57. SPI Timing

SPI Timing Characteristics

Minimum values across full temperature range T_{MIN} = 0°C to T_{MAX} = 85°C, AVDD_5V =5.0V, AVDD=3.3V, AVDD_ADC=1.8V, DVDD=1.8V

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_1	SCLK period	50			ns
t_2	SCLK high time	20			ns
t_3	SCLK low time	20			ns
t_4	Data setup time	5			ns
t_5	Data hold time	5			ns
t_6	$\overline{SEN}$ fall to SCLK rise	8			ns
t_7	Time between last SCLK rising edge to $\overline{SEN}$ rising edge	8			ns
t_8	SDOUT delay	12	20	28	ns

Register Readout

The device includes an option where the contents of the internal registers can be read back. This may be useful as a diagnostic test to verify the serial interface communication between the external controller and the AFE. First, the <REGISTER READOUT ENABLE> bit (Reg0[1]) needs to be set to '1'. Then user should initiate a serial interface cycle specifying the address of the register (A7-A0) whose content has to be read. The data bits are "don't care". The device will output the contents (D15-D0) of the selected register on the SDOUT pin. SDOUT has a typical delay t8 of 20nS from the falling edge of the SCLK. For lower speed SCLK, SDOUT can be latched on the rising edge of SCLK. For higher speed SCLK,e.g. the SCLK period lesser than 60nS, it would be better to latch the SDOUT at the next falling edge of SCLK. The following timing diagram shows this operation (the time specifications follow the same information provided. In the readout mode, users still can access the <REGISTER READOUT ENABLE> through SDATA/SCLK/SEN. To enable serial register writes, set the <REGISTER READOUT ENABLE> bit back to '0'.

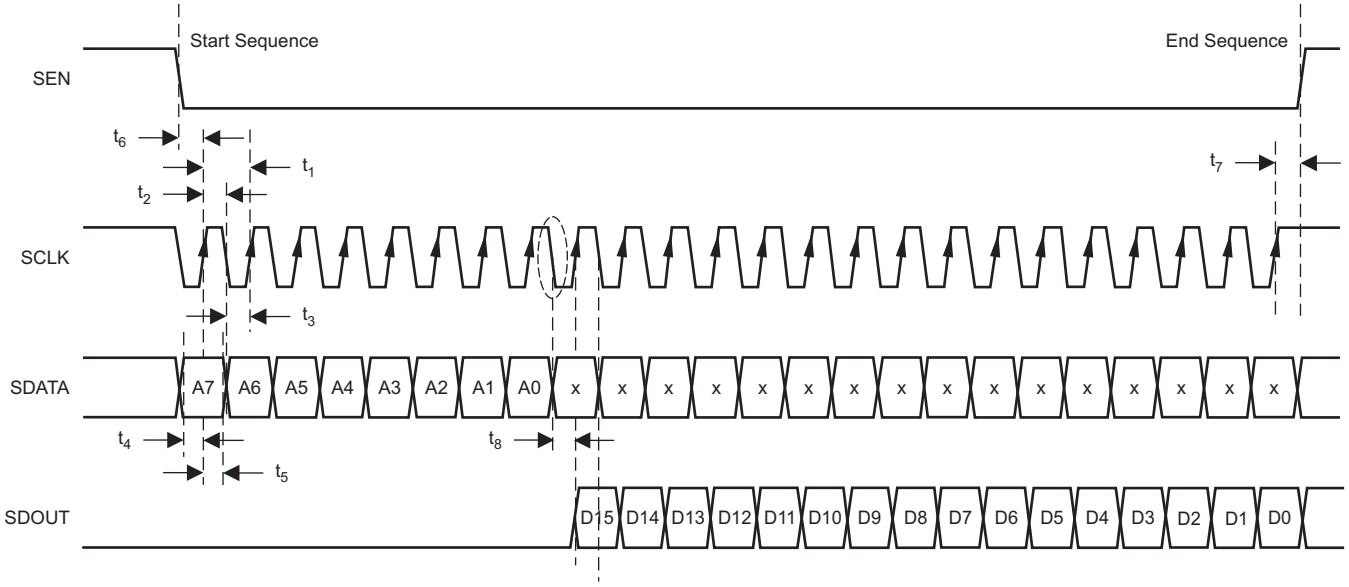
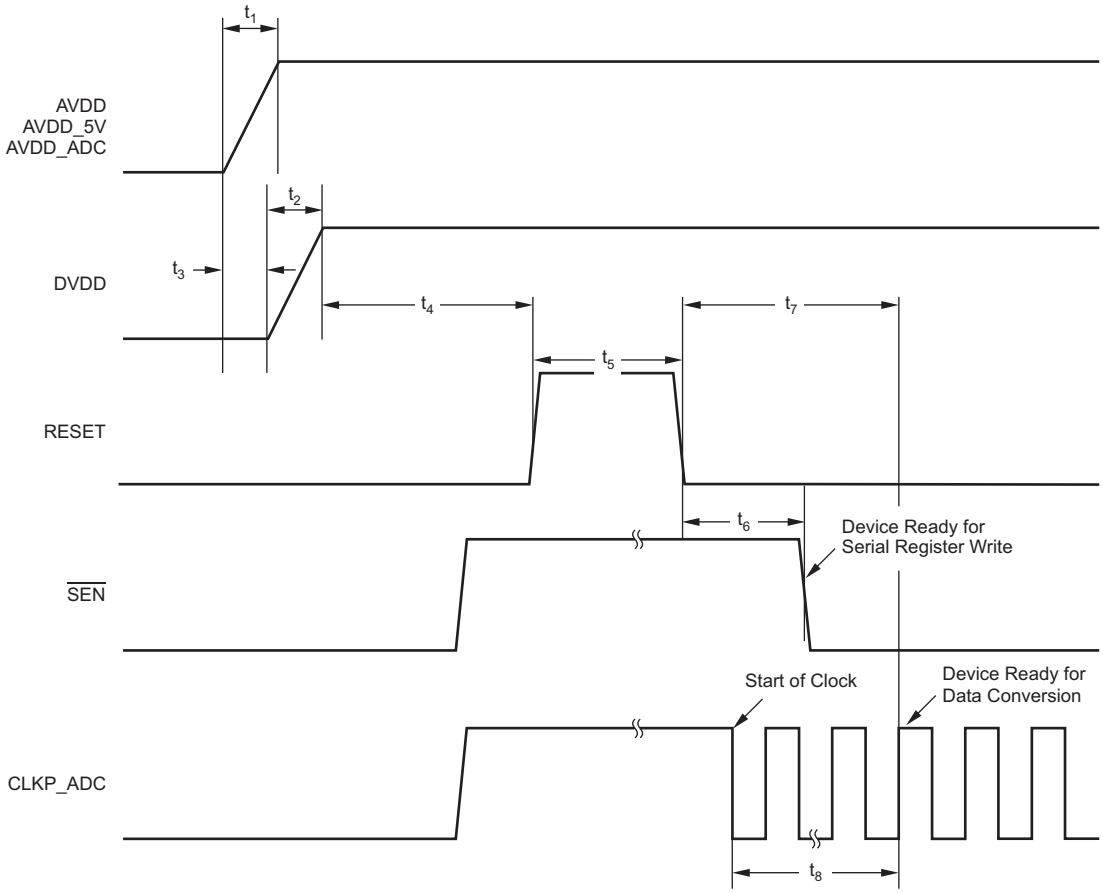


Figure 58. Serial Interface Register Read

The AFE5803 SDOUT buffer is tri-stated and will get enabled only when 0[1] (REGISTER READOUT ENABLE) is enabled. SDOUT pins from multiple AFE5803s can be tied together without any pull-up resistors. Level shifter SN74AUP1T04 can be used to convert 1.8V logic to 2.5V/3.3V logics if needed.



10 µs < t1 < 50 ms, 10 µs < t2 < 50 ms, –10 ms < t3 < 10 ms, t4 > 10 ms, t5 > 100 ns, t6 > 100 ns, t7 > 10 ms, and t8 > 100 µs.

The AVDDx and DVDD power-on sequence does not matter as long as –10ms < t3 < 10ms. Similar considerations apply while shutting down the device.

Figure 59. Recommended Power-up Sequencing and Reset Timing

REGISTER MAP

ADC Register Map

A reset process is required at the AFE5803 initialization stage. Initialization can be done in one of two ways:

1. Through a hardware reset, by applying a positive pulse at the RESET pin
2. Through a software reset, using the serial interface, by setting the SOFTWARE RESET bit to high. Setting this bit initializes the internal registers to the respective default values (all zeros) and then self-resets the SOFTWARE RESET bit to low. In this case, the RESET pin can stay low (inactive).

After reset, all ADC and VCA registers are set to ‘0’, i.e. default settings. During register programming, all reserved/unlisted register bits need to be set as ‘0’. Register settings are maintained when the AFE5803 is in either partial power down mode or complete power down mode.

Table 2. ADC Register Map

ADDRESS (DEC)	ADDRESS (HEX)	Default Value	FUNCTION	DESCRIPTION
0[0]	0x0[0]	0	SOFTWARE_RESET	0: Normal operation; 1: Resets the device and self-clears the bit to '0'
0[1]	0x0[1]	0	REGISTER_READOUT_ENABLE	0:Disables readout; 1: enables readout of register at SDOUT Pin
1[0]	0x1[0]	0	ADC_COMPLETE_PDN	0: Normal 1: Complete Power down
1[1]	0x1[1]	0	LVDS_OUTPUT_DISABLE	0: Output Enabled; 1: Output disabled
1[9:2]	0x1[9:2]	0	ADC_PDN_CH<7:0>	0: Normal operation; 1: Power down. Power down Individual ADC channels. 1[9]→CH8…1[2]→CH1
1[10]	0x1[10]	0	PARTIAL_PDN	0: Normal Operation; 1: Partial Power Down ADC
1[11]	0x1[11]	0	LOW_FREQUENCY_ NOISE_SUPPRESSION	0: No suppression; 1: Suppression Enabled
1[13]	0x1[13]	0	EXT_REF	0: Internal Reference; 1: External Reference. VREF_IN is used. Both 3[15] and 1[13] should be set as 1 in the external reference mode
1[14]	0x1[14]	0	LVDS_OUTPUT_RATE_2X	0: 1x rate; 1: 2x rate. Combines data from 2 channels on 1 LVDS pair. When ADC clock rate is low, this feature can be used
1[15]	0x1[15]	0	SINGLE-ENDED_CLK_MODE	0: Differential clock input; 1: Single-ended clock input
2[2:0]	0x2[2:0]	0	RESERVED	Set to 0
2[10:3]	0x2[10:3]	0	POWER-DOWN_LVDS	0: Normal operation; 1: PDN Individual LVDS outputs. 2[10]→CH8…2[3]→CH1
2[11]	0x2[11]	0	AVERAGING_ENABLE	0: No averaging; 1: Average 2 channels to increase SNR
2[12]	0x2[12]	0	LOW_LATENCY	0: Default Latency with digital features supported, 11 cycle latency 1: Low Latency with digital features bypassed, 8 cycle latency
2[15:13]	0x2[15:3]	0	TEST_PATTERN_MODES	000: Normal operation; 001: Sync; 010: De-skew; 011: Custom; 100:All 1's; 101: Toggle; 110: All 0's; 111: Ramp
3[7:0]	0x3[7:0]	0	INVERT_CHANNELS	0: No inverting; 1:Invert channel digital output. 3[7]→CH8;3[0]→CH1
3[8]	0x3[8]	0	CHANNEL_OFFSET_ SUBSTRACTION_ENABLE	0: No offset subtraction; 1: Offset value Subtract Enabled
3[9:11]	0x3[9:11]	0	RESERVED	Set to 0
3[12]	0x3[12]	0	DIGITAL_GAIN_ENABLE	0: No digital gain; 1: Digital gain Enabled

Table 2. ADC Register Map (continued)

ADDRESS (DEC)	ADDRESS (HEX)	Default Value	FUNCTION	DESCRIPTION
3[14:13]	0x3[14:13]	0	SERIALIZED_DATA_RATE	Serialization factor 00: 14x 01: 16x 10: reserved 11: 12x when 4[1]=1. In the 16x serialization rate, two 0s are filled at two LSBs (see Table 1)
3[15]	0x3[15]	0	ENABLE_EXTERNAL_ REFERENCE_MODE	0: Internal reference mode; 1: Set to external reference mode Note: both 3[15] and 1[13] should be set as 1 when configuring the device in the external reference mode
4[1]	0x4[1]	0	ADC_RESOLUTION_SELECT	0: 14bit; 1: 12bit
4[3]	0x4[3]	0	ADC_OUTPUT_FORMAT	0: 2's complement; 1: Offset binary
4[4]	0x4[4]	0	LSB_MSB_FIRST	0: LSB first; 1: MSB first
5[13:0]	0x5[13:0]	0	CUSTOM_PATTERN	Custom pattern data for LVDS output (2[15:13]=011)
10[8]	0xA[8]	0	SYNC_PATTERN	0: Test pattern outputs of 8 channels are NOT synchronized. 1: Test pattern outputs of 8 channels are synchronized.
13[9:0]	0xD[9:0]	0	OFFSET_CH1	Value to be subtracted from channel 1 code
13[15:11]	0xD[15:11]	0	DIGITAL_GAIN_CH1	0 dB to 6 dB in 0. 2dB steps
15[9:0]	0xF[9:0]	0	OFFSET_CH2	value to be subtracted from channel 2 code
15[15:11]	0xF[15:11]	0	DIGITAL_GAIN_CH2	0dB to 6dB in 0.2 dB steps
17[9:0]	0x11[9:0]	0	OFFSET_CH3	value to be subtracted from channel 3 code
17[15:11]	0x11[15:11]	0	DIGITAL_GAIN_CH3	0 dB to 6 dB in 0.2 dB steps
19[9:0]	0x13[9:0]	0	OFFSET_CH4	value to be subtracted from channel 4 code
19[15:11]	0x13[15:11]	0	DIGITAL_GAIN_CH4	0 dB to 6 dB in 0. 2dB steps
21[0]	0x15[0]	0	DIGITAL_HPF_FILTER_ENABLE _ CH1-4	0: Disable the digital HPF filter; 1: Enable for 1-4 channels
21[4:1]	0x15[4:1]	0	DIGITAL_HPF_FILTER_K_CH1-4	Set K for the high-pass filter (k from 2 to 10, i.e. 0010B to 1010B). This group of four registers controls the characteristics of a digital high-pass transfer function applied to the output data, following the formula: $y(n) = 2^k/(2^k + 1) [x(n) – x(n – 1) + y(n – 1)]$ (see Table 3 and Figure 55)
25[9:0]	0x19[9:0]	0	OFFSET_CH8	value to be subtracted from channel 8 code
25[15:11]	0x19[15:11]	0	DIGITAL_GAIN_CH8	0 dB to 6 dB in 0.2dB steps
27[9:0]	0x1B[9:0]	0	OFFSET_CH7	value to be subtracted from channel 7 code
27[15:11]	0x1B[15:11]	0	DIGITAL_GAIN_CH7	0 dB to 6dB in 0.2 dB steps
29[9:0]	0x1D[9:0]	0	OFFSET_CH6	value to be subtracted from channel 6 code
29[15:11]	0x1D[15:11]	0	DIGITAL_GAIN_CH6	0 dB to 6 dB in 0.2 dB steps
31[9:0]	0x1F[9:0]	0	OFFSET_CH5	value to be subtracted from channel 5 code
31[15:11]	0x1F[15:11]	0	DIGITAL_GAIN_CH5	0 dB to 6 dB in 0.2 dB steps
33[0]	0x21[0]	0	DIGITAL_HPF_FILTER_ENABLE _ CH5-8	0: Disable the digital HPF filter; 1: Enable for 5-8 channels
33[4:1]	0x21[4:1]	0	DIGITAL_HPF_FILTER_K_CH5-8	Set K for the high-pass filter (k from 2 to 10, 010B to 1010B) This group of four registers controls the characteristics of a digital high-pass transfer function applied to the output data, following the formula: $y(n) = 2^k/(2^k + 1) [x(n) – x(n – 1) + y(n – 1)]$ (see Table 3 and Figure 55)
66[15]	0x42[15]	0	DITHER	0: Disable dither function. 1: Enable dither function. Improve the ADC linearity with slight noise degradation.

ADC Register/Digital Processing Description

The ADC in the AFE5803 has extensive digital processing functionalities which can be used to enhance ultrasound system performance. The digital processing blocks are arranged as in Figure 60.

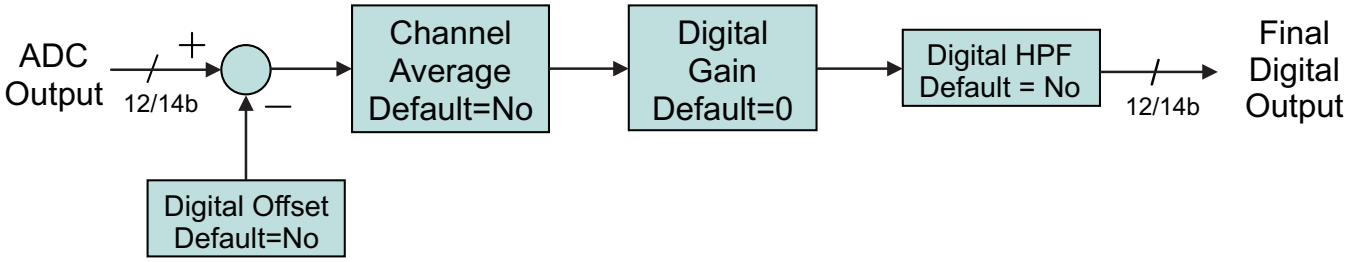


Figure 60. ADC Digital Block Diagram

AVERAGING_ENABLE: Address: 2[11]

When set to 1, two samples, corresponding to two consecutive channels, are averaged (channel 1 with 2, 3 with 4, 5 with 6, and 7 with 8). If both channels receive the same input, the net effect is an improvement in SNR. The averaging is performed as:

- Channel 1 + channel 2 comes out on channel 3
- Channel 3 + channel 4 comes out on channel 4
- Channel 5 + channel 6 comes out on channel 5
- Channel 7 + channel 8 comes out on channel 6

ADC_OUTPUT_FORMAT: Address: 4[3]

The ADC output, by default, is in 2's-complement mode. Programming the ADC_OUTPUT_FORMAT bit to 1 inverts the MSB, and the output becomes straight-offset binary mode.

DIGITAL_GAIN_ENABLE: Address: 3[12]

Setting this bit to 1 applies to each channel i the corresponding gain given by DIGTAL_GAIN_CHi <15:11>. The gain is given as 0dB + 0.2dB × DIGTAL_GAIN_CHi<15:11>. For instance, if DIGTAL_GAIN_CH5<15:11> = 3, channel 5 is increased by 0.6dB gain. DIGTAL_GAIN_CHi <15:11> = 31 produces the same effect as DIGTAL_GAIN_CHi <15:11> = 30, setting the gain of channel i to 6dB.

DIGITAL_HPF_ENABLE

- CH1-4: Address 21[0]
- CH5-8: Address 33[0]

DIGITAL_HPF_FILTER_K_CHX

- CH1-4: Address 21[4:1]
- CH5-8: Address 3[4:1]

This group of registers controls the characteristics of a digital high-pass transfer function applied to the output data, following Equation 1.

$$y(n) = \frac{2^k}{2^k + 1}\left[x(n) - x(n-1) + y(n-1)\right] \quad (1)$$

These digital HPF registers (one for the first four channels and one for the second group of four channels) describe the setting of K. The digital high pass filter can be used to suppress low frequency noise which commonly exists in ultrasound echo signals. The digital filter can significantly benefit near field recovery time due to T/R switch low frequency response. Table 3 shows the cut-off frequency vs K, also see Figure 55.

Table 3. Digital HPF –1dB Corner Frequency vs K and Fs

k	40 MSPS	50 MSPS	65 MSPS
2	2780 KHz	3480 KHz	4520 KHz
3	1490 KHz	1860 KHz	2420 KHz
4	770 KHz	960 KHz	1250 KHz

LOW_FREQUENCY_NOISE_SUPPRESSION: Address: 1[11]

The low-frequency noise suppression mode is especially useful in applications where good noise performance is desired in the frequency band of 0MHz to 1MHz (around dc). Setting this mode shifts the low-frequency noise of the AFE5803 to approximately Fs/2, thereby moving the noise floor around dc to a much lower value. Register bit 1[11] is used for enabling or disabling this feature. When this feature is enabled, power consumption of the device will be increased by approximate 1 mW/CH.

LVDS_OUTPUT_RATE_2X: Address: 1[14]

The output data always uses a DDR format, with valid/different bits on the positive as well as the negative edges of the LVDS bit clock, DCLK. The output rate is set by default to 1X (LVDS_OUTPUT_RATE_2X = 0), where each ADC has one LVDS stream associated with it. If the sampling rate is low enough, two ADCs can share one LVDS stream, in this way lowering the power consumption devoted to the interface. The unused outputs will output zero. To avoid consumption from those outputs, no termination should be connected to them. The distribution on the used output pairs is done in the following way:

- Channel 1 and channel 2 come out on channel 3. Channel 1 comes out first.
- Channel 3 and channel 4 come out on channel 4. Channel 3 comes out first.
- Channel 5 and channel 6 come out on channel 5. Channel 5 comes out first.
- Channel 7 and channel 8 come out on channel 6. Channel 7 comes out first

CHANNEL_OFFSET_SUBSTRACTION_ENABLE: Address: 3[8]

Setting this bit to 1 enables the subtraction of the value on the corresponding OFFSET_CHx<9:0> (offset for channel i) from the ADC output. The number is specified in 2s-complement format. For example, OFFSET_CHx<9:0> = 11 1000 0000 means subtract –128. For OFFSET_CHx<9:0> = 00 0111 1111 the effect is to subtract 127. In effect, both addition and subtraction can be performed. Note that the offset is applied before the digital gain (see DIGITAL_GAIN_ENABLE). The whole data path is 2s-complement throughout internally, with digital gain being the last step. Only when ADC_OUTPUT_FORMAT=1 (straight binary output format) is the 2s-complement word translated into offset binary at the end.

SERIALIZED_DATA_RATE: Address: 3[14:13]

See Table 1 for detail description.

TEST_PATTERN_MODES: Address: 2[15:13]

The AFE5803 can output a variety of test patterns on the LVDS outputs. These test patterns replace the normal ADC data output. The device may also be made to output 6 preset patterns:

1. **Ramp:** Setting Register 2[15:13]=111causes all the channels to output a repeating full-scale ramp pattern. The ramp increments from zero code to full-scale code in steps of 1LSB every clock cycle. After hitting the full-scale code, it returns back to zero code and ramps again.
2. **Zeros:** The device can be programmed to output all zeros by setting Register 2[15:13]=110;
3. **Ones:** The device can be programmed to output all 1s by setting Register 2[15:13]=100;
4. **Deskew Patten:** When 2[15:13]=010; this mode replaces the 14-bit ADC output with the 01010101010101 word.
5. **Sync Pattern:** When 2[15:13]=001, the normal ADC output is replaced by a fixed 11111110000000 word.
6. **Toggle:** When 2[15:13]=101, the normal ADC output is alternating between 1's and 0's. The start state of ADC word can be either 1's or 0's.
7. **Custom Pattern:** It can be enabled when 2[15:13]= 011;. Users can write the required VALUE into register bits <CUSTOM PATTERN> which is Register 5[13:0]. Then the device will output VALUE at its outputs, about 3 to 4 ADC clock cycles after the 24th rising edge of SCLK. So, the time taken to write one value is 24

SCLK clock cycles + 4 ADC clock cycles. To change the customer pattern value, users can repeat writing Register 5[13:0] with a new value. Due to the speed limit of SPI, the refresh rate of the custom pattern may not be high. For example, 128 points custom pattern will take approximately 128 x (24 SCLK clock cycles + 4 ADC clock cycles).

NOTE

only one of the above patterns can be active at any given instant.

SYNC_PATTERN: Address: 10[8]

By enabling this bit, all channels' test pattern outputs are synchronized. When 10[8] is set as 1, the ramp patterns of all 8 channels start simultaneously.

VCA Register Map

Table 4. VCA Register Map

ADDRESS (DEC)	ADDRESS (HEX)	Default Value	FUNCTION	DESCRIPTION
51[0]	0x33[0]	0	RESERVED	0
51[3:1]	0x33[3:1]	0	LPF_PROGRAMMABILITY	000: 15MHz, 010: 20MHz, 011: 30MHz, 100: 10MHz
51[4]	0x33[4]	0	PGA_INTEGRATOR_DISABLE (PGA_HPF_DISABLE)	0: Enable 1: Disables offset integrator for PGA. See explanation for the PGA integrator function in APPLICATION INFORMATION section
51[6:5]	0x33[6:5]	0	PGA_CURRENT_CLAMP_LEVEL	00: –2dBFS; 10: 0dBFS; 01:–4dBFS when 51[7]=0 Note: the current clamp circuit makes sure that PGA output is in linear range. For example, at 00 setting, PGA output HD3 will be worsen by 3dB at –2dBFS ADC input. In normal operation, the current clamp function can be set as 00
51[7]	0x33[7]	0	PGA_CURRENT_CLAMP_DISABLE	0:Enables the PGA current clamp circuit; 1:Disables the PGA current clamp circuit before the PGA outputs. 51[6:5] determines the current clamp level
51[13]	0x33[13]	0	PGA_GAIN_CONTROL	0:24dB; 1:30dB.
52[4:0]	0x34[4:0]	0	ACTIVE_TERMINATION_ INDIVIDUAL_RESISTOR_CNTL	See Table 6 Reg 52[5] should be set as '1' to access these bits
52[5]	0x34[5]	0	ACTIVE_TERMINATION_ INDIVIDUAL_RESISTOR_ENABLE	0: Disables; 1: Enables internal active termination individual resistor control
52[7:6]	0x34[7:6]	0	PRESET_ACTIVE_ TERMINATIONS	00: 50ohm, 01: 100ohm, 10: 200ohm, 11: 400ohm. (Note: the device will adjust resistor mapping (52[4:0]) automatically. 50ohm active termination is NOT supported in 12dB LNA setting. Instead, '00' represents high impedance mode when LNA gain is 12dB)
52[8]	0x34[8]	0	ACTIVE TERMINATION ENABLE	0: Disables; 1: Enables active termination
52[10:9]	0x34[10:9]	0	LNA_INPUT_CLAMP_SETTING	00: Auto setting, 01: 1.5Vpp, 10: 1.15Vpp and 11: 0.6Vpp
52[11]	0x34[11]	0	RESERVED	Set to 0
52[12]	0x34[12]	0	LNA_INTEGRATOR_DISABLE (LNA_HPF_DISABLE)	0: Enables; 1: Disables offset integrator for LNA. See the explanation for this function in the following section
52[14:13]	0x34[14:13]	0	LNA_GAIN	00: 18dB; 01: 24dB; 10: 12dB; 11: Reserved
52[15]	0x34[15]	0	LNA_INDIVIDUAL_CH_CNTL	0: Disable; 1: Enable LNA individual channel control. See Register 57 for details
53[7:0]	0x35[7:0]	0	PDN_CH<7:0>	0: Normal operation; 1: Powers down corresponding channels. Bit7→CH8, Bit6→CH7…Bit0→CH1. PDN_CH will shut down whichever blocks are active
53[8]	0x35[8]	0	RESERVED	Set to 0
53[9]	0x35[9]	0	RESERVED	Set to 0
53[10]	0x35[10]	0	LOW_POWER	0: Low noise mode; 1: Sets to low power mode (53[11]=0). At 30dB PGA, total chain gain may slightly change. See typical characteristics

Table 4. VCA Register Map (continued)

ADDRESS (DEC)	ADDRESS (HEX)	Default Value	FUNCTION	DESCRIPTION
53[11]	0x35[11]	0	MED_POWER	0: Low noise mode; 1: Sets to medium power mode(53[10]=0). At 30dB PGA, total chain gain may slightly change. See typical characteristics
53[12]	0x35[12]	0	PDN_VCAT_PGA	0: Normal operation; 1: Powers down VCAT (voltage-controlled-attenuator) and PGA
53[13]	0x35[13]	0	PDN_LNA	0: Normal operation; 1: Powers down LNA only
53[14]	0x35[14]	0	VCA_PARTIAL_PDN	0: Normal operation; 1: Powers down LNA, VCAT, and PGA partially(fast wake response)
53[15]	0x35[15]	0	VCA_COMPLETE_PDN	0: Normal operation; 1: Powers down LNA, VCAT, and PGA completely (slow wake response). This bit can overwrite 53[14].
54[4:0]	0x36[4:0]	0	BUFFER_AMP_GAIN_CNTL	Selects Feedback resistor for the buffer amplifier see Table 7
54[7]	0x36[7]	0	RESERVED	Set to 0
54[8]	0x36[8]	0	RESERVED	Set to 0
54[9]	0x36[9]	0	RESERVED	Set to 0
57[1:0]	0x39[1:0]	0	CH1_LNA_GAIN_CNTL	00: 18dB; 01: 24dB; 10: 12dB; 11: Reserved REG52[15] should be set as '1'
57[3:2]	0x39[3:2]	0	CH2_LNA_GAIN_CNTL	
57[5:4]	0x39[5:4]	0	CH3_LNA_GAIN_CNTL	00: 18dB; 01: 24dB; 10: 12dB; 11: Reserved REG52[15] should be set as '1'
57[7:6]	0x39[7:6]	0	CH4_LNA_GAIN_CNTL	
57[9:8]	0x39[9:8]	0	CH5_LNA_GAIN_CNTL	
57[11:10]	0x39[11:10]	0	CH6_LNA_GAIN_CNTL	
57[13:12]	0x39[13:12]	0	CH7_LNA_GAIN_CNTL	
57[15:14]	0x39[15:14]	0	CH8_LNA_GAIN_CNTL	
59[3:2]	0x3B[3:2]	0	HPF_LNA	00: 100kHz; 01: 50kHz; 10: 200kHz; 11: 150kHz with 0.015uF on INMx
59[6:4]	0x3B[6:4]	0	DIG_TGC_ATT_GAIN	000: 0dB attenuation; 001: 6dB attenuation; N: ~N×6dB attenuation when 59[7] = 1
59[7]	0x3B[7]	0	DIG_TGC_ATT	0: disable digital TGC attenuator; 1: enable digital TGC attenuator
59[8]	0x3B[8]	0	BUFFER_AMP_PDN	0: Power down; 1: Normal operation
59[9]	0x3B[9]	0	PGA_TEST_MODE	0: Normal operation; 1: PGA outputs appear at test outputs

AFE5803 VCA Register Description

LNA Input Impedances Configuration (Active Termination Programmability)

Different LNA input impedances can be configured through the register 52[4:0]. By enabling and disabling the feedback resistors between LNA outputs and ACTx pins, LNA input impedance is adjustable accordingly. Table 5 describes the relationship between LNA gain and 52[4:0] settings.

The AFE5803 also has 4 preset active termination impedances as described in 52[7:6]. An internal decoder is used to select appropriate resistors corresponding to different LNA gain.

Table 5. Register 52[4:0] Description

52[4:0]/0x34[4:0]	FUNCTION
00000	No feedback resistor enabled
00001	Enables 450 Ω feedback resistor
00010	Enables 900 Ω feedback resistor
00100	Enables 1800 Ω feedback resistor
01000	Enables 3600 Ω feedback resistor
10000	Enables 4500 Ω feedback resistor

Table 6. Register 52[4:0] vs LNA Input Impedances

52[4:0]/0x34[4:0]	00000	00001	00010	00011	00100	00101	00110	00111
LNA:12dB	High Z	150 Ω	300 Ω	100 Ω	600 Ω	120 Ω	200 Ω	86 Ω
LNA:18dB	High Z	90 Ω	180 Ω	60 Ω	360 Ω	72 Ω	120 Ω	51 Ω
LNA:24dB	High Z	50 Ω	100 Ω	33 Ω	200 Ω	40 Ω	66.67 Ω	29 Ω
52[4:0]/0x34[4:0]	**01000**	**01001**	**01010**	**01011**	**01100**	**01101**	**01110**	**01111**
LNA:12dB	1200 Ω	133 Ω	240 Ω	92 Ω	400 Ω	109 Ω	171 Ω	80 Ω
LNA:18dB	720 Ω	80 Ω	144 Ω	55 Ω	240 Ω	65 Ω	103 Ω	48 Ω
LNA:24dB	400 Ω	44 Ω	80 Ω	31 Ω	133 Ω	36 Ω	57 Ω	27 Ω
52[4:0]/0x34[4:0]	**10000**	**10001**	**10010**	**10011**	**10100**	**10101**	**10110**	**10111**
LNA:12dB	1500 Ω	136 Ω	250 Ω	94 Ω	429 Ω	111 Ω	176 Ω	81 Ω
LNA:18dB	900 Ω	82 Ω	150 Ω	56 Ω	257 Ω	67 Ω	106 Ω	49 Ω
LNA:24dB	500 Ω	45 Ω	83 Ω	31 Ω	143 Ω	37 Ω	59 Ω	27 Ω
52[4:0]/0x34[4:0]	**11000**	**11001**	**11010**	**11011**	**11100**	**11101**	**11110**	**11111**
LNA:12dB	667 Ω	122 Ω	207 Ω	87 Ω	316 Ω	102 Ω	154 Ω	76 Ω
LNA:18dB	400 Ω	73 Ω	124 Ω	52 Ω	189 Ω	61 Ω	92 Ω	46 Ω
LNA:24dB	222 Ω	41 Ω	69 Ω	29 Ω	105 Ω	34 Ω	51 Ω	25 Ω

Programmable Feedback Resistors for Buffer Amplifier in TGC Test Mode

Different feedback resistors can be configured for the buffer amplifier through the register 54[4:0] when TGC test mode is enabled. Therefore, certain gain can be applied to the PGA test outputs for CH7 and CH8. Table 7 describes the relationship between the resistor configurations and 54[4:0] settings. Note these 5 resistor are put in parallel. When multiple bits are enabled, the resistance is reduced.

Table 7. Register 54[4:0] Description

54[4:0]	FUNCTION
00000	No feedback resistor enabled
00001	Enables 250 Ω feedback resistor
00010	Enables 250 Ω feedback resistor
00100	Enables 500 Ω feedback resistor
01000	Enables 1000 Ω feedback resistor
10000	Enables 2000 Ω feedback resistor

THEORY OF OPERATION

AFE5803 OVERVIEW

The AFE5803 is a highly integrated Analog Front-End (AFE) solution specifically designed for ultrasound systems in which high performance and small size are required. The AFE5803 integrates a complete time-gain-control (TGC) imaging path. It also enables users to select one of various power/noise combinations to optimize system performance. The AFE5803 contains eight channels; each channels includes a Low-Noise Amplifier (LNA), a Voltage Controlled Attenuator (VCAT), a Programmable Gain Amplifier (PGA), a Low-pass Filter (LPF), and a 14-bit Analog-to-Digital Converter (ADC).

In addition, multiple features in the AFE5803 are suitable for ultrasound applications, such as active termination, individual channel control, fast power up/down response, programmable clamp voltage control, fast and consistent overload recovery, etc. Therefore the AFE5803 brings premium image quality to ultra–portable, handheld systems all the way up to high-end ultrasound systems. Its simplified function block diagram is listed in Figure 61.

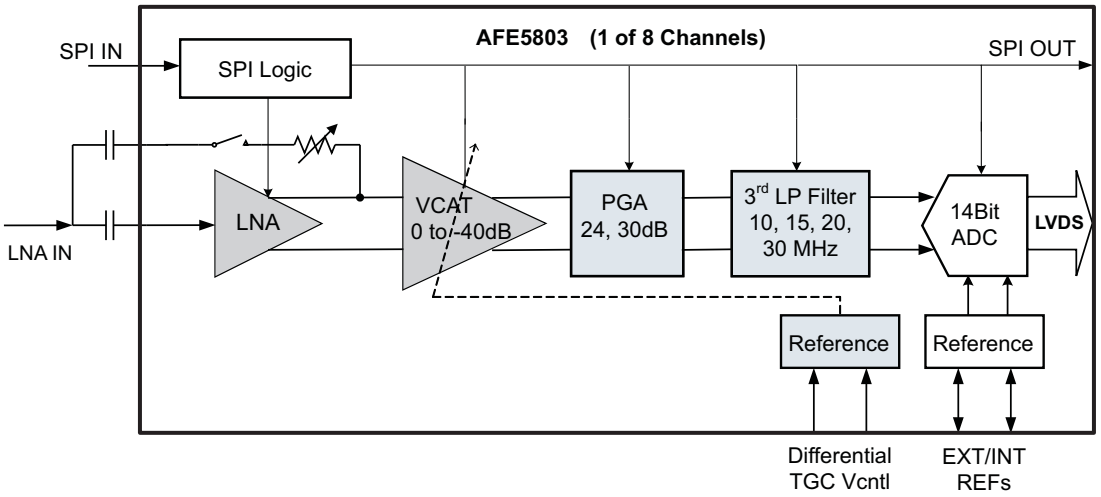


Figure 61. Functional Block Diagram

LOW-NOISE AMPLIFIER (LNA)

In many high-gain systems, a low noise amplifier is critical to achieve overall performance. Using a new proprietary architecture, the LNA in the AFE5803 delivers exceptional low-noise performance, while operating on a low quiescent current compared to CMOS-based architectures with similar noise performance. The LNA performs single-ended input to differential output voltage conversion. It is configurable for a programmable gain of 24/18/12dB and its input-referred noise is only 0.63/0.70/0.9nV/√Hz respectively. Programmable gain settings result in a flexible linear input range up to 1Vpp, realizing high signal handling capability demanded by new transducer technologies. Larger input signal can be accepted by the LNA; however, the signal can be distorted since it exceeds the LNA's linear operation region. Combining the low noise and high input range, a wide input dynamic range is achieved consequently for supporting the high demands from various ultrasound imaging modes.

The LNA input is internally biased at approximately +2.4 V; the signal source should be ac-coupled to the LNA input by an adequately-sized capacitor, e.g. ≥0.1 µF. To achieve low DC offset drift, the AFE5803 incorporates a DC offset correction circuit for each amplifier stage. To improve the overload recovery, an integrator circuit is used to extract the DC component of the LNA output and then fed back to the LNA's complementary input for DC offset correction. This DC offset correction circuit has a high-pass response and can be treated as a high-pass filter. The effective corner frequency is determined by the capacitor C_{BYPASS} connected at INM. With larger capacitors, the corner frequency is lower. For stable operation at the highest HP filer cut-off frequency, a ≥15 nF capacitor can be selected. This corner frequency scales almost linearly with the value of the C_{BYPASS}. For example, 15 nF gives a corner frequency of approximately 100 kHz, while 47 nF can give an effective corner frequency of 33 KHz. The DC offset correction circuit can also be disabled/enabled through register 52[12].

The AFE5803 can be terminated passively or actively. Active termination is preferred in ultrasound application for reducing reflection from mismatches and achieving better axial resolution without degrading noise figure too much. Active termination values can be preset to 50, 100, 200, 400Ω; other values also can be programmed by users through register 52[4:0]. A feedback capacitor is required between ACTx and the signal source as Figure 62 shows. On the active termination path, a clamping circuit is also used to create a low impedance path when overload signal is seen by the AFE5803. The clamp circuit limits large input signals at the LNA inputs and improves the overload recovery performance of the AFE5803. The clamp level can be set to 350 mVpp, 600 mVpp, 1.15 Vpp automatically depending on the LNA gain settings when register 52[10:9]=0. Other clamp voltages, such as 1.15Vpp, 0.6 Vpp, and 1.5 Vpp, are also achievable by setting register 52[10:9]. This clamping circuit is also designed to obtain good pulse inversion performance and reduce the impact from asymmetric inputs.

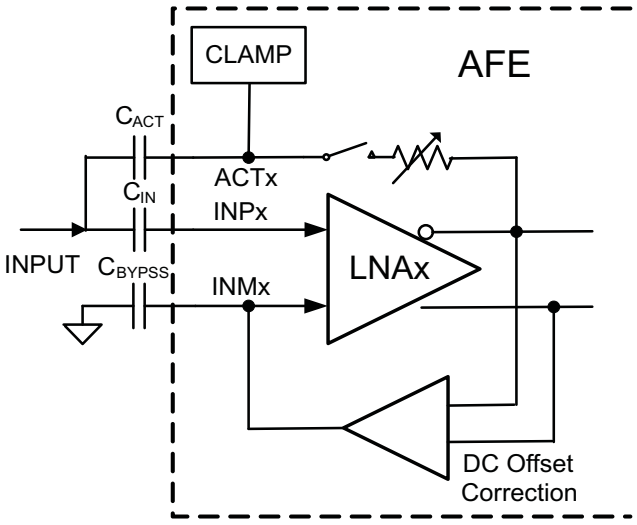


Figure 62. AFE5803 LNA with DC Offset Correction Circuit

VOLTAGE-CONTROLLED ATTENUATOR

The voltage-controlled attenuator is designed to have a linear-in-dB attenuation characteristic; that is, the average gain loss in dB (refer to Figure 2) is constant for each equal increment of the control voltage (VCNTL) as shown in Figure 63. A differential control structure is used to reduce common mode noise. A simplified attenuator structure is shown in the following Figure 63 and Figure 64.

The attenuator is essentially a variable voltage divider that consists of the series input resistor (RS) and seven shunt FETs placed in parallel and controlled by sequentially activated clipping amplifiers (A1 through A7). VCNTL is the effective difference between VCNTLP and VCNTLM. Each clipping amplifier can be understood as a specialized voltage comparator with a soft transfer characteristic and well-controlled output limit voltage. Reference voltages V1 through V7 are equally spaced over the 0V to 1.5Vcontrol voltage range. As the control voltage increases through the input range of each clipping amplifier, the amplifier output rises from a voltage where the FET is nearly OFF to VHIGH where the FET is completely ON. As each FET approaches its ON state and the control voltage continues to rise, the next clipping amplifier/FET combination takes over for the next portion of the piecewise-linear attenuation characteristic. Thus, low control voltages have most of the FETs turned OFF, producing minimum signal attenuation. Similarly, high control voltages turn the FETs ON, leading to maximum signal attenuation. Therefore, each FET acts to decrease the shunt resistance of the voltage divider formed by Rs and the parallel FET network.

Additionally, a digitally controlled TGC mode is implemented to achieve better phase-noise performance in the AFE5803. The attenuator can be controlled digitally instead of the analog control voltage V_{CNTL}. This mode can be set by the register bit 59[7]. The variable voltage divider is implemented as a fixed series resistance and FET as the shunt resistance. Each FET can be turned ON by connecting the switches SW1-7. Turning on each of the switches can give approximately 6dB of attenuation. This can be controlled by the register bits 59[6:4]. This digital control feature can eliminate the noise from the VCNTL circuit and ensure the better SNR and phase noise for TGC path.

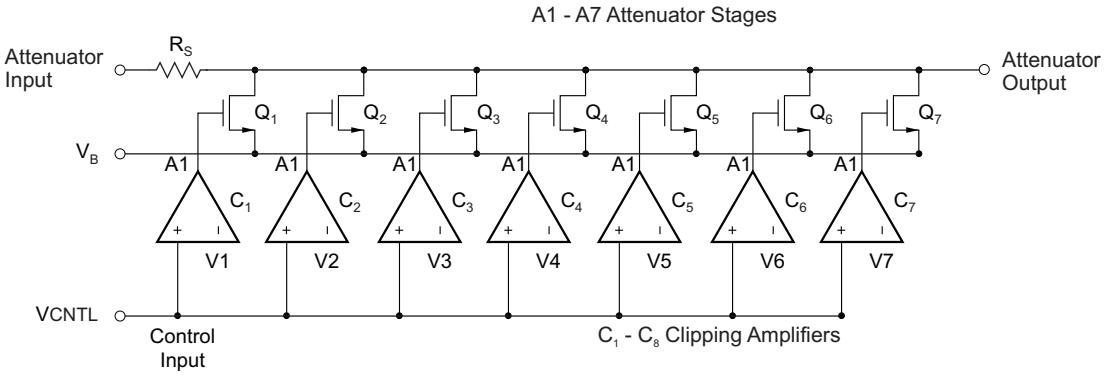


Figure 63. Simplified Voltage Controlled Attenuator (Analog Structure)

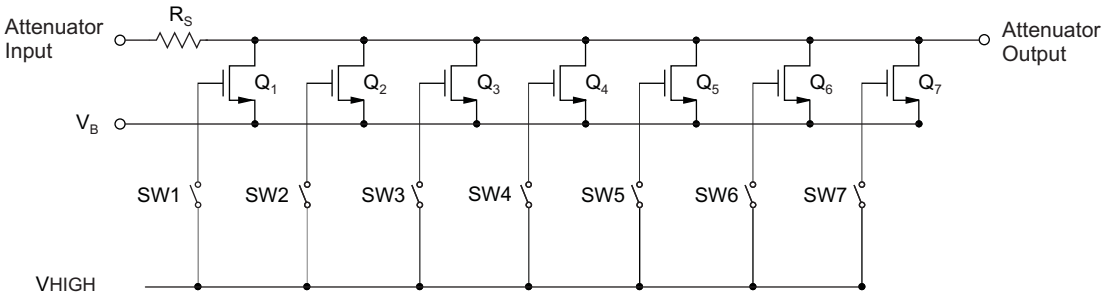


Figure 64. Simplified Voltage Controlled Attenuator (Digital Structure)

The voltage controlled attenuator's noise follows a monotonic relationship to the attenuation coefficient. At higher attenuation, the input-referred noise is higher and vice-versa. The attenuator's noise is then amplified by the PGA and becomes the noise floor at ADC input. In the attenuator's high attenuation operating range, i.e. VCNTL is high, the attenuator's input noise may exceed the LNA's output noise; the attenuator then becomes the dominant noise source for the following PGA stage and ADC. Therefore the attenuator's noise should be minimized compared to the LNA output noise. The AFE5803's attenuator is designed for achieving low noise even at high attenuation (low channel gain) and realizing better SNR in near field. The input referred noise for different attenuations is listed in the below table:

Table 8. Voltage-Controlled-Attenuator noise vs Attenuation

Attenuation (dB)	Attenuator Input Referred noise (nV/rtHz)
–40	10.5
–36	10
–30	9
–24	8.5
–18	6
–12	4
–6	3
0	2

PROGRAMMABLE GAIN AMPLIFIER (PGA)

After the voltage controlled attenuator, a programmable gain amplifier can be configured as 24dB or 30dB with a constant input referred noise of 1.75 nV/rtHz. The PGA structure consists of a differential voltage-to-current converter with programmable gain, current clamp(bias control) circuits, a transimpedance amplifier with a programmable low-pass filter, and a DC offset correction circuit. Its simplified block diagram is shown below:

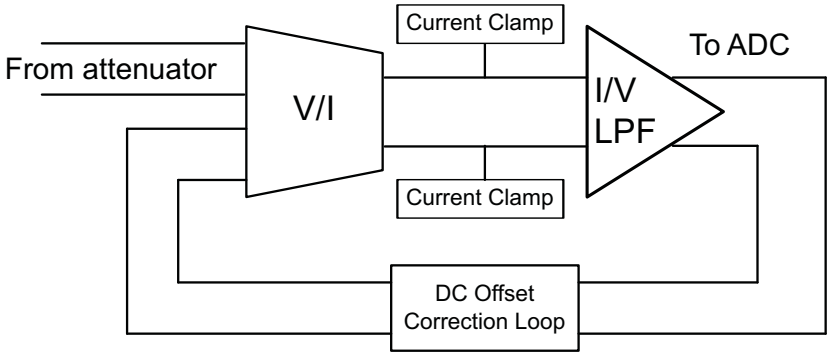


Figure 65. Simplified Block Diagram of PGA

Low input noise is always preferred in a PGA and its noise contribution should not degrade the ADC SNR too much after the attenuator. At the minimum attenuation (used for small input signals), the LNA noise dominates; at the maximum attenuation (large input signals), the PGA and ADC noise dominates. Thus 24 dB gain of PGA achieves better SNR as long as the amplified signals can exceed the noise floor of the ADC.

The PGA current clamp circuit can be enabled (register 51) to improve the overload recovery performance of the AFE. If we measure the standard deviation of the output just after overload, for 0.5 V V_{CNTL}, it is about 3.2 LSBs in normal case, i.e the output is stable in about 1 clock cycle after overload. With the current clamp circuit disabled, the value approaches 4 LSBs meaning a longer time duration before the output stabilizes; however, with the current clamp circuit enabled, there will be degradation in HD3 for PGA output levels > -2dBFS. For example, for a –2dBFS output level, the HD3 degrades by approximately 3dB.

The AFE5803 integrates an anti-aliasing filter in the form of a programmable low-pass filter (LPF) in the transimpedance amplifier. The LPF is designed as a differential, active, 3rd order filter with a typical 18dB per octave roll-off. Programmable through the serial interface, the –1dB frequency corner can be set to one of 10MHz, 15 MHz, 20 MHz, and 30MHz. The filter bandwidth is set for all channels simultaneously.

A selectable DC offset correction circuit is implemented in the PGA as well. This correction circuit is similar to the one used in the LNA. It extracts the DC component of the PGA outputs and feeds back to the PGA's complimentary inputs for DC offset correction. This DC offset correction circuit also has a high-pass response with a cut-off frequency of 80 KHz.

ANALOG TO DIGITAL CONVERTER

The analog-to-digital converter (ADC) of the AFE5803 employs a pipelined converter architecture that consists of a combination of multi-bit and single-bit internal stages. Each stage feeds its data into the digital error correction logic, ensuring excellent differential linearity and no missing codes at the 14-bit level. The 14 bits given out by each channel are serialized and sent out on a single pair of pins in LVDS format. All eight channels of the AFE5803 operate from a common input clock (CLKP/M). The sampling clocks for each of the eight channels are generated from the input clock using a carefully matched clock buffer tree. The 14x clock required for the serializer is generated internally from the CLKP/M pins. A 7x and a 1x clock are also given out in LVDS format, along with the data, to enable easy data capture. The AFE5803 operates from internally-generated reference voltages that are trimmed to improve the gain matching across devices. The nominal values of REFP and REFM are 1.5V and 0.5V, respectively. Alternately, the device also supports an external reference mode that can be enabled using the serial interface.

Using serialized LVDS transmission has multiple advantages, such as a reduced number of output pins (saving routing space on the board), reduced power consumption, and reduced effects of digital noise coupling to the analog circuit inside the AFE5803.

EQUIVALENT CIRCUITS

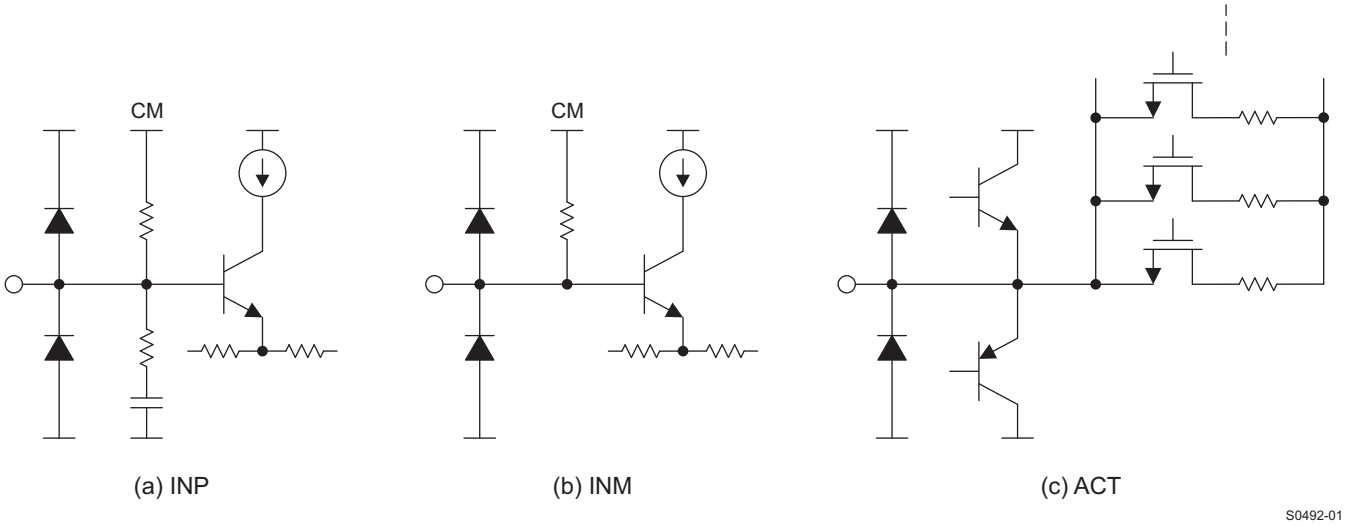


Figure 66. Equivalent Circuits of LNA inputs

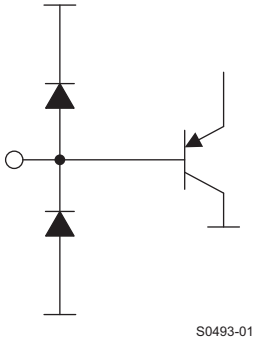


Figure 67. Equivalent Circuits of $V_{CNTLP/M}$

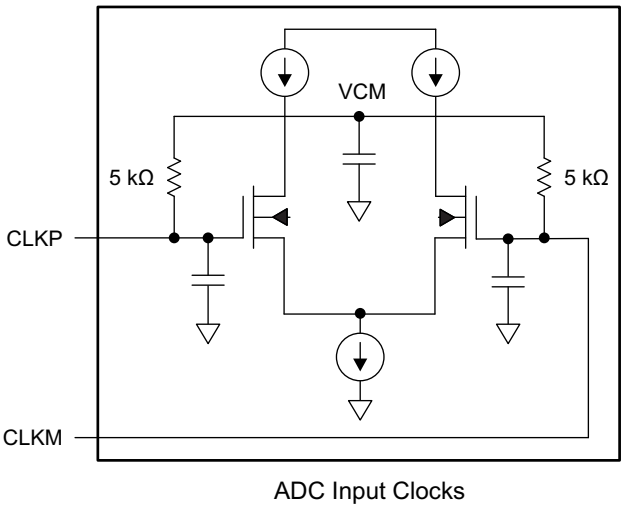


Figure 68. Equivalent Circuits of Clock Inputs

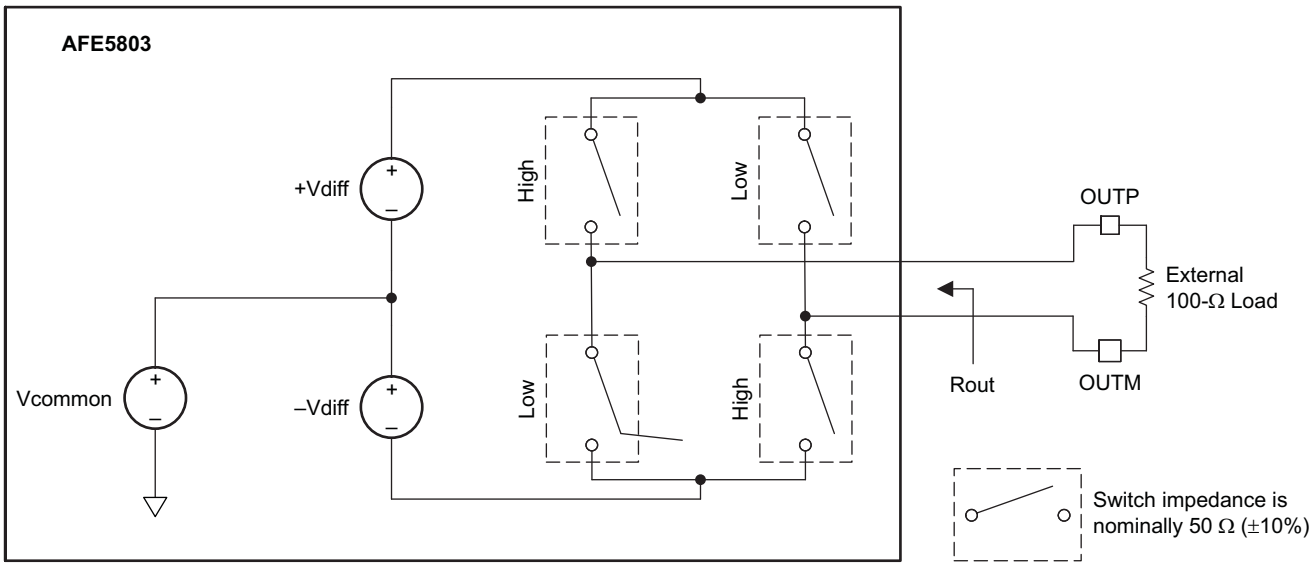


Figure 69. Equivalent Circuits of LVDS Outputs

APPLICATION INFORMATION

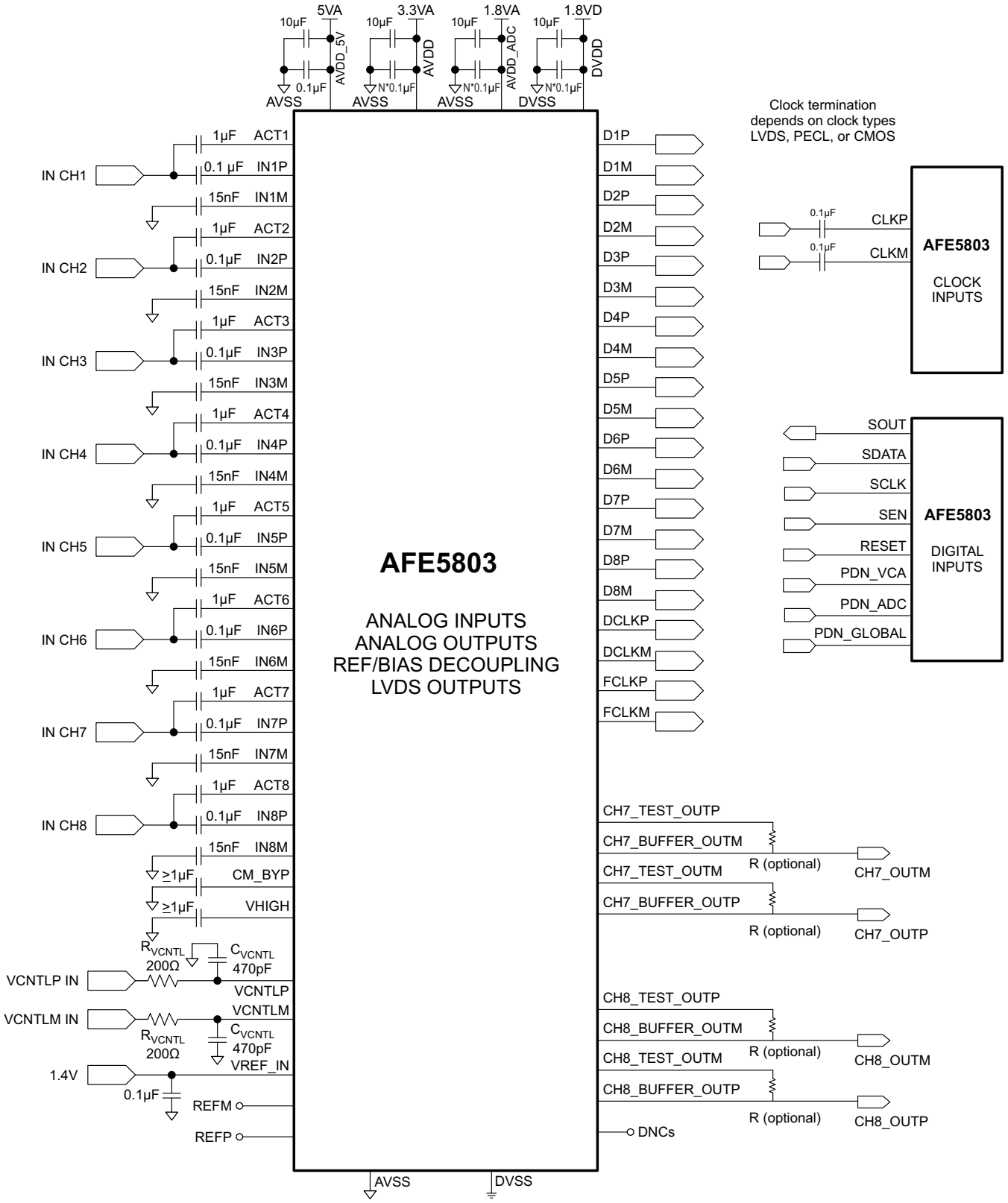


Figure 70. Application Circuit

A typical application circuit diagram is listed above. The configuration for each block is discussed below.

LNA CONFIGURATION

LNA Input Coupling and Decoupling

The LNA closed-loop architecture is internally compensated for maximum stability without the need of external compensation components. The LNA inputs are biased at 2.4 V and AC coupling is required. A typical input configuration is shown in Figure 71. C_{IN} is the input AC coupling capacitor. C_{ACT} is a part of the active termination feedback path. Even if the active termination is not used, the C_{ACT} is required for the clamp functionality. Recommended values for C_{ACT} = 1 µF and C_{IN} are ≥ 0.1 µF. A pair of clamping diodes is commonly placed between the T/R switch and the LNA input. Schottky diodes with suitable forward drop voltage (e.g. the BAT754/54 series, the BAS40 series, the MMBD7000 series, or similar) can be considered depending on the transducer echo amplitude.

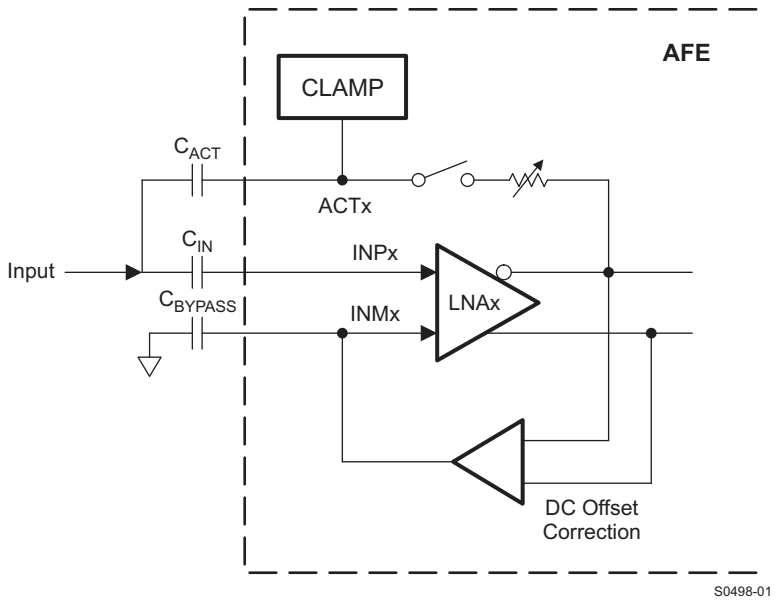


Figure 71. LNA Input Configurations

This architecture minimizes any loading of the signal source that may otherwise lead to a frequency-dependent voltage divider. The closed-loop design yields low offsets and offset drift. C_{BYPASS} (≥0.015 µF) is used to set the high-pass filter cut-off frequency and decouple the complimentary input. Its cut-off frequency is inversely proportional to the C_{BYPASS} value, The HPF cut-off frequency can be adjusted through the register 59[3:2] a Table 9 lists. Low frequency signals at T/R switch output, such as signals with slow ringing, can be filtered out. In addition, the HPF can minimize system noise from DC-DC converters, pulse repetition frequency (PRF) trigger, and frame clock. Most ultrasound systems' signal processing unit includes digital high-pass filters or band-pass filters (BPFs) in FPGAs or ASICs. Further noise suppression can be achieved in these blocks. In addition, a digital HPF is available in the AFE5803 ADC. If low frequency signal detection is desired in some applications, the LNA HPF can be disabled.

Table 9. LNA HPF Settings (C_{BYPASS} = 15 nF)

Reg59[3:2] (0x3B[3:2])	Frequency
00	100 KHz
01	50 KHz
10	200 KHz
11	150 KHz

CM_BYP and VHIGH pins, which generate internal reference voltages, need to be decoupled with ≥1uF capacitors. Bigger bypassing capacitors (>2.2uF) may be beneficial if low frequency noise exists in system.

LNA Noise Contribution

The noise spec is critical for LNA and it determines the dynamic range of entire system. The LNA of the AFE5803 achieves low power and an exceptionally low-noise voltage of 0.63 nV/√Hz, and a low current noise of 2.7 pA/√Hz.

Typical ultrasonic transducer's impedance Rs varies from tens of ohms to several hundreds of ohms. Voltage noise is the dominant noise in most cases; however, the LNA current noise flowing through the source impedance (Rs) generates additional voltage noise.

$$LNA\_Noise_{total} = \sqrt{V^2_{LNAnoise} + R^2_s \times I^2_{LNAnoise}} \quad (2)$$

The AFE5803 achieves low noise figure (NF) over a wide range of source resistances as shown in Figure 29, Figure 30, andFigure 31.

Active Termination

In ultrasound applications, signal reflection exists due to long cables between transducer and system. The reflection results in extra ringing added to echo signals in PW mode. Since the axial resolution depends on echo signal length, such ringing effect can degrade the axial resolution. Hence, either passive termination or active termination, is preferred if good axial resolution is desired. Figure 72 shows three termination configurations:

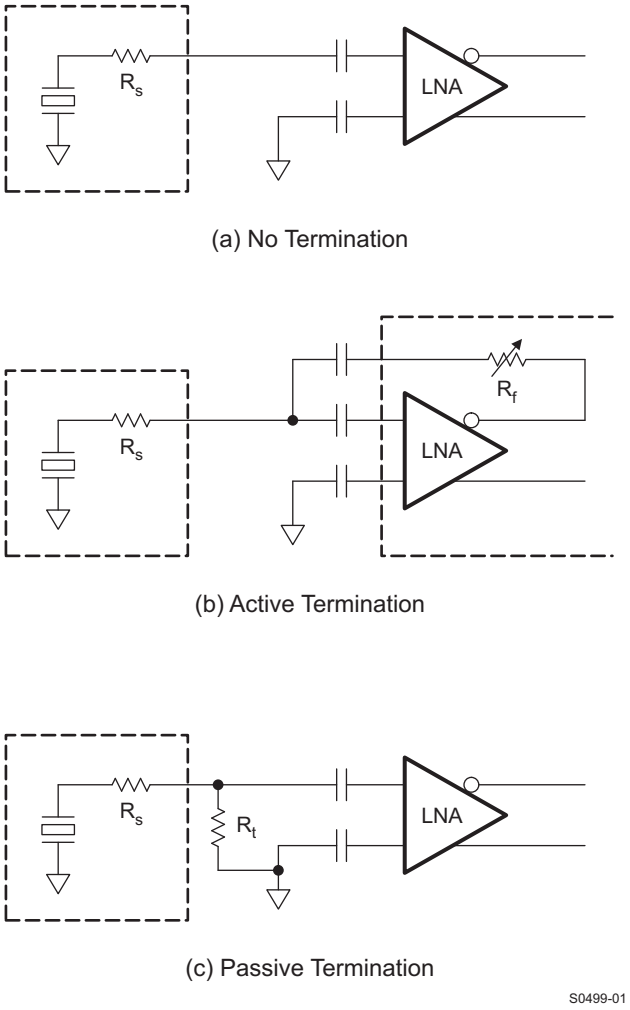


Figure 72. Termination Configurations

Under the no termination configuration, the input impedance of the AFE5803 is about 6 KΩ (8 K//20 pF) at 1 MHz. Passive termination requires external termination resistor R_t, which contributes to additional thermal noise.

The LNA supports active termination with programmable values, as shown in Figure 73 .

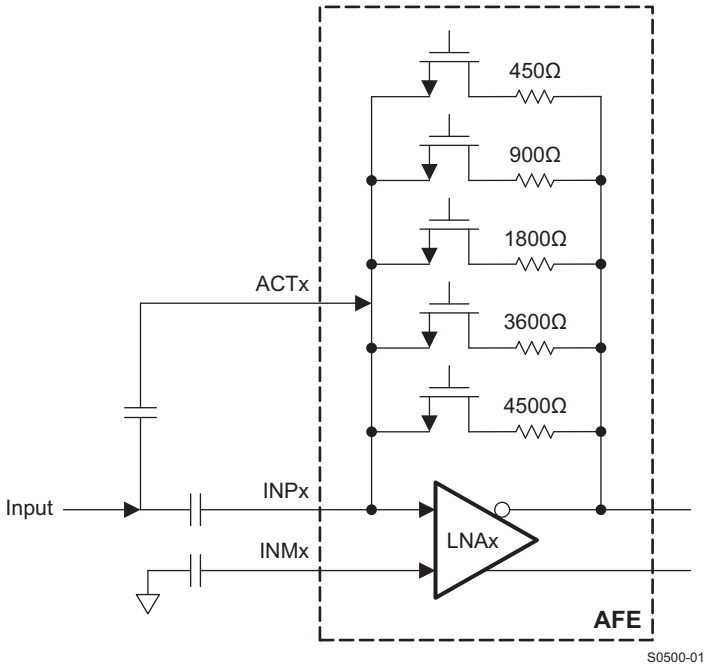


Figure 73. Active Termination Implementation

The AFE5803 has four pre-settings 50,100, 200 and 400 Ω which are configurable through the registers. Other termination values can be realized by setting the termination switches shown in Figure 73. Register [52] is used to enable these switches. The input impedance of the LNA under the active termination configuration approximately follows:

$$Z_{IN} = \frac{R_f}{1 + \frac{A\nu_{LNA}}{2}} \quad (3)$$

Table 5 lists the LNA R_{IN}s under different LNA gains. System designers can achieve fine tuning for different probes.

The equivalent input impedance is given by Equation 4 where R_{IN} (8 K) and C_{IN} (20 pF) are the input resistance and capacitance of the LNA.

$$Z_{IN} = \frac{R_f}{1 + \frac{A\nu_{LNA}}{2}} / /C_{IN} / /R_{IN} \quad (4)$$

Therefore the ZIN is frequency dependent and it decreases as frequency increases shown in Figure 10. Since 2 MHz~10 MHz is the most commonly used frequency range in medical ultrasound, this rolling-off effect doesn't impact system performance greatly. Since each ultrasound system includes multiple transducers with different impedances, the flexibility of impedance configuration is a great plus.

Figure 29, Figure 30, and Figure 31 shows the NF under different termination configurations. It indicates that no termination achieves the best noise figure; active termination adds less noise than passive termination. Thus termination topology should be carefully selected based on each use scenario in ultrasound.

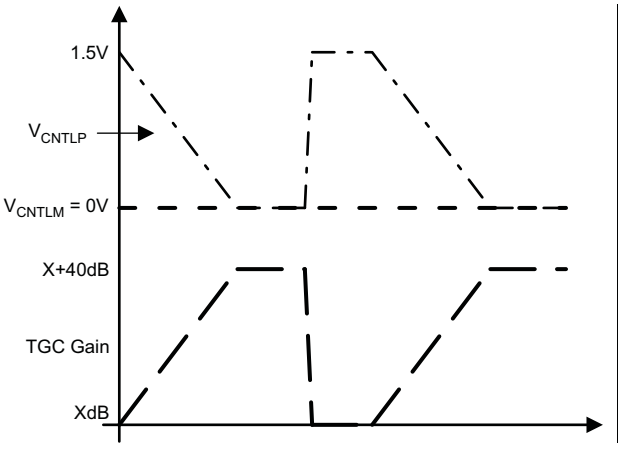
LNA Gain Switch Response

The LNA gain is programmable through SPI. The gain switching time depends on the SPI speed as well as the LNA gain response time. During the switching, glitches might occur and they can appear as artifacts in images. LNA gain switching in a single imaging line may not be preferred, although digital signal processing might be used here for glitch suppression.

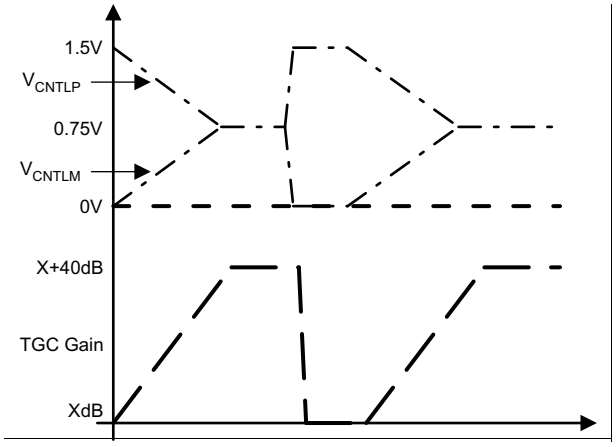
VOLTAGE-CONTROLLED-ATTENUATOR

The attenuator in the AFE5803 is controlled by a pair of differential control inputs, the $V_{CNTLM/P}$ pins. The differential control voltage spans from 0 V to 1.5 V. This control voltage varies the attenuation of the attenuator based on its linear-in-dB characteristic. Its maximum attenuation (minimum channel gain) appears at V_{CNTLP} - V_{CNTLM} = 1.5 V, and minimum attenuation (maximum channel gain) occurs at V_{CNTLP} - V_{CNTLM} = 0. The typical gain range is 40 dB and remains constant, independent of the PGA setting.

When only single-ended V_{CNTL} signal is available, this 1.5 V_{PP} signal can be applied on the V_{CNTLP} pin with the V_{CNTLM} pin connected to ground. As shown in Figure 74, TGC gain curve is inversely proportional to the V_{CNTLP}-V_{CNTLM}.



(a) Single-Ended Input at V_{CNTLP}



(b) Differential Inputs at V_{CNTLP} and V_{CNTLM}

W0004-01

Figure 74. V_{CNTLP} and V_{CNTLM} Configurations

As discussed in the theory of operation, the attenuator architecture uses seven attenuator segments that are equally spaced in order to approximate the linear-in-dB gain-control slope. This approximation results in a monotonic slope; the gain ripple is typically less than ±0.5 dB.

The control voltage input ($V_{CNTLM/P}$ pins) represents a high-impedance input. The $V_{CNTLM/P}$ pins of multiple AFE5803 devices can be connected in parallel with no significant loading effects. When the voltage level (V_{CNTLP} - V_{CNTLM}) is above 1.5 V or below 0 V, the attenuator continues to operate at its maximum attenuation level or minimum attenuation level respectively. It is recommended to limit the voltage from -0.3 V to 2 V.

The AFE5803 gain-control input has a –3 dB bandwidth of approximately 800KHz. This wide bandwidth, although useful in many applications (e.g. fast V_{CNTL} response), can also allow high-frequency noise to modulate the gain control input and finally affect the Doppler performance. In practice, this modulation can be avoided by additional external filtering (RV_{CNTL} and CV_{CNTL}) at $V_{CNTLM/P}$ pins as Figure 69 shows. However, the external filter's cutoff frequency cannot be kept too low as this results in low gain response time. Without external filtering, the gain control response time is typically less than 1 µs to settle within 10% of the final signal level of $1V_{PP}$ (–6 dBFS) output as indicated in Figure 48 and Figure 49.

Typical $V_{CNTLM/P}$ signals are generated by an 8bit to 12bit 10MSPS digital to analog converter (DAC) and a differential operation amplifier. TI's DACs, such as TLV5626 and DAC7821/11 (10 MSPS/12bit), could be used to generate TGC control waveforms. Differential amplifiers with output common mode voltage control (e.g. THS4130 and OPA1632) can connect the DAC to the $V_{CNTLM/P}$ pins. The buffer amplifier can also be configured as an active filter to suppress low frequency noise. More information can be found in the documents SLOS318 and SBAA150. The V_{CNTL} vs Gain curves can be found in Figure 2. The below table also shows the absolute gain vs. V_{CNTL}, which may help program DAC correspondingly.

In PW Doppler and color Doppler modes, V_{CNTL} noise should be minimized to achieve the best close-in phase noise and SNR. Digital V_{CNTL} feature is implemented to address this need in the AFE5803. In the digital V_{CNTL} mode, no external V_{CNTL} is needed.

Table 10. V_{CNTLP}–V_{CNTLM} vs Gain Under Different LNA and PGA Gain Settings (Low Noise Mode)

V_{CNTLP}–V_{CNTLM} (V)	Gain (dB) LNA = 12 dB PGA = 24 dB	Gain (dB) LNA = 18 dB PGA = 24 dB	Gain (dB) LNA = 24 dB PGA = 24 dB	Gain (dB) LNA = 12 dB PGA = 30 dB	Gain (dB) LNA = 18 dB PGA = 30 dB	Gain (dB) LNA = 24 dB PGA = 30 dB
0	36.45	42.45	48.45	42.25	48.25	54.25
0.1	33.91	39.91	45.91	39.71	45.71	51.71
0.2	30.78	36.78	42.78	36.58	42.58	48.58
0.3	27.39	33.39	39.39	33.19	39.19	45.19
0.4	23.74	29.74	35.74	29.54	35.54	41.54
0.5	20.69	26.69	32.69	26.49	32.49	38.49
0.6	17.11	23.11	29.11	22.91	28.91	34.91
0.7	13.54	19.54	25.54	19.34	25.34	31.34
0.8	10.27	16.27	22.27	16.07	22.07	28.07
0.9	6.48	12.48	18.48	12.28	18.28	24.28
1.0	3.16	9.16	15.16	8.96	14.96	20.96
1.1	–0.35	5.65	11.65	5.45	11.45	17.45
1.2	–2.48	3.52	9.52	3.32	9.32	15.32
1.3	–3.58	2.42	8.42	2.22	8.22	14.22
1.4	–4.01	1.99	7.99	1.79	7.79	13.79
1.5	–4	2	8	1.8	7.8	13.8

ADC OPERATION

ADC Clock Distribution

To ensure that the aperture delay and jitter are the same for all channels, the AFE5803 uses a clock tree network to generate individual sampling clocks for each channel. The clock, for all the channels, are matched from the source point to the sampling circuit of each of the eight internal ADCs. The variation on this delay is described in the aperture delay parameter of the output interface timing. Its variation is given by the aperture jitter number of the same table.

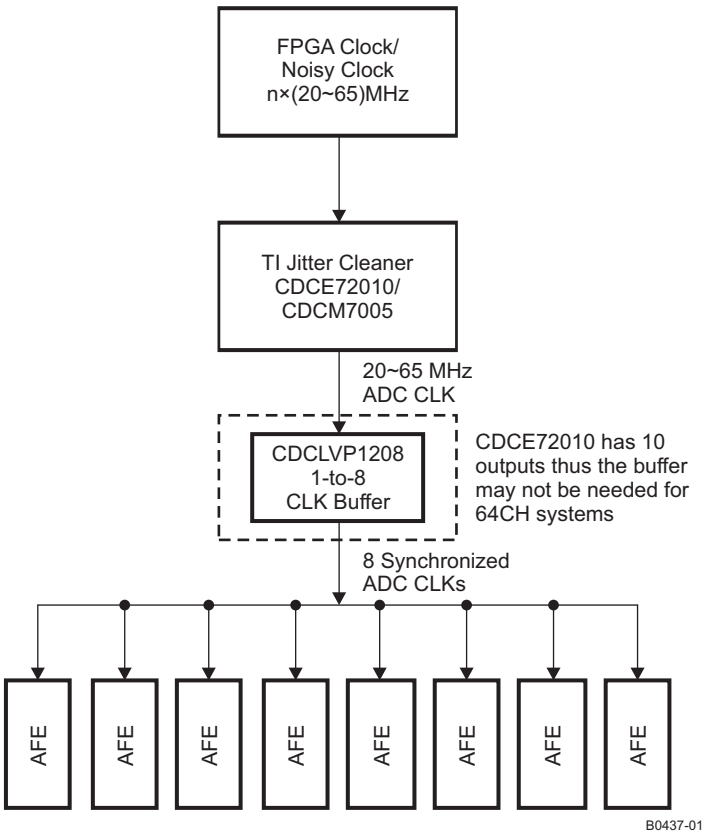


Figure 75. ADC Clock Distribution Network

In the single-end case, it is recommended that the use of low jitter square signals (LVCMOS levels, 1.8 V amplitude). See TI document SLYT075 for further details on the theory.

The jitter cleaner CDCM7005 or CDCE72010 is suitable to generate the AFE5803's ADC clock and ensure the performance for the14 bit ADC with 77 dBFS SNR. A clock distribution network is shown in Figure 75.

The AFE5803 can accept differential LVDS, LVPECL, and other differential clock inputs as well as single-ended clock. AC coupling is required between clock drivers and the AFE5803 clock inputs. When single-ended clock is used, CLKM should be tied to ground. Common clock configurations are illustrated in Figure 76. Appropriate termination is recommended to achieve good signal integrity.

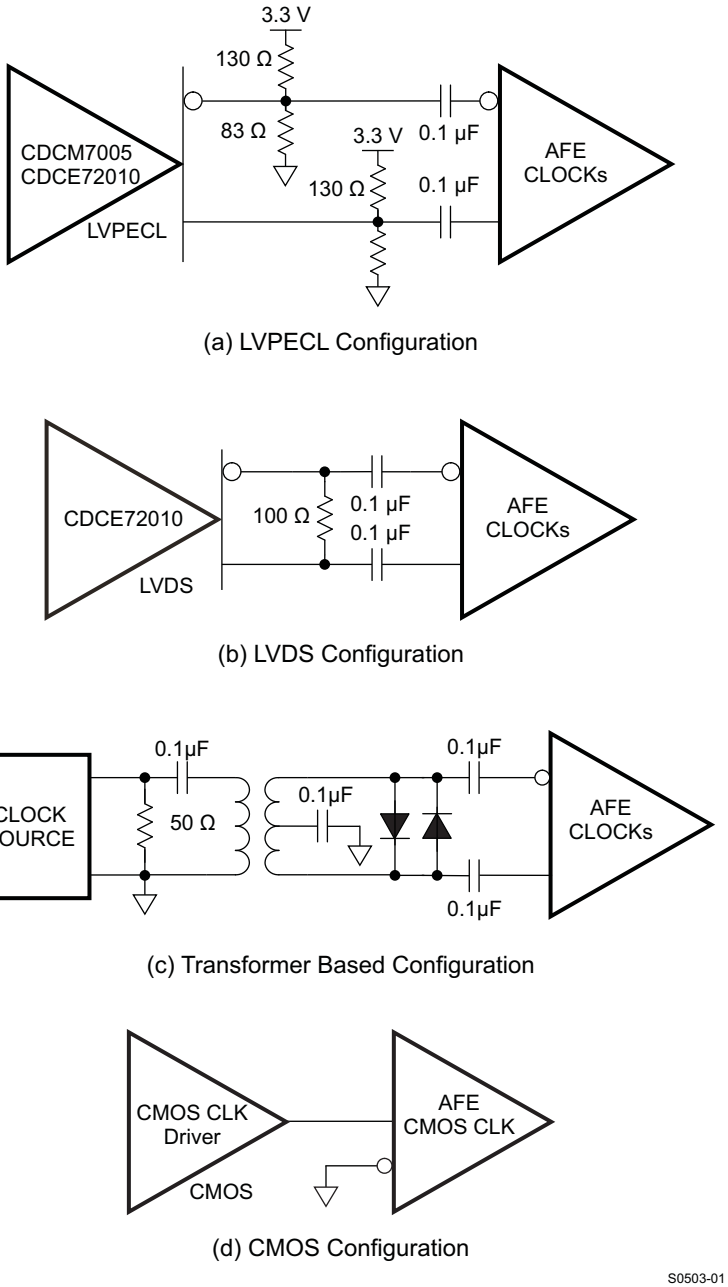


Figure 76. Clock Configurations

Special considerations should be applied in such a clock distribution network design. In typical ultrasound systems, it is preferred that all clocks are generated from a same clock source, such as CW clocks, audio ADC clocks, RF ADC clock, pulse repetition frequency signal, frame clock and etc. By doing this, interference due to clock asynchronization can be minimized.

ADC Reference Circuit

The ADC's voltage reference can be generated internally or provided externally. When the internal reference mode is selected, the REFP/M becomes output pins and should be floated. When 3[15] =1 and 1[13]=1, the device is configured to operate in the external reference mode in which the VREF_IN pin should be driven with a 1.4V reference voltage and REFP/M must be left open. Since the input impedance of the VREF_IN is high, no special drive capability is required for the 1.4V voltage reference

The digital beam-forming algorithm in an ultrasound system relies on gain matching across all receiver channels. A typical system would have about 12 octal AFEs on the board. In such a case, it is critical to ensure that the gain is matched, essentially requiring the reference voltages seen by all the AFEs to be the same. Matching references within the eight channels of a chip is done by using a single internal reference voltage buffer. Trimming the reference voltages on each chip during production ensures that the reference voltages are well-matched across different chips. When the external reference mode is used, a solid reference plane on a printed circuit board can ensure minimal voltage variation across devices. More information on voltage reference design can be found in the document SLYT339. The dominant gain variation in the AFE5803 comes from the VCA gain variation. The gain variation contributed by the ADC reference circuit is much smaller than the VCA gain variation. Hence, in most systems, using the ADC internal reference mode is sufficient to maintain good gain matching among multiple AFE5803s. In addition, the internal reference circuit without any external components achieves satisfactory thermal noise and phase noise performance.

POWER MANAGEMENT

Power/Performance Optimization

The AFE5803 has options to adjust power consumption and meet different noise performances. This feature would be useful for portable systems operated by batteries when low power is more desired. See the electrical characteristics table as well as the typical characteristic plots.

Power Management Priority

Power management plays a critical role to extend battery life and ensure long operation time. The AFE5803 has fast and flexible power down/up control which can maximize battery life. The AFE5803 can be powered down/up through external pins or internal registers. The following table indicates the affected circuit blocks and priorities when the power management is invoked. The higher priority controls can overwrite the lower priority ones.In the device, all the power down controls are logically ORed to generate final power down for different blocks. Thus, the higher priority controls can cover the lower priority ones. The AFE5803 register settings are maintained when the AFE5803 is in either partial power down mode or complete power down mode.

Table 11. Power Management Priority

	Name	Blocks	Priority
Pin	PDN_GLOBAL	All	High
Pin	PDN_VCA	LNA + VCAT+ PGA	Medium
Register	VCA_PARTIAL_PDN	LNA + VCAT+ PGA	Low
Register	VCA_COMPLETE_PDN	LNA + VCAT+ PGA	Medium
Pin	PDN_ADC	ADC	Medium
Register	ADC_PARTIAL_PDN	ADC	Low
Register	ADC_COMPLETE_PDN	ADC	Medium
Register	PDN_VCAT_PGA	VCAT + PGA	Lowest
Register	PDN_LNA	LNA	Lowest

Partial Power-Up/Down Mode

The partial power up/down mode is also called as fast power up/down mode. In this mode, most amplifiers in the signal path are powered down, while the internal reference circuits remain active as well as the LVDS clock circuit, i.e. the LVDS circuit still generates its frame and bit clocks.

The partial power down function allows the AFE5803 to be wake up from a low-power state quickly. This configuration ensures that the external capacitors are discharged slowly; thus a minimum wake-up time is needed as long as the charges on those capacitors are restored. The VCA wake-up response is typically about 2 µs or 1% of the power down duration whichever is larger. The longest wake-up time depends on the capacitors connected at INP and INM, as the wake-up time is the time required to recharge the caps to the desired operating voltages. For 0.1µF at INP and 15nF at INM can give a wake-up time of 2.5ms. For larger capacitors this time will be longer. The ADC wake-up time is about 1 µs. Thus the AFE5803 wake-up time is more dependent on the VCA wake-up time. This also assumes that the ADC clock has been running for at least 50 µs before normal operating mode resumes. The power-down time is instantaneous, less than 1.0µs.

This fast wake-up response is desired for portable ultrasound applications in which the power saving is critical. The pulse repetition frequency of a ultrasound system could vary from 50KHz to 500Hz, while the imaging depth (i.e., the active period for a receive path) varies from 10 µs to hundreds of us. The power saving can be pretty significant when a system's PRF is low. In some cases, only the VCA would be powered down while the ADC keeps running normally to ensure minimal impact to FPGAs.

In the partial power-down mode, the AFE5803 typically dissipates only 26mW/ch, representing an 80% power reduction compared to the normal operating mode. This mode can be set using either pins (PDN_VCA and PDN_ADC) or register bits (VCA_PARTIAL_PDN and ADC_PARTIAL_PDN).

Complete Power-Down Mode

To achieve the lowest power dissipation of 0.7 mW/CH, the AFE5803 can be placed into a complete power-down mode. This mode is controlled through the registers ADC_COMPLETE_PDN, VCA_COMPLETE_PDN or PDN_GLOBAL pin. In the complete power-down mode, all circuits including reference circuits within the AFE5803 are powered down; and the capacitors connected to the AFE5803 are discharged. The wake-up time depends on the time needed to recharge these capacitors. The wake-up time depends on the time that the AFE5803 spends in shutdown mode. 0.1µF at INP and 15 nF at INM can give a wake-up time close to 2.5ms.

VCA TEST MODES

The AFE5803 includes multiple test modes to accelerate system development. The ADC test modes have been discussed in the register description section.

The VCA has a test mode in which the CH7 and CH8 PGA outputs can be brought. By monitoring these PGA outputs, the functionality of VCA operation can be verified. Some registers are related to this test mode. PGA Test Mode Enable: Reg59[9]; Buffer Amplifier Power Down Reg59[8]; and Buffer Amplifier Gain Control Reg54[4:0].

The PGA outputs are connected to the virtual ground pins of the buffer amplifier through 5 kΩ resistors. The PGA outputs can be monitored at the buffer amplifier outputs when the buffer amplifer is enabled. Note that the signals at the buffer amplifier outputs are attenuated due to the 5KΩ resistors. The attenuation coefficient is $R_{INT/EXT}$/5kΩ. See Table 7 for the R_{INT} configuration.

An alternative way is to measure the PGA outputs directly at the CH8_TEST_OUTM/P and CH7_TEST_OUTM/P when the buffer amplifier is powered down.

Based on the buffer amplifier configuration, the registers can be set in different ways:

Configuration 1:

In this configuration, the test outputs can be monitored at CH7/8_TEST_OUTP/M

Reg59[9]=1 ;Test mode enabled

Reg59[8]=0 ;Buffer amplifier powered down

Configuration 2:

In this configuration, the test outputs can be monitored at CH7/8_BUFFER_OUTP/M

Reg59[9]=1 ;Test mode enabled

Reg59[8]=1 ;Buffer amplifier powered on

Reg54[4:0]=10H; Internal feedback 2K resistor enabled. Different values can be used as well

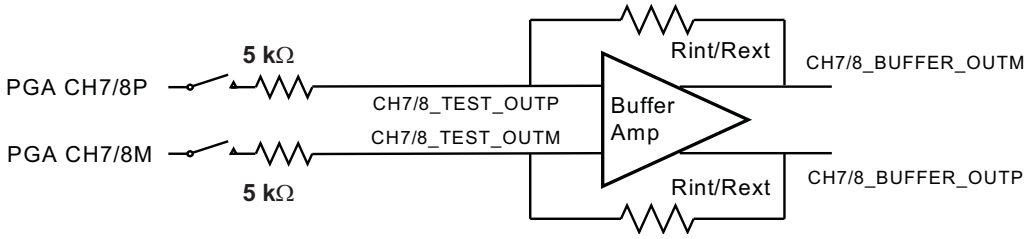


Figure 77. AFE5803 PGA Test Mode

POWER SUPPLY, GROUNDING AND BYPASSING

In a mixed-signal system design, power supply and grounding design plays a significant role. The AFE5803 distinguishes between two different grounds: AVSS(Analog Ground) and DVSS(digital ground). In most cases, it should be adequate to lay out the printed circuit board (PCB) to use a single ground plane for the AFE5803. Care should be taken that this ground plane is properly partitioned between various sections within the system to minimize interactions between analog and digital circuitry. Alternatively, the digital (DVDD) supply set consisting of the DVDD and DVSS pins can be placed on separate power and ground planes. For this configuration, the AVSS and DVSS grounds should be tied together at the power connector in a star layout. In addition, optical isolator or digital isolators, such as ISO7240, can separate the analog portion from the digital portion completely. Consequently they prevent digital noise to contaminate the analog portion. Table 11 lists the related circuit blocks for each power supply.

Table 12. Supply vs Circuit Blocks

POWER SUPPLY	GROUND	CIRCUIT BLOCKS
AVDD (3.3VA)	AVSS	LNA, attenuator, PGA with current clamp and BPF, reference circuits, PGA test mode buffer, VCA SPI
AVDD_5V (5VA)	AVSS	LNA, reference circuits
AVDD_ADC (1.8VA)	AVSS	ADC analog and reference circuits
DVDD (1.8VD)	DVSS	LVDS and ADC SPI

All Bypassing and power supplies for the AFE5803 should be referenced to their corresponding ground planes. All supply pins should be bypassed with 0.1 µF ceramic chip capacitors (size 0603 or smaller). In order to minimize the lead and trace inductance, the capacitors should be located as close to the supply pins as possible. Where double-sided component mounting is allowed, these capacitors are best placed directly under the package. In addition, larger bipolar decoupling capacitors 2.2 µF to 10 µF, effective at lower frequencies) may also be used on the main supply pins. These components can be placed on the PCB in proximity (< 0.5 in or 12.7 mm) to the AFE5803 itself.

The AFE5803 has a number of reference supplies needed to be bypassed, such CM_BYP, VHIGH, and VREF_IN. These pins should be bypassed with at least 1µF; higher value capacitors can be used for better low-frequency noise suppression. For best results, choose low-inductance ceramic chip capacitors (size 0402, > 1 µF) and place them as close as possible to the device pins.

High-speed mixed signal devices are sensitive to various types of noise coupling. One primary source of noise is the switching noise from the serializer and the output buffer/drivers. For the AFE5803, care has been taken to ensure that the interaction between the analog and digital supplies within the device is kept to a minimal amount. The extent of noise coupled and transmitted from the digital and analog sections depends on the effective inductances of each of the supply and ground connections. Smaller effective inductance of the supply and ground pins leads to improved noise suppression. For this reason, multiple pins are used to connect each supply and ground sets. It is important to maintain low inductance properties throughout the design of the PCB layout by use of proper planes and layer thickness.

BOARD LAYOUT

Proper grounding and bypassing, short lead length, and the use of ground and power-supply planes are particularly important for high-frequency designs. Achieving optimum performance with a high-performance device such as the AFE5803 requires careful attention to the PCB layout to minimize the effects of board parasitics and optimize component placement. A multilayer PCB usually ensures best results and allows convenient component placement. In order to maintain proper LVDS timing, all LVDS traces should follow a controlled impedance design. In addition, all LVDS trace lengths should be equal and symmetrical; it is recommended to keep trace length variations less than 150mil (0.150 in or 3.81mm).

Additional details on BGA PCB layout techniques can be found in the Texas Instruments Application Report MicroStar BGA Packaging Reference Guide (SSYZ015B), which can be downloaded from www.ti.com.

REVISION HISTORY

Changes from Original (January 2012) to Revision A **Page**

- Changed Table 3 Digital HPF –1dB Corner Frequency vs K and Fs 27

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AFE5803ZCF	Active	Production	NFBGA (ZCF) | 135	160 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	0 to 85	AFE5803
AFE5803ZCF.A	Active	Production	NFBGA (ZCF) | 135	160 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	0 to 85	AFE5803
AFE5803ZCF.B	Active	Production	NFBGA (ZCF) | 135	160 | JEDEC TRAY (5+1)	-	Call TI	Call TI	0 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

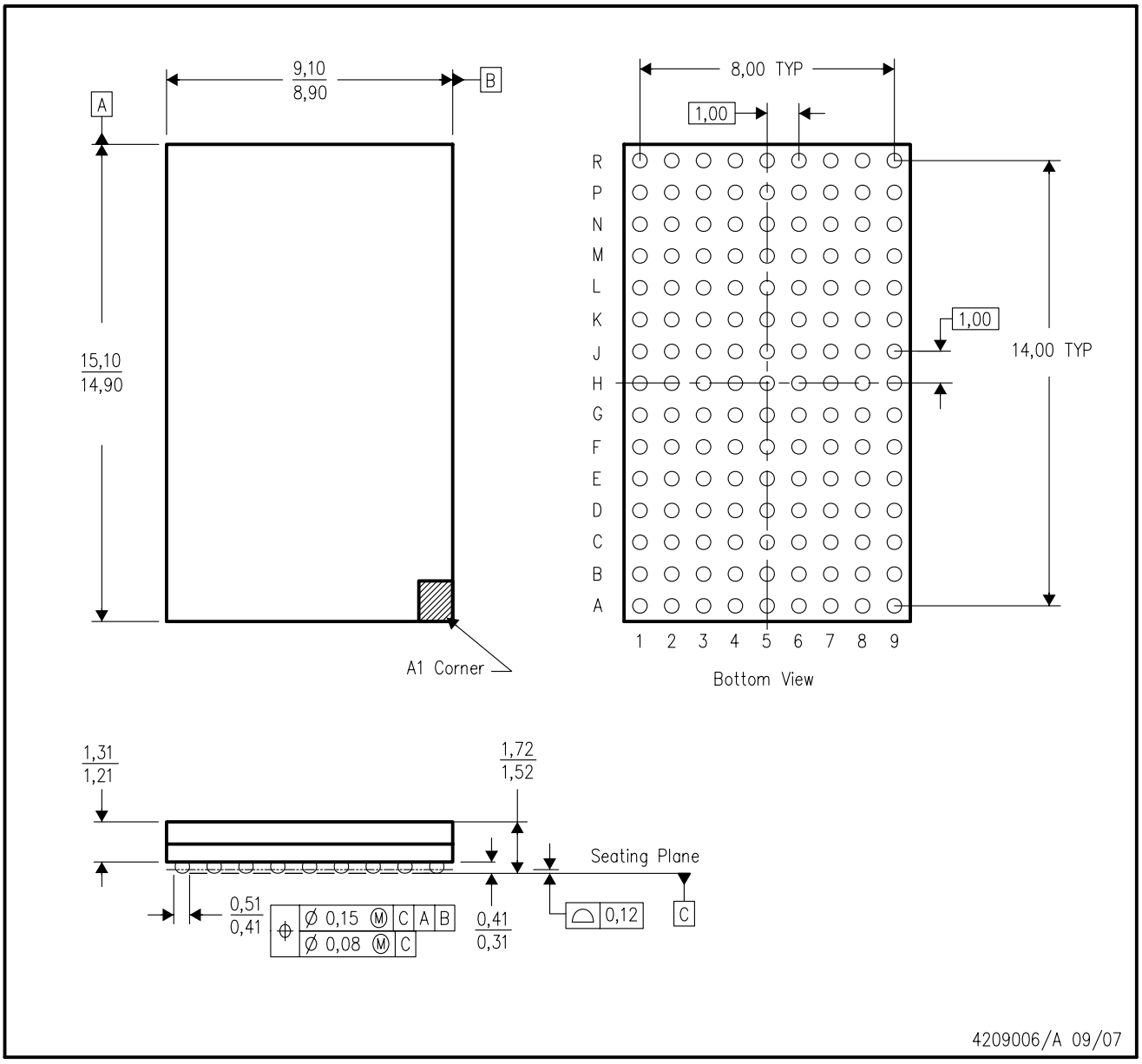
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

ZCF (R–PBGA–N135) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994 .
B. This drawing is subject to change without notice.
C. This is a lead–free solder ball design.

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