# ADS7811

SBAS041A – NOVEMBER 1997 – REVISED NOVEMBER 2006

# 16-Bit 250kHz Sampling CMOS ANALOG-to-DIGITAL CONVERTER

## FEATURES

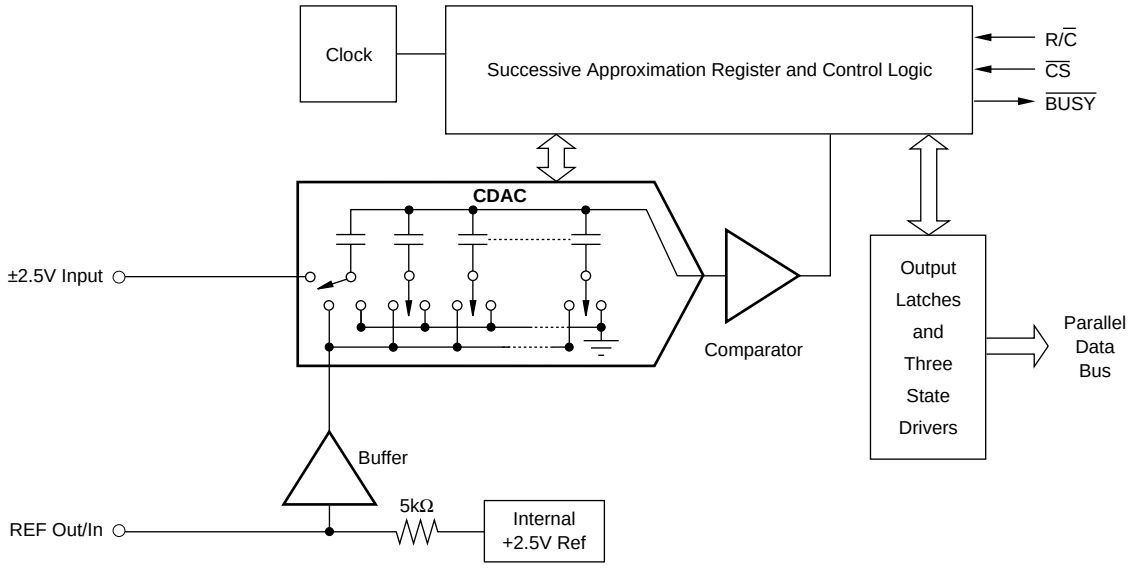
- **250kHz SAMPLING RATE**
- **COMPLETE WITH S/H, REF, CLOCK, ETC.**
- **96dB min SFDR WITH 100kHz INPUT**
- **84dB min SINAD**
- **±2.5V INPUT RANGE**
- **28-LEAD SOIC**

## APPLICATIONS

- **WIRELESS BASE STATIONS**
- **SPECTRUM ANALYSIS**
- **IMAGING SYSTEMS**
- **DATA ACQUISITION**

## DESCRIPTION

The ADS7811 is a complete 16-bit sampling analog-to-digital (A/D) converter featuring excellent AC performance and a 250kHz throughput rate. The design includes a 16-bit capacitor-based SAR A/D converter with an inherent sample and hold (S/H), a precision reference, and an internal clock. Spurious-free dynamic range with a 100kHz full-scale sinewave input is typically greater than 100dB. The ±2.5V input range allows development of precision systems using only ±5V supplies. The converter is available in a 28-lead SOIC package specified for operation over the industrial –25°C to +85°C temperature range.



## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Inputs: $V_{IN}$ | $-V_S$ – 0.3V to $+V_S$ + 0.3V |
| REF | – 0.3V to $+V_S$ + 0.3V |
| CAP | Indefinite Short to GND |
| | Momentary Short to $+V_S$ |
| $+V_S$ | 7V |
| $-V_S$ | –7V |
| Digital Inputs | –0.3V to $+V_S$ + 0.3V |
| Maximum Junction Temperature | +165°C |
| Internal Power Dissipation | 825mW |
| Lead Temperature (soldering, 10s) | +300°C |

## PACKAGE/ORDERING INFORMATION[1]

| PRODUCT | PACKAGE | PACKAGE DESIGNATOR | TEMPERATURE RANGE |
|---|---|---|---|
| ADS7811U | 28-Pin SOIC | DW | –25°C to +85°C |

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI web site at www.ti.com.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

# ELECTRICAL CHARACTERISTICS

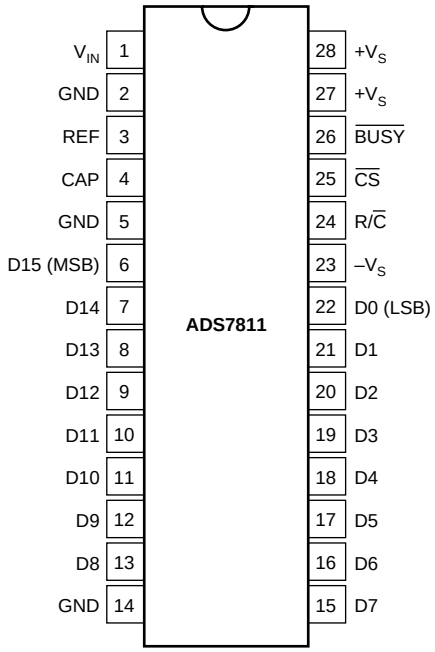
At $T_A$ = –25°C to +85°C, $f_S$ = 250kHz, $+V_S$ = +5V, and $–V_S$ = –5V, using internal reference, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7811U MIN | ADS7811U TYP | ADS7811U MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | | | 16 | Bits |
| **ANALOG INPUT** | | | | | |
| Voltage Range | | | ±2.5V | | V |
| Impedance | After Input Capacitor is Charged | | 100 | | MΩ |
| Capacitance | | | 30 | | pF |
| **THROUGHPUT SPEED** | | | | | |
| Conversion Cycle | Acquire and Convert | | | 4.0 | µs |
| Throughput Rate | | 250 | | | kHz |
| **DC ACCURACY** | | | | | |
| Integral Linearity Error | | | | ±6 | LSB(1) |
| No Missing Codes | | 15 | | | Bits |
| Transition Noise(2) | | | 0.8 | | LSB |
| Full-Scale Error(3) | | | | ±0.5 | % |
| Full-Scale Error Drift | | | ±7 | | ppm/°C |
| Full-Scale Error(3) | External 2.5000V Reference | | ±0.2 | | % |
| Full-Scale Error Drift | External 2.5000V Reference | | 2 | | ppm/°C |
| Bipolar Zero Error | | | | ±10 | mV |
| Bipolar Zero Error Drift | | | ±2 | | ppm/°C |
| Power-Supply Sensitivity | $+V_S$ ±5%, $–V_S$ ±5% | | ±6 | ±16 | LSB |
| **AC ACCURACY** | | | | | |
| Spurious-Free Dynamic Range | $f_{IN}$ = 100kHz | 96 | 100 | | dB(4) |
| Total Harmonic Distortion | $f_{IN}$ = 100kHz | | –98 | –94 | dB |
| Signal-to-(Noise+Distortion) | $f_{IN}$ = 100kHz | 82 | 87 | | dB |
| | –60dB Input | | 28 | | dB |
| Signal-to-Noise | $f_{IN}$ = 100kHz | 82 | 87 | | dB |
| Usable Bandwidth(5) | | | 1 | | MHz |
| Aperture Delay | | | 40 | | ns |
| **REFERENCE** | | | | | |
| Internal Reference Voltage | | 2.48 | 2.5 | 2.52 | V |
| Internal Reference Source Current | | | 1 | | µA |
| Internal Reference Drift | | | 15 | | ppm/°C |
| External Reference Voltage Range | | | 2.5 | | V |
| External Reference Current Drain | $V_{REF}$ = +2.5V | | | 100 | µA |
| **DIGITAL INPUTS** | | | | | |
| Logic Levels | | | | | |
| $V_{IL}$ | | –0.3 | | +0.8 | V |
| $V_{IH}$ | | +2.8 | | $+V_S$ +0.3V | V |
| $I_{IL}$ | | | | ±10 | µA |
| $I_{IH}$ | | | | ±10 | µA |
| **DIGITAL OUTPUTS** | | | | | |
| Data Format | | | Parallel 16 bits | | |
| Data Coding | | | Binary Two's Complement | | |
| $V_{OL}$ | $I_{SINK}$ = 1.6mA | | | +0.4 | V |
| $V_{OH}$ | $I_{SOURCE}$ = 200µA | +4 | | | V |
| Leakage Current | High-Z State, $V_{OUT}$ = 0V to $V_{DIG}$ | | | ±5 | µA |
| Output Capacitance | High-Z State | | | 15 | pF |
| **DIGITAL TIMING** | | | | | |
| Bus Access Time | | | | 83 | ns |
| Bus Relinquish Time | | | | 83 | ns |
| **POWER SUPPLIES** | | | | | |
| $+V_S$ | | +4.75 | +5 | +5.25 | V |
| $–V_S$ | | –5.25 | –5 | –4.75 | V |
| $+I_S$ | | | +30 | | mA |
| $–I_S$ | | | –10 | | mA |
| Power Dissipation | | | 200 | 250 | mW |
| **TEMPERATURE RANGE** | | | | | |
| Specified Performance | | –25 | | +85 | °C |
| Storage | | –55 | | +125 | °C |

NOTES: (1) LSB means Least Significant Bit. For the 16-bit, ±2.5V input ADS7811, one LSB is 76µV.
(2) Typical rms noise at worst case transitions and temperatures.
(3) Full-scale error is the worst case of –Full-Scale or +Full-Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error.
(4) All specifications in dB are referred to a full-scale ±2.5V input.
(5) Usable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB, or 10 bits of accuracy.

## PIN CONFIGURATION

**Top View** **SOIC**



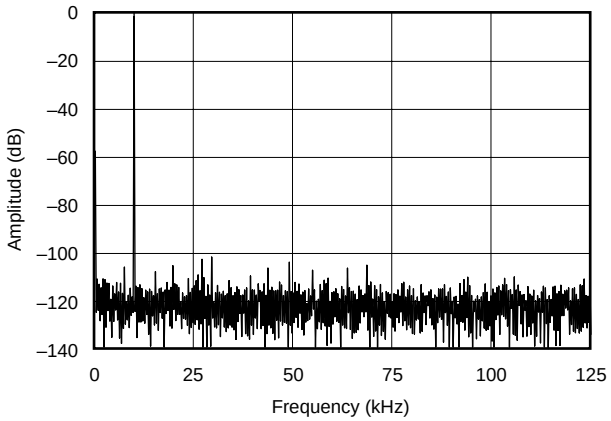

| PIN # | NAME | DESCRIPTION |
|---|---|---|
| 1 | $V_{IN}$ | Analog Input. Full-scale input range is ±2.5V. |
| 2 | GND | Ground. |
| 3 | REF | Reference Input/Output. Outputs internal reference of +2.5V nominal. Can also be driven by external system reference. In both cases, connect to ground with a 0.1µF ceramic capacitor in parallel with 2.2µF tantalum capacitor. |
| 4 | CAP | Reference compensation capacitor. Use a parallel combination of a 0.1µF ceramic capacitor and a 2.2µF tantalum capacitor. |
| 5 | GND | Ground. |
| 6 | D15 (MSB) | Data Bit 15. Most Significant Bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 7 | D14 | Data Bit 14. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 8 | D13 | Data Bit 13. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 9 | D12 | Data Bit 12. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 10 | D11 | Data Bit 11. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 11 | D10 | Data Bit 10. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 12 | D9 | Data Bit 9. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 13 | D8 | Data Bit 8. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 14 | GND | Ground. |
| 15 | D7 | Data Bit 7. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 16 | D6 | Data Bit 6. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 17 | D5 | Data Bit 5. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 18 | D4 | Data Bit 4. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 19 | D3 | Data Bit 3. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 20 | D2 | Data Bit 2. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 21 | D1 | Data Bit 1. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 22 | D0 (LSB) | Data Bit 0. Least Significant Bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, when R/$\overline{C}$ is LOW or when a conversion is in progress. |
| 23 | $-V_S$ | Negative supply input. Nominally –5V. Decouple to analog ground with 0.1µF ceramic and 10µF tantalum capacitors. |
| 24 | R/$\overline{C}$ | Read/convert input. With R/$\overline{C}$ HIGH, $\overline{CS}$ going LOW will enable the output data bits if a conversion is not in progress. With R/$\overline{C}$ LOW, $\overline{CS}$ going LOW will start a conversion if one is not already in progress. |
| 25 | $\overline{CS}$ | Chip select. With R/$\overline{C}$ LOW, $\overline{CS}$ going LOW will initiate a conversion if one is not already in progress. With R/$\overline{C}$ HIGH, $\overline{CS}$ going LOW will enable the output data bits if a conversion is not in progress. |
| 26 | $\overline{BUSY}$ | Busy output. Falls when a conversion is started, and remains LOW until the conversion is completed. With $\overline{CS}$ LOW and R/$\overline{C}$ HIGH, output data will be valid when $\overline{BUSY}$ rises, so that the rising edge can be used to latch the data. $\overline{CS}$ or R/$\overline{C}$ must be HIGH within 250ns after $\overline{BUSY}$ rises or another conversion will start without time for signal acquisition. |
| 27 | $+V_S$ | Positive supply input. Nominally +5V. Connect directly to pin 28. |
| 28 | $+V_S$ | Positive supply input. Nominally +5V. Connect directly to pin 27. Decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors. |

TABLE I. Pin Assignments.

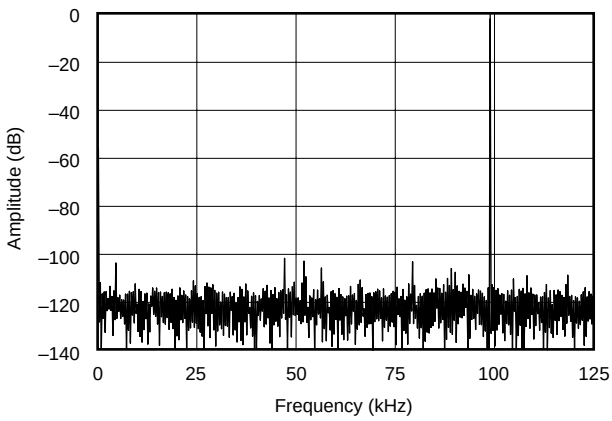
# TYPICAL PERFORMANCE CURVES

At $T_A$ = –25°C to +85°C, $f_S$ = 250kHz, $+V_S$ = +5V, and $–V_S$ = –5V, using internal reference, unless otherwise specified.

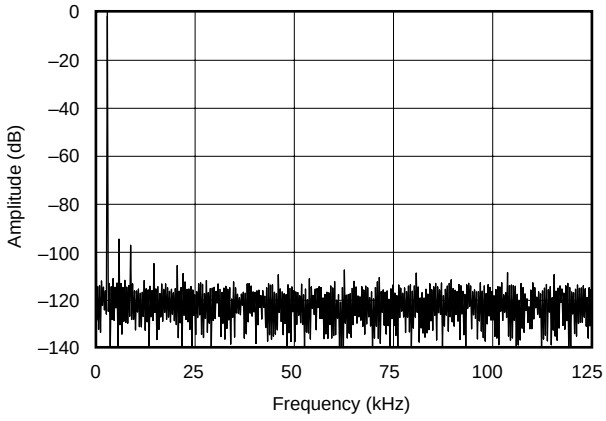
FREQUENCY SPECTRUM
(4096 Point FFT; $f_{IN}$ = 9.9kHz, –0.5dB)



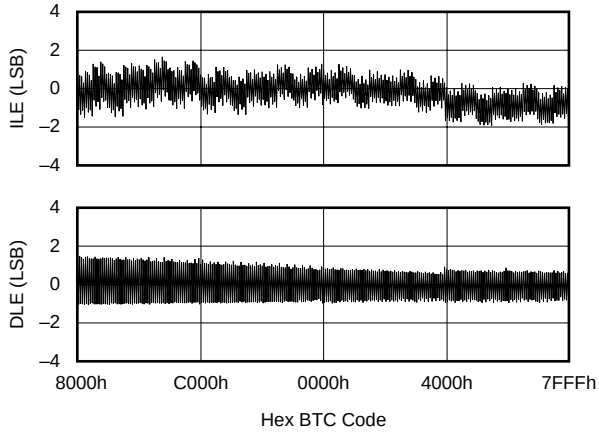

FREQUENCY SPECTRUM
(4096 Point FFT; $f_{IN}$ = 99kHz, –0.5dB)



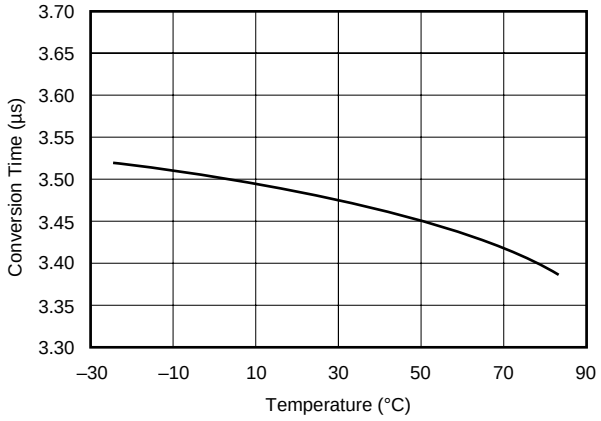

FREQUENCY SPECTRUM
(4096 Point FFT; $f_{IN}$ = 247kHz, –0.5dB)



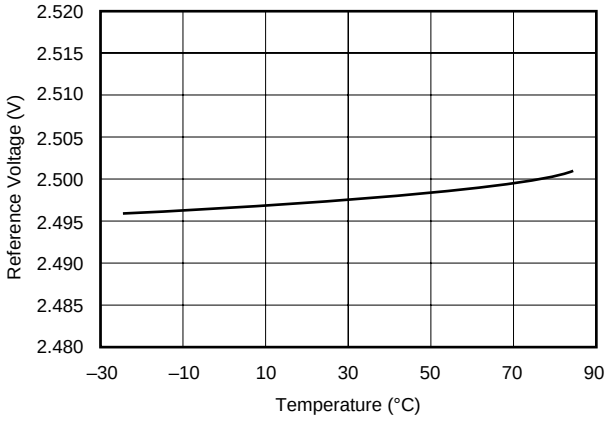

INTEGRAL LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR
vs OUTPUT CODE




CONVERSION TIME ($t_2$ + $t_4$)
vs TEMPERATURE




REFERENCE VOLTAGE
vs TEMPERATURE



# BASIC OPERATION

Figure 1 shows the recommended circuit for operation of the ADS7811. A falling edge on the convert pulse signal places the sample and hold into the hold mode and initiates a conversion. When the conversion is complete, the pins D15 through D0 become active and the result of the conversion is placed on these outputs. In the circuit shown in Figure 1, the rising edge of $\overline{BUSY}$ latches the result into the 74HC574s.

After the conversion is complete, the ADS7811 sample and hold returns to the sample mode and begins acquiring the input signal for the next conversion. Allowing 4µs between falling edges of the convert pulse signal assures adequate acquisition time for the internal sample and hold.

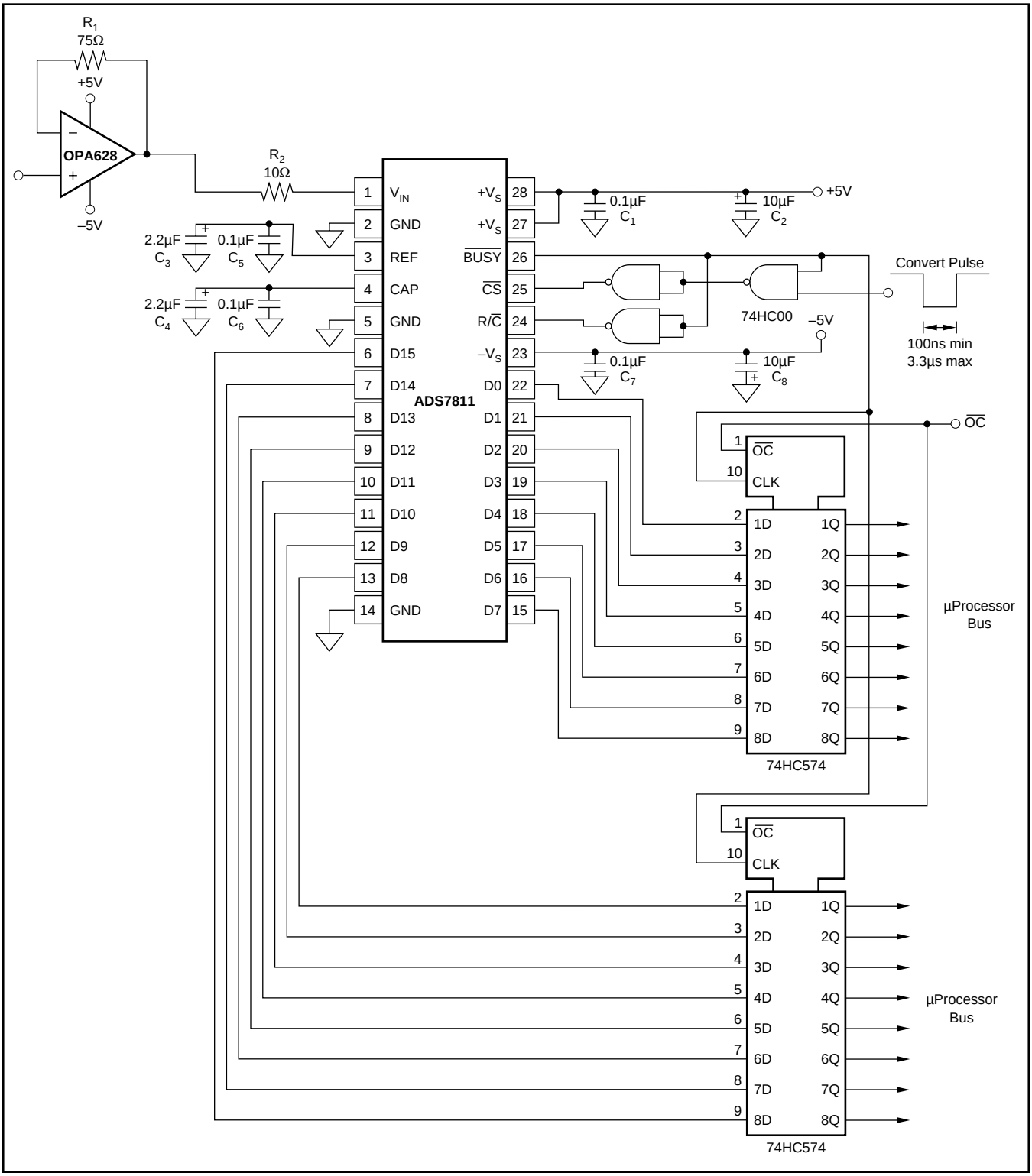



FIGURE 1. Basic Operation.

# TIMING

The timing shown in Figure 2 and Table II is the recommended method of operating the ADS7811. The falling edge of $\overline{CS}$ initiates the conversion. During the conversion, the digital outputs are tri-stated and $\overline{BUSY}$ is LOW. Near the end of the conversion, the digital outputs become active with the most recent conversion result. After a brief delay (see time $t_{11}$ in Figure 2 and Table II), $\overline{BUSY}$ rises. The rising edge of $\overline{BUSY}$ is used to latch the digital result in Figure 1.

### R/$\overline{C}$ AND $\overline{CS}$

The R/$\overline{C}$ (read/convert) and $\overline{CS}$ signals control the start of conversion and, when a conversion is not in progress, the status of the digital outputs D15 through D0. It is possible to start a conversion by taking $\overline{CS}$ LOW and then taking R/$\overline{C}$ LOW. However, this is not recommended and will result in a significant decrease in signal-to-noise ratio. This is due to the digital outputs tri-stating while the sample and hold transitions to the hold mode. The change in digital outputs results in noise being coupled onto the hold capacitor.

If a conversion is not in progress or is just about to finish, the digital outputs will be active when R/$\overline{C}$ is HIGH and $\overline{CS}$ is LOW. This is shown in Figure 2 and Figure 3. It is possible to return $\overline{CS}$ HIGH during the initial part of the conversion (as is done with R/$\overline{C}$) and prevent the digital outputs from becoming active. At a later time, the digital results could be read by taking $\overline{CS}$ LOW. It is also possible to leave R/$\overline{C}$ LOW, take $\overline{CS}$ HIGH during the conversion, and read the results at a later time by taking R/$\overline{C}$ HIGH and $\overline{CS}$ LOW.

Following a conversion, if R/$\overline{C}$ and $\overline{CS}$ are both LOW 250ns after $\overline{BUSY}$ rises, then a new conversion will be initiated without allowing the proper acquisition period for the sample and hold. R/$\overline{C}$ must remain HIGH or $\overline{CS}$ must be taken HIGH within 250ns of $\overline{BUSY}$ rising.

R/$\overline{C}$ and $\overline{CS}$ should remain static prior to that start of conversion and during the later part of a conversion. To start

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_1$ | $\overline{CS}$ to R/$\overline{C}$ Delay | $t_2$ | | 200 | ns |
| $t_2$ | $\overline{CS}$ to $\overline{BUSY}$ Delay | | 40 | | ns |
| $t_3$ | Aperture Delay | | 40 | | ns |
| $t_4$ | $\overline{BUSY}$ LOW | | 3.5 | | µs |
| $t_5$ | R/$\overline{C}$ LOW to $\overline{CS}$ LOW | 100 | | | ns |
| $t_6$ | $\overline{BUSY}$ HIGH to $\overline{CS}$ HIGH | | | 250 | ns |
| $t_7$ | Bus Access Time | | 10 | 83 | ns |
| $t_8$ | Bus Relinquish Time | | | 83 | ns |
| $t_9$ | Throughput Time | | | 4 | µs |
| $t_{10}$ | Conversion Time | | 3.4 | | µs |
| $t_{11}$ | Data Valid to $\overline{BUSY}$ HIGH | 25 | 35 | | ns |
| $t_{12}$ | $\overline{CS}$ to R/$\overline{C}$ Setup Time | 40 | | | ns |

TABLE II. Conversion Timing.

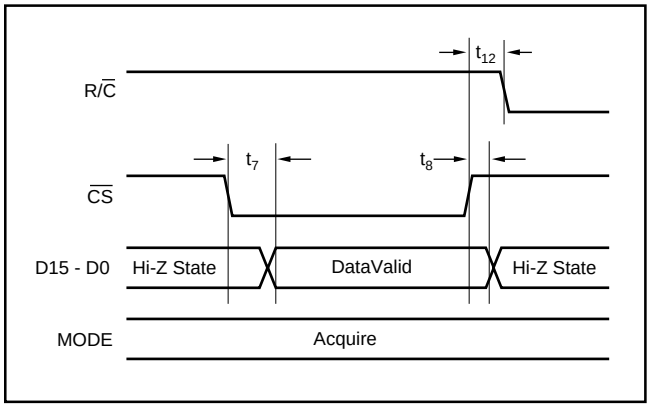



FIGURE 3. Bus Timing.

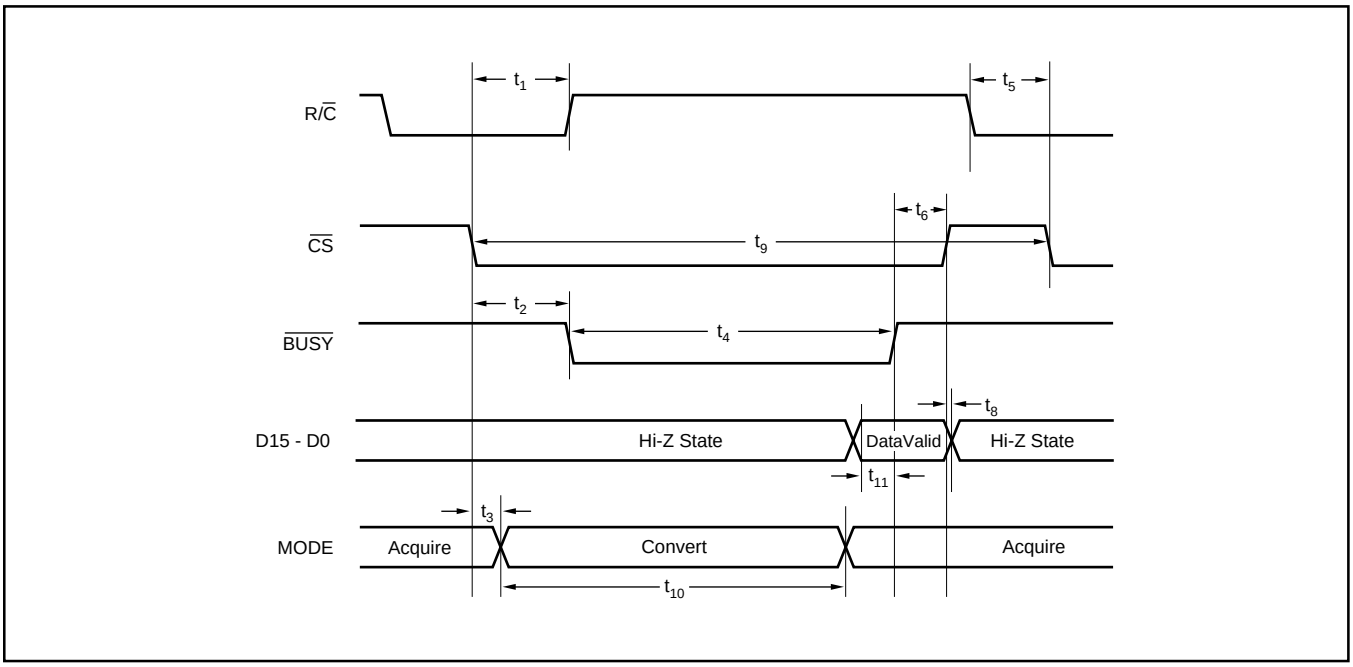



FIGURE 2. ADS7811 Timing.

a conversion, R/$\overline{C}$ should be taken LOW at least 100ns before $\overline{CS}$ is taken LOW. R/$\overline{C}$ and/or $\overline{CS}$ should be taken HIGH during the early part of the conversion, preferably within 200ns of the start of the conversion. If these times are not observed, then there is risk that the transition of these digital signals may affect the conversion result.

The three NAND gates shown in Figure 1 can be used to generate R/$\overline{C}$ and $\overline{CS}$ signals from a single negative going pulse. The pulse must not be longer than 3.3µs or a second conversion may be initiated immediately after the first.

### $\overline{BUSY}$

$\overline{BUSY}$ goes LOW when a conversion is started and remains LOW throughout the conversion. Just prior to $\overline{BUSY}$ going HIGH, the digital outputs become active with the conversion result. Time $t_{11}$, shown in Figure 2, should provide adequate time for the ADS7811 to drive the digital outputs to a valid logic state before $\overline{BUSY}$ rises. As shown in Figure 1 and 2, the rising edge of $\overline{BUSY}$ can be used to latch the digital result into an external component.

## DIGITAL OUTPUT

The ADS7811's digital output is in Binary Two's Complement (BTC) format. Table III shows the relationship between the digital output word and analog input voltage under ideal conditions.

| DESCRIPTION | ANALOG INPUT | DIGITAL OUTPUT | |
|---|---|---|---|
| | | BINARY TWO'S COMPLEMENT | |
| | | BINARY CODE | HEX CODE |
| Full Scale Range | ±2.5V | | |
| Least Significant Bit (LSB) | 76µV | | |
| +Full Scale (2.5V – 1LSB) | 2.499924V | 0111 1111 1111 1111 | 7FFF |
| Midscale | 0V | 0000 0000 0000 0000 | 0000 |
| One LSB below Midscale | –76µV | 1111 1111 1111 1111 | FFFF |
| –Full Scale | –2.5V | 1000 0000 0000 0000 | 8000 |

Table III. Ideal Input Voltages and Output Codes.

## REFERENCE

The ADS7811 can be operated with the internal 2.5V reference or an external reference. By applying an external reference to the REF pin, the internal reference is bypassed. The reference voltage at REF is buffered internally.

The voltage at the reference input sets the full-scale range of the converter. With the internal 2.5V reference, the input range is ±2.5V. Thus, the input range of the converter's analog input is simply $\pm V_{REF}$, where $V_{REF}$ is the voltage at the reference input. Because of internal gain and offset error, the input range will not be exactly $\pm V_{REF}$. The full-scale error of the converter with an external reference will typically be 0.25% or less. The bipolar zero error will be similar to that listed in the Electrical Characteristics Table. The range for the external reference is 2.3V to 2.7V. While the ADS7811 will operate using an external reference, the specifications are only ensured when the internal reference is used.

### REF PIN

The REF pin itself should be bypassed with a 0.1µF ceramic capacitor in parallel with a 2.2µF tantalum capacitor. While both capacitors should be physically close to the ADS7811, it is very important that the ceramic capacitor be placed as close as possible.

The REF voltage should not be used to drive a large load or any load which is dynamic. A large load will reduce the reference voltage and the corresponding input range of the converter. A dynamic load will modulate the reference voltage and this modulation will be present in the converter's output data.

### CAP PIN

The voltage on the CAP pin is the output of the reference buffer. This pin should be bypassed with a 0.1µF ceramic capacitor in parallel with a 2.2µF tantalum capacitor. While both capacitors should be physically close to the ADS7811, it is very important that the ceramic capacitor be placed as close as possible.

The CAP pin connects to the internal reference buffer and directly to the binary weighted capacitor array of the converter. Thus, the signal at the CAP pin has high-frequency glitches which occur at each bit decision. For this reason, the CAP voltage should not be used to provide a reference voltage for external circuitry.

# LAYOUT

The layout of the ADS7811 and accompanying components will be critical for optimum performance. Use of an analog ground plane is essential. Use of +5V and –5V power planes is not critical as long as the supplies are well bypassed, and the traces connecting +5V and –5V to the power connector are not too long or too thin.

The two $+V_S$ power pins of the ADS7811 must be tied together. The voltage source for these pins should also power the input buffer and the 74HC00 shown in Figure 1. This supply should separate from the positive +5V supply for the system's digital logic

Three ground pins are present on the ADS7811: pin 2, pin 5, and pin 14. These should all be tied to the analog ground plane. The analog ground plane should extend underneath all analog signal conditioning components and up to the 74HC574s (or equivalent components) shown in Figure 1. The 74HC574s should not be located more than several inches from the ADS7811.

The ground for the 74HC574s should be connected to the digital ground. The analog ground plane should extend up to the 74HC574s but should be kept at least 1/4" (6mm) distant from the digital ground plane (if present). The analog and digital grounds planes should not overlap at any point.

## INTERMEDIATE LATCHES

The 74HC574s shown in Figure 1 isolate the ADS7811 from digital signals on a microprocessor, digital signal processor (DSP), or microcontroller bus. This is necessary because of the precision needed within the ADS7811. The weight of a single LSB in the ADS7811 is 76μV, and the comparator must be able to resolve differences in voltage to this level. External digital signals which transition during the conversion can easily couple onto the substrate and produce voltages larger than this.

In place of the 74HC574s, it might be possible to use a FIFO or similar type of memory device. For many systems, it may be difficult to go directly from the ADS7811 into a microcontroller or DSP even if the ADS7811 is not connected to shared bus. The reason for this is that the outputs are active only during the acquisition period.

## SIGNAL CONDITIONING

The ADS7811 input essentially consists of a switch and a capacitor. In the acquisition or sample mode, the switch is closed and the input signal drives the capacitor directly. When a conversion is started, the switch is opened capturing the input signal at that moment. This voltage is held on the capacitor for the remainder of the conversion.

While this provides for a wide bandwidth sample and hold function and results in excellent AC performance, this architecture requires a high bandwidth, precision op amp to drive the analog input. The op amp and configuration shown in Figure 1 is highly recommended. The amplifier should be placed within 1 to 2 inches (25 to 50mm) of the ADS7811, and the layout guidelines in the OPA628 data sheet should be strictly followed.

## Revision History

| DATE | REVISION | PAGE | SECTION | DESCRIPTION |
|---|---|---|---|---|
| 11/06 | A | — | Entire Document | Updated document format to current standard; some page layout changed. |
| | | 3 | Electrical Characteristics | Changed Integral Linearity Error from max value ±4 to ±6. |
| | | | | Changed Total Harmonic Distortion max value from –96 to –94. |
| | | | | Changed Signal-to-(Noise+Distortion) min value from 84 to 82. |
| | | | | Changed Signal-to-Noise min value from 84 to 82. |

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| ADS7811U | Active | Production | SOIC (DW) \| 28 | 20 \| TUBE | Yes | Call TI | Level-3-260C-168 HR | -25 to 85 | ADS7811U |
| ADS7811U.A | Active | Production | SOIC (DW) \| 28 | 20 \| TUBE | Yes | Call TI | Level-3-260C-168 HR | -25 to 85 | ADS7811U |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

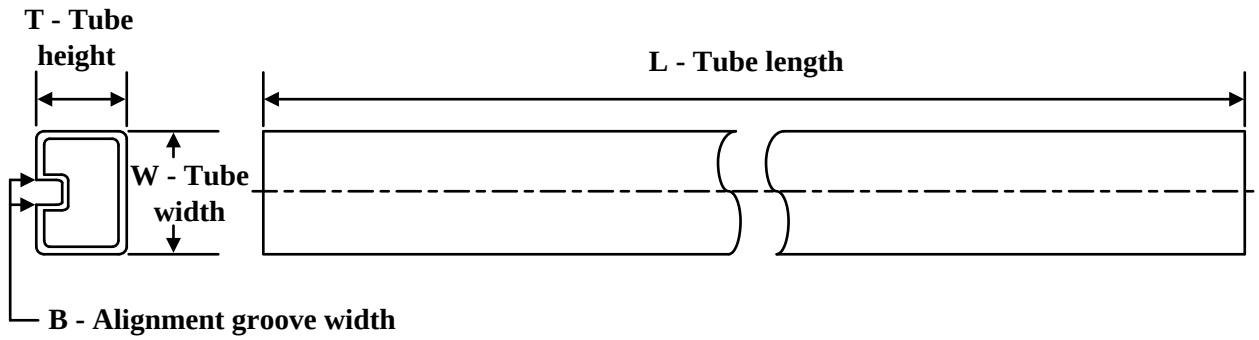
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

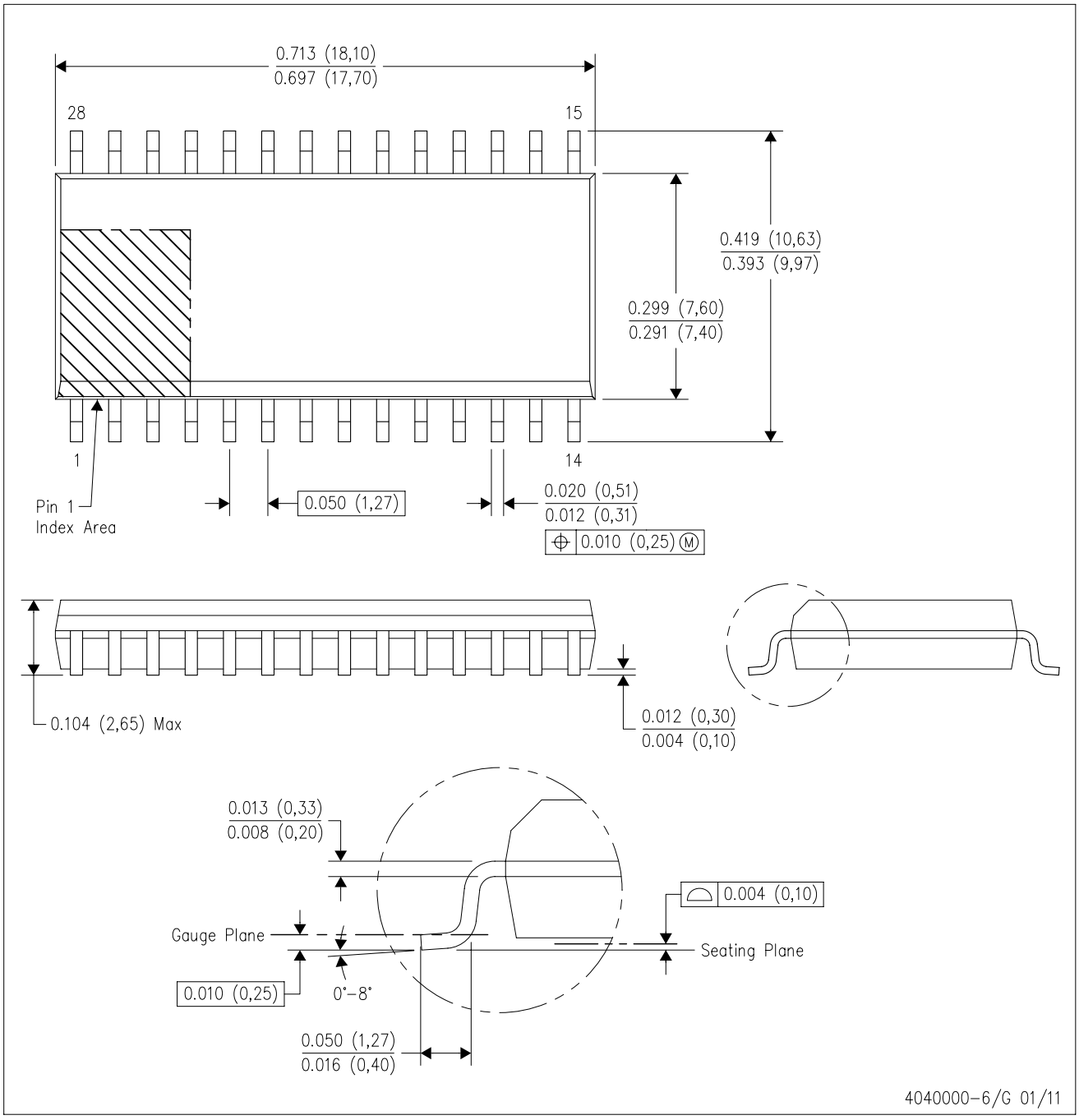
## TUBE




*All dimensions are nominal

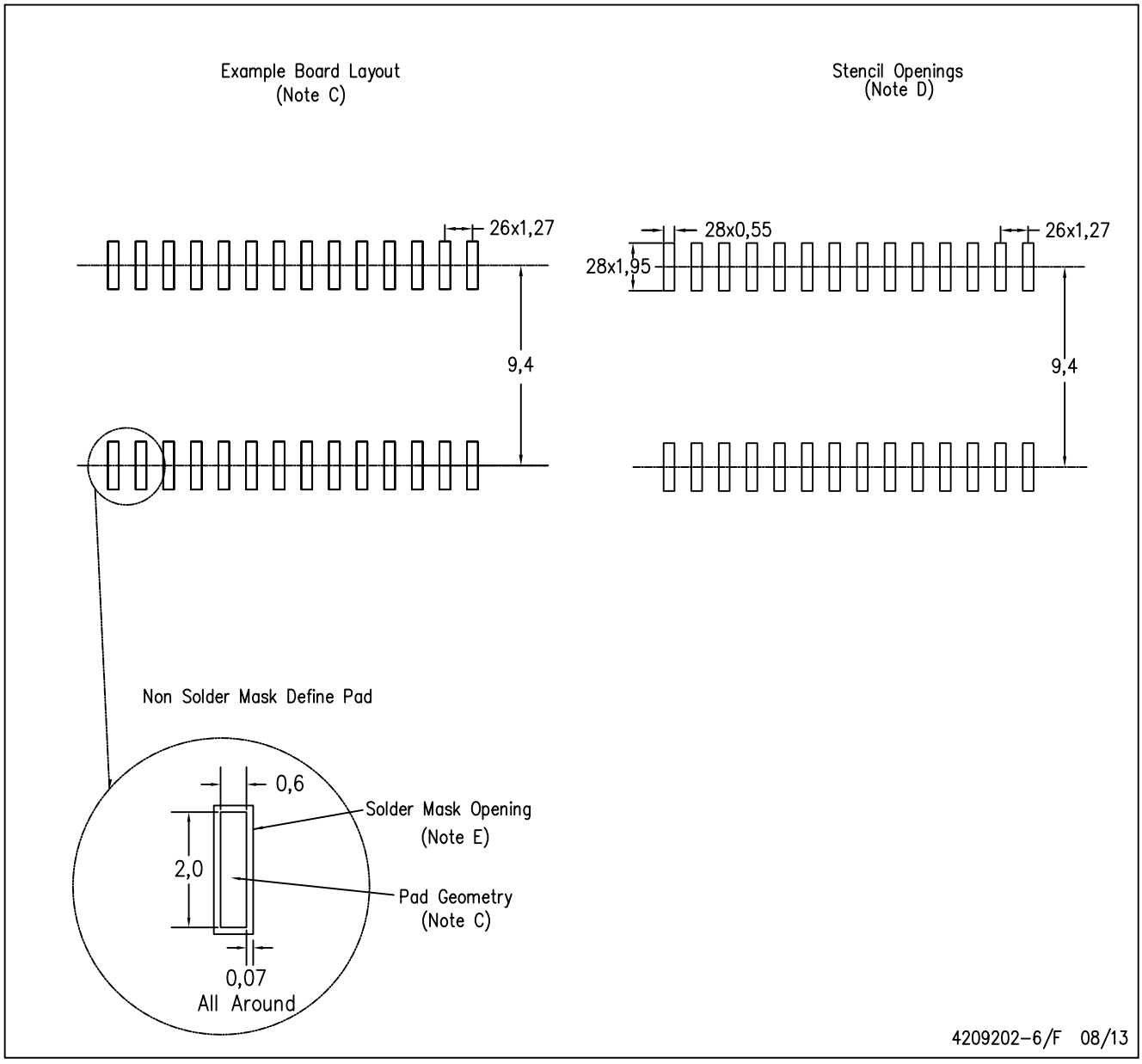
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| ADS7811U | DW | SOIC | 28 | 20 | 507 | 12.83 | 5080 | 6.6 |
| ADS7811U.A | DW | SOIC | 28 | 20 | 507 | 12.83 | 5080 | 6.6 |

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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