Microprocessor-Compatible Sampling CMOS ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **Drop-In Replacement for the ADS774**
- **Complete Sampling ADC with Reference, Clock, and Microprocessor Interface**
- **Fast Acquisition and Conversion: 8.5μs Max Over Temperature**
- **Eliminates External Sample/Hold in Most Applications**
- **Ensured AC and DC Performance**
- **Single +5V Supply Operation**
- **Low Power: 120mW Max**
- **Package Options: SO, 0.6in and 0.3in DIPs(1)**

APPLICATIONS

- **Medical Instrumentation**
- **Data Acquisition Systems**
- **Robotics**
- **Industrial Control**
- **Test Equipment**
- **Digital Signal Processing**
- **DSP Servo Control**

DESCRIPTION

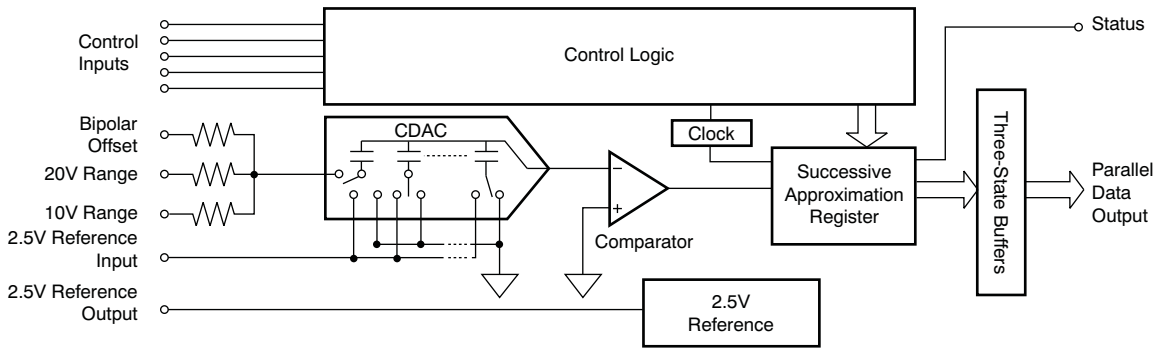
The ADS774H is a 12-bit, successive-approximation analog-to-digital converter (ADC) that uses an innovative capacitor array (CDAC) implemented in low-power CMOS technology. This device is a drop-in replacement for the ADS774, with internal sampling, much lower power consumption, and the ability to operate from a single +5V supply.

The ADS774H is complete with an internal clock, microprocessor interface, three-state outputs, and internal scaling resistors for input ranges of 0V to +10V, 0V to +20V, ±5V, or ±10V. The maximum throughput time is 8.5μs over the full operating temperature range, including both acquisition and conversion.

Complete user control over the internal sampling function facilitates elimination of external sample/hold amplifiers in most existing designs.

The ADS774H requires +5V, with –15V optional. No +15V supply is required. Packages include a 28-pin SO, and 0.3in-wide or 0.6in-wide 28-pin DIPs(1).

(1) DIP-28 package is product preview.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	SINAD(2)	LINEARITY ERROR	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS774HIB (High-Grade)	70dB	±1/2 LSB	DIP-28(3)	NT	–40°C to +85°C	ADS774HIBNT	Rail, 13
				NTD	–40°C to +85°C	ADS774HIBNTD	Rail, 13
	70dB	±1/2 LSB	SO-28	DW	–40°C to +85°C	ADS774HIBDW	Tape and Reel, 28
						ADS774HIBEDWR	Tape and Reel, 1000
ADS774HI (Standard-Grade)	68dB	±1LSB	DIP-28(3)	NT	–40°C to +85°C	ADS774HINTD	Rail, 13
				NTD	–40°C to +85°C	ADS774HINT	Rail, 13
	68dB	±1LSB	SO-28	DW	–40°C to +85°C	ADS774HIDW	Tape and Reel, 28
						ADS774HIDWR	Tape and Reel, 1000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) SINAD is Signal-to-(Noise + Distortion) expressed in dB.
(3) DIP-28 package is product preview.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		ADS774H	UNIT
V_{EE} to Digital Common		$+V_{DD}$ to –16.5	V
V_{DD} to Digital Common		0 to +7	V
Analog Common to Digital Common		±1	V
Control inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common		–0.5 to V_{DD} +0.5	V
Analog inputs (REF IN, Bipolar Offset, 10V Range) to Analog Common		±16.5	V
20V Range to Analog Common		±24	V
Ref Out		Indefinite short to common, momentary short to V_{DD}	
Maximum junction temperature		+165	°C
Power dissipation		1000	mW
Lead temperature (soldering, 10s)		+300	°C
Thermal impedance, θ_{JA}	DIP-28	100	°C/W
	SO-28		

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

All specifications at $T_A = T_{MIN}$ to T_{MAX}, V_{DD} = +5V, V_{EE} = –15V to +5V, sampling frequency of 117kHz, and f_{IN} = 10kHz, unless otherwise noted.

PARAMETER	CONDITIONS	ADS774HI			ADS774HIB[1]			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
SYSTEM PERFORMANCE								
Resolution				12			12	Bits
ANALOG INPUTS								
Voltage range	Unipolar		0 to +10, 0 to +20			0 to +10, 0 to +20		V
	Bipolar		±5, ±10			±5, ±10		V
Impedance	0V to +10V, ±5V	8.5	12		8.5	12		kΩ
	±10V, 0V to +20V	35	50		35	50		kΩ
DIGITAL INPUTS (CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$)								
Voltages	Logic 1	+2.0		+5.5	+2.0		+5.5	V
	Logic 0	–0.5		+0.8	–0.5		+0.8	V
Current		–5	0.1	+5	–5	0.1	+5	µA
Capacitance			5			5		pF
DC ACCURACY								
Linearity error	At +25°C			±1			±1/2	LSB
	T_{MIN} to T_{MAX}[2]			±1			±1/2	LSB
Unipolar offset error	At +25°C (adjustable to zero)			±2			±2	LSB
Unipolar offset	T_{MIN} to T_{MAX}[2]			±4			±3	LSB
Bipolar offset error	At +25°C (adjustable to zero)			±10			±4	LSB
Bipolar offset	T_{MIN} to T_{MAX}[2]			±12			±5	LSB
Full-scale calibration error[3]	At +25°C (adjustable to zero)			±0.25			±0.25	% of FS[4]
	T_{MIN} to T_{MAX}[2]			±0.47			±0.37	% of FS
No missing codes resolution	At +25°C	12			12			Bits
	T_{MIN} to T_{MAX}[2]	12			12			Bits
AC ACCURACY[5]								
Spurious free dynamic range		73	78		76	78		dB
Total harmonic distortion			–77	–72		–77	–75	dB
Signal-to-noise ratio		69	72		71	72		dB
Signal-to-(noise + distortion) ratio		68	71		70	71		dB
Intermodulation distortion	f_{IN1} = 20kHz, f_{IN2} = 23kHz		–75			–75		dB
TEMPERATURE COEFFICIENTS[6]								
Unipolar offset			±1			±1		ppm/°C
Bipolar offset			±2			±2		ppm/°C
Full-scale calibration			±12			±12		ppm/°C
POWER-SUPPLY SENSITIVITY								
Change in full-scale calibration[7]	+4.75V < V_{DD} < +5.25V			±1/2			±1/2	LSB
CONVERSION TIME (Including Acquisition Time)								
t_{AQ} + t_C at +25°C	8-bit cycle		5.5	5.9		5.5	5.9	µs
	12-bit cycle		7.5	8		7.5	8	µs
12-bit cycle, T_{MIN} to T_{MAX}			8	8.5		8	8.5	µs

(1) **Shaded cells** indicate different specifications from standard grade version of device.
(2) Maximum error at T_{MIN} and T_{MAX}.
(3) With fixed 50Ω resistor from REF OUT to REF IN. This parameter is also adjustable to zero at +25°C.
(4) FS in this parametric table means *Full-Scale Range*. That is, for a ±10V input range, FS = 20V; for a 0V to +10V range, FS = 10V.
(5) Based on V_{EE} = +5V, which is the Control Mode; see the *S/H Control Mode and ADC774 Emulation Mode* section.
(6) Using internal reference.
(7) This parameter is the worst-case change in accuracy from accuracy with a +5V supply.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A = T_{MIN}$ to T_{MAX}, V_{DD} = +5V, V_{EE} = –15V to +5V, sampling frequency of 117kHz, and f_{IN} = 10kHz, unless otherwise noted.

PARAMETER		CONDITIONS	ADS774HI			ADS774HIB(1)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SAMPLING DYNAMICS									
Sampling rate		At +25°C	125			125			kHz
		T_{MIN} to T_{MAX}	117			117			kHz
Aperture delay, t_{AP}		with V_{EE} = +5V		20			20		ns
		with V_{EE} = 0V to –15V		1.6			1.6		µs
Aperture uncertainty (jitter)		with V_{EE} = +5V		300			300		ps RMS
		with V_{EE} = 0V to –15V		10			10		ns RMS
Settling time to 0.01% for full-scale input change				1.4			1.4		µs
DIGITAL OUTPUTS (DB_{11} to DB_0, STATUS)									
Output codes		Unipolar	Unipolar straight binary (USB)			Unipolar straight binary (USB)			
		Bipolar	Bipolar offset binary (BOB)			Bipolar offset binary (BOB)			
Logic levels		Logic 0 (I_{SINK} = 1.6mA)			+0.4			+0.4	V
		Logic 1 (I_{SOURCE} = 500µA)	+2.4			+2.4			V
Leakage, data bits only, high-Z state			–5	0.1	+5	–5	0.1	+5	µA
Capacitance				5			5		pF
INTERNAL REFERENCE VOLTAGE									
Voltage			+2.4	+2.5	+2.6	+2.4	+2.5	+2.6	V
Source current available for external loads			0.5			0.5			mA
POWER-SUPPLY REQUIREMENTS									
Voltage	V_{EE}(8)		–16.5		V_{DD}	–16.5		V_{DD}	V
	V_{DD}		+4.5		+5.5	+4.5		+5.5	V
Current	I_{EE}(8)	V_{EE} = –15V		–1			–1		mA
	I_{DD}			+15	+24		+15	+24	mA
Power dissipation, t_{MIN} to t_{MAX}		V_{EE} = 0V to +5V		75	120		75	120	mW
TEMPERATURE RANGE									
Specified			–40		+85	–40		+85	°C
Operating			–40		+85	–40		+85	°C
Storage			–65		+150	–65		+150	°C

(8) V_{EE} is optional, and is only used to set the mode for the internal sample/hold. When V_{EE} = –15V, I_{EE} = –1mA typ; when V_{EE} = 0V, I_{EE} = ±5mA typ; when V_{EE} = +5V, I_{EE} = +167mA typ.

TIMING DIAGRAMS

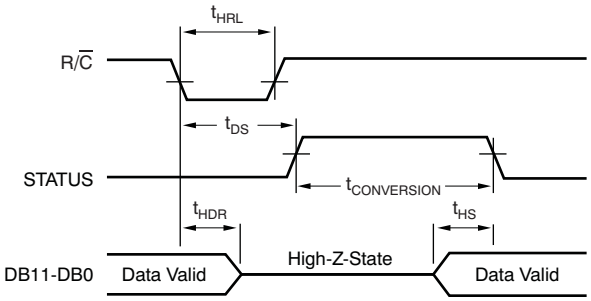


Figure 1. R/$\overline{C}$ Pulse Low: Outputs Enabled After Conversion

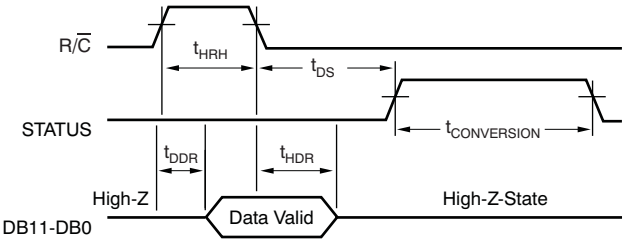
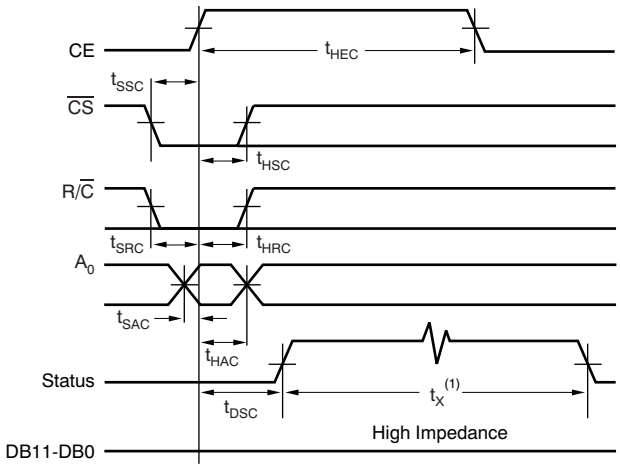


Figure 2. R/$\overline{C}$ Pulse High: Outputs Enabled Only when R/$\overline{C}$ is High



NOTE (1): t_X includes t_{AQ} and t_C in ADC774 Emulation Mode, t_C only in S/H Control Mode.

Figure 3. Conversion Cycle Timing

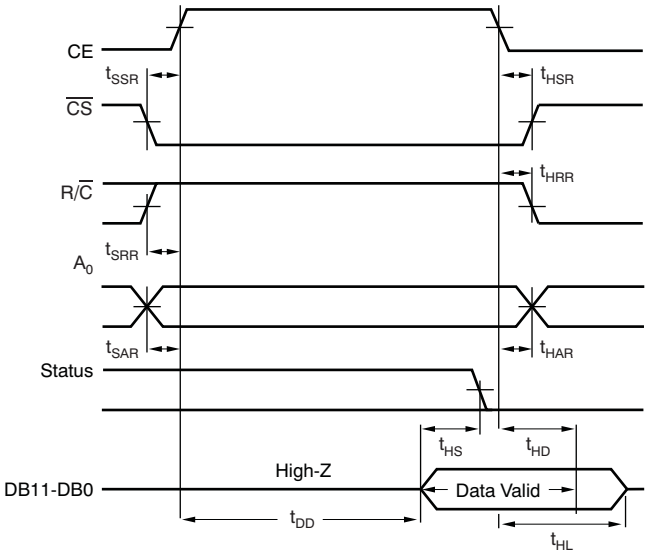


Figure 4. Read Cycle Timing

TIMING REQUIREMENTS: Stand-Alone Mode

SYMBOL	PARAMETER	ADS774H			UNIT
		MIN	TYP	MAX	
t_{HRL}	Low R/$\overline{C}$ pulse width	25			ns
t_{DS}	STS delay from R/$\overline{C}$			200	ns
t_{HDR}	Data valid After R/$\overline{C}$ low	25			ns
t_{HRH}	High R/$\overline{C}$ pulse width	100			ns
t_{DDR}	Data access time			150	ns

TIMING REQUIREMENTS: Fully-Controlled Operation (Convert Mode)

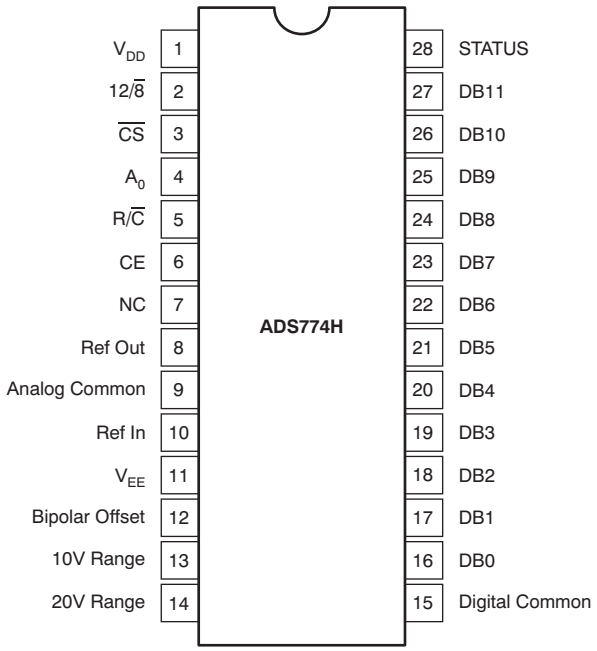
SYMBOL	PARAMETER	ADS774H			UNIT
		MIN	TYP	MAX	
t_{DSC}	STS delay from CE		60	200	ns
t_{HEC}	CE pulse width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE setup	50	20		ns
t_{HSC}	$\overline{CS}$ low during CE high	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE setup	50	0		ns
t_{HRC}	R/$\overline{C}$ low during CE high	50	20		ns
t_{SAC}	A_0 to CE setup	0			ns
t_{HAC}	A_0 valid during CE high	50	20		ns

TIMING REQUIREMENTS: Fully-Controlled Operation (Read Mode)

SYMBOL	PARAMETER	ADS774H			UNIT
		MIN	TYP	MAX	
t_{DD}	Access time from CE		75	150	ns
t_{HD}	Data valid after CE low	25	35		ns
t_{HL}	Output float delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE setup	50	0		ns
t_{SRR}	R/$\overline{C}$ to CE setup	0			ns
t_{SAR}	A_0 to CE setup	50	25		ns
t_{HSR}	$\overline{CS}$ valid after CE low	0			ns
t_{HRR}	R/$\overline{C}$ high after CE low	0			ns
t_{HAR}	A_0 valid after CE low	50			ns
t_{HS}	STATUS delay after data valid	75	150	375	ns

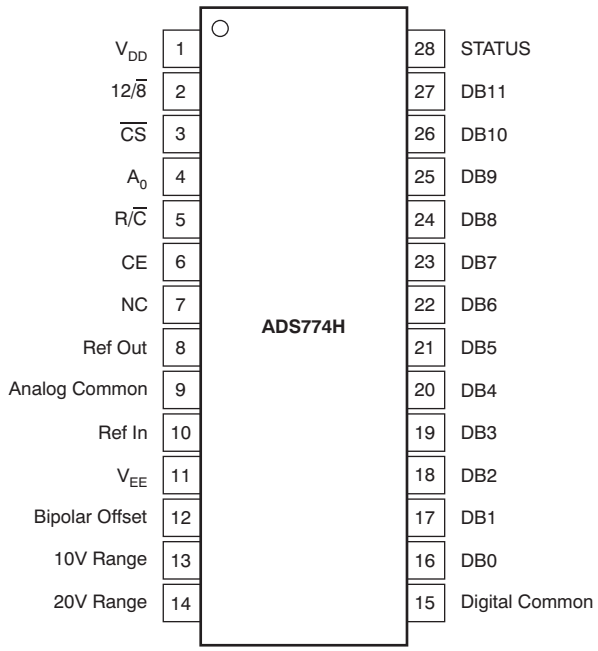
PIN CONFIGURATION

NT, NTD PACKAGES[1]
DIP-28
(TOP VIEW)



(1) NT and NTD (DIP-28) packages are product preview.

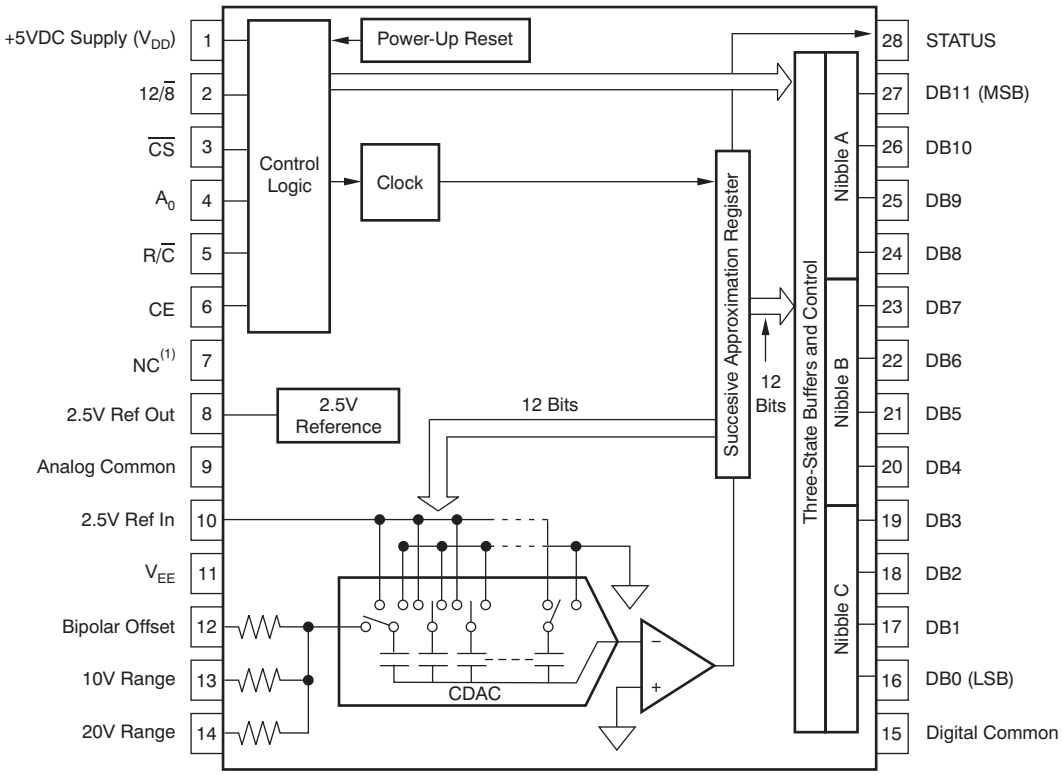
DW PACKAGE
SO-28
(TOP VIEW)



PIN DESCRIPTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
V_{DD}	1	Power	5V digital logic supply
12/$\overline{8}$	2	Input	Data mode select '1' = read '0' = convert
$\overline{CS}$	3	Input	Chip select (active low)
A_0	4	Input	Byte address, short cycle
R/$\overline{C}$	5	Input	Read/Convert '1' = 12-bit '0' = 8-bit
CE	6	Input	Chip enable (active high)
NC	7		Do not connect
Ref Out	8	Output	2.5V reference output
Analog Common	9	Power	Analog ground
Ref In	10	Input	2.5V reference input
V_{EE}	11	Power	–15V to +5V analog supply
Bipolar Offset	12	Input	Connect this pin to REF OUT through a 50Ω resistor for bipolar operation, or connect to Analog Common for unipolar operation.
10V Range	13	Input	0V to 10V or ±5V input span. Do not connect if using a 20V range.
20V Range	14	Input	0V to 20V or ±10V input span. Do not connect if using a 10V range.
Digital Common	15	Power	Digital ground
DB0	16	Output	These pins provide the lower four bits of data when A_0 is high. When A_0 is low, these pins/bits are disabled.
DB1	17	Output	
DB2	18	Output	
DB3	19	Output	
DB4	20	Output	In 12-bit format, these pins output the middle four bits of data. In 8-bit format, they output the middle four bits when A_0 is low, and all 0's when A_0 is high.
DB5	21	Output	
DB6	22	Output	
DB7	23	Output	
DB8	24	Output	In 12-bit format, these pins output the upper four bits of data. In 8-bit format, they output the upper four bits when A_0 is low, and they are disabled when A0 is high.
DB9	25	Output	
DB10	26	Output	
DB11	27	Output	
STATUS	28	Output	Active high when conversion is in progress; active low when complete.

FUNCTIONAL BLOCK DIAGRAM



NOTE (1): Not internally connected.

Input Voltages, Transition Values, and LSB Values

BINARY (BIN) OUTPUT		INPUT VOLTAGE RANGE and MSB VALUES			
Analog Input Voltage Range	**Defined As:**	**±10V**	**±5V**	**0V to +10V**	**0V to +20V**
One least significant bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{10V}{2^n}$	$\frac{20V}{2^n}$
	n = 8	78.13mV	39.06mV	39.06mV	78.13mV
	n = 12	4.88mV	2.44mV	2.44mV	4.88mV
Output transition values					
FFEh to FFFh	+Full-scale calibration	+10V – 3/2LSB	+5V – 3/2LSB	+10V – 3/2LSB	+20V – 3/2LSB
7FFFh to 800h	Midscale calibration (Bipolar offset)	0V – 1/2LSB	0V – 1/2LSB	+5V – 1/2LSB	+10V – 1/2LSB
000h to 001h	Zero calibration (–Full-scale calibration)	–10V – +1/2LSB	–5V + 1/2LSB	0V + 1/2LSB	0V + 1/2LSB

TYPICAL CHARACTERISTICS

At T_A = +25°C; V_{DD} = V_{EE} = +5V, bipolar ±10V input range, and sampling frequency of 110kHz, unless otherwise specified. All plots use 4096 point FFTs.

FREQUENCY SPECTRUM (±10V, 2kHz INPUT)

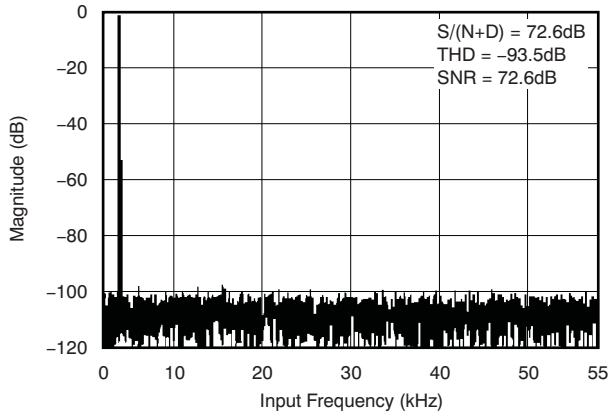


Figure 5.

SIGNAL/(NOISE + DISTORTION) vs INPUT FREQUENCY AND AMBIENT TEMPERATURE

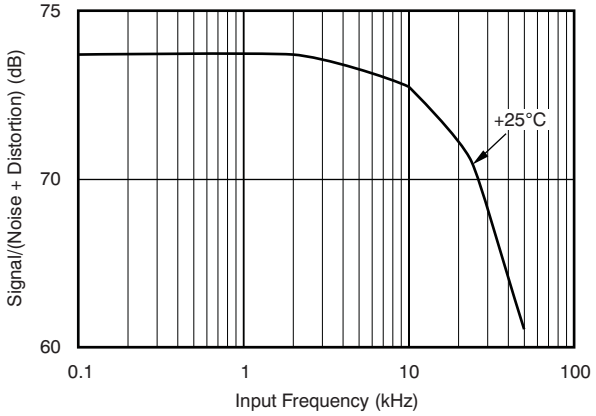


Figure 6.

FREQUENCY SPECTRUM (±10V, 20kHz INPUT)

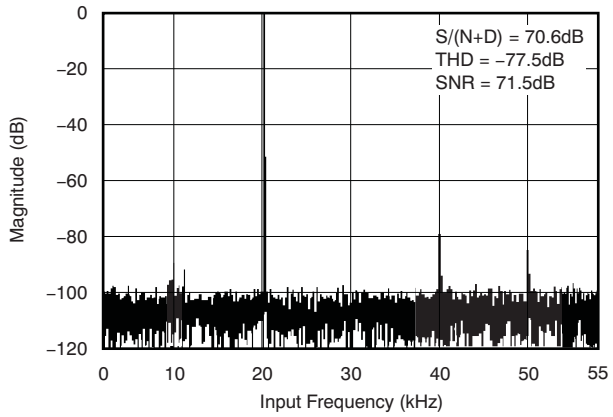


Figure 7.

FREQUENCY SPECTRUM (±1V, 20kHz INPUT)

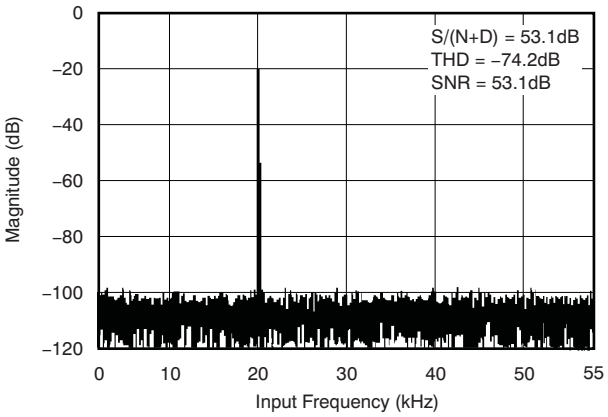


Figure 8.

SPURIOUS FREE DYNAMIC RANGE, SNR, AND THD vs INPUT FREQUENCY

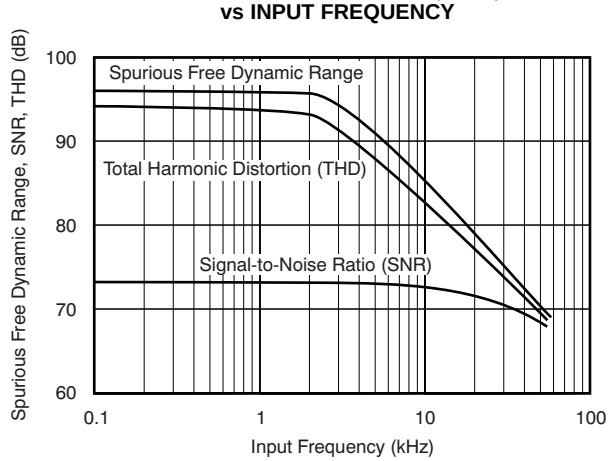


Figure 9.

POWER-SUPPLY REJECTION vs SUPPLY RIPPLE FREQUENCY

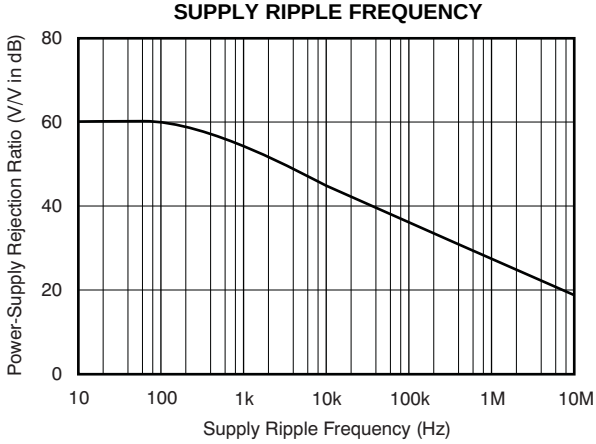


Figure 10.

THEORY OF OPERATION

OVERVIEW

In the ADS774H, the advantages of advanced CMOS technology (such as high logic density, stable capacitors, and precision analog switches) produce a fast, low-power ADC with internal sample/hold.

The charge-redistribution successive-approximation circuitry converts analog input voltages into digital words.

A simple example of a charge-redistribution ADC with only three bits is shown in Figure 11.

SAMPLING

While sampling, the capacitor array switch for the MSB capacitor (S_1) is in position *S*, so that the charge on the MSB capacitor is proportional to the voltage level of the analog input signal. The remaining array switches (S_2 and S_3) are set to position *G*. Switch S_C is closed, setting the comparator input offset to zero.

CONVERSION

When a conversion command is received, switch S_1 opens to capture a charge on the MSB capacitor proportional to the analog input level at the time of the sampling command, and switch S_C opens to float the comparator input. The charge held in the capacitor array can now be moved between the three capacitors in the array by connecting switches S_1, S2, and S_3 to either the *R* position (to connect to the reference) or the *G* position (to connect to GND), thus changing the voltage generated at the comparator input.

During the first approximation, the MSB capacitor is connected through switch S_1 to the reference, while switches S_2 and S_3 are connected to GND. Depending on whether the comparator output is high or low, the logic then latches S_1 in position *R* or *G*. Similarly, the second approximation is made by connecting S_2 to the reference and S_3 to GND, and latching S_2 according to the output of the comparator. After three successive approximation steps have been made, the voltage level at the comparator is within 1/2LSB of GND, and a digital word that represents the analog input can be determined from the positions of S_1, S_2 and S_3.

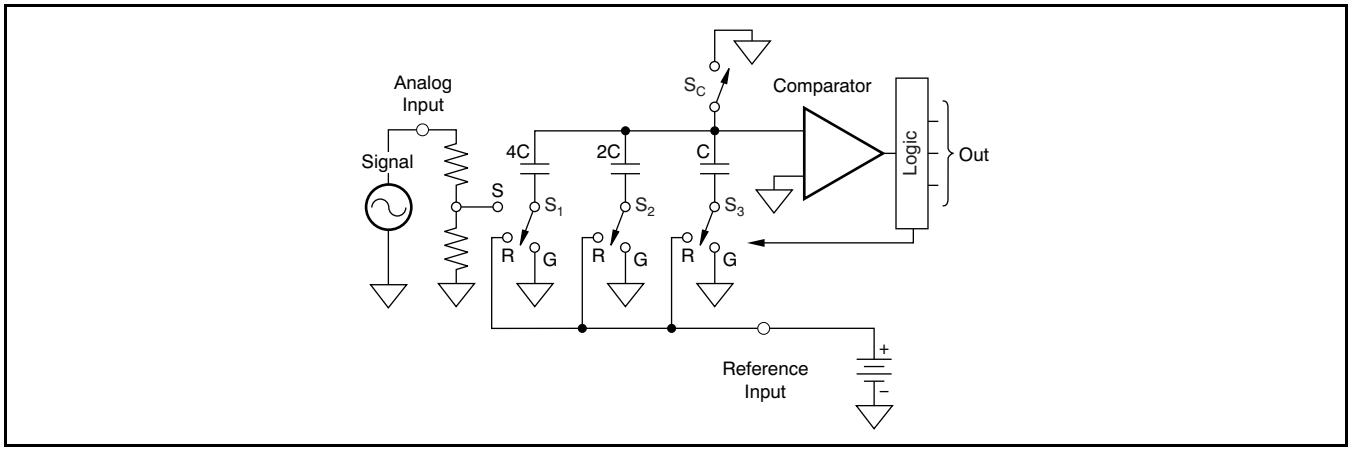


Figure 11. 3-Bit Charge Redistribution ADC

DEVICE OPERATION

BASIC OPERATION

Figure 12 shows the minimum connections required to operate the ADS774H in a basic ±10V range in the Control Mode (discussed in detail in the section, *Sample/Hold (S/H) Control Mode and ADC774 Emulation Mode*). The falling edge of a Convert Command (a pulse that takes pin 5 low for a minimum of 25ns) initiates two actions: first, it switches the ADS774H input to the hold state; second, it begins the conversion process. Pin 28 (STATUS) outputs *high* during the conversion, and falls only after the conversion is completed and the data have been latched on the data output pins (pins 16 to 27). Thus, the falling edge of STATUS on pin 28 can be used to read the data from the conversion. Also, during conversion, the STATUS signal puts the data output pins into a high-Z state and inhibits the input lines. This condition means that pulses on pin 5 are ignored, so that new conversions cannot be initiated during the conversion, either as a result of spurious signals or to short-cycle the ADS774H.

The ADS774H begins acquiring a new sample as soon as the conversion completes, even before the STATUS output falls, and tracks the input signal until the next conversion is started. The ADS774H is designed to complete a conversion and accurately acquire a new signal in 8.5µs (max) over the full operating temperature range, so that conversions can take place at a full 117kHz.

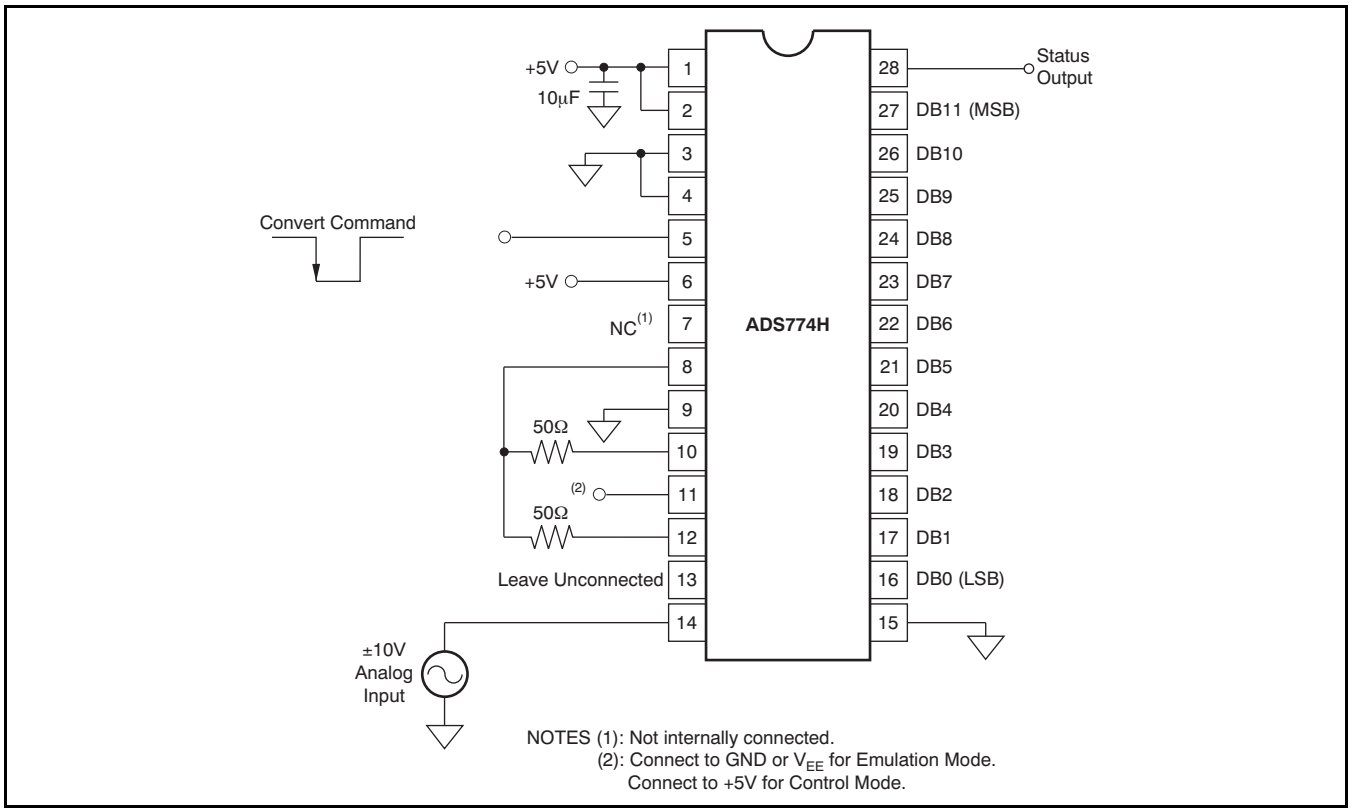


Figure 12. Basic ±10V Operation

CONTROLLING THE ADS774H

The ADS774H can easily interface with most microprocessors and other digital systems. The microprocessor may take full control of each conversion, or the converter may operate in a stand-alone mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready: choosing either 12 bits all at once, or the eight MSBs followed by the four LSBs in a left-justified format. The five control inputs (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$, and CE) are all TTL-/CMOS-compatible. The functions of the control inputs are described in Table 1. The control function truth table is shown in Table 2.

Table 1. Control Line Functions

DESIGNATION	DEFINITION	FUNCTION
CE (pin 6)	Chip Enable (active high)	Must be high ('1') to either initiate a conversion or read output data. 0-to-1 edge may be used to initiate a conversion.
$\overline{CS}$ (pin 3)	Chip Select (active low)	Must be low ('0') to either initiate a conversion or read output data. 1-to-0 edge may be used to initiate a conversion.
R/$\overline{C}$ (pin 5)	Read/Convert '1' = Read '0' = Convert	Must be low ('0') to initiate either 8- or 12-bit conversions. 1-to-0 edge may be used to initiate a conversion. Must be high ('1') to read output data. 0-to-1 edge may be used to initiate a read operation.
A_0 (pin 4)	Byte Address, short cycle	In the start-convert mode, A_0 selects either 8-bit (A_0 = '1') or 12-bit (A_0 = '0') conversion mode. When reading output data in two 8-bit bytes, A_0 = '0' accesses eight MSBs (high byte) and A_0 = '1' accesses four LSBs and trailing 0s (low byte).
12/$\overline{8}$ (pin 2)	Data Mode select '1' = 12-bit '0' = 8-bit	When reading output data, 12/$\overline{8}$ = '1' enables all 12 output bits simultaneously. 12/$\overline{8}$ = '0' enables the MSBs or LSBs as determined by the A_0 line.

Table 2. Control Input Truth Table

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable eight MSBs only
1	0	1	0	1	Enable four LSBs plus four trailing zeroes

STAND-ALONE OPERATION

For stand-alone operation, control of the converter is accomplished by a single control line connected to R/$\overline{C}$. In this mode, $\overline{CS}$ and A_0 are connected to digital common, and CE and 12/$\overline{8}$ are connected to +5V. The output data are presented as 12-bit words. Stand-alone mode is used in systems that contain dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a high-to-low transition of R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is high and STATUS is low. Thus, there are two possible modes of operation: data can be read with either a positive pulse on R/$\overline{C}$, or a negative pulse on STATUS. In either case, the R/$\overline{C}$ pulse must remain low for a minimum of 25ns.

Figure 1 illustrates timing with an R/$\overline{C}$ pulse that goes low and returns high during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enabled for external access of the data after the conversion completes.

Figure 2 illustrates the timing when a positive R/$\overline{C}$ pulse is used. In this mode, the output data from the previous conversion are enabled during the time R/$\overline{C}$ is high. A new conversion starts on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high-impedance state until the next occurrence of a high R/$\overline{C}$ pulse. Timing specifications for stand-alone operation are listed in the TIming Requirements table for Stand-Alone Mode.

FULLY-CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the A_0 input, which is latched upon receipt of a conversion start transition (described in the next section). If A_0 is latched high, the conversion continues for eight bits. The full 12-bit conversion occurs if A_0 is low. If all 12 bits are read following an 8-bit conversion, the four LSBs (DB0–DB3) are low (logic 0). A_0 is latched because it is also involved in enabling the output buffers. No other control inputs are latched.

CONVERSION START

The converter initiates a conversion based on a transition that occurs on any of three logic inputs (CE, $\overline{CS}$, and R/$\overline{C}$) as shown in Table 2. Conversion is initiated by the last of the three inputs to reach the required state; therefore, all three inputs may be dynamically controlled. If necessary, all three inputs may change state simultaneously; in this case, the nominal delay time is the same regardless of which input actually starts the conversion. If it is desired that a particular input establish the actual start of conversion, the other two inputs should be stable for a minimum of 50ns before the transition of the critical input. Timing relationships for the start of conversion timing are illustrated in Figure 3. The timing specifications for timing are listed in the Timing Requirements tables for Fully-Controlled Operation Convert Mode and Read Mode.

The STATUS output indicates the current state of the converter because it is in a high state only during conversion. During this time the three-state output buffers remain in a high-impedance state, and therefore data cannot be read during conversion. Furthermore, during this period, additional transitions of the three digital inputs that control conversion are ignored, so that conversion cannot be prematurely terminated or restarted. However, if A_0 changes state after the beginning of the conversion, any additional start conversion transition will latch the new state of A_0, and possibly generate an incorrect conversion length (8 bits as opposed to 12 bits) for that conversion.

READING OUTPUT DATA

After conversion is initiated, the output data buffers remain in a high-impedance state until the following four logic conditions are simultaneously met: R/$\overline{C}$ high, STATUS low, CE high, and $\overline{CS}$ low. Upon satisfying these conditions, the data lines are enabled according to the state of inputs 12/$\overline{8}$ and A_0. See Figure 4 for the timing diagram, and the Timing Requirements tables for Fully-Controlled Operation Convert Mode and Read Mode for timing specifications.

In most applications, the 12/$\overline{8}$ input is hard-wired in either the high or low condition, although it is fully TTL- and CMOS-compatible and may be actively driven if desired. When 12/$\overline{8}$ is high, all 12 output lines (DB0 to DB11) are enabled simultaneously for full data word transfer to a 12-bit or 16-bit bus. In this situation, the A_0 state is ignored when reading the data.

When 12/$\overline{8}$ is low, the data is presented in the form of two 8-bit bytes, with selection of the byte of interest accomplished by the state of A_0 during the read cycle. When A_0 is low, the byte addressed contains the eight MSBs. When A_0 is high, the byte addressed contains the four LSBs from the conversion followed by four logic zeroes that have been forced by the control logic. The left-justified formats of the two 8-bit bytes are shown in Table 3. Connection of the ADS774H to an 8-bit bus for data transfer is illustrated in Figure 13. The design of the ADS774H ensures that the A_0 input may be toggled at any time with no damage to the converter; the outputs that are tied together in Figure 13 cannot be enabled at the same time. The A_0 input is usually driven by the least significant bit of the address bus to allow storage of the output data word in two consecutive memory locations.

Table 3. 12-Bit Data Format for 8-Bit Systems

Word 1

Processor	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Converter	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4

Word 2

Processor	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Converter	DB3	DB2	DB1	DB0	0	0	0	0

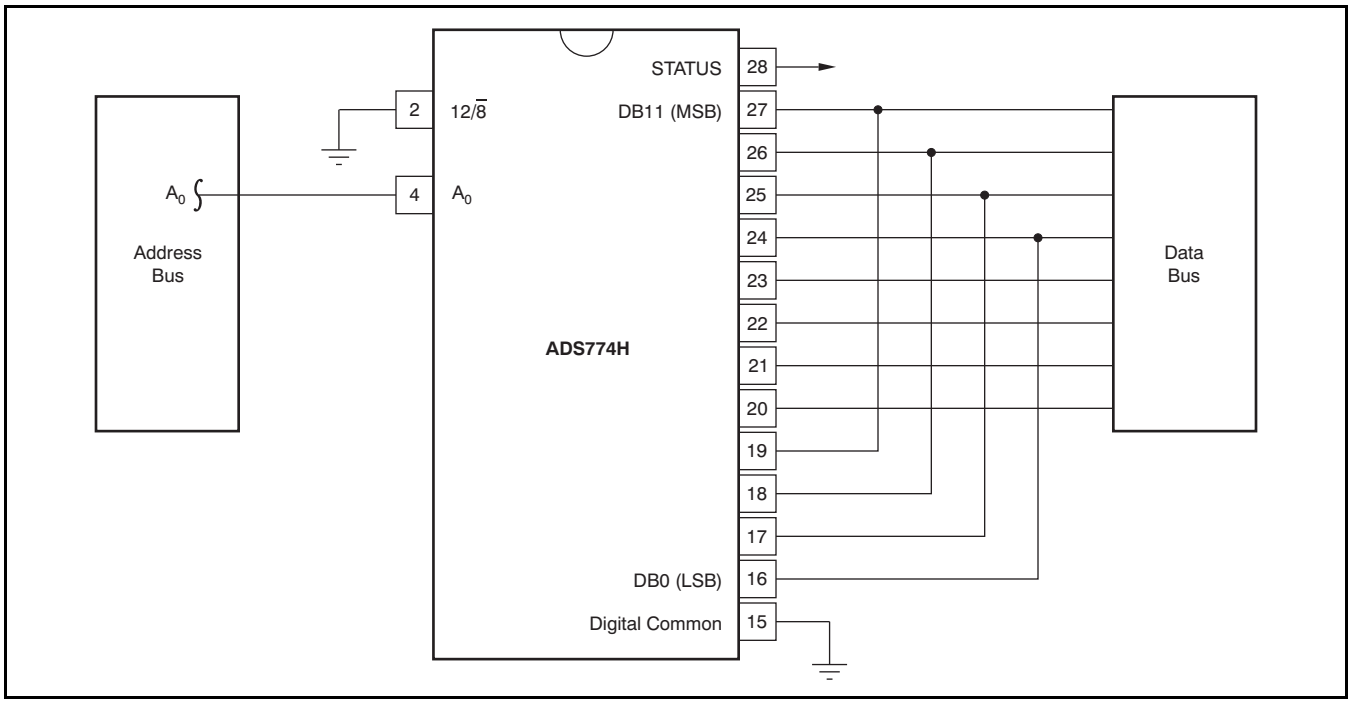


Figure 13. Connection to an 8-Bit Bus

SAMPLE/HOLD (S/H) CONTROL MODE AND ADC774 EMULATION MODE

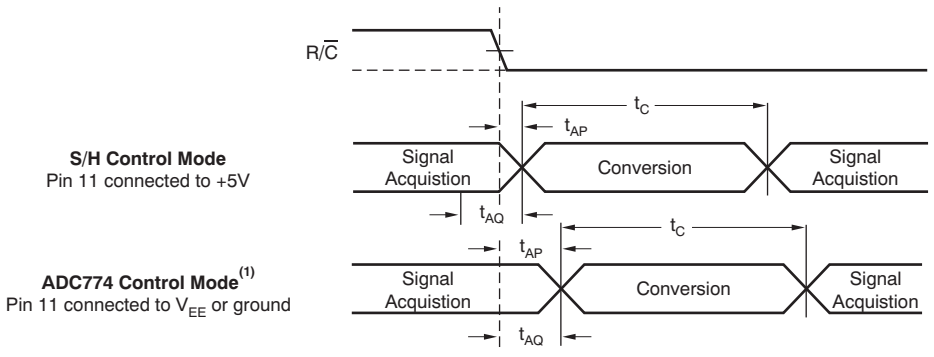
As with the ADS774, Emulation Mode allows the ADS774H to be dropped into most existing ADC774 sockets without changes to other system hardware or software. In existing sockets, the analog input is held stable during the conversion period so that accurate conversions can proceed, but the input can change rapidly at any time before the conversion starts. Emulation Mode uses the stability of the analog input during the conversion period to both acquire and convert in a maximum of 8µs (8.5µs over temperature.) In fact, system throughput can be increased, because the input to the ADS774H can start slewing before the end of a conversion (after the acquisition time), which is not possible with existing ADC774s.

The Control Mode is provided to allow full use of the internal sample/hold, eliminating the need for an external sample/hold in most applications. As compared with systems using separate sample/hold and ADC stages, the ADS774H in the Control Mode also eliminates the need for one of the control signals, usually the convert command. The command that puts the internal sample/hold in the hold state also initiates a conversion, reducing timing constraints in many systems.

The basic difference between these two modes is the assumptions about the state of the input signal both before and during the conversion. These differences are shown in Figure 14 and Table 4. In the Control Mode, it is assumed that during the required 1.4µs acquisition time, the signal is not changing faster than the ADS774H can track. No assumption is made about the input level after the convert command arrives, because the input signal is sampled and conversion begins immediately after the convert command. This architecture means that a convert command can also be used to switch an input multiplexer or change gains on a programmable gain amplifier, allowing the input signal to settle before the next acquisition at the end of the conversion. Because aperture jitter is minimized in the Control Mode, a high input frequency can be converted without an external sample/hold.

In the Emulation Mode, a delay time is introduced between the convert command and the start of conversion to allow the ADS774H enough time to acquire the input signal before converting. This delay time increases the effective aperture delay time from 0.02µs to 1.6µs, but allows the ADS774H to replace the ADC774 in most circuits without additional changes. In designs where the input to the ADS774H is changing rapidly in the 200ns before a convert command, system performance may be enhanced by delaying the convert command by 200ns.

When using the ADS774H in the Emulation Mode to replace existing converters in current designs, a sample/hold amplifier often precedes the converter. In these cases, no additional delay in the convert command is needed. The existing sample/hold does not slew excessively when going from the sample mode to the hold mode before a conversion. In both modes, as soon as the conversion completes, the internal sample/hold circuit immediately begins slewing to track the input signal.



NOTE (1): In the ADC774 Emulation Mode, a convert command triggers a delay that allows the ADS774H adequate time to acquire the input signal before converting.

Figure 14. Signal Acquisition and Conversion Timing

Table 4. Conversion Timing, T_{MIN} to T_{MAX}

SYMBOL	PARAMETER	S/H CONTROL MODE (Pin 11 Connected to +5V)			ADC774 EMULATION MODE (Pin 11 Connected to 0V to –15V)			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
	Throughput Time:							
$t_{AQ} + t_C$	12-bit conversions		8	8.5		8	8.5	µs
	8-bit conversions		6	6.3		6	6.3	µs
	Conversion Time:							
t_C	12-bit conversions		6.4			6.4		µs
	8-bit conversions		4.4			4.4		µs
t_{AQ}	Acquisition time		1.4			1.4		µs
t_{AP}	Aperture delay		20			1600		ns
t_J	Aperture uncertainty		0.3			10		ns

INSTALLATION

LAYOUT CONSIDERATIONS

Analog (pin 9) and digital (pin 15) commons are not connected together internally in the ADS774H, but should be connected together as close to the unit as possible, and to an analog common ground plane beneath the converter on the component side of the board. In addition, a wide conductor pattern should run directly from pin 9 to the analog supply common, and a separate wide conductor pattern from pin 15 to the digital supply common.

If the single-point system common cannot be established directly at the converter, pin 9 and pin 15 must be connected together at the converter. A single wide conductor pattern then connects these two pins to the system common. In either case, the common return of the analog input signal should be referenced to pin 9 of the ADC. This configuration prevents any voltage drops that may occur in the power-supply common returns from appearing in series with the input signal.

The speed of the ADS774H requires special caution regarding whichever input pin is not used. For 10V input ranges, pin 14 (20V range) must be unconnected; for 20V input ranges, pin 13 (10V range) must be unconnected. In both cases, the unconnected input should be shielded with a ground plane to reduce noise pickup.

In particular, the unused input pin should not be connected to any capacitive load, including high-impedance switches. Even a few picofarads on the unused pin can degrade acquisition time.

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, these traces should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common. If external full-scale and offset potentiometers are used, the potentiometers and associated resistors should be located as close as possible to the ADS774H.

POWER-SUPPLY DECOUPLING

On the ADS774H, +5V (to Pin 1) is the only power supply required for correct operation. Pin 7 is not connected internally, so there is no problem in existing ADC774 sockets where this is connected to +15V. Pin 11 (V_{EE}) is only used as a logic input to select modes of control over the sampling function as described above. When used in an existing ADC774 socket, the –15V on pin 11 selects the ADC774 Emulation Mode. Pin 11 is used as a logic input; therefore, it is immune to typical supply variations.

The +5V supply should be bypassed with a 10µF tantalum capacitor located close to the converter to promote noise-free operations, as shown in Figure 12. Noise on the power-supply lines can degrade the converter performance. Noise and spikes from a switching power supply are especially troublesome.

RANGE CONNECTIONS

The ADS774H offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V, or ±10V. Figure 15 and Figure 16 show the necessary connections for each of these ranges, along with the optional gain and offset trim circuits. If a 10V input range is required, the analog input signal should be connected to pin 13 of the converter. A signal that requires a 20V range is connected to pin 14. In either case, the other pin of the two is left unconnected. Pin 12 (Bipolar Offset) is connected either to Pin 9 (Analog Common) for unipolar operation, or to Pin 8 (2.5V Ref Out), or the external reference, for bipolar operation. Full-scale and offset adjustments are described in the *Optional External Full-Scale and Offset Adjustments* section.

The input impedance of the ADS774H is typically 50kΩ in the 20V ranges and 12kΩ in the 10V ranges.

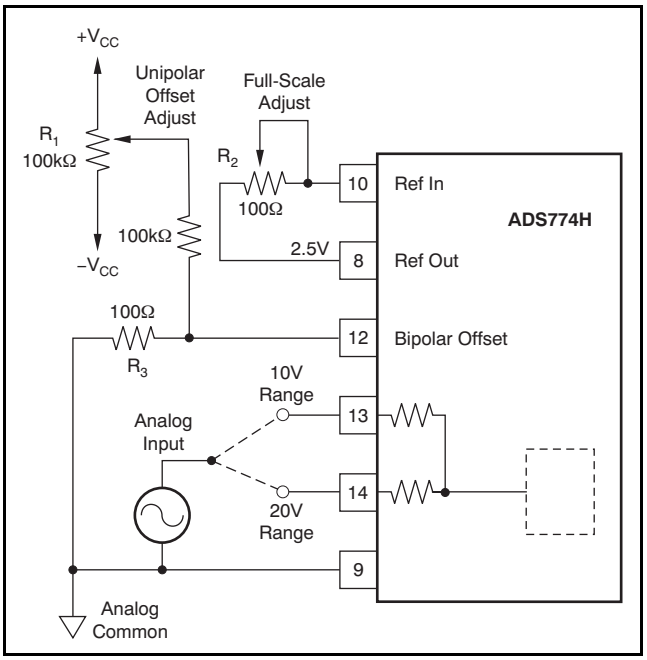


Figure 15. Unipolar Configuration

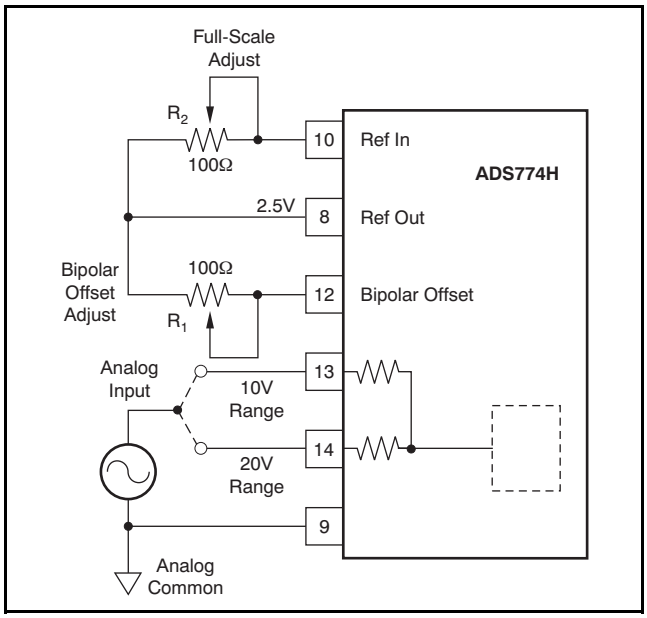


Figure 16. Bipolar Configuration

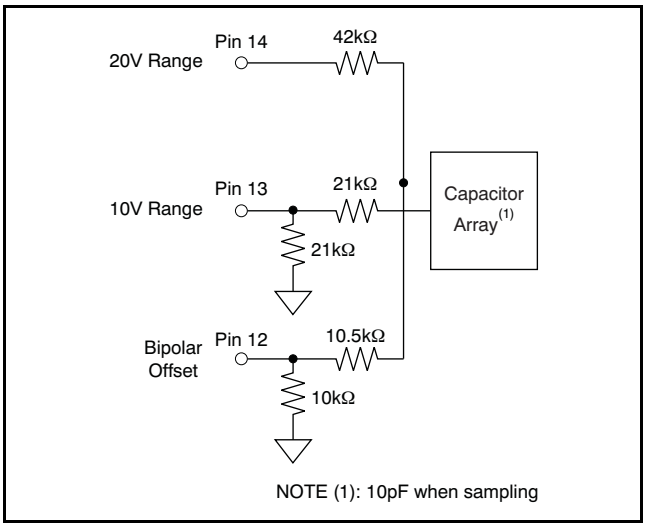


Figure 17. ADS774H Input Structure

INPUT STRUCTURE

Figure 17 shows the resistor divider input structure of the ADS774H. Because the input is driving a capacitor in the CDAC during acquisition, the input is looking into a high impedance node.

To understand how this circuit works, it is necessary to know that the input range on the internal sampling capacitor is from 0V to +3.33V, and that the analog input to the ADS774H must be converted to this range. The unipolar 20V range can be used as an example of how the divider network functions. In 20V operation, the analog input goes into pin 14. Pin 13 is left unconnected and pin 12 is connected to pin 9, analog common. From Figure 17, it is clear that the input to the capacitor array is the analog input voltage on pin 14 divided by the resistor network (42kΩ + 42kΩ || 10.5kΩ). A 20V input at pin 14 is divided to 3.33V at the capacitor array, while a 0V input at pin 14 gives 0V at the capacitor array.

SINGLE-SUPPLY OPERATION

The ADS774H is designed to operate from a single +5V supply and work with all of the unipolar and bipolar input ranges, in either Control Mode or Emulation Mode, as described in the *Sample/Hold (S/H) Control Mode and ADC744 Emulation Mode* section. Pin 7 is not connected internally. This input is where +12V or +15V is supplied on traditional ADC774s. Pin 11, the –12V or –15V supply input on traditional ADC774s, is used only as a logic input on the ADS774H. There is a resistor divider internally on pin 11 to reduce that input to a correct logic level within the ADS774H, and this resistor will add 10mW to 15mW to the power consumption of the ADS774H when –15V is supplied to pin 11. To minimize power consumption in a system, pin 11 can be simply grounded (for Emulation Mode) or tied to +5V (for Control Mode.)

There are no other modifications required for the ADS774H to function with a single +5V supply.

CALIBRATION

Optional External Full-Scale and Offset Adjustments

Offset and full-scale errors may be trimmed to zero using external offset and full-scale trim potentiometers connected to the ADS774H as shown in Figure 15 and Figure 16, respectively, for unipolar and bipolar operation.

Calibration Procedure: Unipolar Ranges

If external adjustments of full-scale and offset are not required, replace R_2 in Figure 15 with a 50Ω 1% metal film resistor and connect pin 12 to pin 9, omitting the other adjustment components.

If adjustment is required, connect the converter as shown in Figure 15. Sweep the input through the end-point transition voltage (0V + 1/2LSB; +1.22mV for the 10V range, +2.44mV for the 20V range) that causes the output code to be DB0 on (high). Adjust potentiometer R_1 until DB0 alternately toggles on and off with all other bits off. Then, adjust the full-scale by applying an input voltage of nominal full-scale minus 3/2LSB, the value that should cause all bits to be on. This value is +9.9963V for the 10V range and +19.9927V for the 20V range. Adjust potentiometer R_2 until bits DB1 to DB11 are on, and DB0 is toggling on and off.

Calibration Procedure: Bipolar Ranges

If external adjustments of full-scale and bipolar offset are not required, replace the potentiometers in Figure 16 by 50Ω, 1% metal film resistors.

If adjustments are required, connect the converter as shown in Figure 16. The calibration procedure is similar to that described above for unipolar operation, except that the offset adjustment is performed with an input voltage that is 1/2LSB above the minus full-scale value (–4.9988V for the ±5V range, –9.9976V for the ±10V range). Adjust R_1 for DB0 to toggle on and off with all other bits off. To adjust the full-scale range, apply a dc input signal that is 3/2LSB below the nominal plus full-scale value (+4.9963V for ±5V range, +9.9927V for ±10V range) and adjust R_2 for DB0 to toggle on and off with all other bits off.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS774HIBDW	NRND	Production	SOIC (DW) | 28	20 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-	ADS774HI
ADS774HIBDW.A	NRND	Production	SOIC (DW) | 28	20 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	See ADS774HIBDW	ADS774HI
ADS774HIBDWR	NRND	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-	ADS774HI
ADS774HIBDWR.A	NRND	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	See ADS774HIBDWR	ADS774HI
ADS774HIDW	NRND	Production	SOIC (DW) | 28	20 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-	ADS774HI
ADS774HIDW.A	NRND	Production	SOIC (DW) | 28	20 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	See ADS774HIDW	ADS774HI
ADS774HIDWR	NRND	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-	ADS774HI
ADS774HIDWR.A	NRND	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	See ADS774HIDWR	ADS774HI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

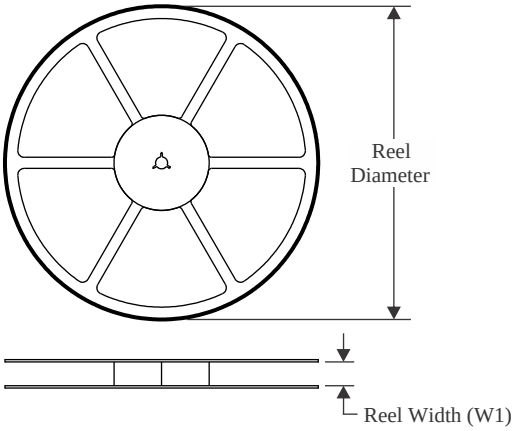
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

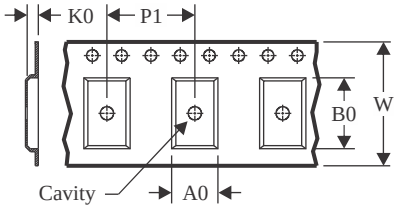
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

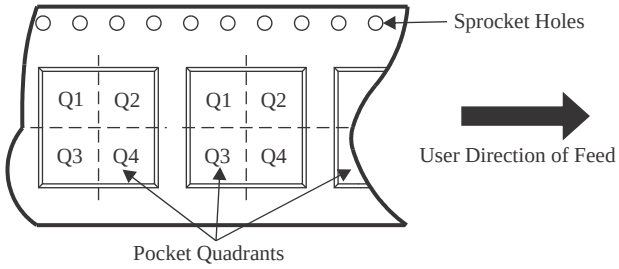


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

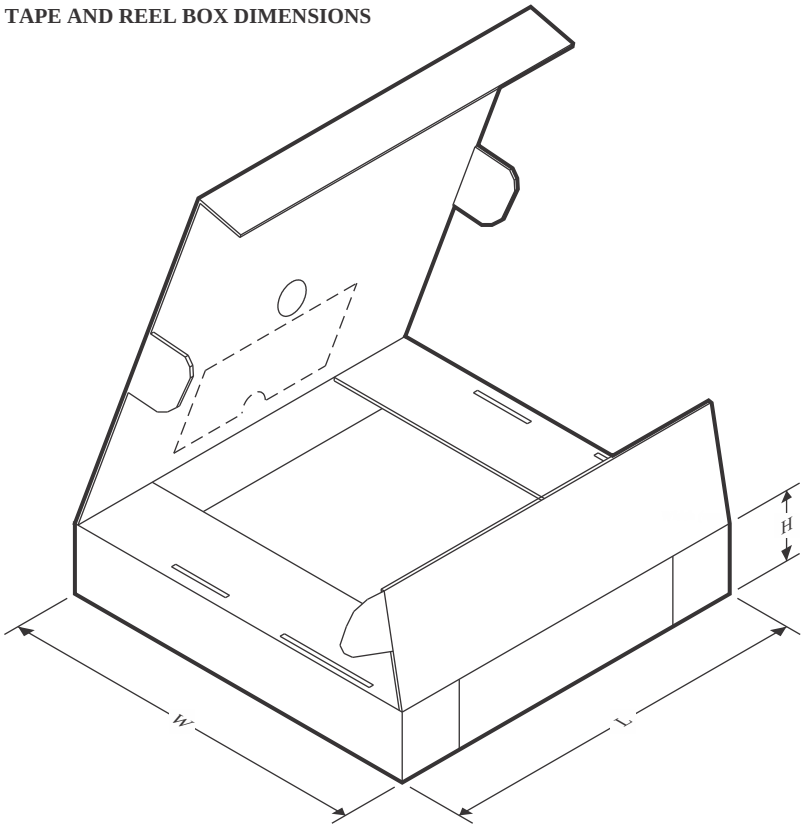
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS774HIBDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
ADS774HIDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

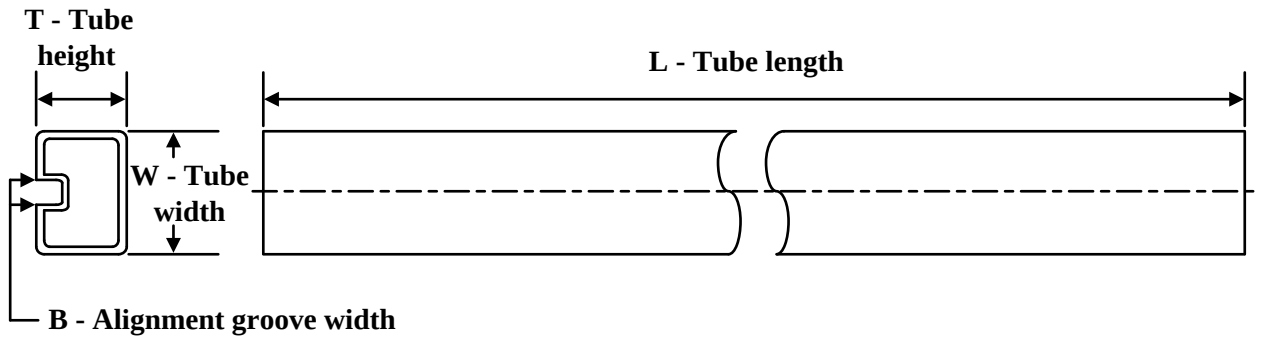
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS774HIBDWR	SOIC	DW	28	1000	356.0	356.0	53.0
ADS774HIDWR	SOIC	DW	28	1000	356.0	356.0	53.0

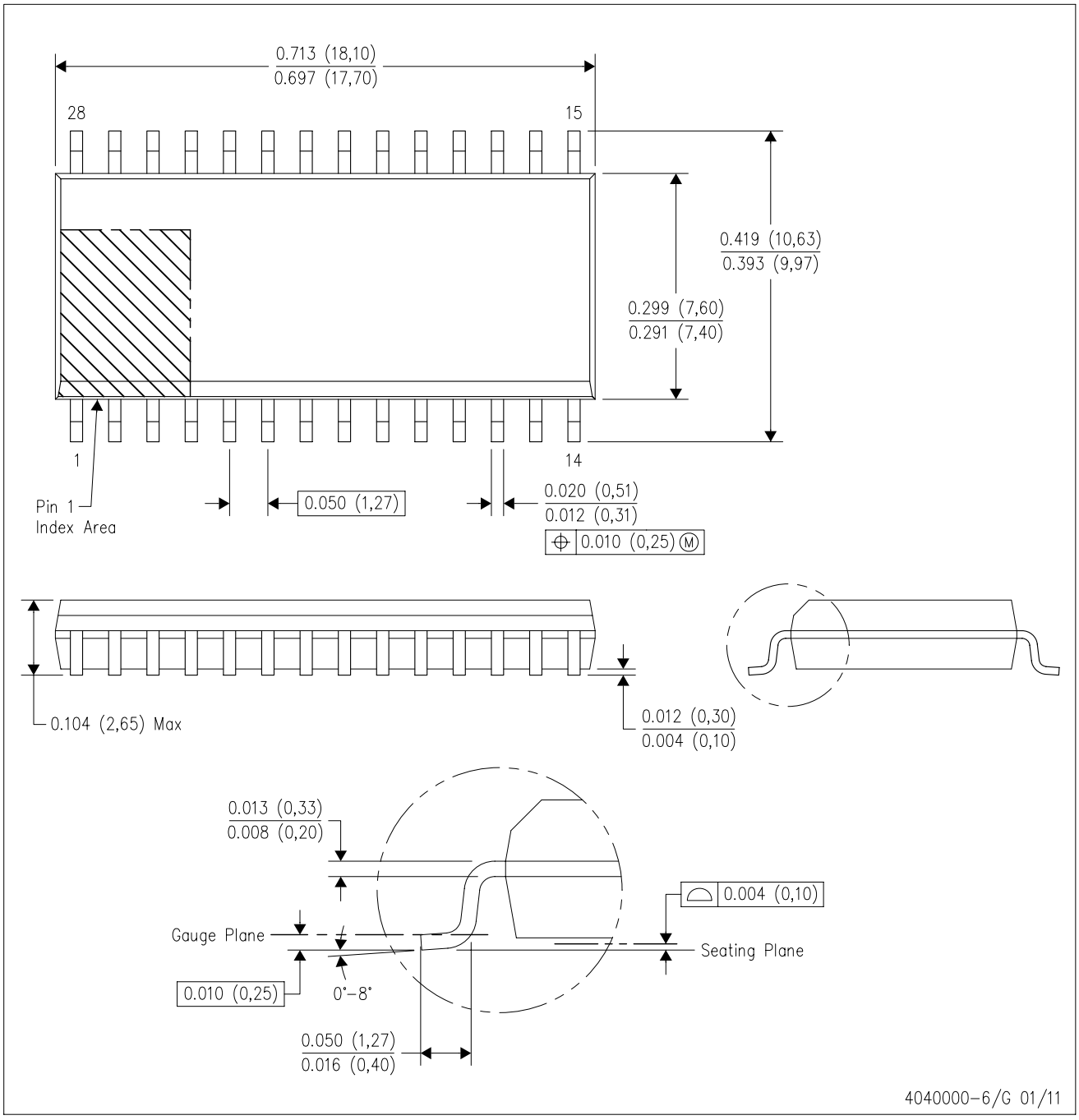
TUBE



*All dimensions are nominal

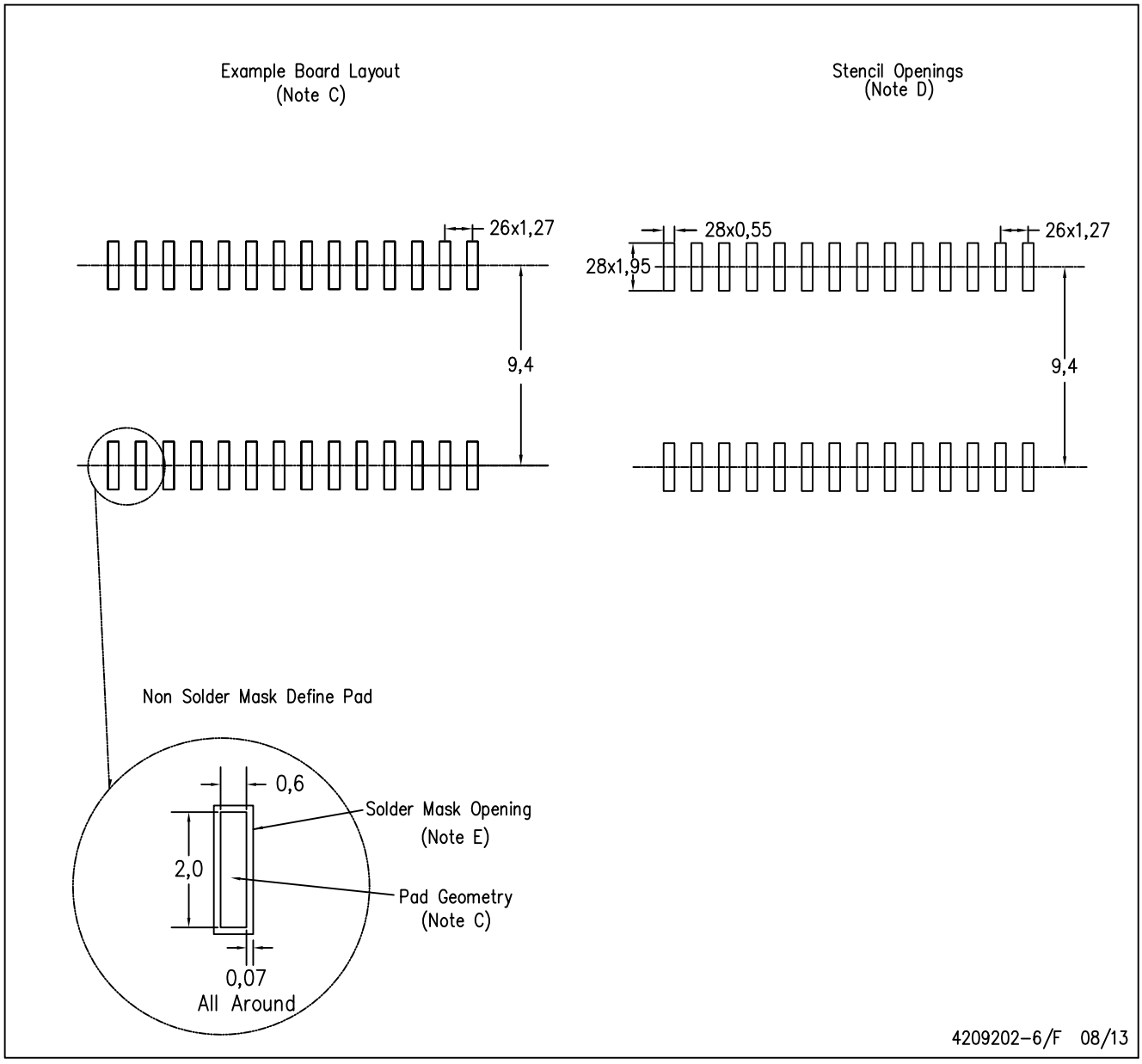
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ADS774HIBDW	DW	SOIC	28	20	507	12.83	5080	6.6
ADS774HIBDW.A	DW	SOIC	28	20	507	12.83	5080	6.6
ADS774HIDW	DW	SOIC	28	20	507	12.83	5080	6.6
ADS774HIDW.A	DW	SOIC	28	20	507	12.83	5080	6.6

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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