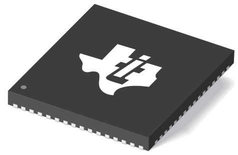


具有双数据速率 (DDR) 低压差分信令 (LVDS) 和并行 CMOS 输出的双通道，11 位，250 每秒百万次采样 (MSPS) 模数转换器 (ADC)

查询样品: **ADS62P19**

特性

- 最大采样率：**250MSPS**
- **11** 位分辨率
- 总体功耗：**250MSPS** 时为 **1.25W**
- 输出选项：
  - **DDR LVDS** 和并行 **CMOS**
- 可编程增益：
  - 针对信噪比 **(SNR) /** 无杂散动态范围 **(SFDR)** 平衡，高达 **6dB**
- **DC** 偏移校正
- 串扰：**90dB**
- 支持低至 **400mV$_{PP}$**输入时钟振幅，差分值
- 支持内部和外部基准
- 封装：**9mm x 9mm** 四方扁平无引线 **(QFN)-64** 封装

说明

ADS62P19 是采样速率高达 250MSPS 的双通道，11 位，模数转换器 (ADC) 系列的产品成员。 此器件在一个紧凑型 QFN-64 封装内将高动态性能与低功耗组合在了一起。 这个功能性使得此器件非常适合于多载波、宽带宽通信应用。

ADS62P19 具有可被用于在较低满量程输入范围内改进无杂散动态范围 (SFDR) 性能的增益选项。 此器件还包括一个 dc 偏移校正环路，此环路可被用于消除 ADC 偏移。 还提供了双数据速率 (DDR) 低压差分信令 (LVDS) 和并行互补金属氧化物半导体 (CMOS) 数字输出接口。

虽然此器件包含内部基准，但是删除了传统基准引脚和相关的去耦电容器。 但是，此器件仍可由一个外部基准驱动。 此器件可在工业温度范围（-40°C 至 +85°C）内工作。

ADS62Pxx 高速系列

分辨率	200MSPS	210 MSPS	250MSPS
11 位	ADS62C17	—	ADS62P19
12 位	—	ADS62P28	ADS62P29
14 位	—	ADS62P48	ADS62P49

表 **1.** 性能摘要

170MHz 输入频率时	增益 (dB)	ADS62P19	ADS62P28	ADS62P29	ADS62P48	ADS62P49
SFDR，dBc	0	75	78	75	78	75
	6	82	84	82	84	82
信噪比和失真率 (SINAD)，dBFS	0	65.3	68.7	68.3	70.1	69.8
	6	64	65.8	65.8	66.3	66.5
模拟功率，W	—	1	0.92	1	0.92	1

English Data Sheet: SLAS937

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	TRANSPORT MEDIA
ADS62P19	QFN-64	RGC	–40°C to +85°C	Tape and Reel
ADS62P28	QFN-64	RGC	–40°C to +85°C	Tape and Reel
ADS62P29	QFN-64	RGC	–40°C to +85°C	Tape and Reel
ADS62P48	QFN-64	RGC	–40°C to +85°C	Tape and Reel
ADS62P49	QFN-64	RGC	–40°C to +85°C	Tape and Reel

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		VALUE	UNIT
Supply voltage range	AVDD	–0.3 V to 3.9	V
	DRVDD	–0.3 V to 2.2	V
Voltage between AGND and DRGND		–0.3 to 0.3	V
Voltage between AVDD to DRVDD	AVDD leads DRVDD during power-up and DRVDD leads AVDD during power-down	–0.3 to 4.2	V
Voltage between DRVDD to AVDD	DRVDD leads AVDD during power-up and AVDD leads DRVDD during power-down	–2.5 to 1.7	V
Voltage applied to external pin	VCM (in external reference mode)	–0.3 to 2.0	V
Voltage applied to analog input pins	INP_A, INM_A, INP_B, INM_B	–0.3 to minimum (3.6, AVDD + 0.3)	V
Voltage applied to input pins	CLKP, CLKM(2), RESET, SCLK, SDATA, SEN, CTRL1, CTRL2, CTRL3	–0.3 to AVDD + 0.3	V
Temperature range	Operating free-air, T_A	–40 to +85	°C
	Operating junction, T_J	+125	°C
	Storage, T_{stg}	–65 to +150	°C
Electrostatic discharge (ESD) rating	Human body model (HBM)	2	kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) When AVDD is turned off, TI recommends switching off the input clock (or ensuring the voltage on CLKP, CLKM is < |0.3 V|). This setting prevents the ESD protection diodes at the clock input pins from turning on.

THERMAL INFORMATION

THERMAL METRIC(1)		ADS62P19 RGC PACKAGE 64 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	23.0	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	10.5	
θ_{JB}	Junction-to-board thermal resistance	4.2	
ψ_{JT}	Junction-to-top characterization parameter	0.1	
ψ_{JB}	Junction-to-board characterization parameter	4.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.57	

(1) 有关传统和新的热 度量的更多信息，请参阅*IC 封装热度量*应用报告， SPRA953。

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
SUPPLIES						
AVDD	Analog supply voltage		3.15	3.3	3.6	V
DRVDD	Digital supply voltage		1.7	1.8	1.9	V
ANALOG INPUTS						
	Differential input voltage range			2		V_{PP}
	Input common-mode voltage			1.5 ± 0.1		V
	Voltage applied on CM in external reference mode			1.5 ± 0.05		V
	Maximum analog input frequency	With 2-V_{pp} input amplitude (1)		500		MHz
		With 1-V_{pp} input amplitude (1)		800		MHz
CLOCK INPUT						
	Input clock sample rate	Low-speed mode disabled (default mode after reset)	> 80		250 (2)	MSPS
		Low-speed mode enabled (3)	1		80	MSPS
		With multiplexed mode enabled (4)	1		65	MSPS
	Input clock amplitude differential (V_{CLKP} – V_{CLKM}) (5) (6)	Sine wave, ac-coupled	0.2	1.5		V_{PP}
		LVPECL, ac-coupled		1.6		V_{PP}
		LVDS, ac-coupled		0.7		V_{PP}
		LVCMOS, single-ended, ac-coupled		3.3		V
	Input clock duty cycle		40%	50%	60%	
DIGITAL OUTPUTS						
C_{LOAD}	Maximum external load capacitance from each output pin to DRGND			5		pF
R_{LOAD}	Differential load resistance between the LVDS output pairs (LVDS mode)			100		Ω
T_A	Operating free-air temperature		–40		85	°C

(1) See the *Theory of Operation* section for information.
(2) With LVDS interface only; maximum recommended sample rate with CMOS interface is 210 MSPS.
(3) Use the ENABLE LOW SPEED MODE register bit; refer to the *Serial Register Map* section for information.
(4) See the *Multiplexed Output Mode* section for information.
(5) Refer to Figure 25.
(6) Refer to Figure 1 for the definition of clock amplitude.

ELECTRICAL CHARACTERISTICS: GENERAL

Typical values are at T_A = +25°C, AVDD = 3.3 V, DRVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, and internal reference mode, unless otherwise noted.

Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 3.3 V, and DRVDD = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
V_{ID}	Differential input voltage range	0-dB gain		2		V_{PP}
	Differential input resistance	At dc, see Figure 45		> 1		MΩ
	Differential input capacitance	See Figure 46		3.5		pF
	Analog input bandwidth	With 25-Ω source impedance		700		MHz
	Analog input common-mode current	Per channel		3.6		µA/MSPS
VCM	Common-mode output voltage			1.5		V
VCM	Output current capability			±4		mA
DC ACCURACY						
E_O	Offset error		–20	±2	20	mV
	Temperature coefficient of offset error			0.02		mV/°C
	Variation of offset error with supply			0.5		mV/V
	Two sources of gain error: internal reference inaccuracy and channel gain error					
E_{GREF}	Gain error resulting from internal reference inaccuracy alone		–1	±0.2	1	% FS
E_{GCHAN}	Gain error of channel alone (1)		–1	±0.2	1	% FS
	Temperature coefficient of E_{GCHAN}			0.002		Δ%/°C
	Gain matching (2)	Difference in gain errors between two channels within the same device	–2		2	%FS
		Difference in gain errors between two channels across two devices	–4		4	%FS
POWER SUPPLY						
IAVDD	Analog supply current			305	350	mA
IDRVDD	Output buffer supply current	LVDS interface with 100-Ω external termination		133	175	mA
		CMOS interface, f_{IN} = 2 MHz, f_S = 210 MSPS, no external load capacitance (3)(4)		91		mA
AVDD	Analog power			1.01	1.15	W
DVDD	Digital power	LVDS interface		0.24	0.315	W
	Global power down			45	100	mW

(1) This parameter is specified by design and characterization; not tested in production.
(2) For two channels within the same device, only the channel gain error matters because the reference is common for both channels.
(3) In CMOS mode, the DRVDD current scales with the sampling frequency, the load capacitance on output pins, input frequency, and the supply voltage (see Figure 31 and the *CMOS Interface Power Dissipation* section in the Application Information).
(4) The maximum DRVDD current with CMOS interface depends on the actual load capacitance on the digital output lines. Note that the maximum recommended load capacitance on each digital output line is 10 pF.

ELECTRICAL CHARACTERISTICS: ADS62P19

Typical values are at T_A = +25°C, AVDD = 3.3 V, DRVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, and internal reference mode, unless otherwise noted. Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 3.3 V, and DRVDD = 1.8 V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SNR	Signal to noise ratio, LVDS	f_{IN} = 20 MHz			66.5		dBFS
		f_{IN} = 60 MHz			66.4		dBFS
		f_{IN} = 100 MHz			66.1		dBFS
		f_{IN} = 170 MHz	0-dB gain	64.5	65.9		dBFS
			6-dB gain		64.1		dBFS
		f_{IN} = 230 MHz			65.4		dBFS
SINAD	Signal to noise and distortion ratio, LVDS	f_{IN} = 20 MHz			66.5		dBFS
		f_{IN} = 60 MHz			66.3		dBFS
		f_{IN} = 100 MHz			65.9		dBFS
		f_{IN} = 170 MHz	0-dB gain	63.5	65.3		dBFS
			6-dB gain		64		dBFS
		f_{IN} = 230 MHz			65.2		dBFS
ENOB	Effective number of bits	f_{IN} = 170 MHz			10.6		LSB
DNL	Differential nonlinearity	f_{IN} = 170 MHz		–0.6	±0.1		LSB
INL	Integrated nonlinearity	f_{IN} = 170 MHz			±0.5	±2.5	LSB
SFDR	Spurious-free dynamic range	f_{IN} = 20 MHz			89		dBc
		f_{IN} = 60 MHz			85		dBc
		f_{IN} = 100 MHz			78		dBc
		f_{IN} = 170 MHz		69.5	75		dBc
		f_{IN} = 230 MHz			77		dBc
	Spurious-free dynamic range (excluding HD2, HD3)	f_{IN} = 20 MHz			98		dBc
		f_{IN} = 60 MHz			95		dBc
		f_{IN} = 100 MHz			88		dBc
		f_{IN} = 170 MHz		75	88		dBc
		f_{IN} = 230 MHz			87		dBc
HD2	Second-order harmonic distortion	f_{IN} = 20 MHz			93		dBc
		f_{IN} = 60 MHz			90		dBc
		f_{IN} = 100 MHz			90		dBc
		f_{IN} = 170 MHz		69.5	85		dBc
		f_{IN} = 230 MHz			85		dBc
HD3	Third-order harmonic distortion	f_{IN} = 20 MHz			89		dBc
		f_{IN} = 60 MHz			85		dBc
		f_{IN} = 100 MHz			78		dBc
		f_{IN} = 170 MHz		69.5	75		dBc
		f_{IN} = 230 MHz			77		dBc
THD	Total harmonic distortion	f_{IN} = 20 MHz			87		dBc
		f_{IN} = 60 MHz			83.5		dBc
		f_{IN} = 100 MHz			77.5		dBc
		f_{IN} = 170 MHz		68	74		dBc
		f_{IN} = 230 MHz			75		dBc
IMD	Two-tone intermodulation distortion	f_1 = 46 MHz, f_2 = 50 MHz, each tone at –7 dBFS			87		dBFS
		f_1 = 185 MHz, f_2 = 190 MHz, each tone at –7 dBFS			85		dBFS
	Crosstalk	Up to 200-MHz crosstalk frequency			90		dB
	Input overload recovery	Recovery to within 1% (of final value) for 6-dB overload with sine-wave input			1		Clock cycles
PSRR	AC power-supply rejection ratio	For 100-mV_{PP} signal on AVDD supply			25		dB

DIGITAL CHARACTERISTICS

The dc specifications refer to the condition where the digital outputs do not switch, but are permanently at a valid logic level '0' or '1'. AVDD = 3.3 V and DRVDD = 1.8 V.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS (CTRL1, CTRL2, CTRL3, RESET, SCLK, SDATA, SEN[(1)])							
V_{IH}	High-level input voltage		All digital inputs support 1.8-V and 3.3-V CMOS logic levels	1.3			V
V_{IL}	Low-level input voltage		All digital inputs support 1.8-V and 3.3-V CMOS logic levels			0.4	V
I_{IH}	High-level input current	SDATA, SCLK[(2)]	V_{HIGH} = 3.3 V		16		μA
		SEN[(3)]	V_{HIGH} = 3.3 V		10		μA
I_{IL}	Low-level input current	SDATA, SCLK	V_{LOW} = 0 V		0		μA
		SEN	V_{LOW} = 0 V		–20		μA
C_I	Input capacitance				4		pF
DIGITAL OUTPUTS (CMOS INTERFACE: DA[10:0], DB[10:0], CLKOUT, SDOUT)							
V_{OH}	High-level output voltage		I_{OH} = 1 mA	DRVDD – 0.1	DRVDD		V
V_{OL}	Low-level output voltage		I_{OL} = 1 mA		0	0.1	V
C_O	Output capacitance (internal to device)				2		pF
DIGITAL OUTPUTS (LVDS INTERFACE)							
V_{ODH}	High-level output differential voltage		With external 100-Ω termination	275	350	425	mV
V_{ODL}	Low-level output differential voltage		With external 100-Ω termination	–425	–350	–275	mV
V_{OCM}	Output common-mode voltage			1	1.15	1.4	V
C_O	Output capacitance		Capacitance inside the device from each output to ground		2		pF

(1) SCLK, SDATA, and SEN function as digital input pins in serial configuration mode.
(2) SDATA, SCLK, RESET, CTRL1, CTRL2, and CTRL3 have an internal 100-kΩ pull-down resistor.
(3) SEN has an internal 100-kΩ pull-up resistor to AVDD. SEN can also be driven by 1.8-V or 3.3-V CMOS buffers because the pull-up resistor is weak.

TIMING REQUIREMENTS: LVDS AND CMOS MODES[1]

Typical values are at T_A = +25°C, AVDD = 3.3 V, DRVDD = 1.8 V, sampling frequency = 250 MSPS, sine-wave input clock, 1.5-V_{PP} clock amplitude, C_{LOAD} = 5 pF[2], and R_{LOAD} = 100 Ω[3], unless otherwise noted. Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 3.3 V, and DRVDD = 1.7 V to 1.9 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_a	Aperture delay		0.7	1.2	1.7	ns
	Aperture delay matching	Between two channels within the same device		±50		ps
t_j	Aperture jitter			145		f_S RMS
	Wake-up time	Time to valid data after exiting STANDBY mode		1	3	µs
		Time to valid data after exiting global power-down		20	50	µs
		Time to valid data after stopping and restarting the input clock		10		Clock cycles
	ADC latency[4]			22		Clock cycles
DDR LVDS MODE[5]						
t_{su}	Data setup time	Data valid[6] to CLKOUTP zero-crossing	0.55	0.9		ns
t_h	Data hold time	CLKOUTP zero-crossing to data becoming invalid[6]	0.55	0.95		ns
t_{PDI}	Clock propagation delay	Input clock falling edge crossover to output clock rising edge crossover *100 MSPS ≤ sampling frequency ≤ 250 MSPS* *t_S = 1 / sampling frequency*	$t_{PDI} = 0.69 \times t_S + t_{delay}$			
t_{delay}			4.2	5.7	7.2	ns
	t_{delay} skew	Difference in t_{delay} between two devices operating at same temperature and DRVDD supply voltage		±500		ps
	LVDS bit clock duty cycle	Differential clock duty cycle (CLKOUTP – CLKOUTM) *100 MSPS ≤ sampling frequency ≤ 250 MSPS*		52%		
t_{RISE}, t_{FALL}	Data rise time, Data fall time	Rise time measured from –100 mV to +100 mV Fall time measured from +100 mV to –100 mV *1 MSPS ≤ sampling frequency ≤ 250 MSPS*		0.14		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from –100 mV to +10 0mV Fall time measured from +100 mV to –100 mV *1 MSPS ≤ sampling frequency ≤ 250 MSPS*		0.14		ns
t_{OE}	Output buffer enable to data delay	Time to valid data after output buffer becomes active		100		ns

(1) Timing parameters are ensured by design and characterization and are not tested in production.
(2) C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground.
(3) R_{LOAD} is the differential load resistance between the LVDS output pair.
(4) At higher clock frequencies, t_{PDI} is greater than one clock period and overall latency = ADC latency + 1.
(5) Measurements are done with a transmission line of 100-Ω characteristic impedance between the device and load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(6) Data valid refers to a logic high of +100.0 mV and a logic low of –100.0 mV.

TIMING REQUIREMENTS: LVDS AND CMOS MODES[1] (continued)

Typical values are at T_A = +25°C, AVDD = 3.3 V, DRVDD = 1.8 V, sampling frequency = 250 MSPS, sine-wave input clock, 1.5-V_{PP} clock amplitude, C_{LOAD} = 5 pF[2], and R_{LOAD} = 100 Ω[3], unless otherwise noted. Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 3.3 V, and DRVDD = 1.7 V to 1.9 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PARALLEL CMOS MODE[7] (At f_S = 210 MSPS)						
t_{START}	Input clock to data delay	Input clock falling edge crossover to start of data valid[8]			2.5	ns
t_{DV}	Data valid time	Time interval of valid data[8]	1.7	2.7		ns
t_{PDI}	Clock propagation delay	Input clock falling edge crossover to output clock rising edge crossover *100 MSPS ≤ sampling frequency ≤ 150 MSPS* *t_S = 1 / sampling frequency*	$t_{PDI} = 0.28 \times t_S + t_{delay}$			
t_{delay}			5.5	7.0	8.5	ns
	Output clock duty cycle	Output clock duty cycle , CLKOUT *100 MSPS ≤ sampling frequency ≤ 150 MSPS*		43%		
t_{RISE}, t_{FALL}	Data rise time, Data fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD *1 ≤ sampling frequency ≤ 210 MSPS*		1.2		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD *1 ≤ sampling frequency ≤ 150 MSPS*		0.8		ns
t_{OE}	Output buffer enable (OE) to data delay[9]	Time to valid data after output buffer becomes active		100		ns

(7) For f_S > 150 MSPS, TI recommends using an external clock for data capture instead of the device output clock signal (CLKOUT).
(8) Data valid refers to a logic high of 1.26 V and a logic low of 0.54 V.
(9) The output buffer enable is controlled by serial interface register 40h. The output buffer becomes active when serial control data for the output buffer are latched on the 16th SCLK falling edge when SEN is low.

Table 2. LVDS Timings at Lower Sampling Frequencies

SAMPLING FREQUENCY (MSPS)	SETUP TIME (ns)			HOLD TIME (ns)			t_{PDI} (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
210	0.75	1.1		0.75	1.15		7.5	9	10.5
185	0.9	1.25		0.85	1.25		7.9	9.4	10.9
153	1.15	1.55		1.1	1.5		8.7	10.2	11.7
125	1.6	2		1.45	1.85		9.7	11.2	12.7
< 80 (enable low-speed mode for f_S ≤ 80)[1]	2			2					
1 ≤ f_S ≤ 80 (enable low-speed mode for f_S ≤ 80)[1]								12.6	

(1) Low-speed mode can only be enabled with the serial interface configuration.

Table 3. CMOS Timings at Lower Sampling Frequencies with Respect to Input Clock

SAMPLING FREQUENCY (MSPS)	TIMINGS SPECIFIED WITH RESPECT TO INPUT CLOCK					
	t_{START} (ns)			DATA VALID TIME (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX
210			2.5	1.7	2.7	
190			1.9	2	3	
170			0.9	2.7	3.7	
150			6	3.6	4.6	

Table 4. CMOS Timings at Lower Sampling Frequencies with Respect to CLKOUT

SAMPLING FREQUENCY (MSPS)	TIMINGS SPECIFIED WITH RESPECT TO CLKOUT								
	SETUP TIME (ns)			HOLD TIME (ns)			t_{PDI} (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
170	2.1	3.7		0.35	1.0		7.1	8.6	10.1
150	2.8	4.4		0.5	1.2		7.4	8.9	10.4
125	3.8	5.4		0.8	1.5		7.7	9.2	10.7
< 80 (enable low-speed mode for $f_S \le 80$)(1)	5			1.2					
$1 \le f_S \le 80$ (enable low-speed mode for $f_S \le 80$)(1)								9	

(1) Low-speed mode can only be enabled with the serial interface configuration.

PARAMETRIC MEASUREMENT INFORMATION

TIMING DIAGRAMS

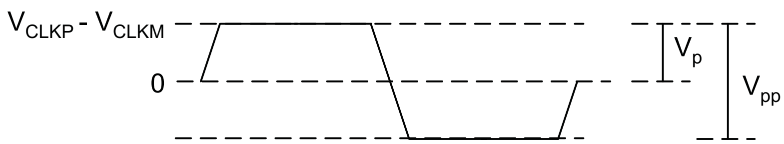
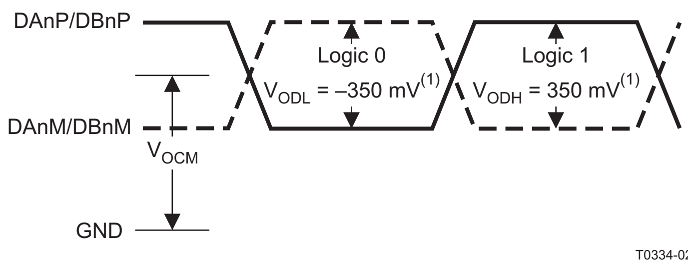


Figure 1. Clock Amplitude Definition Diagram



(1) With external 100-Ω termination

Figure 2. LVDS Output Voltage Levels

PARAMETRIC MEASUREMENT INFORMATION (continued)

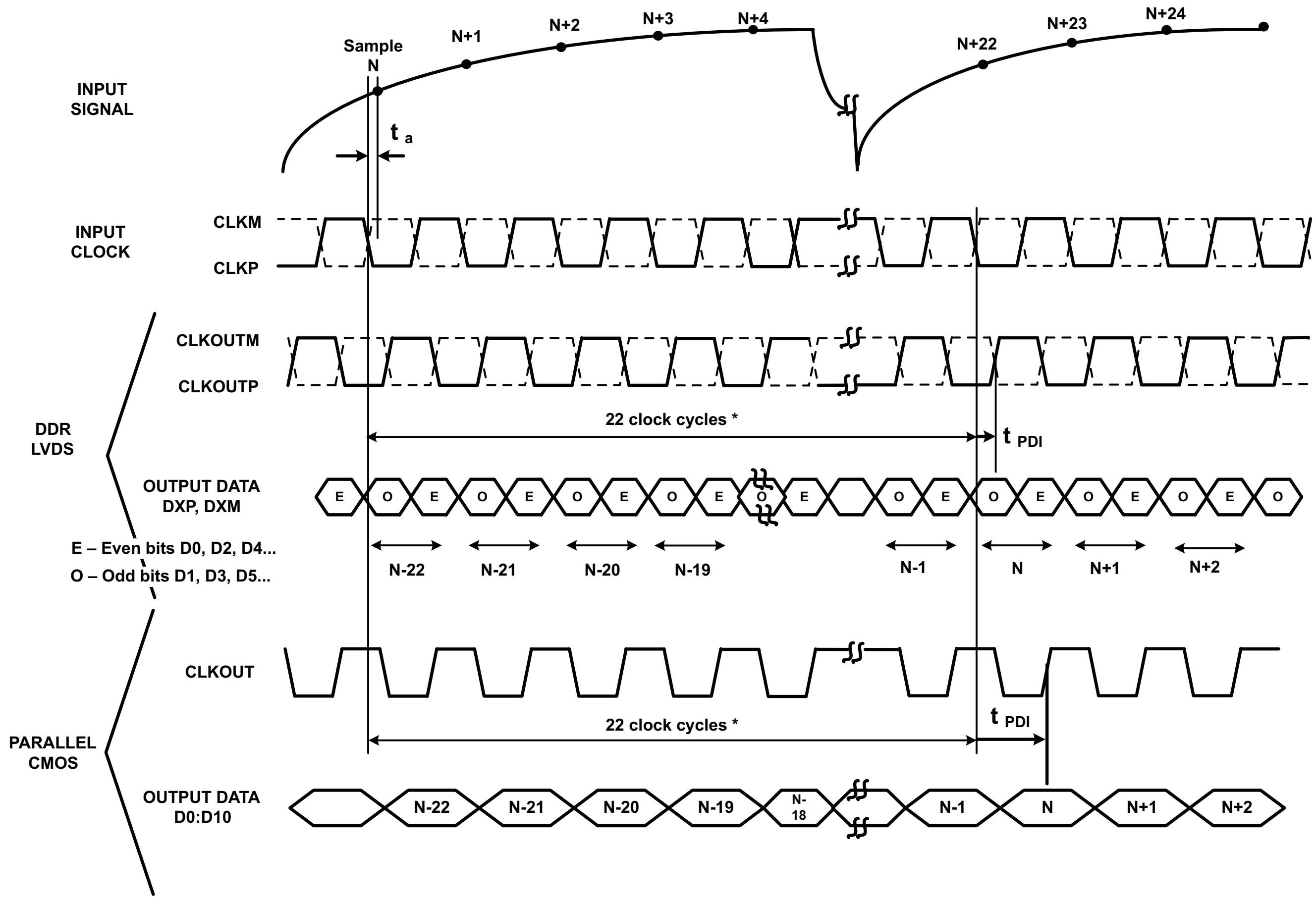


Figure 3. Latency Diagram

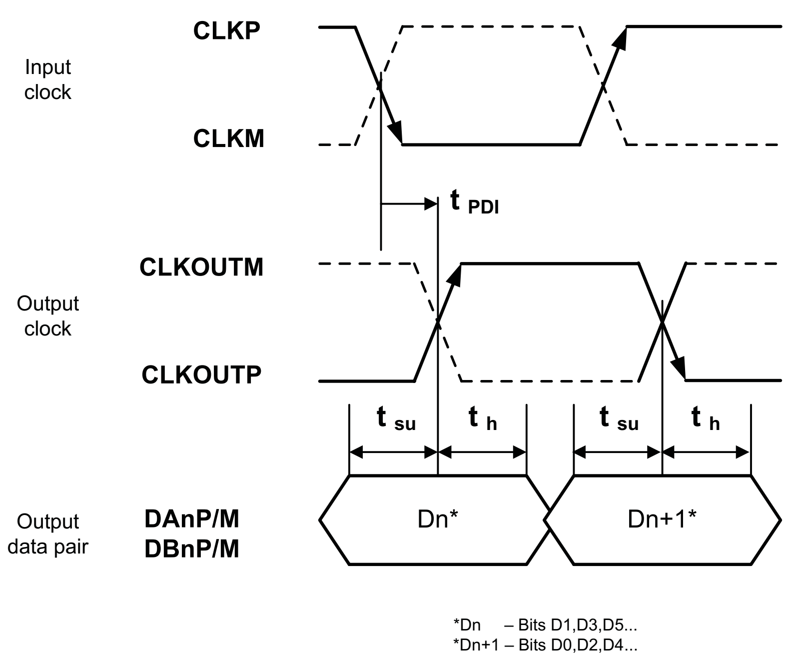
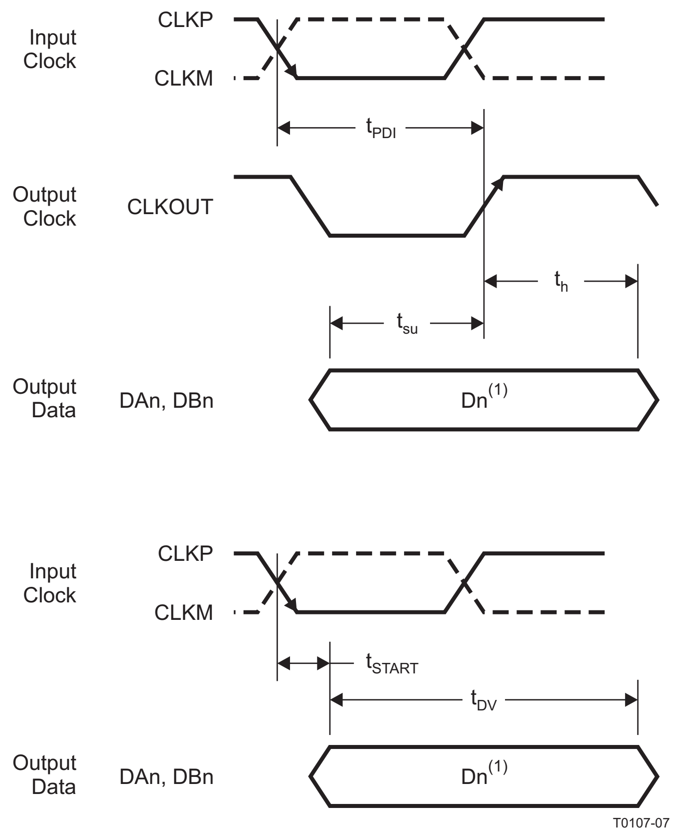


Figure 4. LVDS Interface Timing

PARAMETRIC MEASUREMENT INFORMATION (continued)



(1) Dn = bits D0, D1, D2, and so forth of channels A and B.

Figure 5. CMOS Interface Timing

PARAMETRIC MEASUREMENT INFORMATION (continued)

SERIAL INTERFACE

Table 5. SERIAL INTERFACE TIMING CHARACTERISTICS(1)

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (= 1 / t_{SCLK})	> dc		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DS}	SDATA setup time	25			ns
t_{DH}	SDATA hold time	25			ns

(1) Typical values are at T_A = +25°C, minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 3.3 V, and DRVDD = 1.8 V, unless otherwise noted.

Serial Register Readout

The device includes an option where the contents of the internal registers can be read back. This functionality may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC. In order to achieve read back:

- First, set the SERIAL READOUT register bit to '1'. This setting also disables any further writes into the registers.
- Initiate a serial interface cycle specifying the address of the register (A[7:0]) whose content must be read.
- The device outputs the contents (D[7:0]) of the selected register on the SDOUT pin (pin 64).
- The external controller can latch the contents at the SCLK falling edge.
- To enable register writes, reset the SERIAL READOUT register bit to '0'. SDOUT is a CMOS output pin; the readout functionality is available whether the ADC output data interface is LVDS or CMOS.

When SERIAL READOUT is disabled, the SDOUT pin is forced low by the device (and is not put in high-impedance). If serial readout is not used, the SDOUT pin must float. Note that contents of register 00h cannot be read back.

Table 6. Reset Timing (only when the serial interface is used)(1)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from power-up of AVDD and DRVDD to RESET pulse active	1			ms
t_2	Reset pulse duration	Pulse duration of active RESET signal	10			ns
					1	µs
t_3	Register write delay	Delay from RESET disable to SEN active	100			ns

(1) Typical values are at T_A = +25°C, minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, unless otherwise noted.

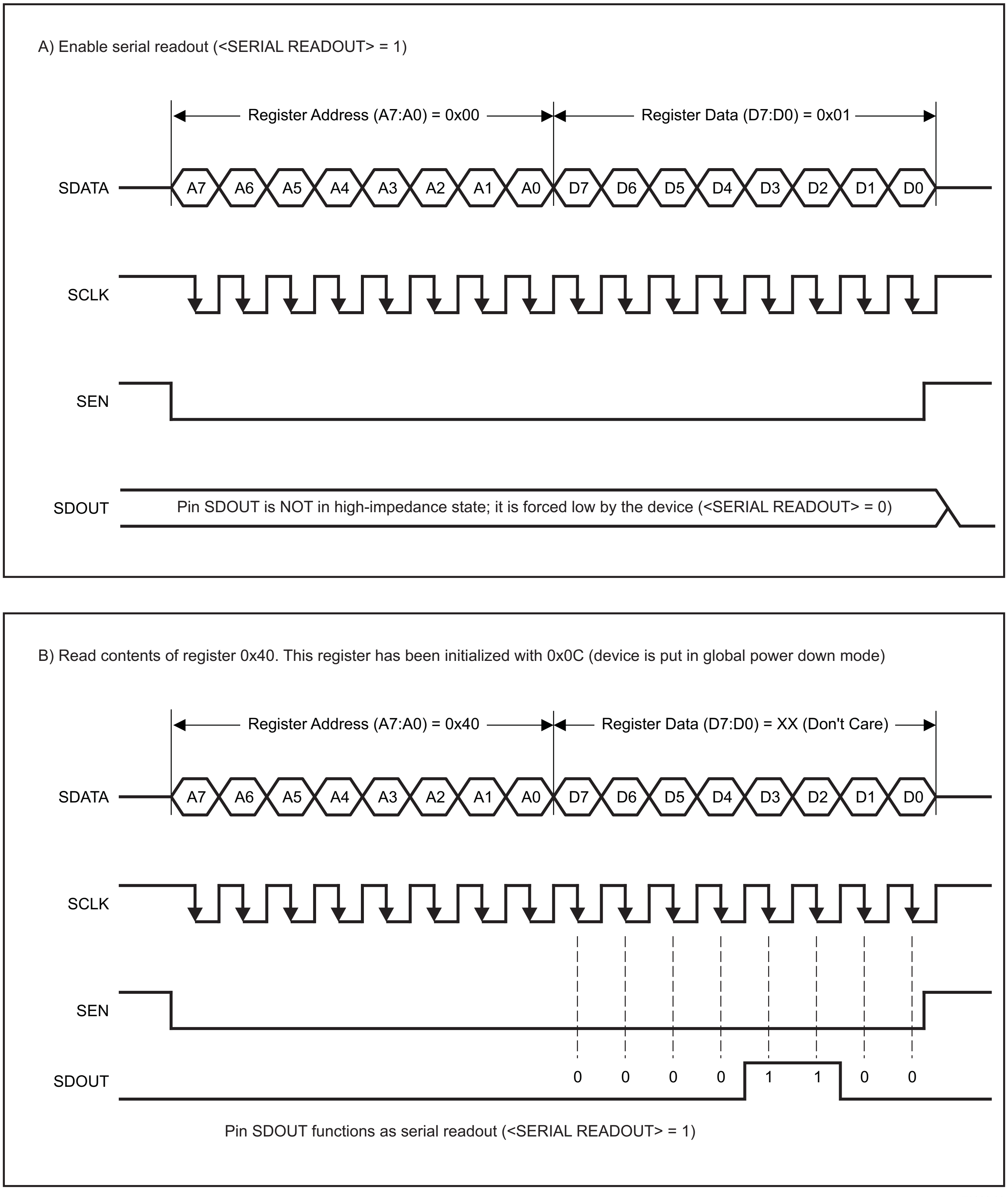
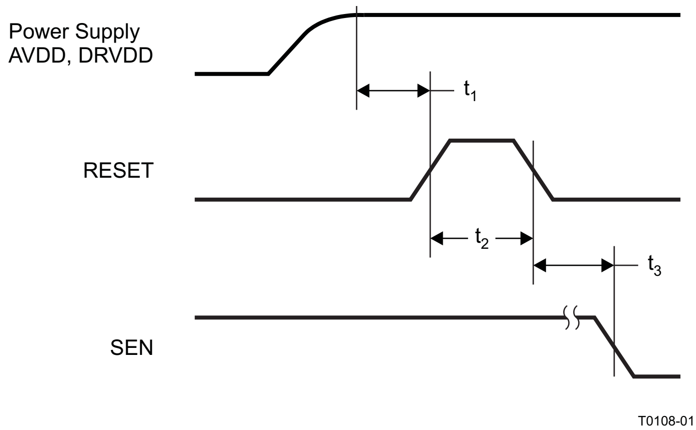


Figure 6. Serial Readout



NOTE: A high-going pulse on the RESET pin is required in serial interface mode in case of initialization through hardware reset. For parallel interface operation, RESET must be permanently tied high.

Figure 7. Reset Timing Diagram

PIN CONFIGURATIONS

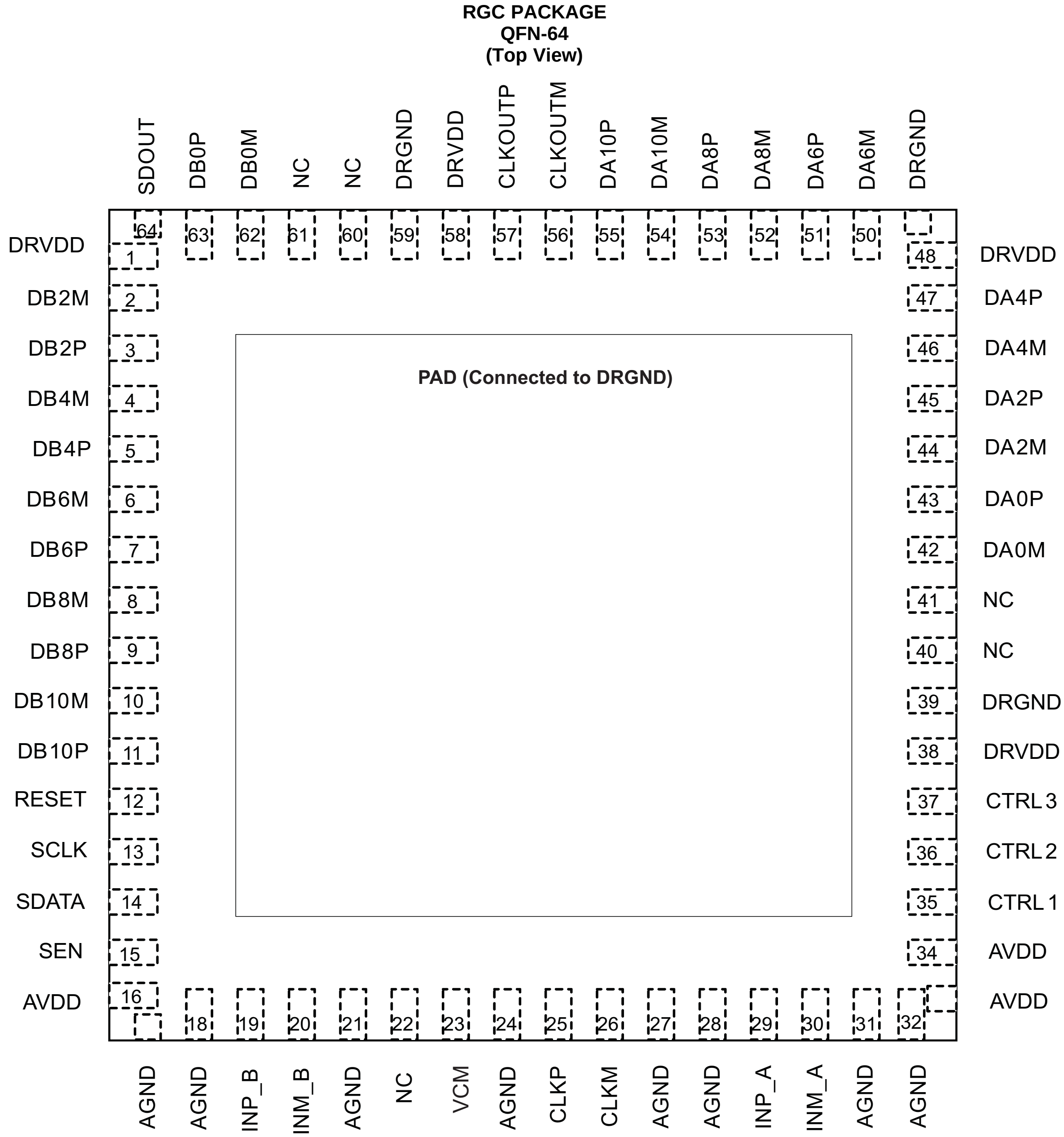


Figure 8. LVDS Mode

PIN DESCRIPTIONS (LVDS MODE)

PIN		NO. OF PINS	I/O	DESCRIPTION
NAME	NO.			
AGND	17, 18, 21, 24, 27, 28, 31, 32	8	I	Analog ground
AVDD	16, 33, 34	3	I	Analog power supply
CLKM	26	1	I	Differential clock input
CLKP	25	1	I	Differential clock input
CLKOUTM	56	1	O	Differential output clock, complement

PIN DESCRIPTIONS (LVDS MODE) (continued)

PIN		NO. OF PINS	I/O	DESCRIPTION
NAME	NO.			
CLKOUTP	57	1	O	Differential output clock, true
CTRL1	35	1	I	Digital control input pins. Together, these pins control various power-down modes. Each pin has an internal 100-kΩ pull-down resistor.
CTRL2	36	1	I	
CTRL3	37	1	I	
DA0P, DA0M	Refer to Figure 8	2	O	Differential output data pair, 0 and D0 multiplexed; channel A
DA2P, DA2M	Refer to Figure 8	2	O	Differential output data D1 and D2 multiplexed; channel A
DA4P, DA4M	Refer to Figure 8	2	O	Differential output data D3 and D4 multiplexed; channel A
DA6P, DA6M	Refer to Figure 8	2	O	Differential output data D5 and D6 multiplexed; channel A
DA8P, DA8M	Refer to Figure 8	2	O	Differential output data D7 and D8 multiplexed; channel A
DA10P, DA10M	Refer to Figure 8	2	O	Differential output data D9 and D10 multiplexed; channel A
DB0P, DB0M	Refer to Figure 8	2	O	Differential output data pair, 0 and D0 multiplexed; channel B
DB2P, DB2M	Refer to Figure 8	2	O	Differential output data D1 and D2 multiplexed; channel B
DB4P, DB4M	Refer to Figure 8	2	O	Differential output data D3 and D4 multiplexed; channel B
DB6P, DB6M	Refer to Figure 8	2	O	Differential output data D5 and D6 multiplexed; channel B
DB8P, DB8M	Refer to Figure 8	2	O	Differential output data D7 and D8 multiplexed; channel B
DB10P, DB10M	Refer to Figure 8	2	O	Differential output data D9 and D10 multiplexed; channel B
DRGND	39, 49, 59, PAD	4	I	Output buffer ground
DRVDD	1, 38, 48, 58	4	I	Output buffer supply
INM_A	30	1	I	Differential analog input, channel A
INP_A	29	1	I	Differential analog input, channel A
INM_B	20	1	I	Differential analog input, channel B
INP_B	19	1	I	Differential analog input, channel B
NC	Refer to Figure 8	5		Do not connect
RESET	12	1	I	Serial interface RESET input. When using the serial interface mode, the internal registers ***must*** be initialized through a hardware RESET by applying a high-going pulse on this pin or by using a software reset option. Refer to the *Serial Interface* section. In parallel interface mode, the RESET pin must be permanently tied high. (SCLK and SEN are used as parallel control pins in this mode.) This pin has an internal 100-kΩ pull-down resistor.
SCLK	13	1	I	This pin functions as serial interface clock input when RESET is low. SCLK controls the internal or external reference selection when RESET is tied high. See Table 8 for detailed information. This pin has an internal 100-kΩ pull-down resistor.
SDATA	14	1	I	Serial interface data input. SDATA has an internal 100-kΩ pull-down resistor. This pin has no function in parallel interface mode and can be tied to ground.
SDOUT	64	1	O	This pin functions as a serial interface register readout when the SERIAL READOUT bit is enabled. When SERIAL READOUT is '0', this pin forces a logic low and is not 3-stated.
SEN	15	1	I	This pin functions as a serial interface enable input when RESET is low. SEN controls data format and interface type selection when RESET is tied high. See Table 9 for detailed information. This pin has an internal 100-kΩ pull-up resistor to AVDD.
VCM	23	1	IO	Internal reference mode. Common-mode voltage output. External reference mode. Reference input; the voltage forced on this pin sets the internal references.

RGC PACKAGE
QFN-64
(Top View)

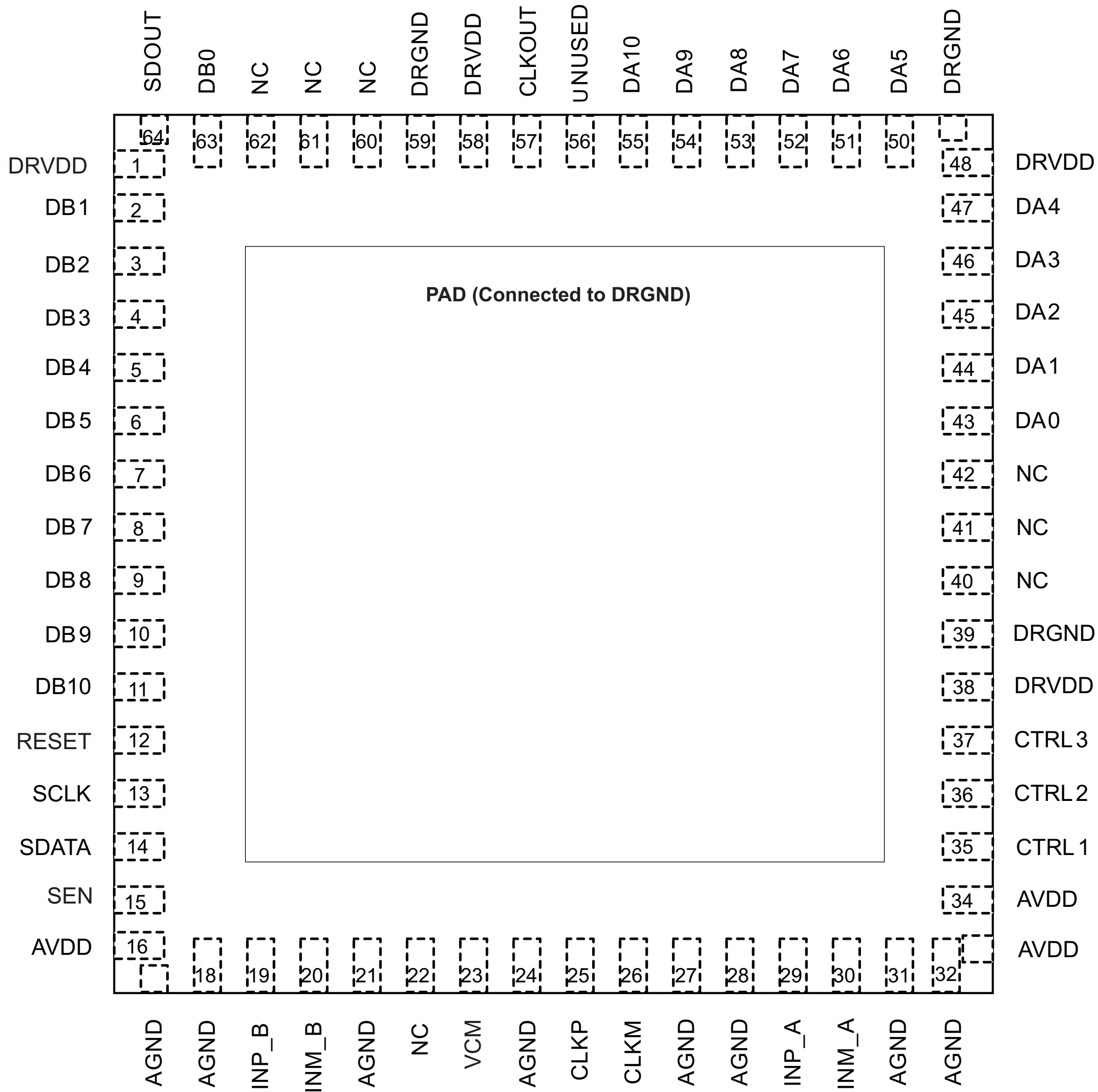


Figure 9. CMOS Mode

PIN DESCRIPTIONS (CMOS MODE)

PIN		NO. OF PINS	I/O	DESCRIPTION
NAME	NO.			
AVDD	16, 33, 34	3	I	Analog power supply
AGND	17, 18, 21, 24, 27, 28, 31, 32	8	I	Analog ground
CLKM	26	1	I	Differential clock input
CLKP	25	1	I	Differential clock input
CLKOUT	57	1	O	CMOS output clock
CTRL1	35	1	I	Digital control input pins. Together, these pins control various power-down modes. Each pin has an internal 100-kΩ pull-down resistor.
CTRL2	36	1	I	
CTRL3	37	1	I	
DA0 to DA10	Refer to Figure 9	11	O	Channel A ADC output data bits, CMOS levels
DB0 to DB10	Refer to Figure 9	11	O	Channel B ADC output data bits, CMOS levels
DRGND	39, 49, 59, PAD	4	I	Output buffer ground
DRVDD	1, 38, 48, 58	4	I	Output buffer supply
INM_A	30	1	I	Differential analog input, channel A
INP_A	29	1	I	Differential analog input, channel A
INM_B	20	1	I	Differential analog input, channel B
INP_B	19	1	I	Differential analog input, channel B
NC	Refer to Figure 9	7		Do not connect
RESET	12	1	I	Serial interface RESET input. When using the serial interface mode, the internal registers must be initialized through a hardware RESET by applying a high-going pulse on this pin or by using a software reset option. Refer to the *Serial Interface* section. In parallel interface mode, the RESET pin must be permanently tied high. (SCLK and SEN are used as parallel control pins in this mode.) This pin has an internal 100-kΩ pull-down resistor.
SCLK	13	1	I	This pin functions as a serial interface clock input when RESET is low. SCLK controls the internal or external reference selection when RESET is tied high. See Table 8 for detailed information. This pin has an internal 100-kΩ pull-down resistor.
SDATA	14	1	I	Serial interface data input. This pin has an internal 100-kΩ pull-down resistor. SDATA has no function in parallel interface mode and can be tied to ground.
SDOUT	64	1	O	This pin functions as a serial interface register readout when the SERIAL READOUT bit is enabled. When SERIAL READOUT is '0', this pin forces a logic low and is not 3-stated.
SEN	15	1	I	This pin functions as a serial interface enable input when RESET is low. SEN controls data format and interface type selection when RESET is tied high. See Table 9 for detailed information. This pin has an internal 100-kΩ pull-up resistor to AVDD.
VCM	23	1	IO	Internal reference mode. Common-mode voltage output. External reference mode. Reference input; the voltage forced on this pin sets the internal references.

FUNCTIONAL BLOCK DIAGRAM

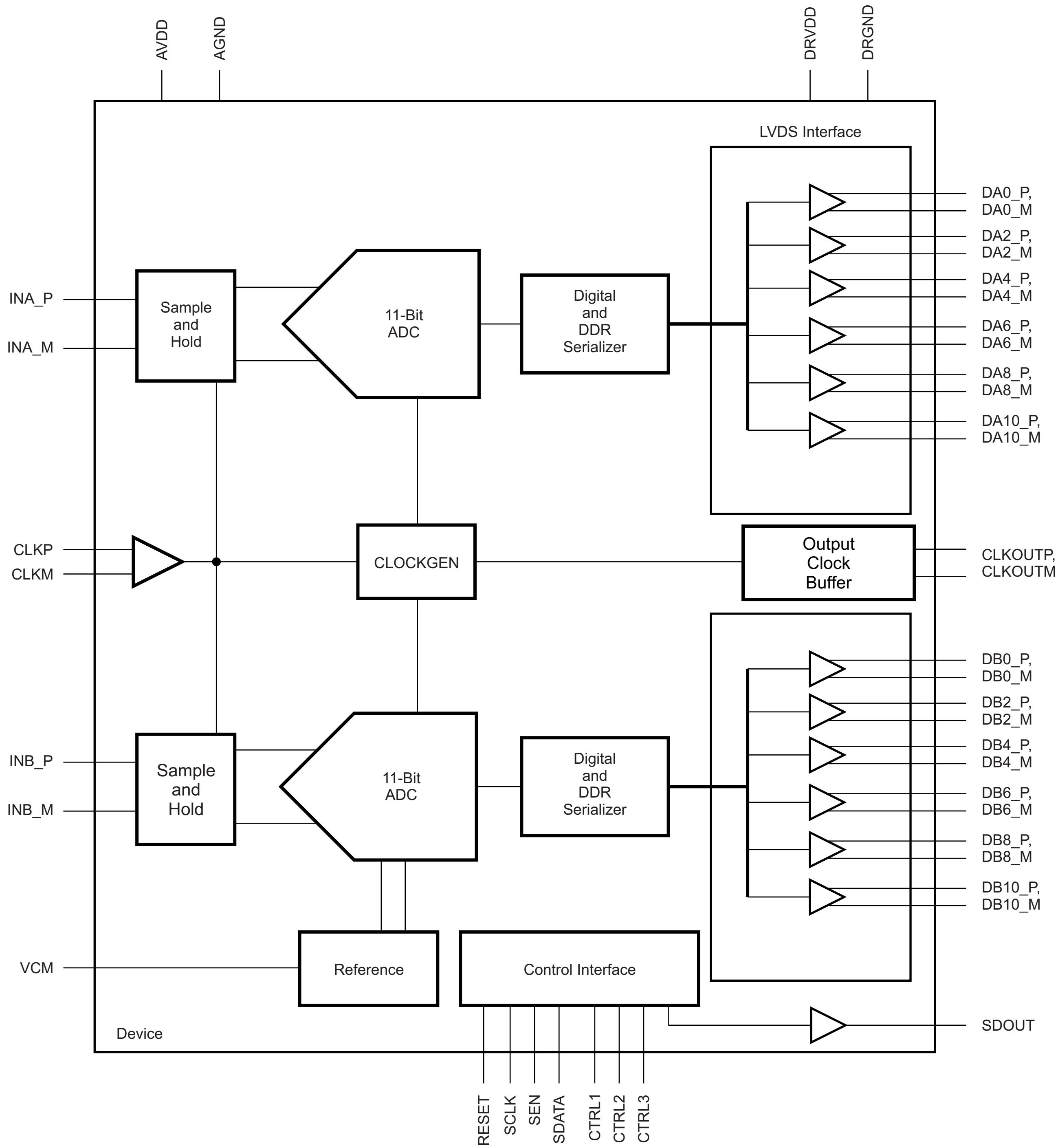


Figure 10. Block Diagram

TYPICAL CHARACTERISTICS

All plots are at T_A = +25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine-wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, internal reference mode, 0-dB gain, LVDS output interface, and 32K point FFT, unless otherwise noted.

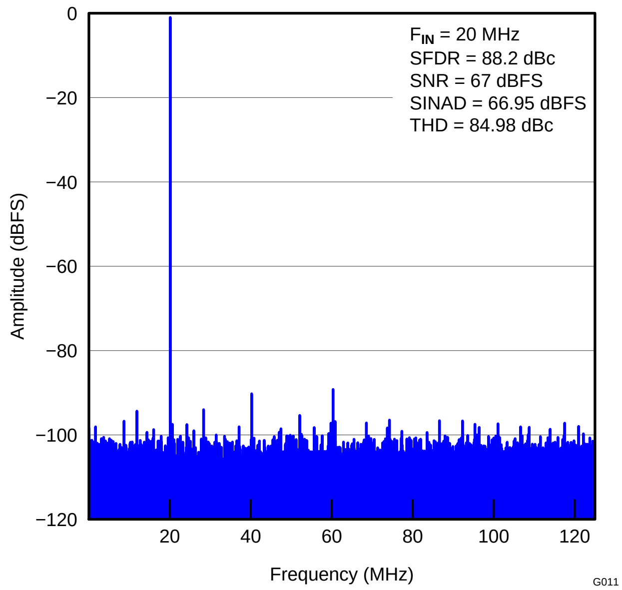


Figure 11. FFT FOR 20-MHz INPUT SIGNAL

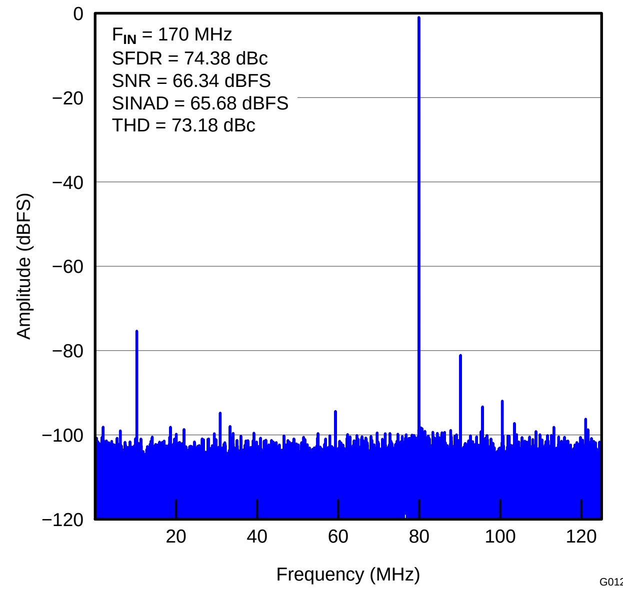


Figure 12. FFT FOR 170-MHz INPUT SIGNAL

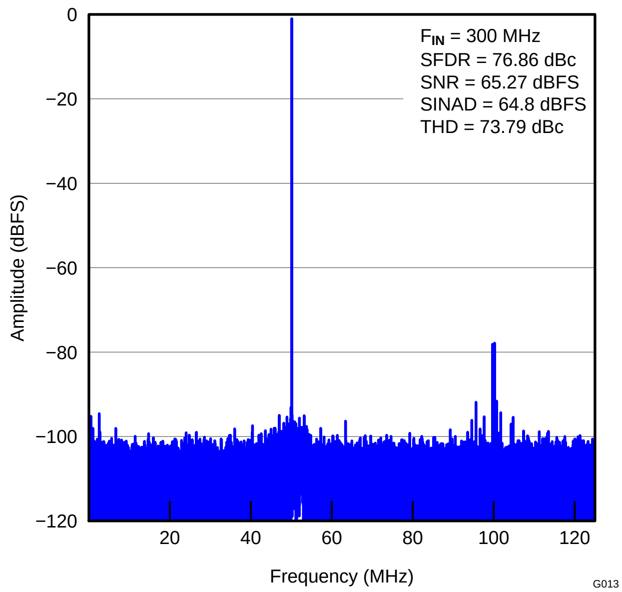


Figure 13. FFT FOR 300-MHz INPUT SIGNAL

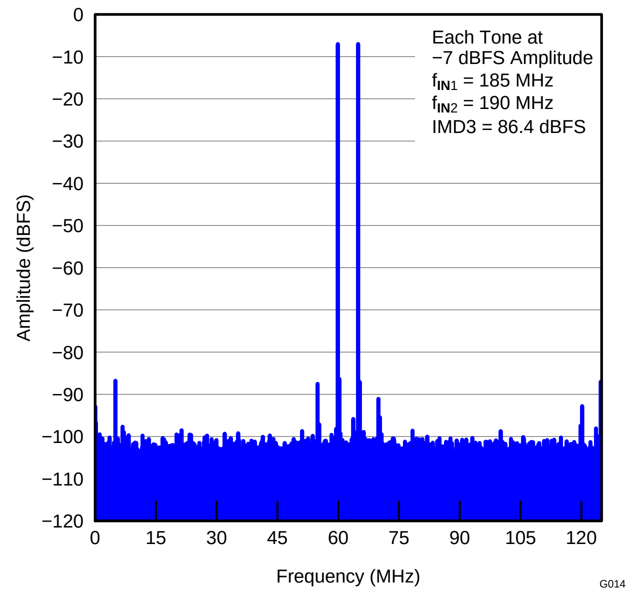


Figure 14. FFT FOR TWO-TONE INPUT SIGNAL

TYPICAL CHARACTERISTICS (continued)

All plots are at T_A = +25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine-wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, internal reference mode, 0-dB gain, LVDS output interface, and 32K point FFT, unless otherwise noted.

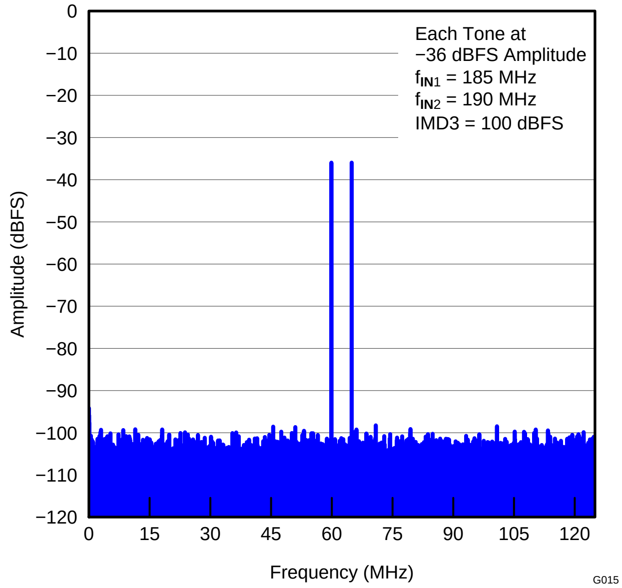


Figure 15. FFT FOR TWO-TONE INPUT SIGNAL

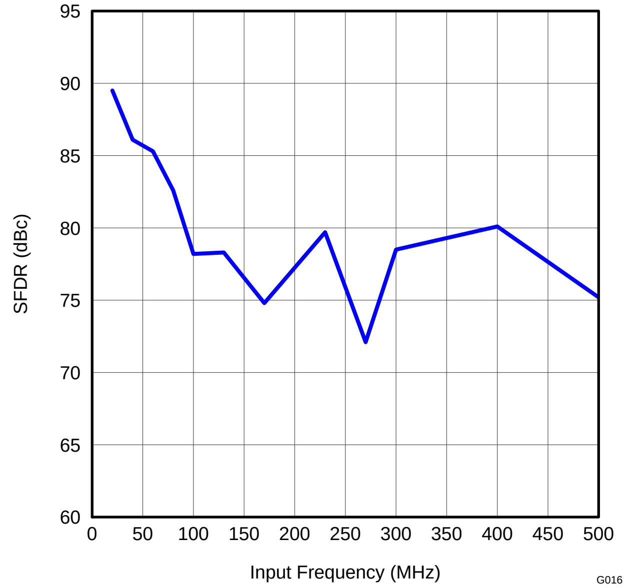


Figure 16. SFDR vs INPUT FREQUENCY

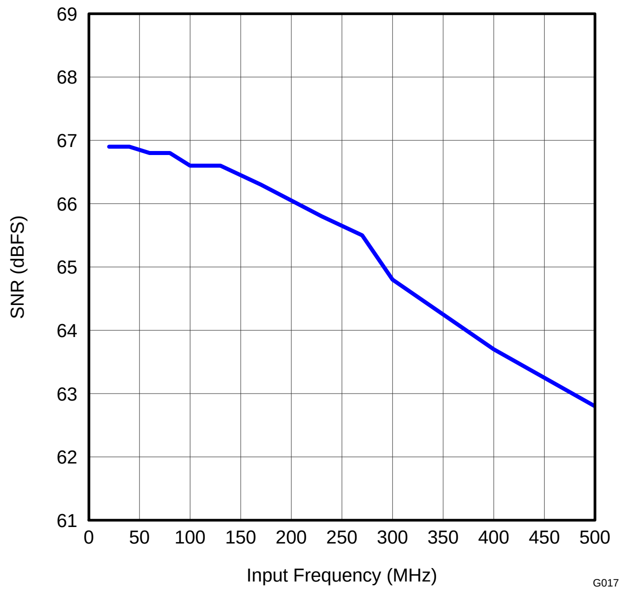


Figure 17. SNR vs INPUT FREQUENCY

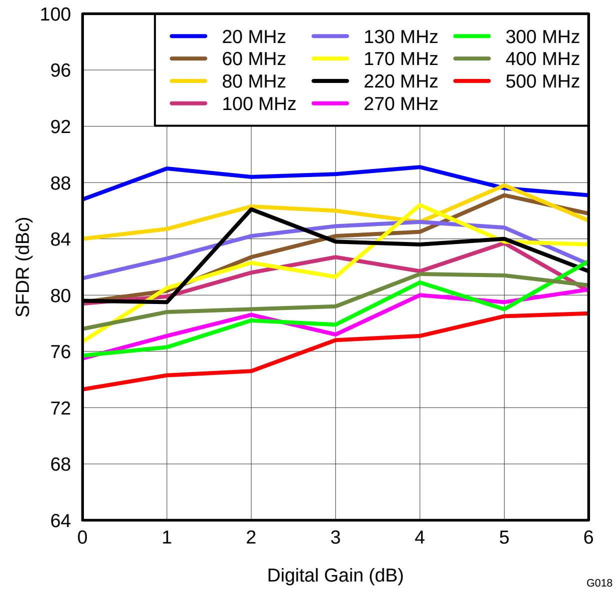


Figure 18. SFDR vs INPUT FREQUENCY ACROSS GAIN

TYPICAL CHARACTERISTICS (continued)

All plots are at T_A = +25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine-wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, internal reference mode, 0-dB gain, LVDS output interface, and 32K point FFT, unless otherwise noted.

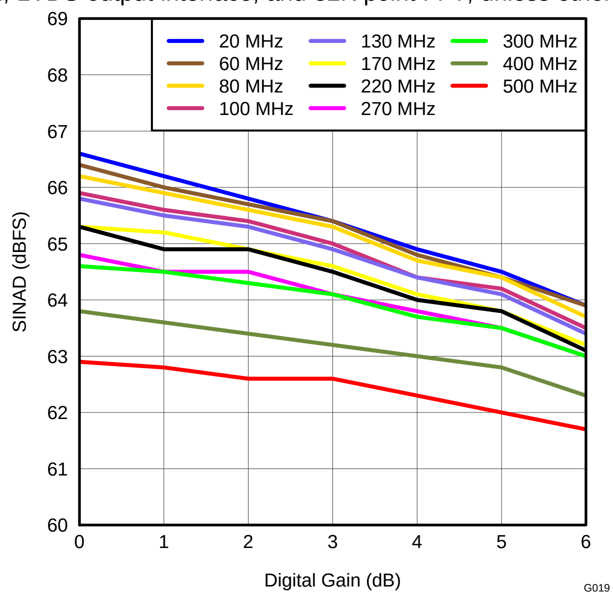


Figure 19. SINAD vs INPUT FREQUENCY ACROSS GAIN

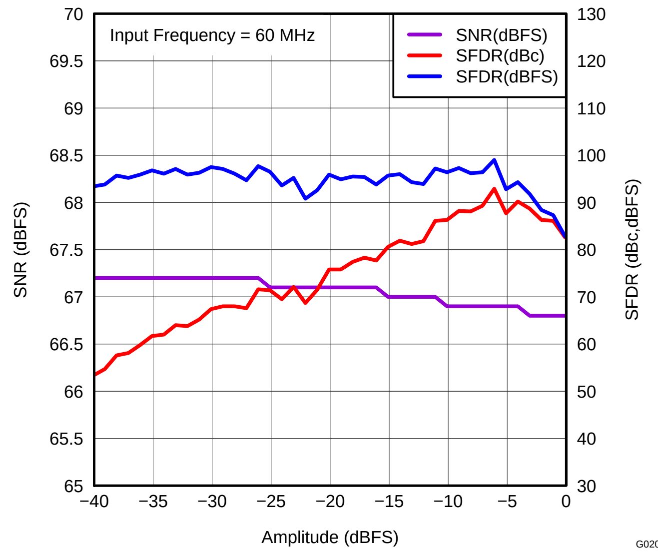


Figure 20. PERFORMANCE vs INPUT AMPLITUDE (Single Tone)

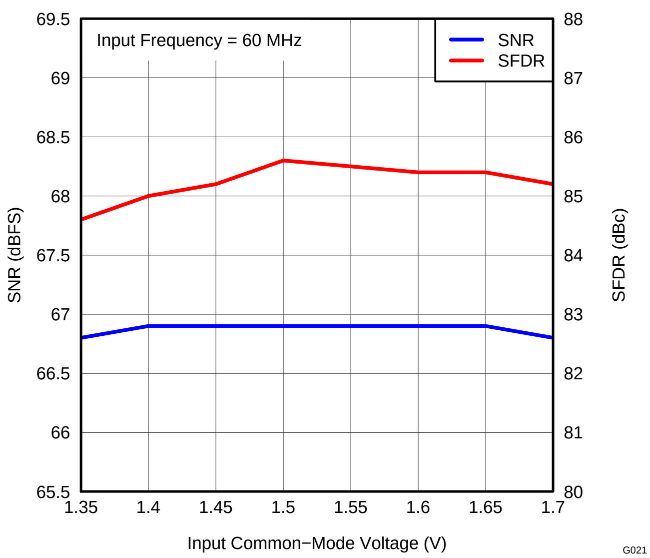


Figure 21. PERFORMANCE vs COMMON-MODE INPUT VOLTAGE

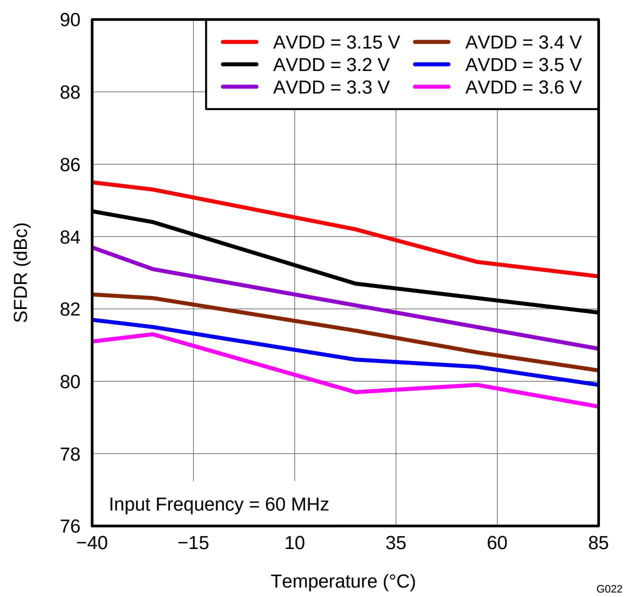


Figure 22. SFDR vs AVDD SUPPLY VOLTAGE

TYPICAL CHARACTERISTICS (continued)

All plots are at T_A = +25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine-wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, internal reference mode, 0-dB gain, LVDS output interface, and 32K point FFT, unless otherwise noted.

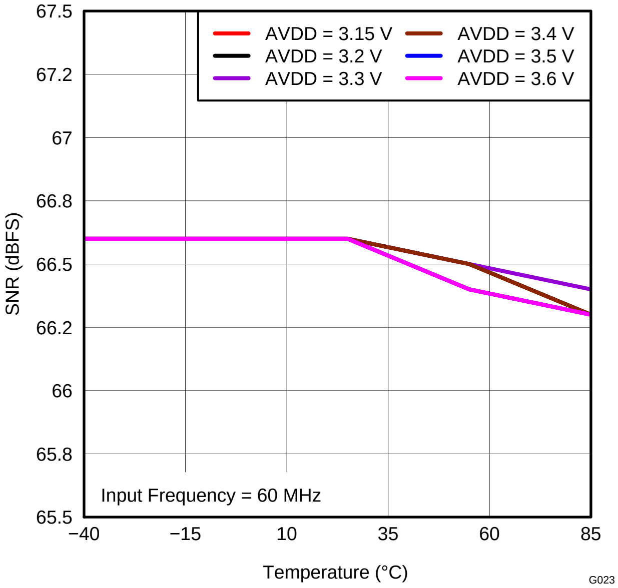


Figure 23. SNR vs AVDD SUPPLY VOLTAGE

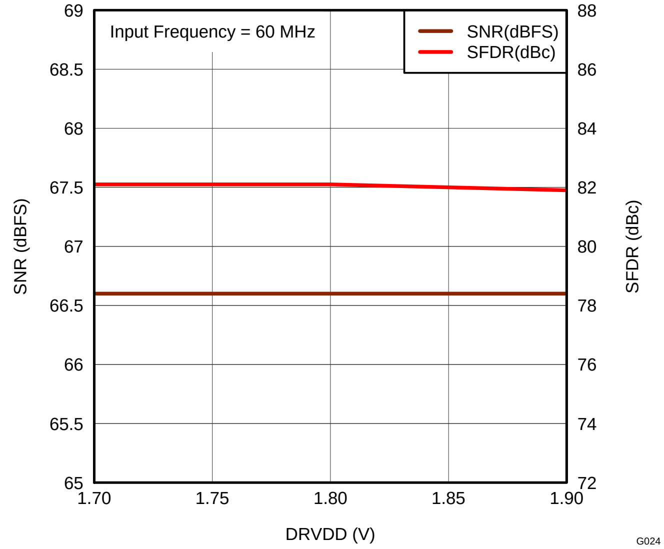


Figure 24. PERFORMANCE vs DRVDD SUPPLY VOLTAGE

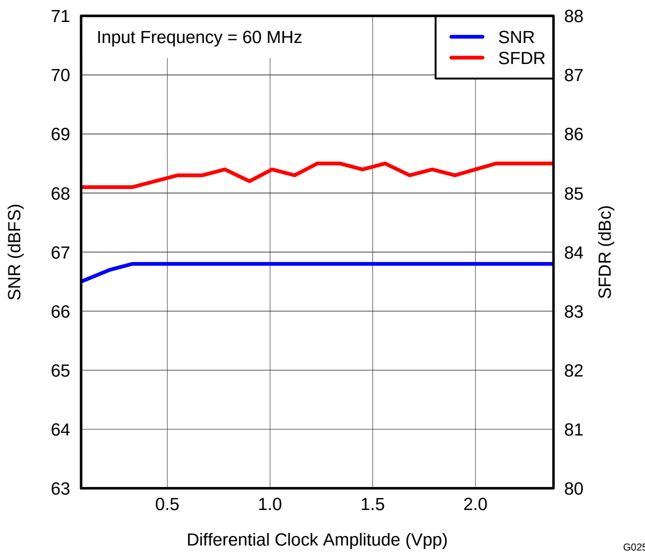


Figure 25. PERFORMANCE vs INPUT CLOCK AMPLITUDE

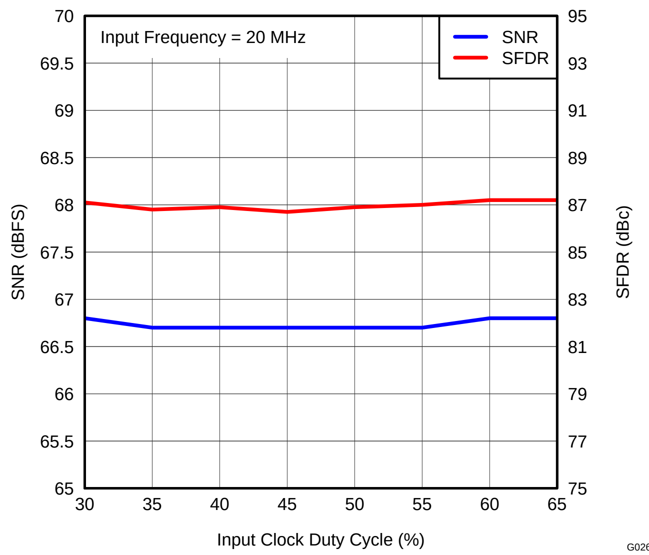


Figure 26. PERFORMANCE vs INPUT CLOCK DUTY CYCLE

TYPICAL CHARACTERISTICS (continued)

All plots are at T_A = +25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine-wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, internal reference mode, 0-dB gain, LVDS output interface, and 32K point FFT, unless otherwise noted.

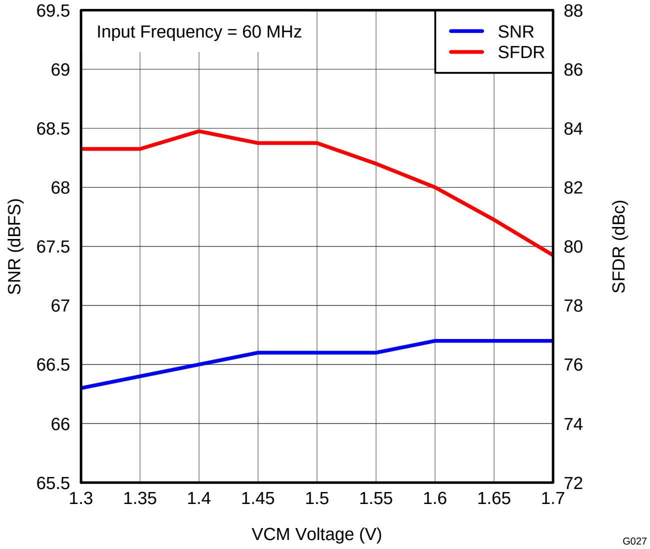


Figure 27. PERFORMANCE IN EXTERNAL REFERENCE MODE

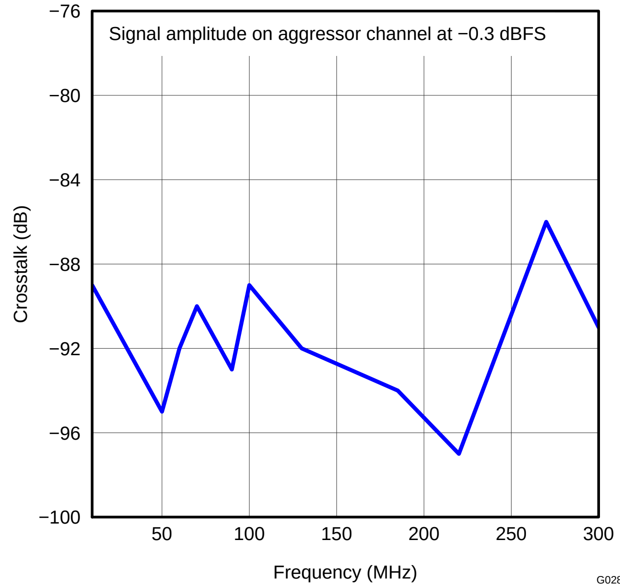


Figure 28. CROSSTALK vs FREQUENCY

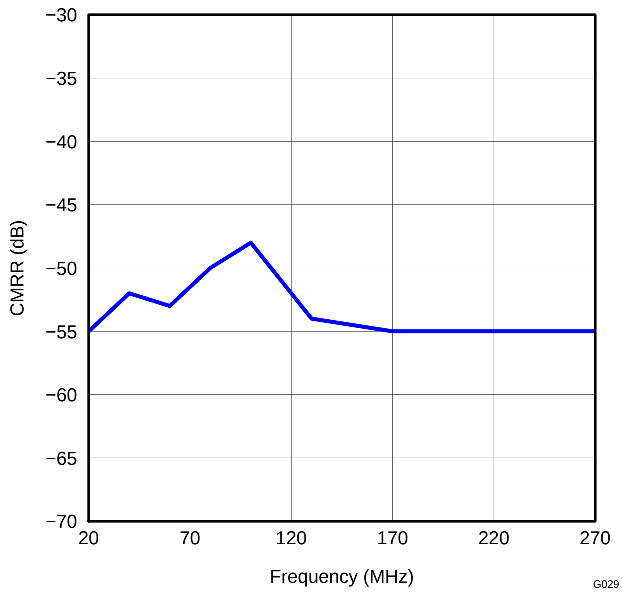


Figure 29. CMRR vs FREQUENCY

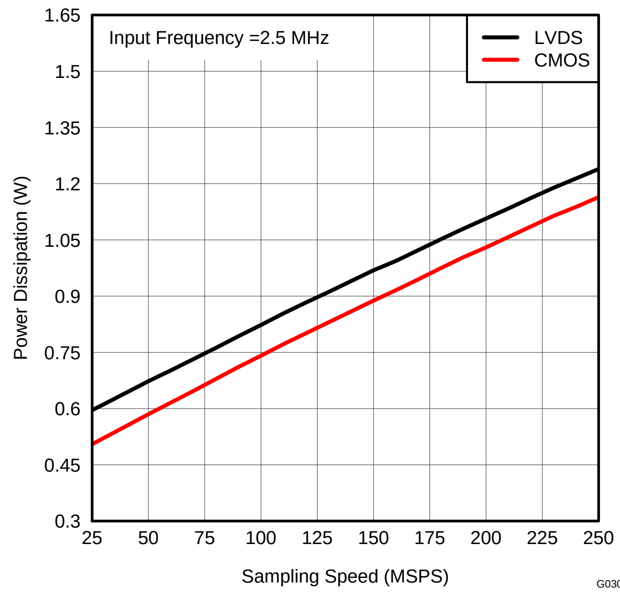


Figure 30. POWER DISSIPATION vs SAMPLING FREQUENCY

TYPICAL CHARACTERISTICS (continued)

All plots are at T_A = +25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine-wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, internal reference mode, 0-dB gain, LVDS output interface, and 32K point FFT, unless otherwise noted.

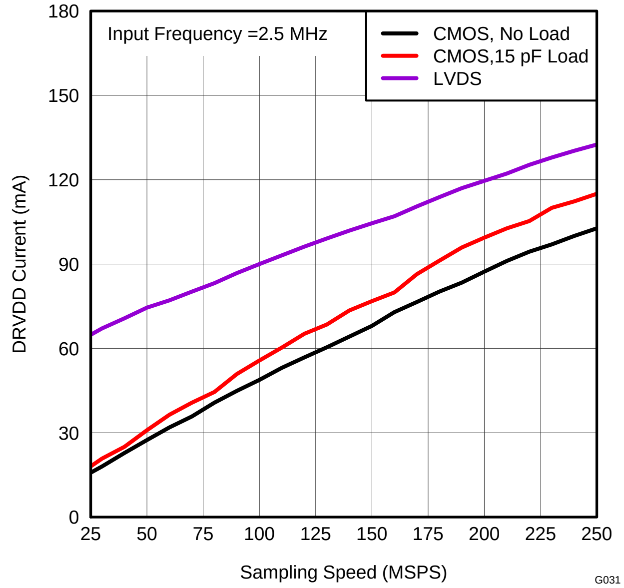


Figure 31. DRVDD CURRENT vs SAMPLING FREQUENCY

TYPICAL CHARACTERISTICS: Contour

All plots are at T_A = +25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine-wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, internal reference mode, 0-dB gain, LVDS output interface, and 32K point FFT, unless otherwise noted.

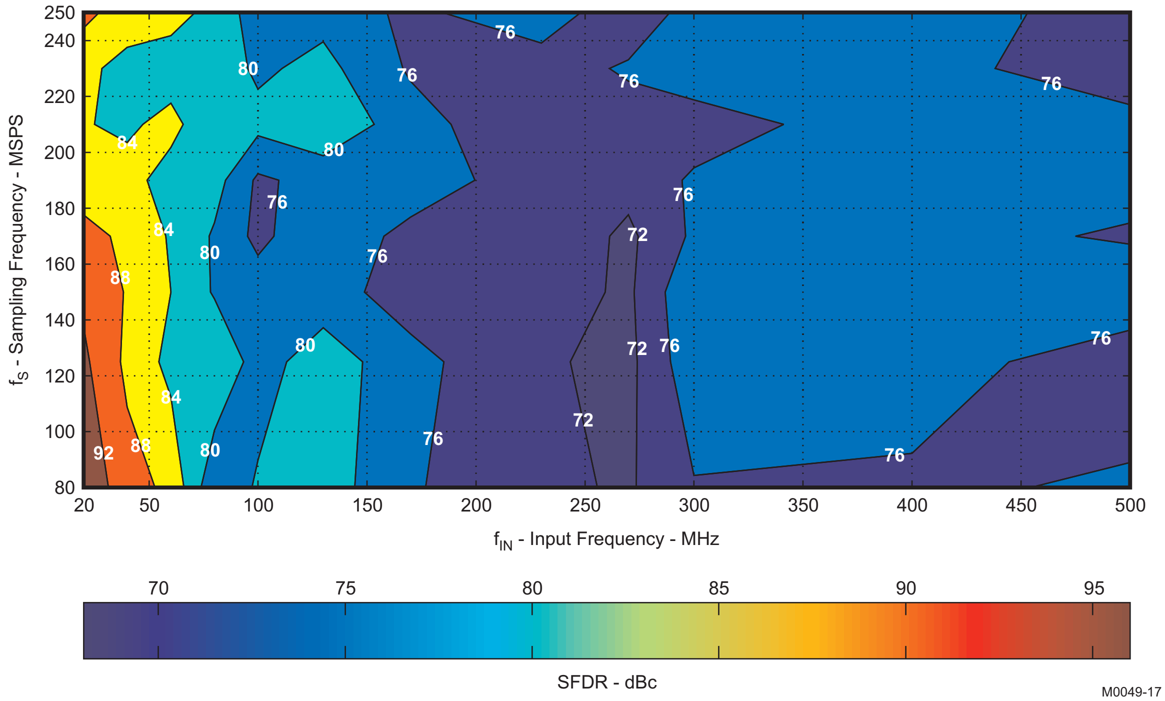


Figure 32. SFDR CONTOUR (0-dB Gain, up to 500 MHz)

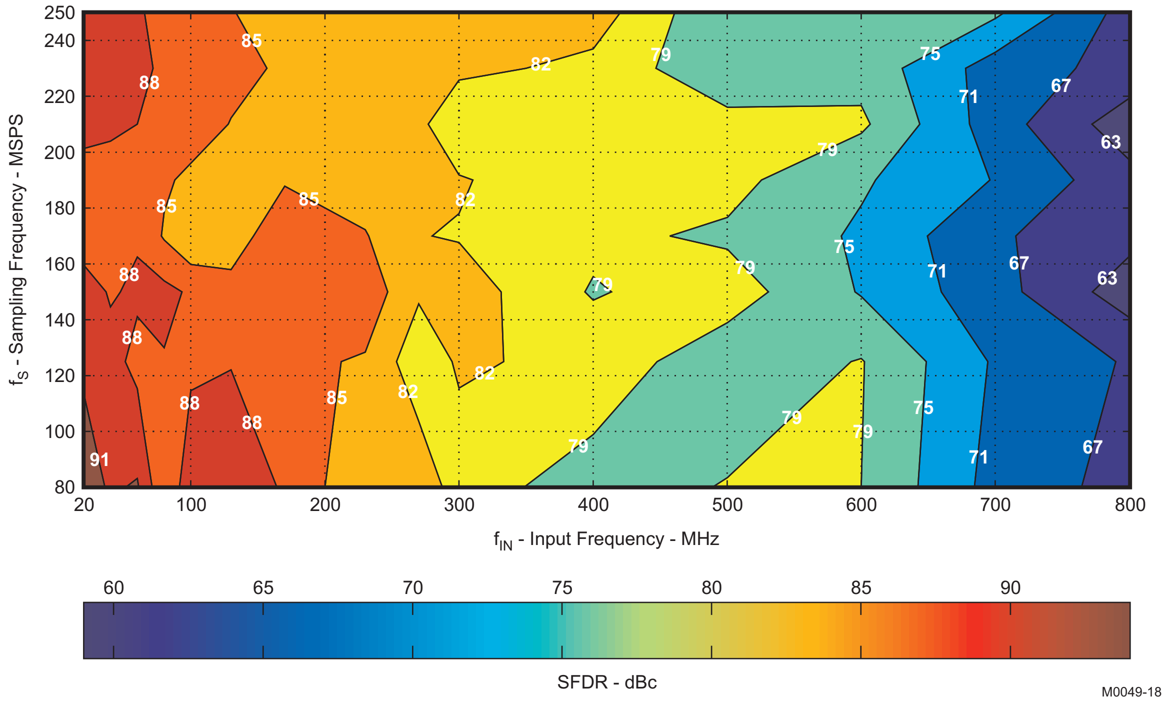


Figure 33. SFDR CONTOUR (6-dB Gain, up to 800 MHz)

TYPICAL CHARACTERISTICS: Contour (continued)

All plots are at T_A = +25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine-wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, internal reference mode, 0-dB gain, LVDS output interface, and 32K point FFT, unless otherwise noted.

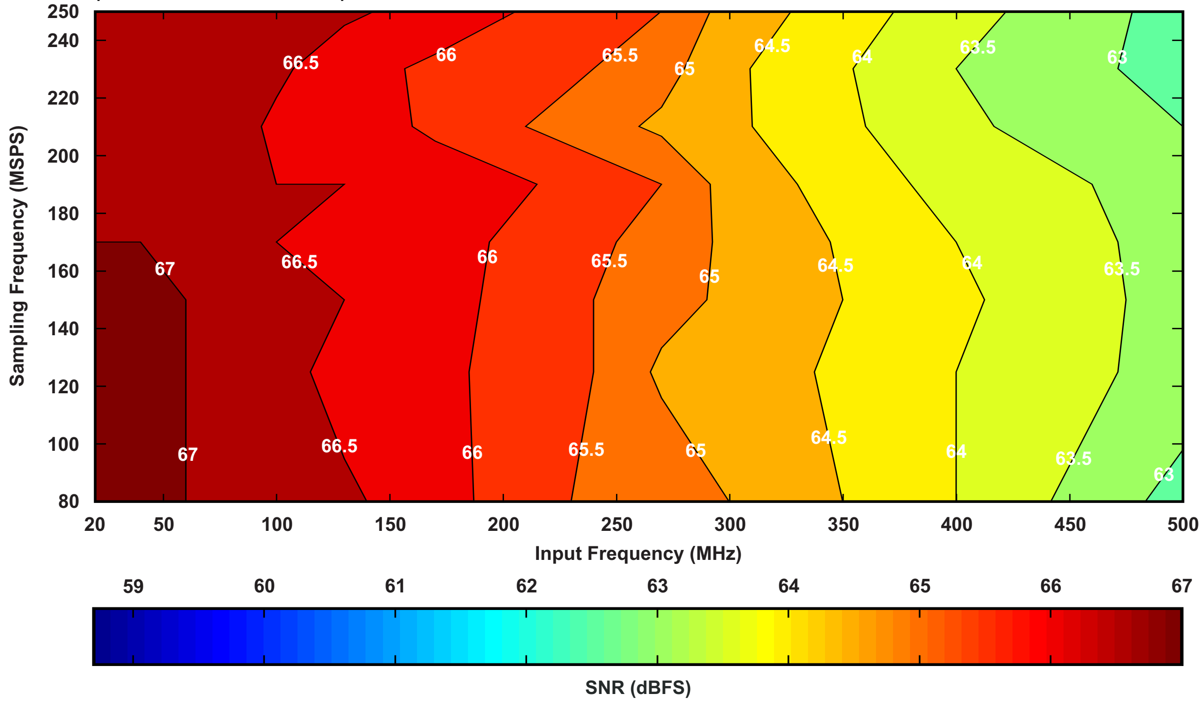


Figure 34. SNR CONTOUR
(0-dB Gain, up to 500 MHz)

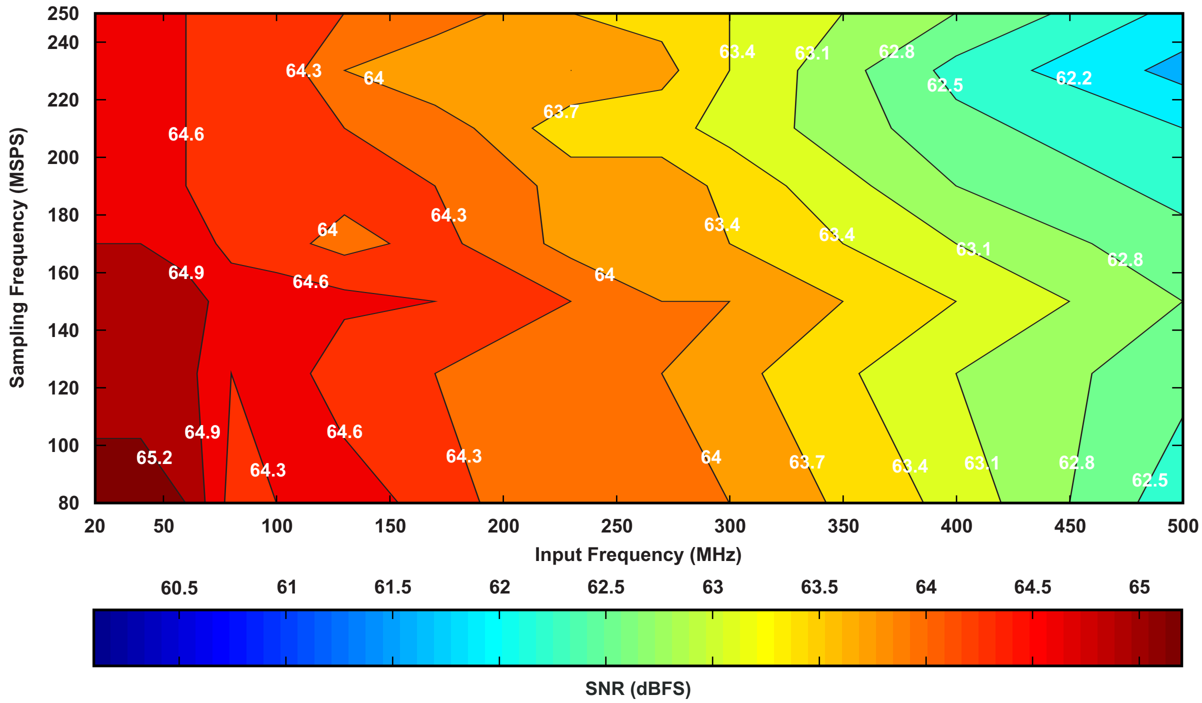


Figure 35. SNR CONTOUR
(6-dB Gain, up to 800 MHz)

DEVICE CONFIGURATION

The ADS62P19 can be configured independently using either parallel interface control or serial interface programming.

PARALLEL CONFIGURATION ONLY

To put the device in parallel configuration mode, keep RESET tied high (AVDD or DRVDD).

With RESET high, the SEN, SCLK, CTRL1, CTRL2, and CTRL3 pins can be used to directly control certain modes of the ADC. The device can be easily configured by connecting the parallel pins to the correct voltage levels (as described in Table 7 to Table 10). There is no need to apply a reset and the SDATA pin can be connected to ground.

In this mode, SEN and SCLK function as parallel interface control pins. Frequently-used functions can be controlled in this mode (such as power-down modes, internal and external reference, selection between LVDS and CMOS interface, and output data format). Table 7 lists a brief description of the modes controlled by the four parallel pins.

Table 7. Parallel Pin Definition

PIN	TYPE OF PIN	CONTROLS MODES
SCLK	Analog control pins (controlled by analog voltage levels, see Figure 36)	Internal and external reference
SEN		LVDS and CMOS interface and output data format
CTRL1	Digital control pins (controlled by digital logic levels)	Controls power-down modes
CTRL2		
CTRL3		

Table 8. SCLK Control Pin

VOLTAGE APPLIED ON SCLK	DESCRIPTION
0 +200 mV / 0 mV	Internal reference
(3 / 8) AVDD ±200 mV	External reference
(5 / 8) AVDD ±200mV	External reference
AVDD 0 mV / –200 mV	Internal reference

Table 9. SEN Control Pin

VOLTAGE APPLIED ON SEN	DESCRIPTION
0 +200 mV / 0 mV	Twos complement, DDR LVDS output
(3 / 8) AVDD ±200 mV	Offset binary, DDR LVDS output
(5 / 8) AVDD ±200 mV	Offset binary, parallel CMOS output
AVDD 0 mV / –200 mV	Twos compliment, parallel CMOS output

Table 10. CTRL1, CTRL2, and CTRL3 Pins(1)

CTRL1	CTRL2	CTRL3	DESCRIPTION
Low	Low	Low	Normal operation
Low	Low	High	Not available
Low	High	Low	Not available
Low	High	High	Not available
High	Low	Low	Global power down
High	Low	High	Channel B standby
High	High	Low	Channel A standby
High	High	High	MUX mode of operation, Channel A and B data is multiplexed and output on ***DA10 to DA0*** pins.(2)

(1) See the *POWER DOWN* section in the *Application Information*.
(2) Low-speed mode must be enabled for the multiplexed output mode (MUX mode). Therefore, MUX mode only functions with the serial interface configuration and is not supported with the parallel configuration.

SERIAL INTERFACE CONFIGURATION ONLY

To exercise this mode, the serial registers must first be reset to the default values and the RESET pin must be kept low. SEN, SDATA, and SCLK function as serial interface pins in this mode and can be used to access the internal registers of the ADC. The registers can be reset either by applying a pulse on the RESET pin or by setting the RESET bit high. The *Serial Interface* section describes the register programming and reset in more detail.

DETAILS OF PARALLEL CONFIGURATION ONLY

The functions controlled by each parallel pin are described in this section. A simple way of configuring the parallel pins is shown in Figure 36.

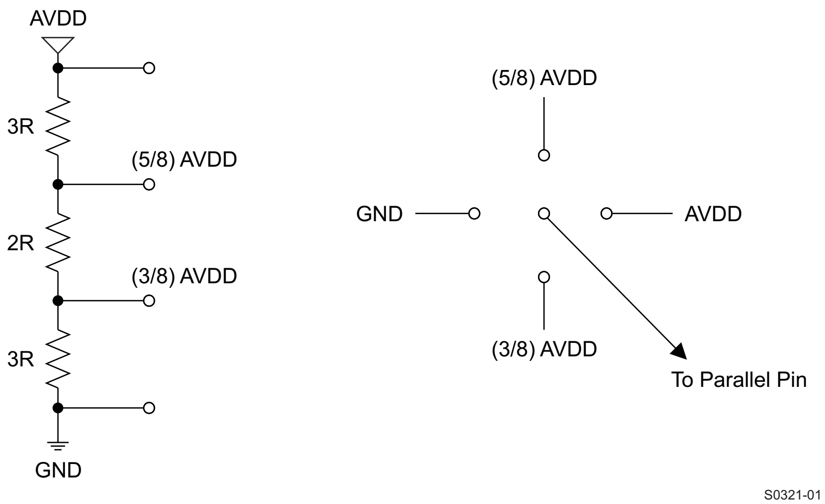


Figure 36. Simple Scheme to Configure Parallel Pins

USING BOTH SERIAL INTERFACE AND PARALLEL CONTROLS

For increased flexibility, a combination of serial interface registers and parallel pin controls (CTRL1 to CTRL3) can also be used to configure the device. To allow this flexibility, keep RESET low. The parallel interface control pins (CTRL1 to CTRL3) are available. After power-up, the device is automatically configured as per the voltage settings on these pins (see Table 6). SEN, SDATA, and SCLK function as serial interface digital pins and are used to access the ADC internal registers. The registers must first be reset to the default values either by applying a pulse on the RESET pin or by setting the RST bit to '1'. After reset, the RESET pin must be kept low. The *Serial Interface* section describes register programming and reset in more detail.

SERIAL INTERFACE

The ADC has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), and SDATA (serial interface data) pins. Serially shift bits into the device is enabled when SEN is low. SDATA serial data are latched at every SCLK falling edge when SEN is active (low). The serial data are loaded into the register every 16th SCLK falling edge when SEN is low. In case the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse.

The first eight bits form the register address and the remaining eight bits are the register data. The interface can function with SCLK frequencies from 20 MHz down to very low speeds (of a few hertz) and also with a non-50% SCLK duty cycle.

Register Initialization

After power-up, the internal registers must be initialized to the default values. This initialization can be accomplished in one of two ways:

1. Either through a hardware reset by applying a high-going pulse on the RESET pin (of widths greater than 10 ns), as shown in Figure 37,

   or

2. By applying a software reset. Using the serial interface, set the RESET bit (bit D7 in register 00h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

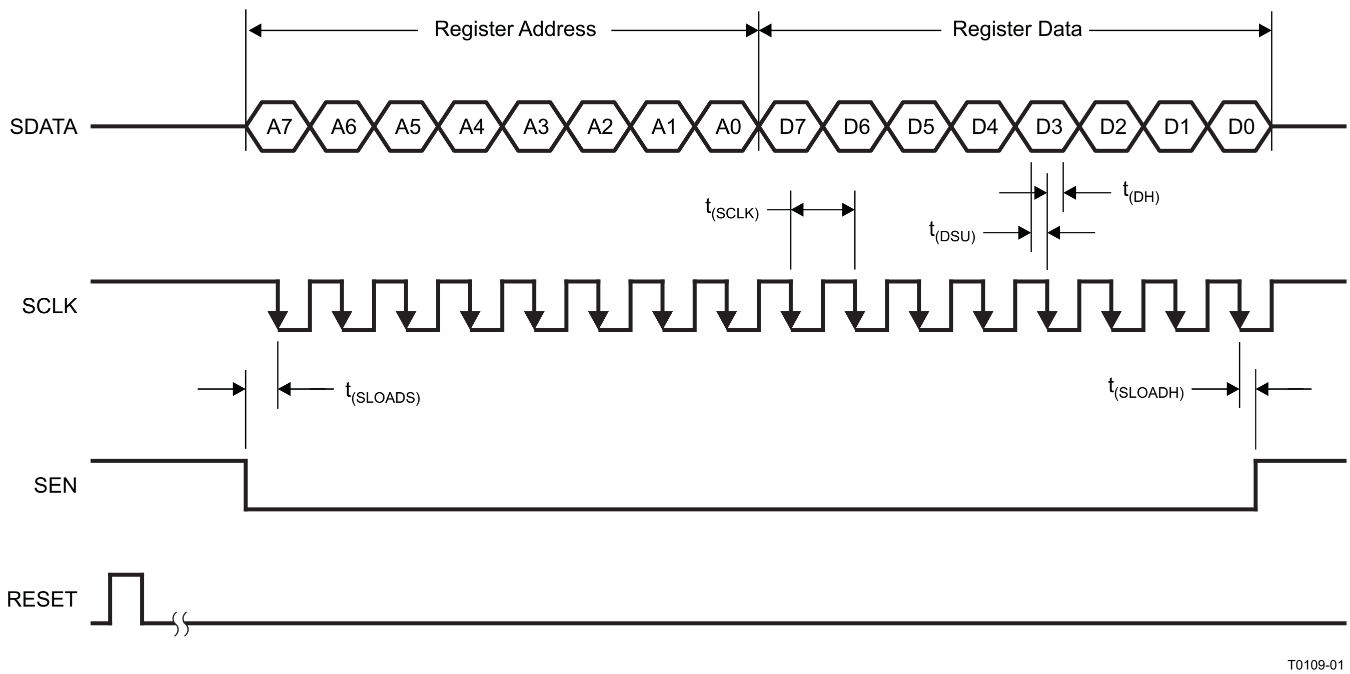


Figure 37. Serial Interface Timing

SERIAL REGISTER MAP

Table 11. Summary of Functions Supported by Serial Interface(1)

REGISTER ADDRESS	REGISTER FUNCTIONS							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
00	RESET	0	0	0	0	0	0	SERIAL READOUT
20	0	0	0	0	0	ENABLE LOW SPEED MODE	0	0
3F	0	REF	0	0	0	0	STANDBY	0
40	0	0	0	0	POWER DOWN MODES			
41	LVDS CMOS	0	0	0	0	0	0	0
44	CLKOUT EDGE CONTROL						0	0
50	0	ENABLE INDIVIDUAL CHANNEL CONTROL	0	0	0	DATA FORMAT		0
51	CUSTOM PATTERN LOW					0	0	0
52	0	0	CUSTOM PATTERN HIGH					
53	0	ENABLE OFFSET CORRECTION, CH A	0	0	0	0	0	0
55	GAIN PROGRAMMABILITY, CH A				OFFSET CORRECTION TIME CONSTANT, CH A			
57	0	FINE GAIN ADJUST, CH A						
62	0	0	0	0	0	TEST PATTERNS, CH A		
63	0	0	OFFSET PEDESTAL, CH A			0	0	0
66	0	ENABLE OFFSET CORRECTION, CH B	0	0	0	0	0	0
68	GAIN PROGRAMMABILITY, CH B				OFFSET CORRECTION TIME CONSTANT, CH B			
6A	0	FINE GAIN ADJUST, CH B						
75	0	0	0	0	0	TEST PATTERNS, CH B		
76	0	0	OFFSET PEDESTAL, CH B			0	0	0

(1) Multiple functions in a register can be programmed in a single write operation.

DESCRIPTION OF SERIAL REGISTERS

Table 12. Register 00h

D7	D6	D5	D4	D3	D2	D1	D0
RESET	0	0	0	0	0	0	SERIAL READOUT

Bit D7 **RESET: Software reset**

1 = Software reset applied; resets all internal registers and self-clears to '0'.

Bits D[6:1] **Always write '0'**

Bit D0 **SERIAL READOUT**

0 = Serial readout disabled. SDOUT is forced low by the device (and not put in high-impedance state).

1 = Serial readout enabled. SDOUT functions as a serial data readout.

Table 13. Register 20h

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	ENABLE LOW-SPEED MODE	0	0

Bits D[7:3] **Always write '0'**

Bit D2 **ENABLE LOW-SPEED MODE**

0 = Low-speed mode disabled; use for sampling frequencies > 80 MSPS

1 = Enable low-speed mode for sampling frequencies ≤ 80 MSPS

Bits D[1:0] **Always write '0'**

Table 14. Register 3Fh

D7	D6	D5	D4	D3	D2	D1	D0
0	REF		0	0	0	STANDBY	0

Bit D7 **Always write '0'**

Bits D[6:5] **REF: Internal or external reference selection**

00 = Internal reference enabled

01 = Do not use

10 = Do not use

11 = External reference enabled

Bits D[4:2] **Always write '0'**

Bit D1 **STANDBY**

0 = Normal operation

1 = Both ADC channels are put in standby. Internal references and output buffers are active. This architecture results in a quick wake-up time from standby.

Bit D0 **Always write '0'**

Table 15. Register 40h

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	POWER DOWN MODES			

Bits D[3:0] **POWER DOWN MODES**

0000 = The CTRL1, CTRL2, and CTRL3 pins determine the power-down modes.

1000 = Normal operation

1001 = Output buffer disabled for channel B

1010 = Output buffer disabled for channel A

1011 = Output buffer disabled for channel A and B

1100 = Global power-down

1101 = Channel B standby

1110 = Channel A standby

1111 = Multiplexed mode (MUX), only with CMOS interface.
Channel A and B data are multiplexed and output on ***the DA10 to DA0*** pins. Refer to the *Multiplexed Output Mode* section in the *Application Information* for additional information.

Table 16. Register 41h

D7	D6	D5	D4	D3	D2	D1	D0
LVDS CMOS	0	0	0	0	0	0	0

Bit D7 **LVDS CMOS: Output interface**

0 = Parallel CMOS interface

1 = DDR LVDS interface

Bits D[6:0] **Always write '0'**

Table 17. Register 44h

D7	D6	D5	D4	D3	D2	D1	D0
CLKOUT EDGE CONTROL						0	0

Bits D[7:2] **CLKOUT EDGE CONTROL: Output clock edge control**

These bits control the output clock edge. The output clock rising and falling edge position settings are different for the LVDS and CMOS interfaces.

LVDS INTERFACE

Bits D[7:5] **CLKOUT POSN: Output clock rising edge position**[1]

000 = Default output clock position (refer to the Timing Requirements table)

100 = Default output clock position (refer to the Timing Requirements table)

101 = Falling edge shifted (delayed) by + (4 / 26) × t_S[2]

110 = Falling edge shifted (advanced) by – (7 / 26) × t_S

111 = Falling edge shifted (advanced) by – (4 / 26) × t_S

Bits D[4:2] **CLKOUT POSN: Output clock falling edge position**[1]

000 = Default output clock position (refer to the Timing Requirements table)

100 = Default output clock position (refer to the Timing Requirements table)

101 = Rising edge shifted (delayed) by + (4 / 26) × t_S

110 = Rising edge shifted (advanced) by – (7 / 26) × t_S

111 = Rising edge shifted (advanced) by – (4 / 26) × t_S

CMOS INTERFACE

Bits D[7:5] **CLKOUT POSN: Output clock rising edge position**[1]

000 = Default output clock position (refer to the Timing Requirements table)

100 = Default output clock position (refer to the Timing Requirements table)

101 = Rising edge shifted (delayed) by + (4 / 26) × t_S

110 = Rising edge shifted (advanced) by – (7 / 26) × t_S

111 = Rising edge shifted (advanced) by – (4 / 26) × t_S

Bits D[4:2] **CLKOUT POSN: Output clock falling edge position**[1]

000 = Default output clock position (refer to the Timing Requirements table)

100 = Default output clock position (refer to the Timing Requirements table)

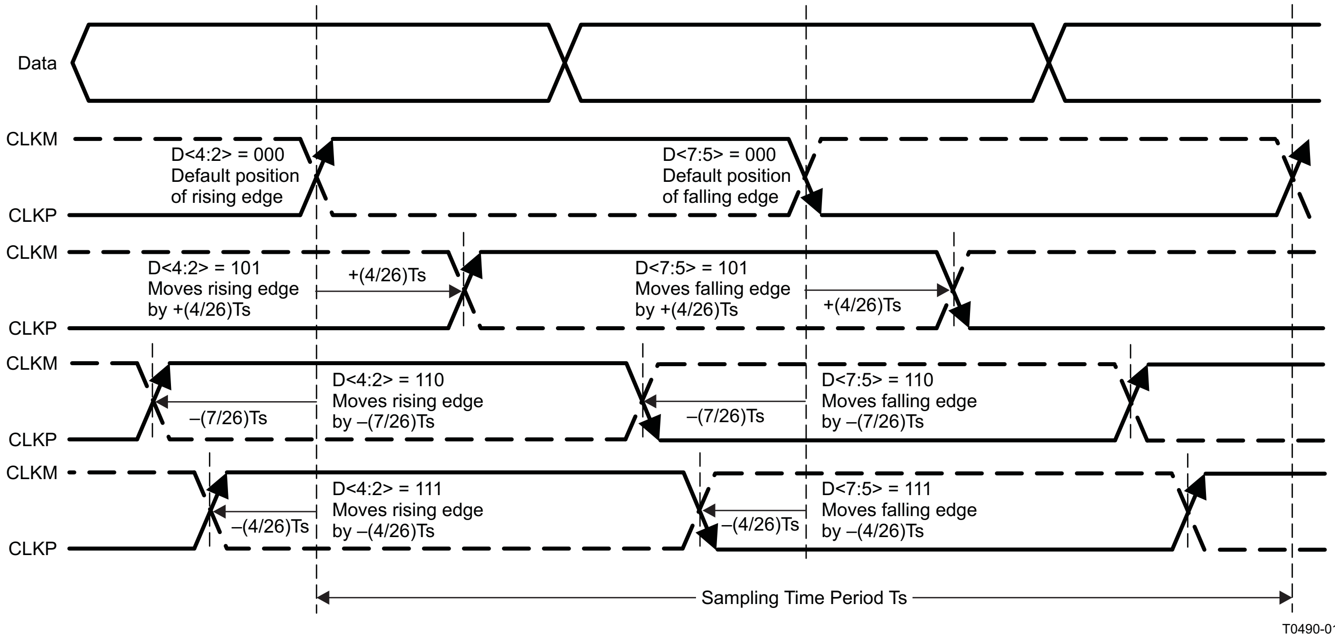
101 = Falling edge shifted (delayed) by + (4 / 26) × t_S

110 = Falling edge shifted (advanced) by – (7 / 26) × t_S

111 = Falling edge shifted (advanced) by – (4 / 26) × t_S

Bits D[1:0] **Always write '0'. These bit settings are the same for both LVDS and CMOS interfaces.**

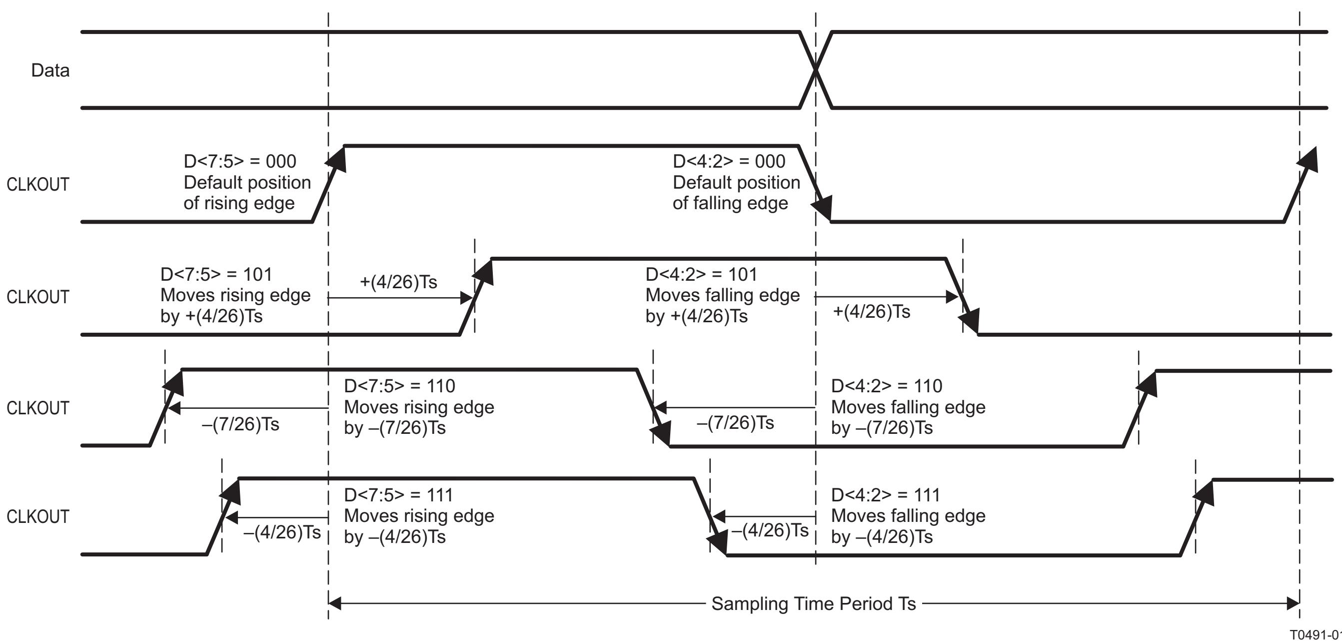
(1) Keep the same duty cycle, move both edges by the same amount (for instance, write both D[4:2] and D[7:5] to be the same value).
(2) t_S = 1 / sampling frequency.



(1) Keep the same duty cycle, move both edges by same amount (for instance, write both D[4:2] and D[7:5] to be the same value).

(2) Refer to the Timing Requirements table for default output clock position.

Figure 38. LVDS Interface Output Clock Edge Movement (Serial Register 0x44)



(1) Keep the same duty cycle, move both edges by same amount (for instance, write both D[4:2] and D[7:5] to be the same value).

(2) Refer to the Timing Requirements table for default output clock position.

Figure 39. CMOS Interface Output Clock Edge Movement (Serial Register 44h)

Table 18. Register 50h

D7	D6	D5	D4	D3	D2	D1	D0
0	ENABLE INDIVIDUAL CHANNEL CONTROL	0	0	0	DATA FORMAT		0

Bit D7 **Always write '0'**

Bit D6 **ENABLE INDIVIDUAL CHANNEL CONTROL**

0 = Common control: both channels use common control settings for test patterns, offset correction, fine gain, and gain correction. These settings can be specified in a single set of registers.

1 = Independent control: both channels can be programmed with independent control settings for test patterns, and offset correction. Separate registers are available for each channel.

Bits D[2:1] **DATA FORMAT: Twos complement or offset binary**

10 = Twos complement

11 = Offset binary

Bit D0 **Always write '0'**

Table 19. Register 51h

D7	D6	D5	D4	D3	D2	D1	D0
CUSTOM PATTERN LOW					0	0	0

Bits D[7:3] **CUSTOM PATTERN LOW**

Five lower custom pattern bits are available at the output instead of ADC data.

Bits D[2:0] **Always write '0'**

Table 20. Register 52h

D7	D6	D5	D4	D3	D2	D1	D0
0	0	CUSTOM PATTERN HIGH					

Bits D[7:6] **Always write '0'**

Bits D[5:0] **CUSTOM PATTERN HIGH**

Six upper custom pattern bits are available at the output instead of ADC data.

Use this mode with the TEST PATTERNS register bits (register 62h).

Table 21. Register 53h

D7	D6	D5	D4	D3	D2	D1	D0
0	ENABLE OFFSET CORRECTION, CH A	0	0	0	0	0	0

Bit D7 **Always write '0'**

Bit D6 **ENABLE OFFSET CORRECTION: Common, channel A, offset correction enable**

Offset correction enable control for both channels (with common control) or for channel A only (with independent control).

0 = Offset correction disabled

1 = Offset correction enabled

Bits D[5:0] **Always write '0'**

Table 22. Register 55h

D7	D6	D5	D4	D3	D2	D1	D0
GAIN PROGRAMMABILITY, CH A				OFFSET CORRECTION TIME CONSTANT, CH A			

Bits D[7:4] **GAIN PROGRAMMABILITY, CH A: Common, channel A**

Gain control for both channels (with common control) or for channel A only (with independent control).

0000 = 0-dB gain (default after reset)

0001 = 0.5-dB gain

0010 = 1.0-dB gain

0011 = 1.5-dB gain

0100 = 2.0-dB gain

0101 = 2.5-dB gain

0110 = 3.0-dB gain

0111 = 3.5-dB gain

1000 = 4.0-dB gain

1001 = 4.5-dB gain

1010 = 5.0-dB gain

1011 = 5.5-dB gain

1100 = 6.0-dB gain

Bits D[3:0] **OFFSET CORRECTION TIME CONSTANT, CH A: Common, channel A, offset correction time constant**

Correction loop time constant in number of clock cycles.
Applies to both channels (with common control) or for channel A only (with independent control).

0000 = 256 k

0001 = 512 k

0010 = 1 M

0011 = 2 M

0100 = 4 M

0101 = 8 M

0110 = 16 M

0111 = 32 M

1000 = 64 M

1001 = 128 M

1010 = 256 M

1011 = 512 M

Table 23. Register 57h

D7	D6	D5	D4	D3	D2	D1	D0
0	FINE GAIN ADJUST, CH A						

Bit D7 **Always write '0'**

Bits D[6:0] **FINE GAIN ADJUST, CH A: Common, channel A (+0.001 dB to +0.134 dB, in 128 steps)**

Using the FINE GAIN ADJUST register bits, the channel gain can be trimmed in fine steps. The trim is only additive, and has 128 steps and a range of 0.134 dB. The relationship between the FINE GAIN ADJUST bits and the trimmed channel gain is:

Δ channel gain = 20 × log10[1 + (FINE GAIN ADJUST / 1024)]

Note that the total device gain = ADC gain + Δ channel gain. ADC gain is determined by the GAIN PROGRAMMABILITY register bits.

Table 24. Register 62h

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	TEST PATTERNS, CH A		

Bits D[2:0] **TEST PATTERNS, CH A: Test Patterns to verify data capture**

Applies to both channels (with common control) or for channel A only with independent control. Note that in LVDS mode, the test pattens come out as 12-bit data with the LSB (the dummy bit) coming out at the output clock rising edge. The analog path, however, gives out only 11-bit data where the dummy bit is always '0'. While capturing, the dummy bit can always be ignored and the remaining 11 bits should be processed.

000 = Normal operation

001 = Outputs all 0s

010 = Outputs all 1s

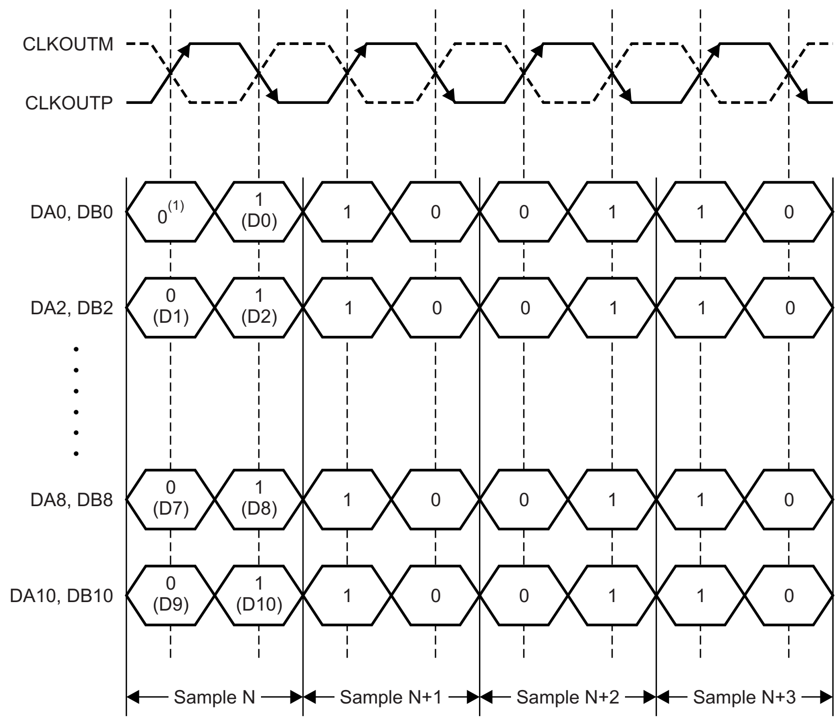
011 = Outputs toggle pattern; see Figure 40 and Figure 41 for LVDS and CMOS mode test pattern timing diagrams. Output data D[10:0] alternates between *01010101010* and *10101010101* every clock cycle.

100 = Outputs digital ramp
Output data increments by one LSB (11-bit) every eighth clock cycle from code 0 to code 2047.

101 = Outputs custom pattern (use registers 51h and 52h for setting the custom pattern); see Figure 43 for an example of a custom pattern.

110 = Unused

111 = Unused

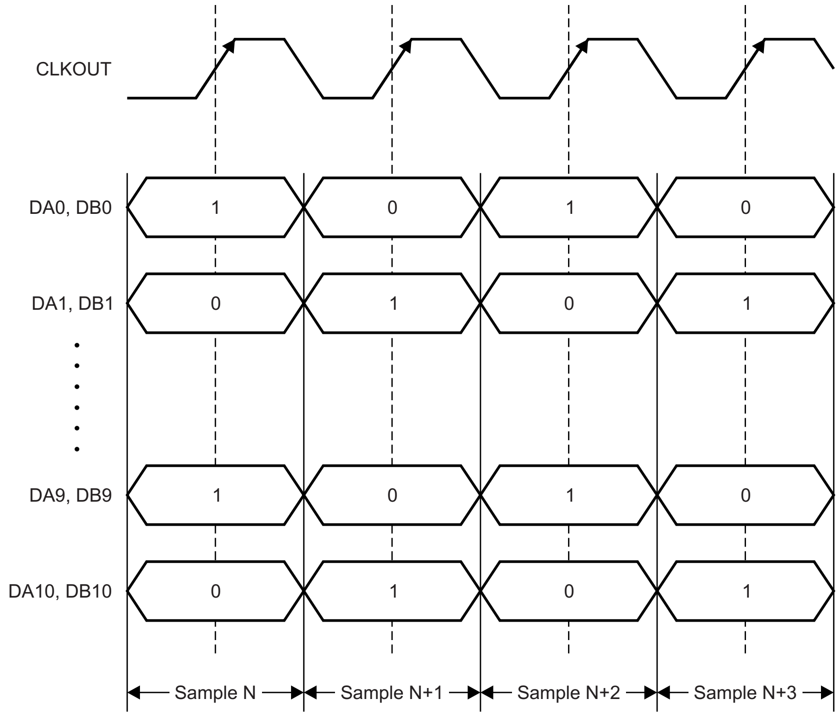


(1) This bit is the dummy bit.

NOTE: Even bits output at the CLKOUTP rising edge and odd bits output at the CLKOUTP falling edge.

NOTE: Output toggles at half the sampling rate (f_S / 2) in this test mode.

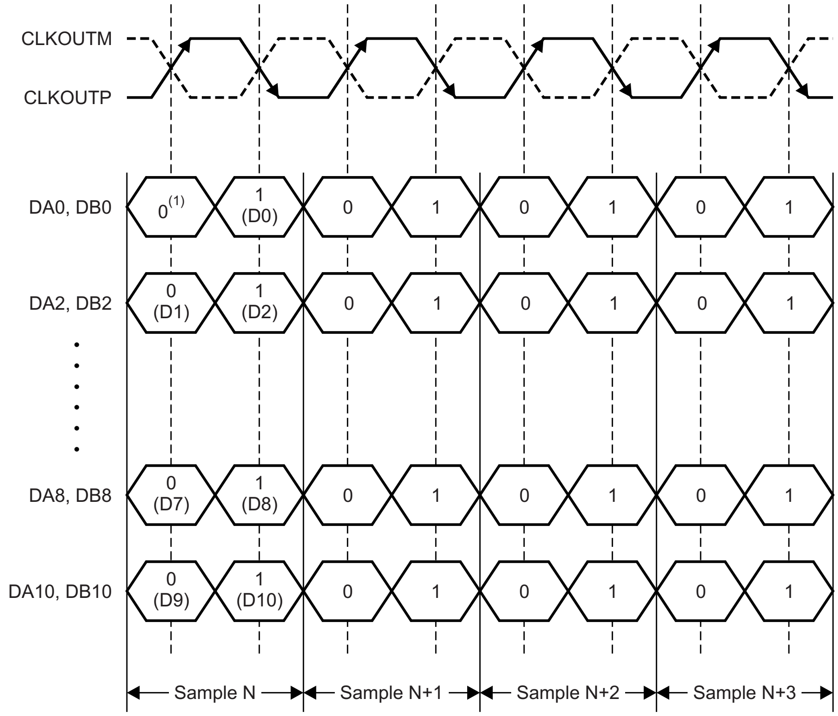
Figure 40. Output Toggle Pattern (Serial Register 62h, D[2:0] = 011) in LVDS Mode



NOTE: Output toggles at half the sampling rate (f_S / 2) in this test mode.

Figure 41. Output Toggle Pattern (Serial Register 62h, D[2:0] = 011) in CMOS Mode

Figure 42. Example: Register 51h = A1h and Register 52h = 2Ah to Toggle Output at f_S



(1) This bit is the dummy bit.

NOTE: Even bits output at the CLKOUTP rising edge, and odd bits output at the CLKOUTP falling edge.

NOTE: Output toggles at the sampling rate (f_S) in this test mode.

Figure 43. Output Custom Pattern (Serial Register 62h, D[2:0] = 101) in LVDS Mode

Table 25. Register 63h

D7	D6	D5	D4	D3	D2	D1	D0
0	0	OFFSET PEDESTAL, CH A			0	0	0

Bits D[7:6] **Always write '0'**

Bits D[5:3] **OFFSET PEDESTAL, CH A: Common, channel A**

When the offset correction is enabled, the final converged value (after the offset is corrected) is the ideal ADC mid-code value of 1024. A pedestal can be added to the final converged value by programming these bits. Thus, the final converged value is = ideal mid-code + PEDESTAL.
See the *Offset Correction* section in the *Application Information*.

Applies to both channels (with common control) or for channel A only (with independent control).

011 = PEDESTAL is 3 LSB

010 = PEDESTAL is 2 LSB

001 = PEDESTAL is 1 LSB

000 = PEDESTAL is 0 LSB

111 = PEDESTAL is –1 LSB

110 = PEDESTAL is –2 LSB

101 = PEDESTAL is –3 LSB

100 = PEDESTAL is –4 LSB

Bits D[2:0] **Always write '0'**

Table 26. Register 66h

D7	D6	D5	D4	D3	D2	D1	D0
0	ENABLE OFFSET CORRECTION, CH B	0	0	0	0	0	0

Bit D7 **Always write '0'**

Bit D6 **ENABLE OFFSET CORRECTION, CH B: Offset correction enable**

Offset correction enable control for channel B (only with independent control).

0 = Offset correction disabled

1 = Offset correction enabled

Bits D[5:0] **Always write '0'**

Table 27. Register 68h

D7	D6	D5	D4	D3	D2	D1	D0
GAIN PROGRAMMABILITY, CH B				OFFSET CORRECTION TIME CONSTANT, CH B			

Bits D[7:4] **GAIN PROGRAMMABILITY, CH B: Gain programmability to 0.5-dB steps**

Applies to channel B (only with independent control).

0000 = 0-dB gain (default after reset)

0001 = 0.5-dB gain

0010 = 1.0-dB gain

0011 = 1.5-dB gain

0100 = 2.0-dB gain

0101 = 2.5-dB gain

0110 = 3.0-dB gain

0111 = 3.5-dB gain

1000 = 4.0-dB gain

1001 = 4.5-dB gain

1010 = 5.0-dB gain

1011 = 5.5-dB gain

1100 = 6.0-dB gain

Bits D[3:0] **OFFSET CORRECTION TIME CONSTANT, CH B: Correction loop time constant in number of clock cycles.**

Applies to channel B (only with independent control)

0000 = 256 k

0001 = 512 k

0010 = 1 M

0011 = 2 M

0100 = 4 M

0101 = 8 M

0110 = 16 M

0111 = 32 M

1000 = 64 M

1001 = 128 M

1010 = 256 M

1011 = 512 M

Table 28. Register 6Ah

D7	D6	D5	D4	D3	D2	D1	D0
FINE GAIN ADJUST, CH B							

Bits D[7:0] **FINE GAIN ADJUST, CH B: +0.001 dB to +0.134 dB, in 128 steps**

Using the FINE GAIN ADJUST register bits, the channel gain can be trimmed in fine steps. The trim is only additive, and has 128 steps and a range of 0.134 dB. The relationship between the FINE GAIN ADJUST bits and the trimmed channel gain is:

Δ channel gain = 20 × log10[1 + (FINE GAIN ADJUST / 1024)]

Note that the total device gain = ADC gain + Δ channel gain. The ADC gain is determined by the GAIN PROGRAMMABILITY register bits.

Table 29. Register 75h

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	TEST PATTERNS, CH B		

Bits D[7:3] **Always write '0'**

Bits D[2:0] **TEST PATTERNS, CH B: Test patterns to verify data capture**

Applies to channel B only with independent control. Note that in LVDS mode, the test pattens come out as 12-bit data with the LSB (the dummy bit) coming out at the output clock rising edge. The analog path, however, gives out only 11-bit data where the dummy bit is always '0'. While capturing, the dummy bit can always be ignored and the remaining 11 bits should be processed.

000 = Normal operation

001 = Outputs all 0s

010 = Outputs all 1s

011 = Outputs toggle pattern; see Figure 40 and Figure 41 for LVDS and CMOS modes.
Output data D[10:0] alternates between *01010101010* and *10101010101* every clock cycle.

100 = Outputs digital ramp
Output data increments by one LSB (11-bit) every eighth clock cycle from code 0 to code 2047.

101 = Outputs custom pattern (use registers 51 and 52 for setting the custom pattern); see Figure 43 for an example of a custom pattern.

110 = Unused

111 = Unused

Table 30. Register 76h

D7	D6	D5	D4	D3	D2	D1	D0
0	0	OFFSET PEDESTAL, CH B			0	0	0

Bits D[7:6] **Always write '0'**

Bits D[5:3] **OFFSET PEDESTAL, CH B: Common, channel B**

When the offset correction is enabled, the final converged value (after the offset is corrected) is the ideal ADC mid-code value of 1024. A pedestal can be added to the final converged value by programming these bits. Thus, the final converged value is = ideal mid-code + PEDESTAL. See the *Offset Correction* section in the *Application Information*.

Applies to channel B (only with independent control).

011 = PEDESTAL is 3 LSB

010 = PEDESTAL is 2 LSB

001 = PEDESTAL is 1 LSB

000 = PEDESTAL is 0 LSB

111 = PEDESTAL is –1 LSB

110 = PEDESTAL is –2 LSB

101 = PEDESTAL is –3 LSB

100 = PEDESTAL is –4 LSB

Bits D[2:0] **Always write '0'**

APPLICATION INFORMATION

THEORY OF OPERATION

The ADS62P19 is a high-performance, low-power, dual-channel, 11-bit analog-to-digital converter (ADC) with sampling rates up to 250 MSPS. At every input clock falling edge, the analog input signal of each channel is sampled simultaneously. The sampled signal in each channel is converted by a pipeline of low-resolution stages. In each stage, the sampled and held signal is converted by a high-speed, low-resolution, flash sub-ADC. The difference (residue) between the stage input and the quantized equivalent is gained and propagates to the next stage.

At every clock, each succeeding stage resolves the sampled input with greater accuracy. The digital outputs from all stages are combined in a digital correction logic block and are processed digitally to create the final code, after a data latency of 22 clock cycles. The digital output is available as either DDR LVDS or parallel CMOS and is coded in either straight offset binary or binary twos complement format. The dynamic offset of the first stage sub-ADC limits the maximum analog input frequency to approximately 500 MHz (with 2-V_{PP} amplitude) and approximately 800 MHz (with 1-V_{PP} amplitude).

ANALOG INPUT

The analog input consists of a switched-capacitor-based differential sample-and-hold architecture, as shown in Figure 44. This differential topology results in very good ac performance, even for high input frequencies at high sampling rates. The INP and INM pins must be externally biased around a common-mode voltage of 1.5 V, available on the VCM pin. For a full-scale differential input, each input pin (INP, INM) must swing symmetrically between VCM + 0.5 V and VCM – 0.5 V, resulting in a 2-V_{PP} differential input swing. The input sampling circuit has a high 3-dB bandwidth that extends up to 700 MHz (measured from the input pins to the sampled voltage).

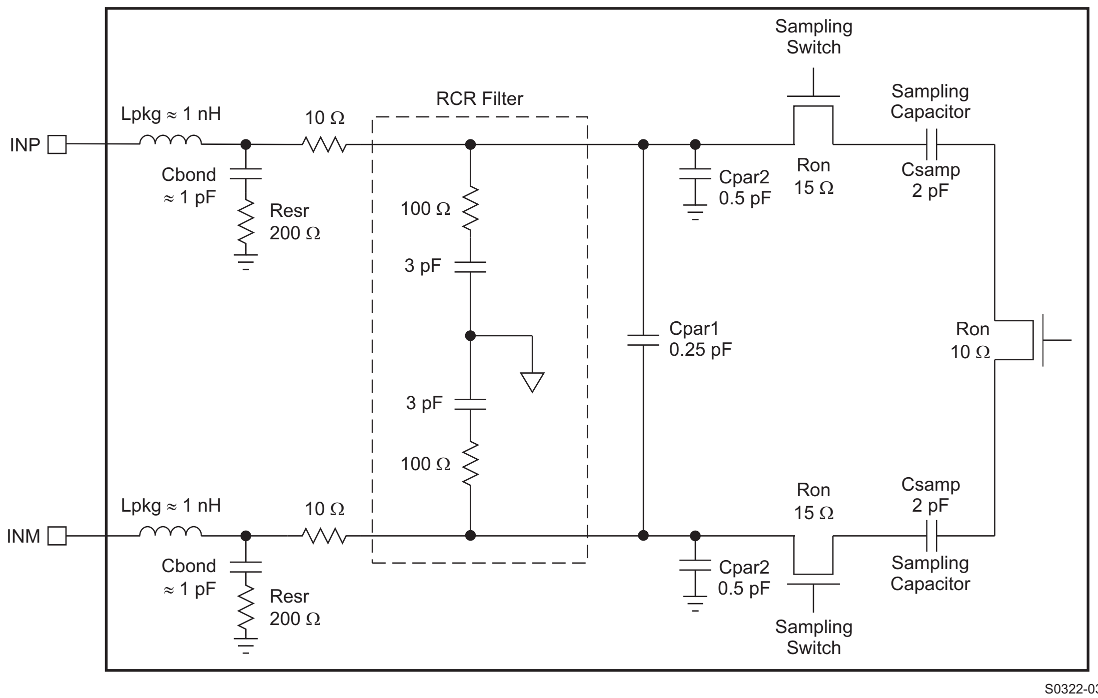


Figure 44. Analog Input Circuit

Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This configuration improves the common-mode noise immunity and even-order harmonic rejection. A 5-Ω to 15-Ω resistor in series with each input pin is recommended to damp out ringing caused by package parasitic.

SFDR performance can be limited because of several reasons: the effect of sampling glitches (as described in this section), nonlinearity of the sampling circuit, and nonlinearity of the quantizer that follows the sampling circuit. Depending on the input frequency, sample rate, and input amplitude, one of these restrictions plays a dominant part in limiting performance.

At very high input frequencies (greater than approximately 300 MHz), SFDR is determined largely by the device sampling circuit nonlinearity. At low input amplitudes, the quantizer nonlinearity usually limits performance.

Glitches are caused by the opening and closing of the sampling switches. The driving circuit should present a low source impedance to absorb these glitches. Otherwise, these glitches might limit performance, mainly at low input frequencies (up to approximately 200 MHz). Low impedance (less than 50 Ω) must also be presented for the common-mode switching currents. This impedance can be achieved by using two resistors from each input terminated to the common-mode voltage (VCM).

The device includes an internal R-C filter from each input to ground. The purpose of this filter is to absorb the sampling glitches inside the device itself. The cutoff frequency of the R-C filter involves a trade-off. A lower cutoff frequency (larger C) absorbs glitches better, but reduces the input bandwidth. On the other hand, with a higher cutoff frequency (smaller C), bandwidth support is maximized. However, the sampling glitches must be supplied by the external drive circuit. This configuration has limitations because of the presence of the package bond-wire inductance.

In the ADS62P19, the R-C component values have been optimized while supporting high input bandwidth (up to 700 MHz). However, in applications with input frequencies up to 200 MHZ to 300 MHz, the filtering of the glitches can be improved further using an external R-C-R filter (see Figure 47 and Figure 48).

In addition, the drive circuit may have to be designed to provide a low insertion loss over the desired frequency range and matched impedance to the source. During this process, ADC input impedance must be considered. Figure 45 and Figure 46 show the impedance ($Z_{IN} = R_{IN} \parallel C_{IN}$) at the ADC input pins.

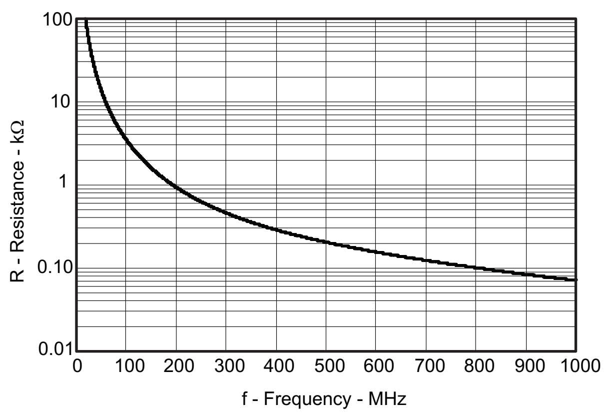


Figure 45. ADC Analog Input Resistance (R_{IN}) Across Frequency

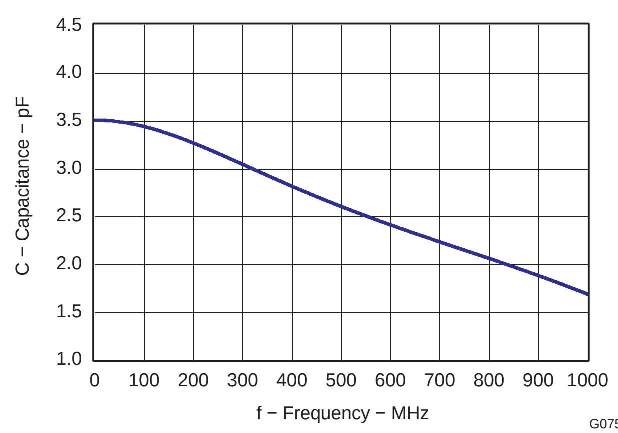


Figure 46. ADC Analog Input Capacitance (C_{IN}) Across Frequency

Driving Circuit

Two example driving circuit configurations are shown in Figure 47 and Figure 48, one optimized for low bandwidth (low input frequencies) and the other one for high bandwidth to support higher input frequencies. In Figure 47, an external R-C-R filter using 22 pF is used. Together with the series inductor (39 nH), this combination forms a filter and absorbs the sampling glitches. Because of the large capacitor (22 pF) in the R-C-R and the 15-Ω resistors in series with each input pin, the drive circuit has low bandwidth and supports low input frequencies (< 100 MHz).

To support higher input frequencies (up to approximately 300 MHz, as shown in Figure 48), the capacitance used in the R-C-R is reduced to 3.3 pF and the series inductors are shorted out. Together with the lower series resistors (5 Ω), this drive circuit provides high bandwidth and supports high input frequencies. Transformers such as ADT1-1WT or ETC1-1-13 can be used up to 300 MHz.

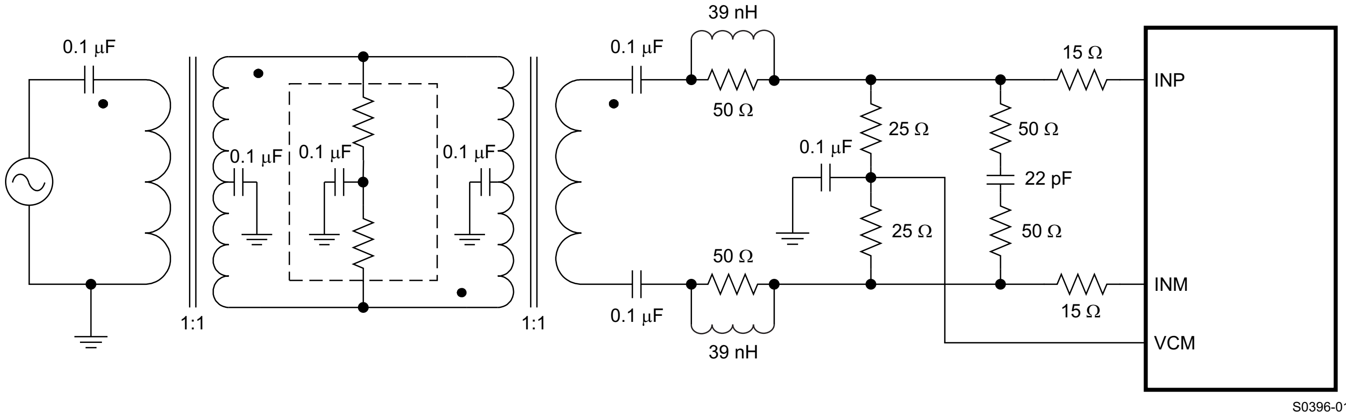


Figure 47. Drive Circuit With Low Bandwidth (for Low Input Frequencies)

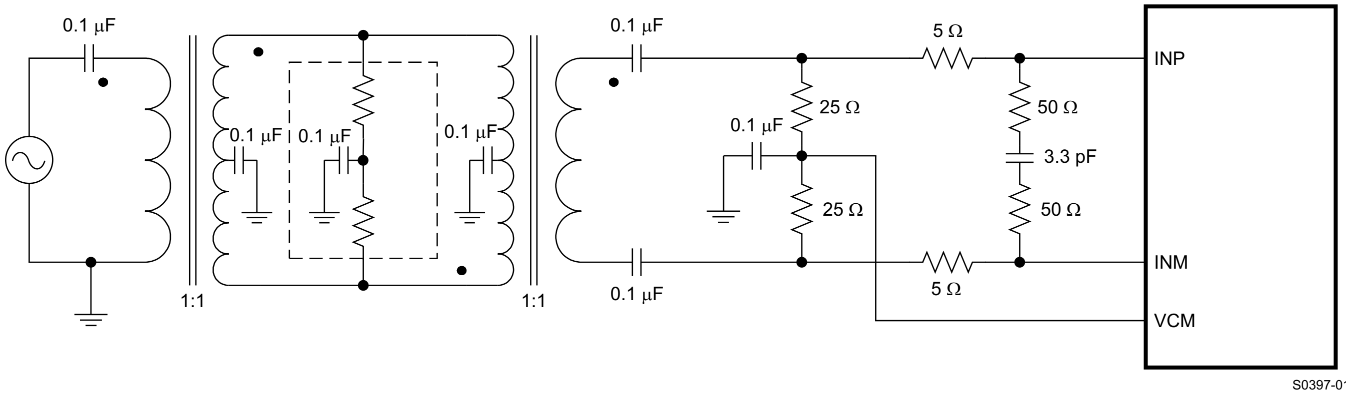


Figure 48. Drive Circuit With High Bandwidth (for High Input Frequencies)

Without the external R-C-R filter, the drive circuit has very high bandwidth and can support very high input frequencies (> 300 MHz). For example, a transmission line transformer such as ADTL2-18 can be used, as shown in Figure 49. Note that both drive circuits are terminated by 50 Ω near the ADC side. The termination is accomplished by a 25-Ω resistor from each input to the 1.5-V common-mode (VCM) from the device. This configuration allows the analog inputs to be biased around the required common-mode voltage.

The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch and good performance is obtained for high-frequency input signals. An additional termination resistor pair may be required between the two transformers, as described in Figure 47, Figure 48, and Figure 49. The center point of this termination is connected to ground to improve the balance between the P and M side. The values of the terminations between the transformers and on the secondary side must be chosen to obtain an effective 50 Ω (in the case of a 50-Ω source impedance).

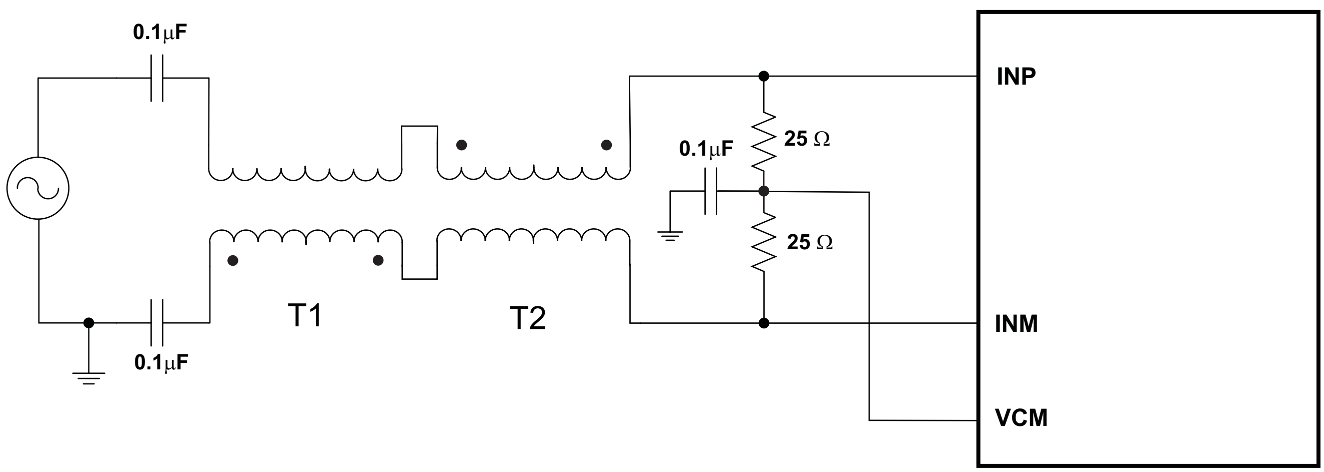


Figure 49. Drive Circuit with Very High Bandwidth (> 300 MHz)

These examples show 1:1 transformers used with a 50-Ω source. As explained in the *Drive Circuit Requirements* section, this structure helps present a low source impedance to absorb the sampling glitches. With a 1:4 transformer, the source impedance is 200 Ω. The higher impedance can lead to degradation in performance, compared to the case with 1:1 transformers.

For applications where only a band of frequencies are used, the drive circuit can be tuned to present a low impedance for the sampling glitches. Figure 50 shows an example with 1:4 transformer, tuned for a band at approximately 150 MHz.

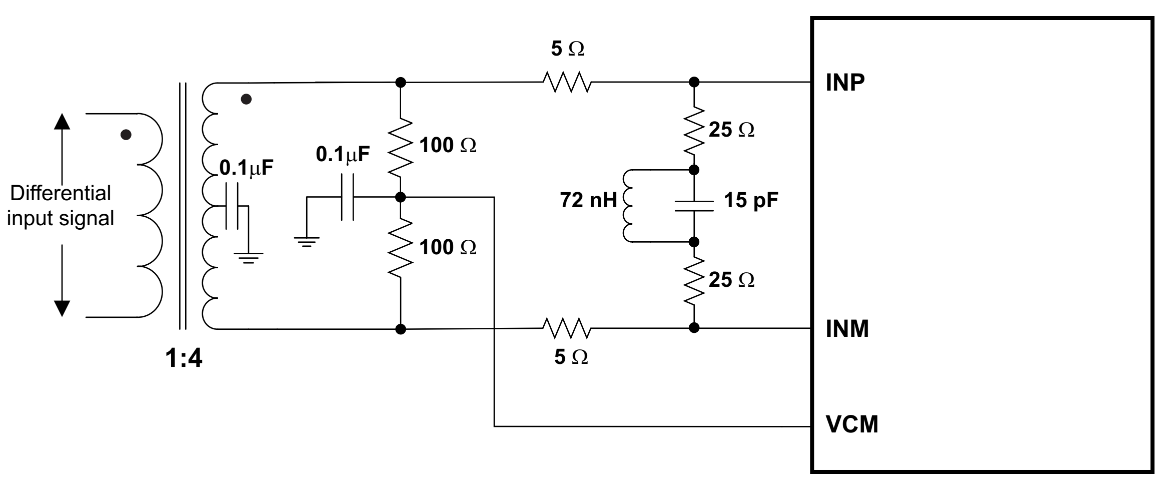


Figure 50. Drive Circuit with a 1:4 Transformer

Input Common-Mode

To ensure a low-noise common-mode reference, the VCM pin is filtered with a 0.1-μF low-inductance capacitor connected to ground. The VCM pin is designed to directly drive the ADC inputs. The ADC input stage sinks a common-mode current in the order of 3.6 μA per MSPS (approximately 900 μA at 250 MSPS).

REFERENCE

The ADS62P19 has built-in internal references (REFP and REFM) that require no external components. Design schemes are used to linearize the converter load detected by the references; this functionality and the on-chip integration of the requisite reference capacitors eliminates the need for external decoupling. The full-scale input range of the converter can be controlled in the external reference mode as explained in Figure 51. The internal or external reference modes can be selected by programming the REF serial interface register bit.

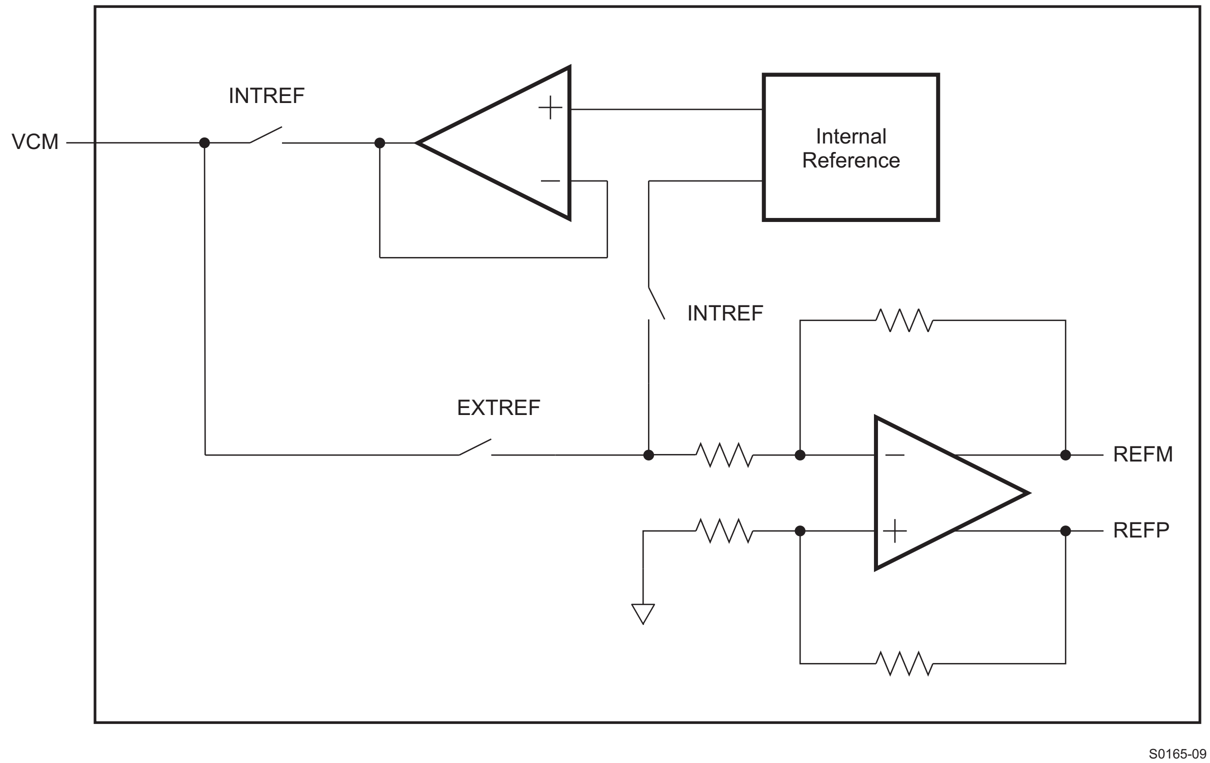


Figure 51. Reference Section

Internal Reference

When the device is in internal reference mode, the REFP and REFM voltages are generated internally. The common-mode voltage (1.5 V, nominal) is output on the VCM pin, which can be used to externally bias the analog input pins.

External Reference

When the device is in external reference mode, the VCM functions as a reference input pin. The voltage forced on the VCM pin is buffered and gained by 1.33 internally, generating the REFP and REFM voltages. The differential input voltage corresponding to full-scale is given by the following:

Full-scale differential input peak-to-peak = (voltage forced on VCM) × 1.33

In this mode, the 1.5-V common-mode voltage to bias the input pins must be generated externally.

CLOCK INPUT

The ADS62P19 clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to VCM using internal 5-kΩ resistors, as shown in Figure 52. This configuration allows using transformer-coupled drive circuits for sine-wave clock or ac-coupling for LVPECL and LVDS clock sources (Figure 53, Figure 54, and Figure 55).

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM (pin 11) connected to ground with a 0.1-μF capacitor; see Figure 56. For best performance, the clock inputs must be driven differentially, thus reducing susceptibility to common-mode noise. For high input frequency sampling, TI recommends using a clock source with very low jitter. Bandpass filtering of the clock source can help reduce the effect of jitter. There is no change in performance with a non-50% duty cycle clock input.

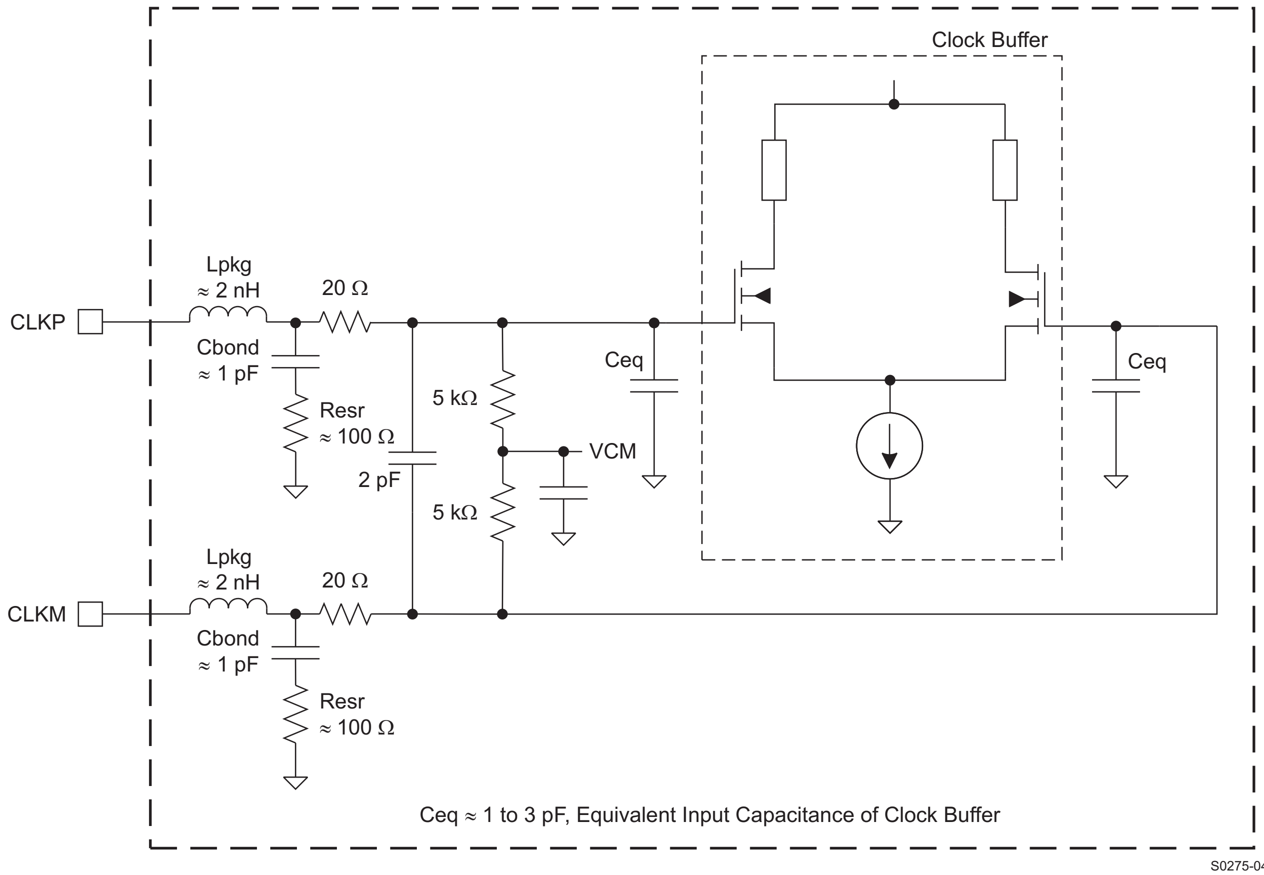


Figure 52. Internal Clock Buffer

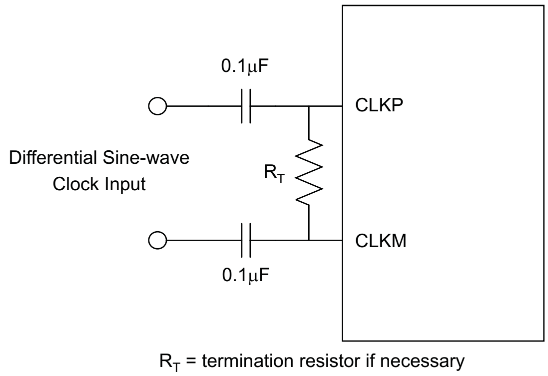


Figure 53. Differential Sine-Wave Clock Driving Circuit

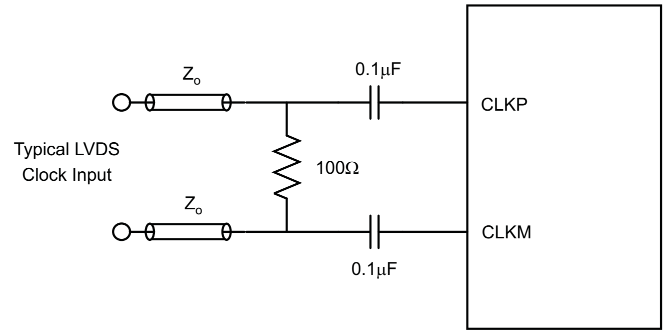


Figure 54. Typical LVDS Clock Driving Circuit

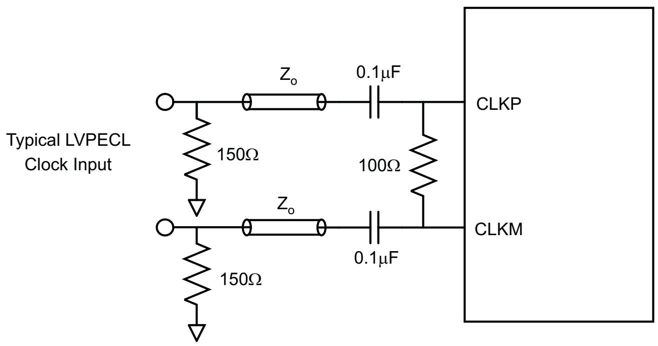


Figure 55. Typical LVPECL Clock Driving Circuit

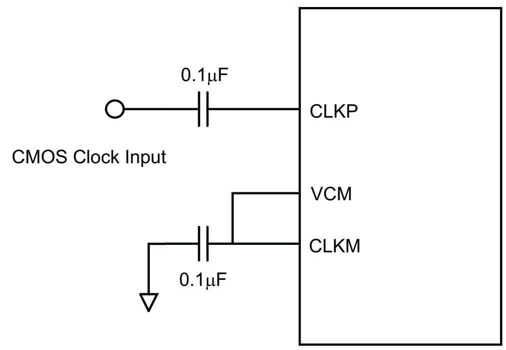


Figure 56. Typical LVCMOS Clock Driving Circuit

GAIN PROGRAMMABILITY

The ADS62P19 includes gain settings that can be used to obtain improved SFDR performance (compared to no gain). Gain is programmable from 0 dB to 6 dB (in 0.5-dB steps). For each gain setting, the analog input full-scale range scales proportionally, as shown in Table 31. SFDR improvement is achieved at the expense of SNR; for each 1-dB gain step, SNR degrades by approximately 1 dB. SNR degradation is reduced at high input frequencies. As a result, gain is very useful at high input frequencies because SFDR improvement is significant with marginal degradation in SNR. Therefore, gain can be used to trade-off between SFDR and SNR. Note that the default gain after reset is 0 dB.

Table 31. Full-Scale Range Across Gains

GAIN (dB)	DESCRIPTION	FULL-SCALE (V_{PP})
0	Default after reset	2
1	Fine, programmable	1.78
2	Fine, programmable	1.59
3	Fine, programmable	1.42
4	Fine, programmable	1.26
5	Fine, programmable	1.12
6	Fine, programmable	1.00

OFFSET CORRECTION

The ADS62P19 has an internal offset correction algorithm that estimates and corrects dc offset up to ±10 mV. The correction can be enabled with the ENABLE OFFSET CORRECTION serial register bit. When enabled, the algorithm estimates the channel offset and applies the correction every clock cycle. The correction loop time constant is a function of the sampling clock frequency. The time constant can be controlled using the OFFSET CORR TIME CONSTANT register bits, as described in Table 32.

After the offset is estimated, the correction can be frozen by setting ENABLE OFFSET CORRECTION back to '0'. When frozen, the last estimated value is used for offset correction every clock cycle. The correction does not affect the phase of the signal. Note that offset correction is disabled by default after reset.

Table 32. Time Constant of Offset Correction Algorithm

OFFSET CORR TIME CONSTANT (D[3:0])	TIME CONSTANT (TC_{CLK}, NUMBER OF CLOCK CYCLES)	TIME CONSTANT (Seconds, Equal to $TC_{CLK} \times 1 / f_S$) (1)
0000	256 k	1 ms
0001	512 k	2 ms
0010	1 M	4 ms
0011	2 M	8 ms
0100	4 M	17 ms
0101	8 M	33 ms
0110	16 M	67 ms
0111	32 M	134 ms
1000	64 M	268 ms
1001	128 M	536 ms
1010	256 M	1.1 s
1011	512 M	2.2 s
1100	Reserved	—
1101	Reserved	—
1110	Reserved	—
1111	Reserved	—

(1) Sampling frequency, f_S = 250 MSPS.

POWER DOWN

The ADS62P19 has two power-down modes: global power down and individual channel standby. These modes can be set using either the serial register bits or the control pins (CTRL1 to CTRL3). Table 33 describes the power-down modes.

Table 33. Need Title

POWER-DOWN MODES	CONFIGURE WITH				WAKE-UP TIME
	SERIAL INTERFACE	PARALLEL CONTROL PINS			
Normal operation	POWER DOWN MODES = 0000	Low	Low	Low	—
Output buffer disabled for channel B	POWER DOWN MODES = 1001	Not Available			—
Output buffer disabled for channel A	POWER DOWN MODES = 1010	Not Available			—
Output buffer disabled for channel A and B	POWER DOWN MODES = 1011	Not Available			—
Global power-down	POWER DOWN MODES = 1100	High	Low	Low	Slow (30 μs)
Channel B standby	POWER DOWN MODES = 1101	High	Low	High	Fast (1 μs)
Channel A standby	POWER DOWN MODES = 1110	High	High	Low	Fast (1 μs)
Multiplexed (MUX) mode; output data of channel A and B are multiplexed and available on the **DA[10:0]** pins.(1)	POWER DOWN MODES = 1111	High	High	High	—

(1) Low-speed mode must be enabled for the multiplexed output mode (MUX mode). Therefore, MUX mode only functions with the serial interface configuration and is not supported with the parallel configuration.

Global Power Down

In this mode, the entire chip (including both ADCs, internal reference, and output buffers) is powered down, resulting in a reduced total power dissipation of approximately 45 mW. The output buffers are in high-impedance state. The wake-up time from the global power-down to data becoming valid in normal mode is typically 30 μs.

Channel Standby

In this mode, the ADC for each channel can be powered down. The internal references are active, resulting in a quick wake-up time of 1 μs. The total power dissipation in standby is approximately 475 mW.

Input Clock Stop

In addition, the converter enters a low-power mode when the input clock frequency falls below 1 MSPS. The power is approximately 275 mW.

POWER-SUPPLY SEQUENCE

During power-up, the AVDD and DRVDD supplies can come up in any sequence. The two supplies are separated in the device. Externally, they can be driven from separate supplies or from a single supply.

DIGITAL OUTPUT INFORMATION

The ADS62P19 provides 11-bit data and an output clock synchronized with the data.

Output Interface

Two output interface options are available: double data rate (DDR) LVDS and parallel CMOS. These options can be selected using the LVDS_CMOS serial interface register bit or using the DFS pin in parallel configuration mode.

DDR LVDS Outputs

In this mode, the data bits and clock are output using low-voltage differential signal (LVDS) levels. Two data bits are multiplexed and output on each LVDS differential pair, as shown in Figure 57.

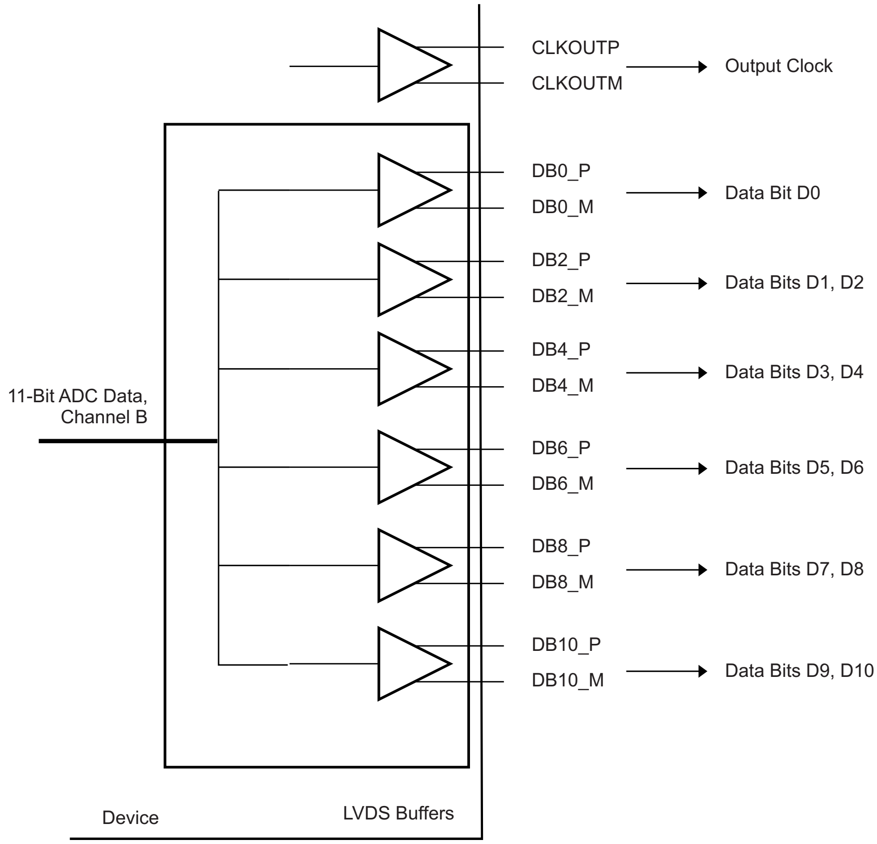
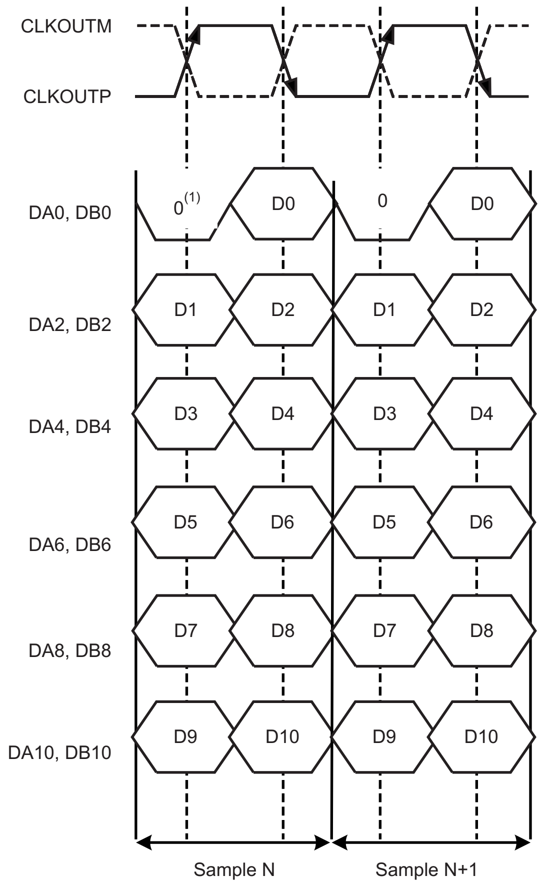


Figure 57. LVDS Outputs

Even data bits (D0, D2, D4, and so forth) are output at the CLKOUTP rising edge and the odd data bits (D1, D3, D5, and so forth) are output at the CLKOUTP falling edge. Both the CLKOUTP rising and falling edges must be used to capture all the data bits (see Figure 58).



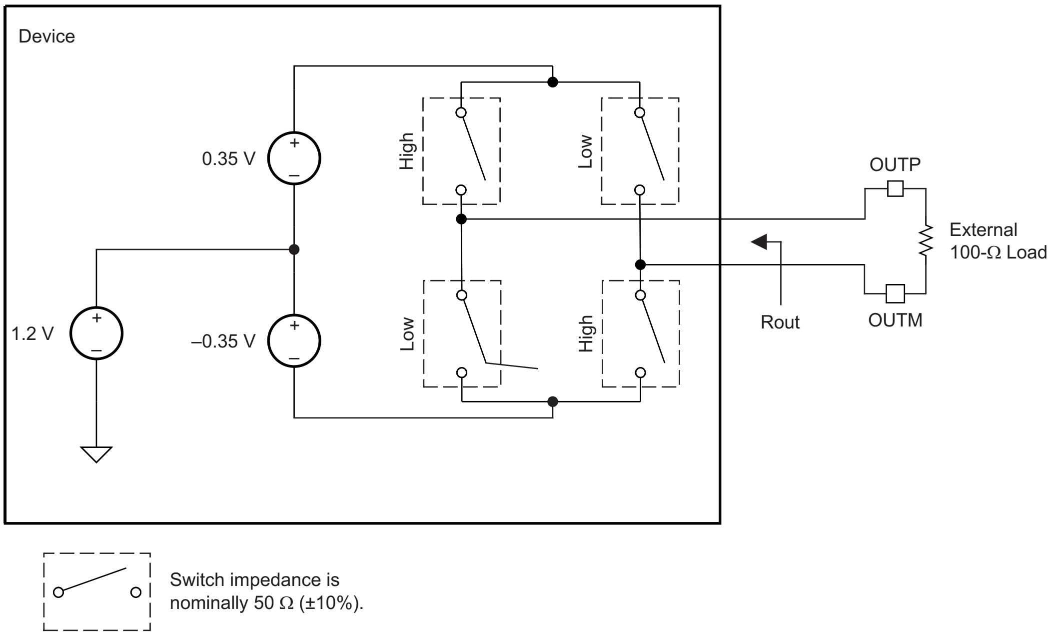
(1) Bit 0 is the dummy bit.

Figure 58. DDR LVDS Interface

LVDS Buffer

The equivalent circuit of each LVDS output buffer is shown in Figure 59. The buffer is designed to present an output impedance of 100 Ω (R_{OUT}). The differential outputs can be terminated at the receive end by a 100-Ω termination.

The buffer output impedance behaves like a source-side series termination. By absorbing reflections from the receiver end, the buffer output impedance helps improve signal integrity. Note that this internal termination cannot be disabled and its value cannot be changed.



NOTE: When the high switches are closed, OUTP = 1.375 V and OUTM = 1.025 V. When the low switches are closed, OUTP = 1.025 V and OUTM = 1.375 V. When either high or low switches are closed, R_{OUT} = 100 Ω.

Figure 59. LVDS Buffer Equivalent Circuit

Parallel CMOS Interface

In CMOS mode, each data bit is output on a separate pin as a CMOS voltage level for every clock cycle, as shown in Figure 60. This mode is recommended only up to 210 MSPS, beyond which the CMOS data outputs do not have sufficient time to settle to valid logic levels.

For sampling frequencies up to 150 MSPS, the output clock (CLKOUT) rising edge can be used to latch data in the receiver. The output data setup and hold times (with respect to CLKOUT) are specified in the Timing Requirements table up to 150 MSPS.

For sampling frequencies above 150 MSPS, TI recommends using an external clock to capture data. The delay from the input clock to output data and the data valid times are specified up to 210 MSPS. These timings can be used to delay the input clock appropriately and use it to capture data. When using the CMOS interface, the load capacitance detected by the data and clock output pins must be minimized by using short traces on the board.

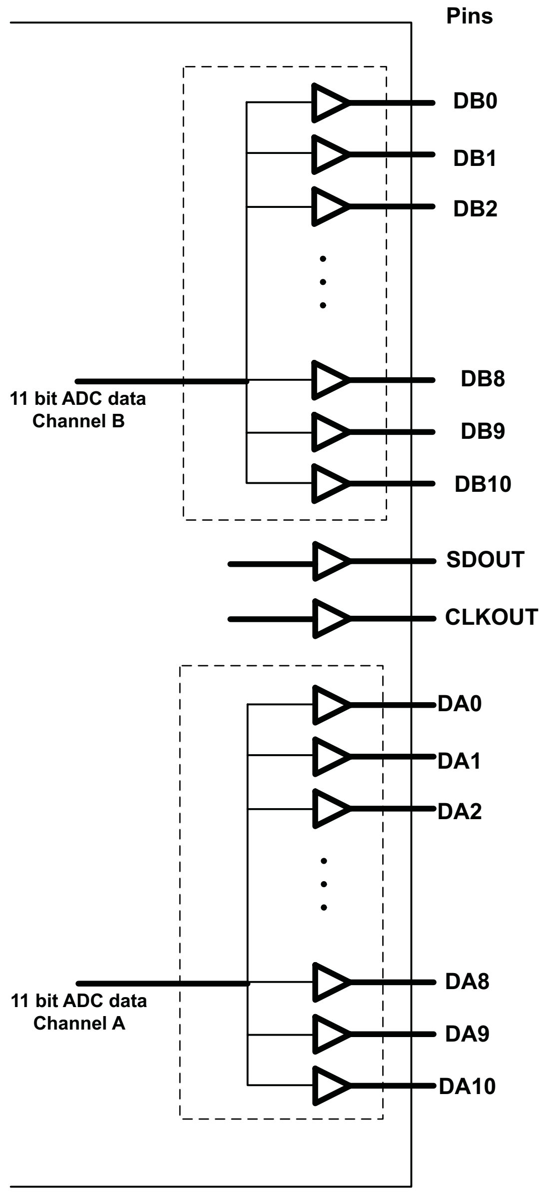


Figure 60. CMOS Outputs

CMOS Interface Power Dissipation

With CMOS outputs, the DRVDD current scales with the sampling frequency and the load capacitance on every output pin. Maximum DRVDD current occurs when each output bit toggles between '0' and '1' every clock cycle. In actual applications, this condition is unlikely to occur. Actual DRVDD current is determined by the average number of output bits switching, which is a function of the sampling frequency and the nature of the analog input signal.

Digital current resulting from CMOS output switching = $C_L \times DRVDD \times (N \times f_{AVG})$,

Where:

C_L = load capacitance,

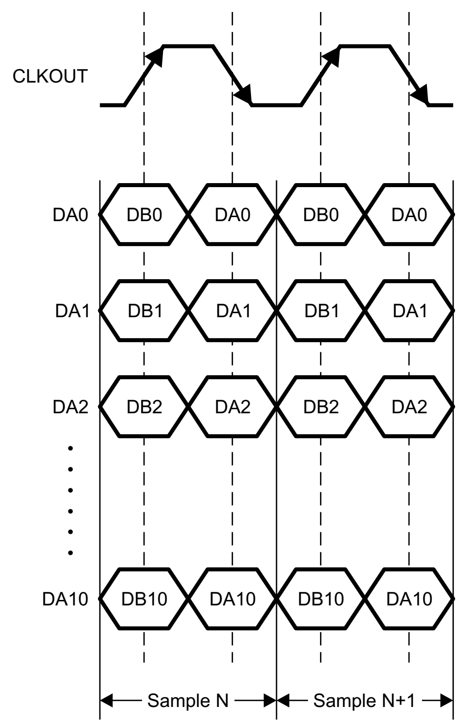
$N \times f_{AVG}$ = average number of output bits switching.

Refer to Figure 31 for a plot of the current with various load capacitances across sampling frequencies at 2.5-MHz analog input frequency.

Multiplexed Output Mode (Only with CMOS Interface)

In this mode, the digital outputs of both channels are multiplexed and output on a single bus (pins DA[10:0]). Channel B data bits are output at the CLKOUT rising edge, and channel A data bits are output at the CLKOUT falling edge. Channel B output data pins (DB[10:0]) are 3-stated; refer to Figure 61 for details. Because the output data rate on the DA bus is effectively doubled, this mode is recommended only for low sampling frequencies (less than 65 MSPS).

Low-speed mode must be enabled for the multiplexed output mode (MUX mode). Therefore, MUX mode only functions with the serial interface configuration and is not supported with the parallel configuration. This mode can be enabled with the POWER DOWN MODES register bits or the parallel pins (CTRL1 to CTRL3).



(1) Both channel outputs are output on the channel A output data lines.

(2) Channel A outputs are output on the output clock falling edges, whereas channel B outputs are output on the output clock rising edges.

Figure 61. Multiplexed Output Mode Timing

Output Data Format

Two output data formats are supported: twos complement and offset binary. These modes can be selected using the DATA FORMAT serial interface register bit or by controlling the DFS pin in parallel configuration mode.

In the event of an input voltage overdrive, the digital outputs go to the appropriate full-scale level. For a positive overdrive, the output code is 7FFh in offset binary output format, and 3FFh in twos complement output format. For a negative input overdrive, the output code is 000h in offset binary output format and 400h in twos complement output format.

BOARD DESIGN CONSIDERATIONS

Grounding: A single ground plane is sufficient to provide good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. See the *ADS62PXX EVM User's Guide* (SLAU237) for details on layout and grounding.

Supply Decoupling: Because the ADS62P19 already includes internal decoupling, minimal external decoupling can be used without loss in performance. Note that decoupling capacitors can help filter external power-supply noise, thus the optimum number of capacitors depends on the actual application. The decoupling capacitors should be placed very close to the converter supply pins.

Exposed Pad: In addition to providing a path for heat dissipation, the pad is also internally electrically connected to the digital ground. Therefore, the exposed pad must be soldered to the ground plane for best thermal and electrical performance. For detailed information, see application notes *QFN Layout Guidelines* (SLOA122) and *QFN/SON PCB Attachment* (SLUA271).

DEFINITION OF SPECIFICATIONS

Analog Bandwidth: The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value.

Aperture Delay: The delay in time between the input sampling clock rising edge and the actual time at which the sampling occurs. This delay is different across channels. The maximum variation is specified as aperture delay variation (channel-to-channel).

Aperture Uncertainty (Jitter): The sample-to-sample variation in aperture delay.

Clock Pulse Duration and Duty Cycle: The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse duration) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum Conversion Rate: The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate, unless otherwise noted.

Minimum Conversion Rate: The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL): An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral Nonlinearity (INL): INL is the deviation of the ADC transfer function from a best-fit line determined by a least-squares-curve fit of that transfer function, measured in units of LSBs.

Gain Error: Gain error is the deviation of the ADC actual input full-scale range from its ideal value. Gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error resulting from reference inaccuracy and error resulting from the channel. Both errors are specified independently as E_{GREF} and E_{GCHAN}, respectively.

To a first-order approximation, the total gain error is $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$.

For example, if $E_{TOTAL} = \pm0.5\%$, the full-scale input varies from $(1 – 0.5 / 100) \times FS_{ideal}$ to $(1 + 0.5 / 100) \times FS_{ideal}$.

Offset Error: Offset error is the difference, given in number of LSBs, between the ADC actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into millivolts.

Temperature Drift: The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}. Temperature drift is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference of $T_{MAX} – T_{MIN}$.

Signal-to-Noise Ratio (SNR): SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and the first nine harmonics.

$$SNR = 10Log^{10} \frac{P_S}{P_N} \tag{1}$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Signal-to-Noise and Distortion (SINAD): SINAD is the ratio of the power of the fundamental (P_S) to the power of all other spectral components, including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10Log^{10} \frac{P_S}{P_N + P_D} \tag{2}$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Effective Number of Bits (ENOB): ENOB is a measure of the converter performance as compared to the theoretical limit based on quantization noise.

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02} \quad (3)$$

Total Harmonic Distortion (THD): THD is the ratio of the power of the fundamental (P_S) to the power of the first nine harmonics (P_D).

$$\text{THD} = 10\text{Log}^{10}\ \frac{P_S}{P_N} \quad (4)$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR): SFDR is the ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion (IMD3): IMD3 is the ratio of the power of the fundamental (at frequencies f_1 and f_2) to the power of the worst spectral component at either frequency ($2f_1 - f_2$) or ($2f_2 - f_1$). IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

DC Power-Supply Rejection Ratio (DC PSRR): DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. DC PSRR is typically given in units of millivolts per volt.

AC Power-Supply Rejection Ratio (AC PSRR): AC PSRR is the measure of rejection of variations in the supply voltage by the ADC. If ΔV_{SUP} is the change in supply voltage and ΔV_{OUT} is the resultant change of the ADC output code (referred to the input), then:

$$\text{PSRR} = 20\text{Log}^{10}\ \frac{\Delta V_{OUT}}{\Delta V_{SUP}} \quad \text{(Expressed in dBc)} \quad (5)$$

Voltage Overload Recovery: The number of clock cycles taken to recover to less than 1% error after an overload on the analog inputs. This overload recovery is tested by separately applying a sine-wave signal with a 6-dB positive and negative overload. The deviation of the first few samples after the overload (from the expected values) is noted.

Common-Mode Rejection Ratio (CMRR): CMRR is the measure of rejection of variation in the analog input common-mode by the ADC. If ΔV_{CM_IN} is the change in the common-mode voltage of the input pins and ΔV_{OUT} is the resultant change of the ADC output code (referred to the input), then:

$$\text{CMRR} = 20\text{Log}^{10}\ \frac{\Delta V_{OUT}}{\Delta V_{CM}} \quad \text{(Expressed in dBc)} \quad (6)$$

Crosstalk (only for multichannel ADCs): Crosstalk is a measure of the internal coupling of a signal from an adjacent channel into the channel of interest. Crosstalk is specified separately for coupling from the immediate neighboring channel (near-channel) and for coupling from a channel across the package (far-channel). Crosstalk is usually measured by applying a full-scale signal in the adjacent channel. Crosstalk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. Crosstalk is typically expressed in dBc (dB to carrier).

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS62P19IRGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ62P19
ADS62P19IRGCR.A	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ62P19
ADS62P19IRGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ62P19
ADS62P19IRGCT.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ62P19

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

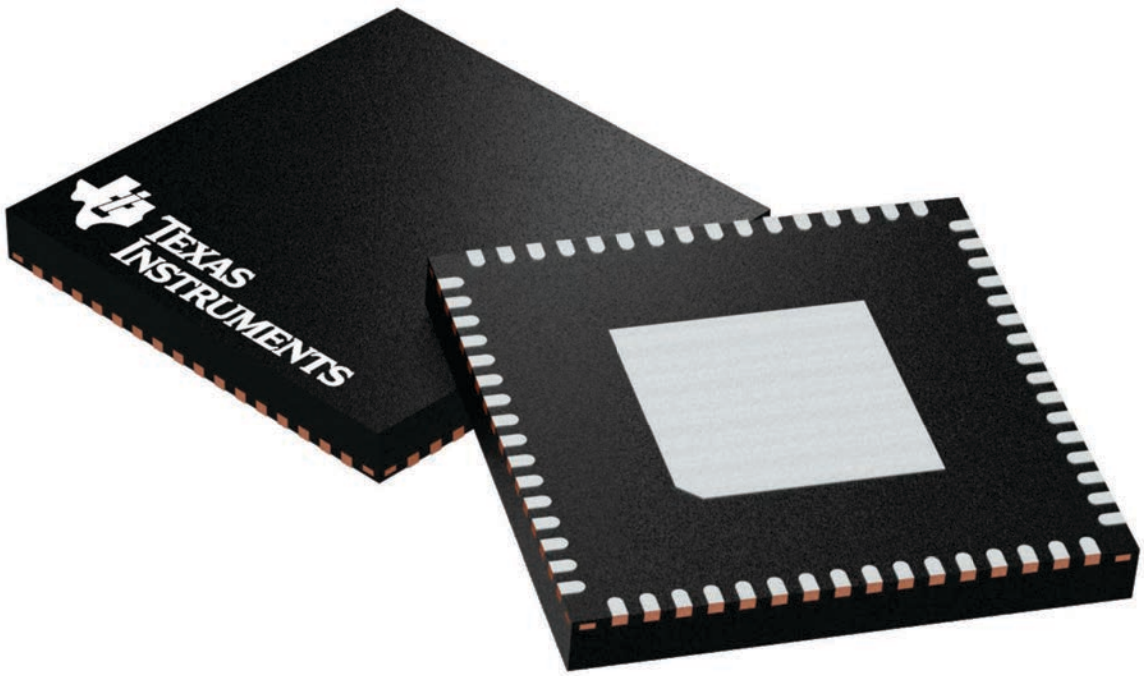
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

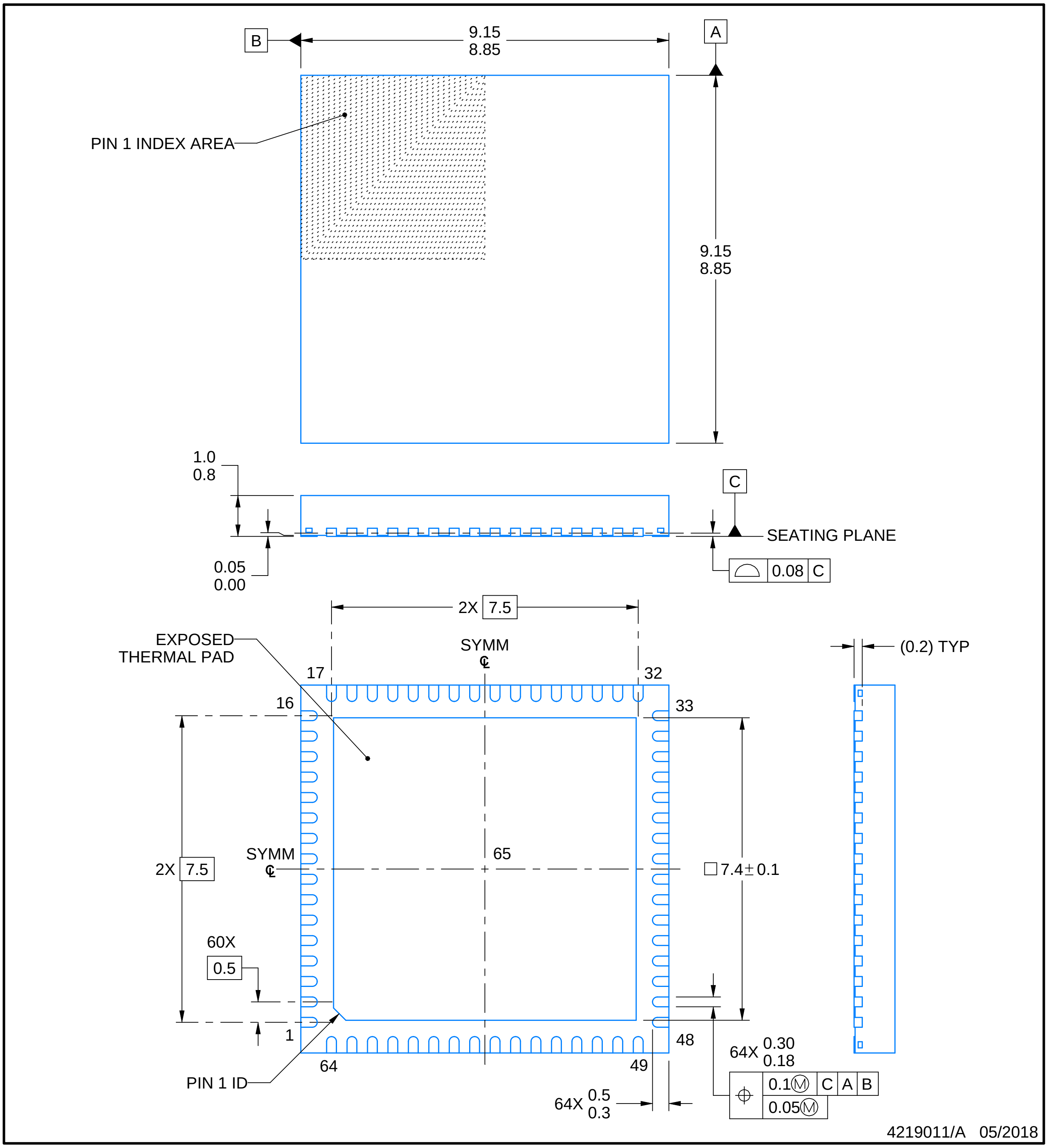
9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



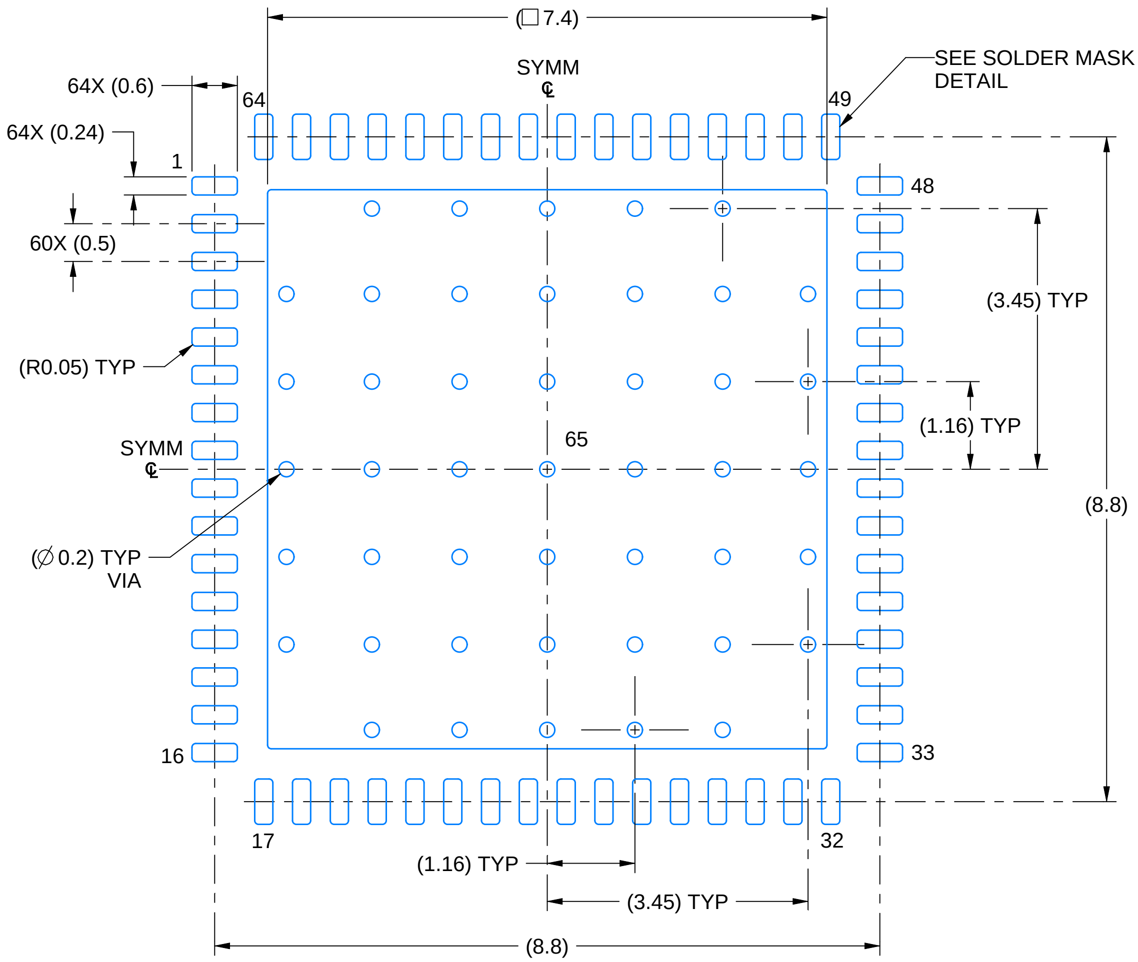
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224597/A

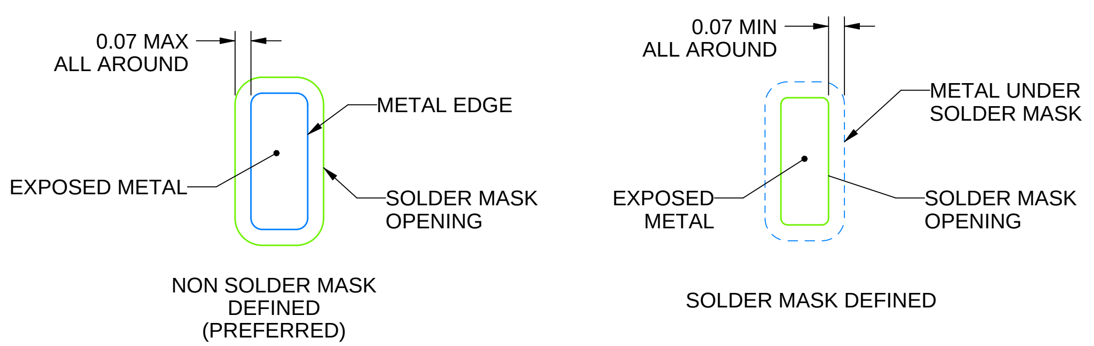


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

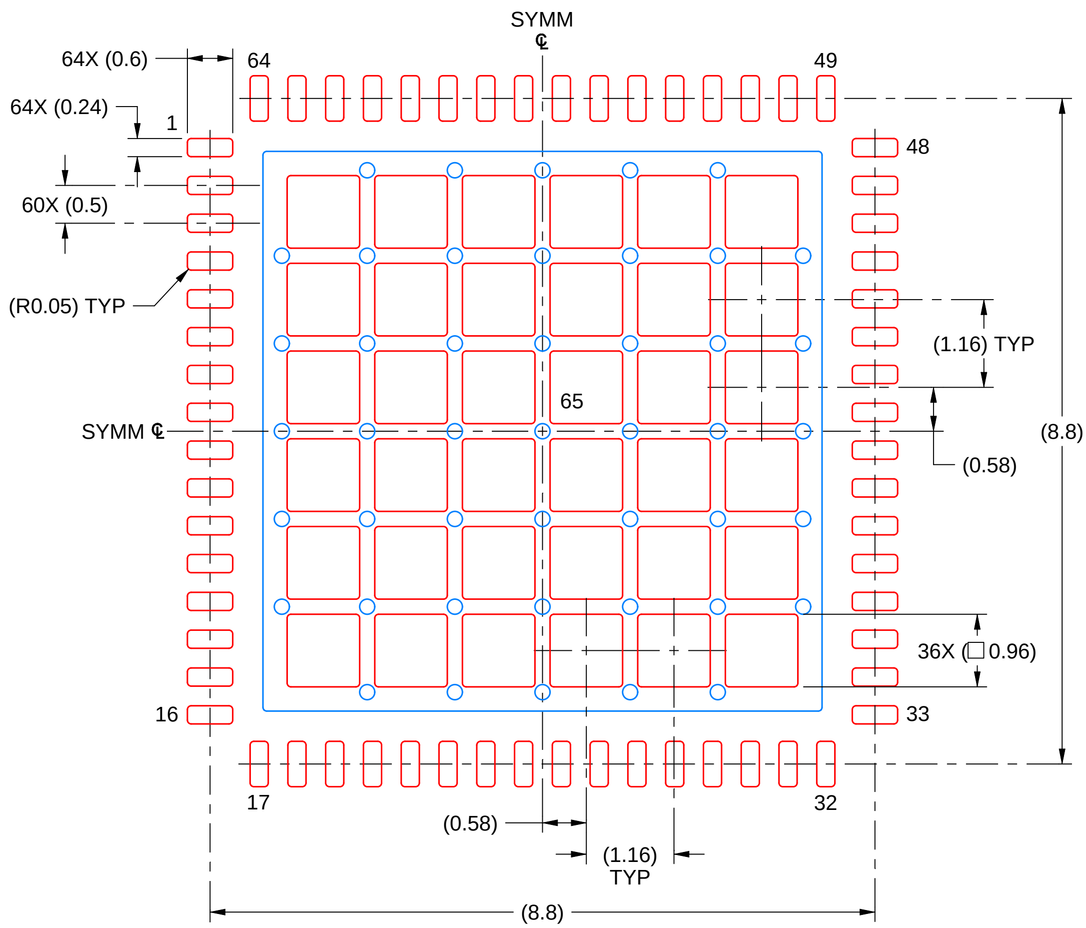


SOLDER MASK DETAILS

4219011/A 05/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
61% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219011/A 05/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265