Dual Channel IF Receiver with SNRBoost^{3G}

Check for Samples: ADS58C28

FEATURES

- **Maximum Sample Rate: 200MSPS**
- **High Dynamic Performance:**
  - **83dBc SFDR at 140MHz**
  - **72.5dBFS SNR with 60MHz BW Using SNRBoost^{3G} Technology**
- **SNRBoost^{3G} Highlights:**
  - **Supports Wide Bandwidth (up to 60MHz)**
  - **Programmable Bandwidths: 20MHz, 30MHz, and 40MHz**
  - **Flat Noise Floor within the Band**
  - **Independent SNRBoost^{3G} Coefficients for Both Channels**
- **Output Interface:**
  - **Double Data Rate (DDR) LVDS with Programmable Swing and Strength:**
    - **Standard Swing: 350mV**
    - **Low Swing: 200mV**
    - **Default Strength: 100Ω termination**
    - **2x Strength: 50Ω termination**
  - **Compatible with GC6016**
  - **1.8V Parallel CMOS Interface Also Supported**
- **Ultralow Power with Single 1.8V Supply:**
  - **470mW Total Power**
  - **710mW Total Power (200MSPS) with SNRBoost^{3G} on Both Channels**
- **Programmable Gain up to 6dB for SNR/SFDR Trade-off**
- **DC Offset Correction**
- **Supports Low Input Clock Amplitude**
- **Package: QFN-64 (9mm × 9mm)**

DESCRIPTION

The ADS58C28 is a dual-channel, 11-bit analog-to-digital converter (ADC) with sampling rates up to 200MSPS. The device uses innovative design techniques to achieve high dynamic performance, while consuming extremely low power at 1.8V supply. This architecture makes it well-suited for multi-carrier, wide bandwidth communications applications.

The ADS58C28 uses third-generation SNRBoost^{3G} technology to overcome SNR limitation as a result of quantization noise (for bandwidths less than Nyquist, $f_S/2$). Enhancements in the SNRBoost^{3G} technology allow support for SNR improvements over wide bandwidths (up to 60MHz). In addition, separate SNRBoost^{3G} coefficients can also be programmed for each channel.

The device has a digital gain function that can be used to improve SFDR performance at lower full-scale input ranges. It includes a dc offset correction loop that can be used to cancel the ADC offset. The digital outputs of all channels are output as double data rate (DDR) low-voltage differential signaling (LVDS) together with an LVDS clock output. The low data rate of this interface (400MBPS at 200MSPS sample rate) makes it possible to use low-cost field-programmable gate array (FPGA)-based receivers. The strength of the LVDS output buffers can be increased to support 50Ω differential termination. This increase allows the output clock signal to be connected to two separate receiver chips with an effective 50Ω termination (such as the two clock ports of the GC5330). The same digital output pins can also be configured as a parallel 1.8V CMOS interface.

The device includes internal references while the traditional reference pins and associated decoupling capacitors have been eliminated. The ADS58C28 is specified over the industrial temperature range (–40°C to +85°C).

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	ECO PLAN(2)	LEAD/BALL FINISH	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
ADS58C28	QFN-64	RGC	–40°C to +85°C	GREEN (RoHS, no Sb/Br)	Cu/NiPdAu	AZ58C28	ADS58C28IRGC	Tape and reel
							ADS58C28IRGC	Tape and reel

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

(2) Eco Plan is the planned eco-friendly classification. Green (RoHS, no Sb/Br): TI defines *Green* to mean Pb-Free (RoHS compatible) and free of Bromine- (Br) and Antimony- (Sb) based flame retardants. Refer to the Quality and Lead-Free (Pb-Free) Data web site for more information.

The ADS58C28 is pin-compatible with the previous generation ADS62C17 converter; this architecture enables easy migration. However, there are some important differences between the generations, summarized in Table 1.

Table 1. Migrating from the ADS62C17

ADS62C17	ADS58C28
PINS	
Pin 22 is NC (not connected)	Pin 22 is AVDD
Pins 38 and 58 are DRVDD	Pins 38 and 58 are NC (do not connect pins)
Pins 39 and 59 are DRGND	Pins 39 and 59 are NC (do not connect pins)
SUPPLY	
AVDD is 3.3V	AVDD is 1.8V
DRVDD is 1.8V	No change
INPUT COMMON-MODE VOLTAGE	
CM is 1.5V	CM is 0.95V
SERIAL INTERFACE	
Protocol: 8-bit register address and 8-bit register data	No change in protocol New serial register map
PARALLEL CONFIGURATION	
SCLK pin controls internal and external reference mode	SCLK pin enables low-speed mode
EXTERNAL REFERENCE	
Supported	Not supported

ABSOLUTE MAXIMUM RATINGS(1)

		ADS58C28		UNIT
		MIN	MAX	
Supply voltage range, AVDD		–0.3	2.1	V
Supply voltage range, DRVDD		–0.3	2.1	V
Voltage between AGND and DRGND		–0.3	0.3	V
Voltage between AVDD to DRVDD (when AVDD leads DRVDD)		–2.4	2.4	V
Voltage between DRVDD to AVDD (when DRVDD leads AVDD)		–2.4	2.4	V
Voltage applied to input pins	INP, INM	–0.3	Minimum (1.9, AVDD + 0.3)	V
	CLKP, CLKM(2)	–0.3	AVDD + 0.3	V
	RESET, SCLK, SDATA, SEN, CTRL1, CTRL2, CTRL3	–0.3	+3.9	V
Operating free-air temperature range, T_A		–40	+85	°C
Operating junction temperature range, T_J			+125	°C
Storage temperature range, T_{stg}		–65	+150	°C
ESD, Human body model (HBM)			2	kV

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) When AVDD is turned off, it is recommended to switch off the input clock (or ensure the voltage on CLKP, CLKM is less than |0.3V|. This prevents the ESD protection diodes at the clock input pins from turning on.

THERMAL INFORMATION

THERMAL METRIC(1)		ADS58C28	UNITS
		RGC	
		64 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	23.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	10.9	
θ_{JB}	Junction-to-board thermal resistance	4.3	
ψ_{JT}	Junction-to-top characterization parameter	0.1	
ψ_{JB}	Junction-to-board characterization parameter	4.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range, unless otherwise noted.

		MIN	NOM	MAX	UNIT
SUPPLIES					
Analog supply voltage, AVDD		1.75	1.8	1.9	V
Digital supply voltage, DRVDD		1.7	1.8	1.9	V
ANALOG INPUTS					
Differential input voltage range	Default, SNRBoost^{3G} disabled		2		V_{PP}
	SNRBoost^{3G} enabled		1.6		V_{PP}
Input common-mode voltage			VCM(1) ± 0.05		V
Maximum analog input frequency with $2V_{PP}$ input amplitude(2)			400		MHz
Maximum analog input frequency with $1V_{PP}$ input amplitude(2)			600		MHz
CLOCK INPUT					
Input clock sample rate(3)	Default after reset LOW SPEED mode disabled	> 80		200	MSPS
	LOW SPEED mode enabled	1		80	MSPS
Input clock amplitude differential ($V_{CLKP} – V_{CLKM}$)	Sine wave, ac-coupled	0.2	1.5		V_{PP}
	LVPECL, ac-coupled		1.6		V_{PP}
	LVDS, ac-coupled		0.7		V_{PP}
	LVCMOS, single-ended, ac-coupled		1.8		V
Input clock duty cycle	Default after reset LOW SPEED mode disabled	35	50	65	%
	LOW SPEED mode enabled	40	50	60	%
DIGITAL OUTPUTS					
Maximum external load capacitance from each output pin to DRGND, C_{LOAD}			10		pF
Differential load resistance between the LVDS output pairs (LVDS mode), R_{LOAD}			100		Ω
HIGH-PERFORMANCE MODES(4)(5)					
High-performance mode	Set this register bit to get best performance across sample clock and input signal frequencies	Register address = 03h, data = 03h			
High-frequency mode	Set these register bits for high input signal frequencies (> 200MHz)	Register address = 4Ah, data = 01h			
		Register address = 58h, data = 01h			
Operating free-air temperature, T_A		–40		+85	°C

(1) VCM, typically 0.95V, is the voltage measured on the VCM pin when the input clock is switched off.
(2) See the *Theory of Operation* section in the Application Information
(3) See description for LOW SPEED mode in the *Serial Interface Configuration* section.
(4) It is recommended to use these modes to obtain best performance.
(5) See the *Serial Interface Configuration* section for details on register programming.

ELECTRICAL CHARACTERISTICS

Typical values are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, sampling frequency = 200MSPS, 50% clock duty cycle, –1dBFS differential analog input, and LVDS and CMOS interfaces, unless otherwise noted.
Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8V, and DRVDD = 1.8V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTION						
Resolution					11	Bits
ANALOG INPUTS						
	Differential input voltage range			2		V_{PP}
	Differential input resistance (at 200MHz, see Figure 55)			0.75		kΩ
	Differential input capacitance (at 200MHz, see Figure 56)			3.7		pF
	Analog input bandwidth			550		MHz
	Analog input common-mode current (per input pin of each channel)			1.5		µA/MSPS
	VCM common-mode voltage output			0.95		V
	VCM output current capability			4		mA
POWER SUPPLY						
IAVDD	Analog supply current			141	163	mA
IDRVDD	Output buffer supply current LVDS interface	350mV LVDS swing with 100Ω external termination after reset		120	130	mA
	Analog power			254		mW
	Digital power LVDS interface			216		mW
	Global power-down				15	mW
DC ACCURACY						
DNL	Differential nonlinearity	f_{IN} = 170MHz	–0.6		0.6	LSB
INL	Integral nonlinearity	f_{IN} = 170MHz	–1.5	0.3	1.5	LSB
	Offset error	Specified across devices and channels within a device	–15		15	mV
There are two sources of gain error: internal reference inaccuracy and channel gain error						
	Gain error as a result of internal reference inaccuracy alone	Specified across devices and channels within a device	–2		2	%FS
	Gain error of channel alone(1)	Specified across devices and channels within a device		±0.1	±1	%FS
	Channel gain error temperature coefficient			0.002		Δ%/°C

(1) Specified by design and characterization; not tested in production.

ELECTRICAL CHARACTERISTICS

Typical values are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, sampling frequency = 200MSPS, 50% clock duty cycle, –1dBFS differential analog input, SNRBoost^{3G} disabled, and LVDS and CMOS interfaces, unless otherwise noted.
Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8V, and DRVDD = 1.8V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SNR Signal-to-noise ratio, **LVDS**	f_{IN} = 20MHz		66.8		dBFS
	f_{IN} = 100MHz		66.4		
	f_{IN} = 170MHz	65	66		
SINAD Signal-to-noise and distortion ratio	f_{IN} = 20MHz		66.7		dBFS
	f_{IN} = 100MHz		66.3		
	f_{IN} = 170MHz	64.5	65.8		
SFDR Spurious-free dynamic range	f_{IN} = 20MHz		82		dBc
	f_{IN} = 100MHz		84		
	f_{IN} = 170MHz	70.5	80		
THD Total harmonic distortion	f_{IN} = 20MHz		80		dBc
	f_{IN} = 100MHz		81		
	f_{IN} = 170MHz	69.5	78		
HD2 Second-harmonic distortion	f_{IN} = 20MHz		82		dBc
	f_{IN} = 100MHz		85		
	f_{IN} = 170MHz	70.5	79		
HD3 Third-harmonic distortion	f_{IN} = 20MHz		86		dBc
	f_{IN} = 100MHz		86		
	f_{IN} = 170MHz	70.5	85		
Worst Spur Other than second and third harmonics	f_{IN} = 20MHz		90		dBc
	f_{IN} = 100MHz		89		
	f_{IN} = 170MHz	74.5	88		
IMD Two-tone intermodulation distortion	F1 = 185MHz, F2 = 190MHz, each tone at –7dBFS		83		dBFS
Input overload recovery	Recovery to within 1% (of final value) for 6dB overload with sine wave input		1		Clock cycles
Crosstalk	With a full-scale 170MHz signal on aggressor and a full-scale 20MHz signal on victim		96		dB
PSRR AC power-supply rejection ratio	For 50mV_{PP} signal on AVDD supply		20		dB

DIGITAL CHARACTERISTICS

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at valid logic level 0 or 1. AVDD = 1.8V and DRVDD = 1.8V.

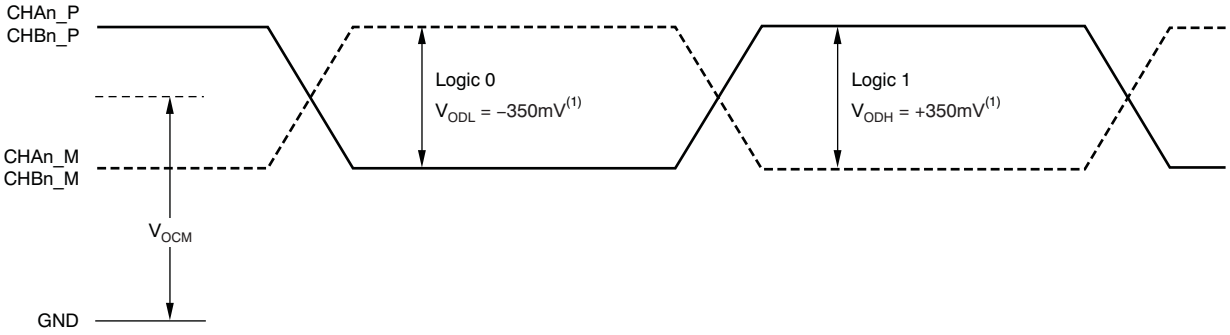
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS—RESET, SCLK, SDATA, SEN, CTRL1, CTRL2, and CTRL3						
High-level input voltage		RESET, SCLK, SDATA and SEN support 1.8V and 3.3V CMOS logic levels.	1.3			V
Low-level input voltage					0.4	V
High-level input current	SDATA, SCLK(1)	V_{HIGH} = 1.8V		10		µA
	SEN(2)	V_{HIGH} = 1.8V		0		µA
Low-level input current	SDATA, SCLK	V_{LOW} = 0V		0		µA
	SEN	V_{LOW} = 0V		–10		µA
DIGITAL OUTPUTS—CMOS INTERFACE (CHx_Dn, SDOUT)						
High-level output voltage			DRVDD – 0.1	DRVDD		V
Low-level output voltage				0	0.1	V
DIGITAL OUTPUTS—LVDS INTERFACE (CHxP/M, CLKOUTP/M)						
V_{ODH}, High-level output voltage(3)		Standard swing LVDS	270	350	430	mV
V_{ODL}, Low-level output voltage(3)		Standard swing LVDS	–430	–350	–270	mV
V_{ODH}, High-level output voltage(3)		Low swing LVDS(4)		200		mV
V_{ODL}, Low-level output voltage(3)		Low swing LVDS(4)		–200		mV
V_{OCM}, Output common-mode voltage			0.9	1.05	1.25	V

(1) SDATA and SCLK have an internal 150kΩ pull-down resistor.
(2) SEN has an internal 150kΩ pull-up resistor to AVDD.
(3) With external 100Ω termination.
(4) See the *LVDS Output Data and Clock Buffers* section.

Table 2. SNR Enhancement with SNRBoost^{3G} Enabled(1)

BANDWIDTH (MHz)	SNR WITHIN SPECIFIED BANDWIDTH (dBFS)					
	IN DEFAULT MODE (SNRBoost^{3G} Disabled)			WITH SNRBoost^{3G} ENABLED(2)(3)		
	MIN	TYP	MAX	MIN	TYP	MAX
60		68.3		69.7	72.5	
40		70		71.8	74	
30		71.1		72.8	74.7	
20		72.5		74.4	76	

(1) SNRBoost^{3G} bathtub centered at (3/4) × f_S, –2dBFS input applied at f_{IN} = 140MHz, sampling frequency = 200MSPS.
(2) Using suitable filters. See note on SNRBoost^{3G} in the *SNR Enhancement Using SNRBoost* section.
(3) Specified by characterization.

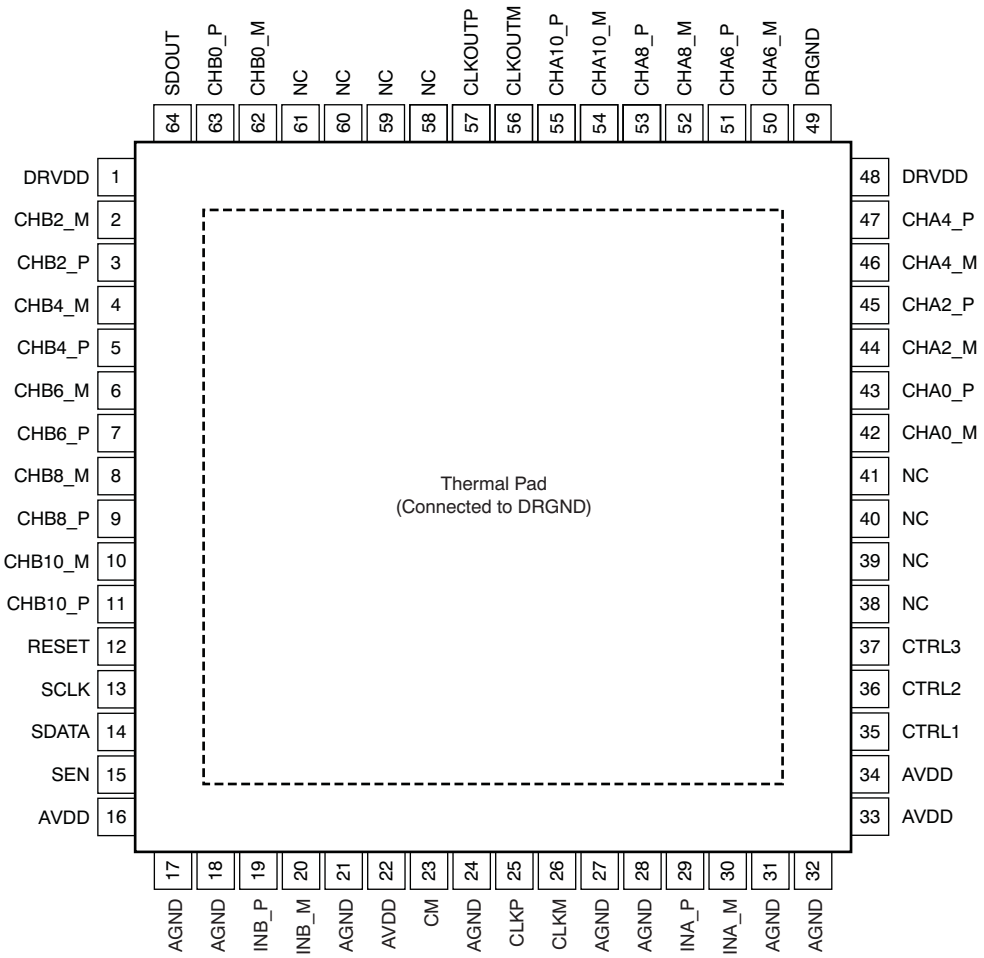


(1) With external 100Ω termination.

Figure 1. LVDS Voltage Levels

PIN CONFIGURATION (LVDS MODE)

RGC PACKAGE(1)
QFN-64
(TOP VIEW)



(2) The PowerPAD™ is connected to DRGND.

(3) NC = no connection.

Figure 2. ADS58C28 LVDS Pinout

Pin Assignments (LVDS Mode)

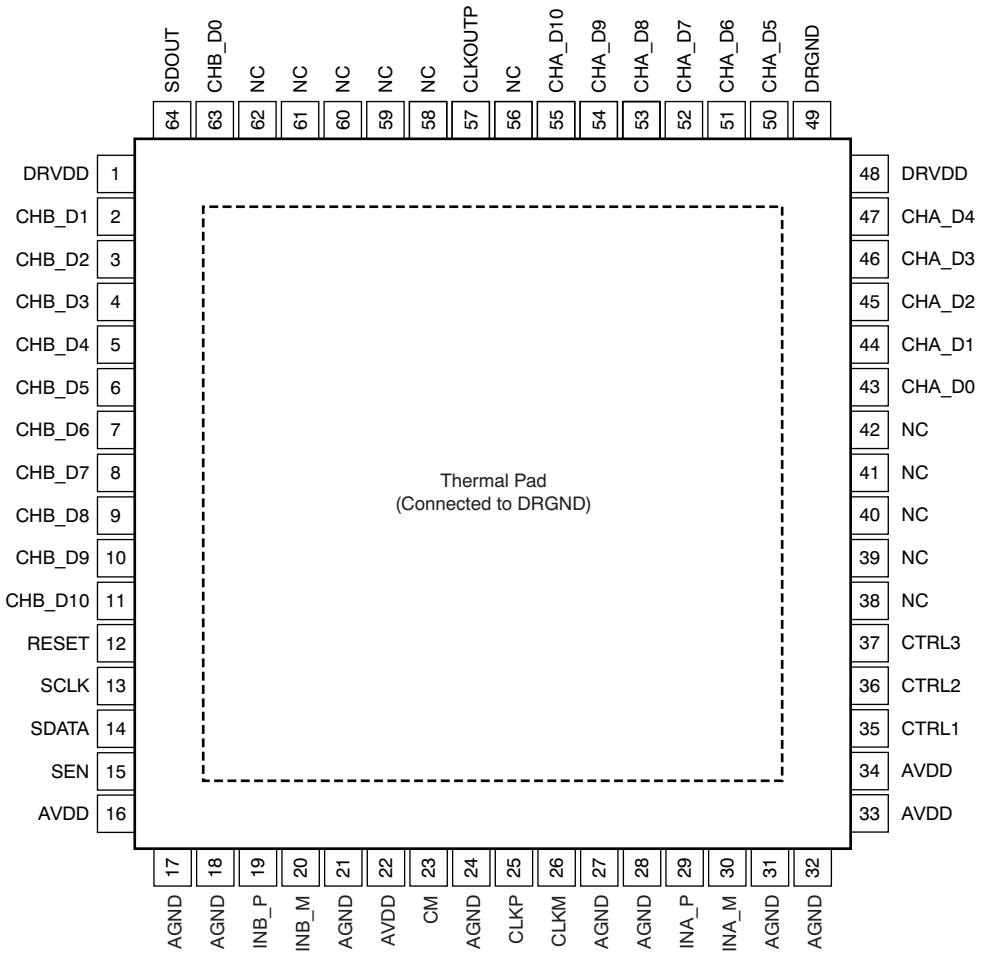
PIN NAME	PIN NUMBER	# OF PINS	FUNCTION	DESCRIPTION
AVDD	16, 22, 33, 34	4	Input	Analog power supply
AGND	17, 18, 21, 24, 27, 28, 31, 32	8	Input	Analog ground
CLK_P	25	1	Input	Differential clock positive input
CLK_M	26	1	Input	Differential clock negative input
INA_P	29	1	Input	Differential analog positive input, channel A
INA_M	30	1	Input	Differential analog negative input, channel A
INB_P	19	1	Input	Differential analog positive input, channel B
INB_M	20	1	Input	Differential analog negative input, channel B
CM	23	1	Output	This pin outputs the common-mode voltage (0.95V) that can be used externally to bias the analog input pins

Pin Assignments (LVDS Mode) (continued)

PIN NAME	PIN NUMBER	# OF PINS	FUNCTION	DESCRIPTION
RESET	12	1	Input	Serial interface RESET input. When using the serial interface mode, the internal registers must be initialized through a hardware RESET by applying a high pulse on this pin or by using the software reset option; refer to the *Serial Interface Configuration* section. In parallel interface mode, the RESET pin must be permanently tied high. SCLK and SEN are used as parallel control pins in this mode. This pin has an internal 100kΩ pull-down resistor.
SCLK	13	1	Input	This pin functions as a serial interface clock input when RESET is low. It controls the low-speed mode selection when RESET is tied high; see Table 6 for detailed information. This pin has an internal 100kΩ pull-down resistor.
SDATA	14	1	Input	Serial interface data input; this pin has an internal 100kΩ pull-down resistor.
SEN	15	1	Input	This pin functions as a serial interface enable input when RESET is low. It controls the output interface and data format selection when RESET is tied high; see Table 7 for detailed information. This pin has an internal 150kΩ pull-up resistor to AVDD.
SDOUT	64	1	Output	This pin functions as a serial interface register readout when the READOUT bit is enabled. When READOUT = 0, this pin forces a logic low and is not put in 3-state.
CTRL1	35	1	Input	Digital control input pins. Together, they control the SNRBoost^{3G}, power-down, and multiplexed modes.
CTRL2	36	1	Input	Digital control input pins. Together, they control the SNRBoost^{3G}, power-down, and multiplexed modes.
CTRL3	37	1	Input	Digital control input pins. Together, they control the SNRBoost^{3G}, power-down, and multiplexed modes.
CLKOUT_P	57	1	Output	Differential output clock, true
CLKOUT_M	56	1	Output	Differential output clock, complement
CHA0_P, CHA0_M	Refer to Figure 2	2	Output	Channel A differential output data pair, 0 and D0 multiplexed
CHA2_P, CHA2_M	Refer to Figure 2	2	Output	Channel A differential output data D1 and D2 (multiplexed and true)
CHA4_P, CHA4_M	Refer to Figure 2	2	Output	Channel A differential output data D3 and D4 (multiplexed and true)
CHA6_P, CHA6_M	Refer to Figure 2	2	Output	Channel A differential output data D5 and D6 (multiplexed and true)
CHA8_P, CHA8_M	Refer to Figure 2	2	Output	Channel A differential output data D7 and D8 (multiplexed and true)
CHA10_P, CHA10_M	Refer to Figure 2	2	Output	Channel A differential output data D9 and D10 (multiplexed and true)
CHB0_P, CHB0_M	Refer to Figure 2	2	Output	Channel B differential output data pair, 0 and D0 multiplexed
CHB2_P, CHB2_M	Refer to Figure 2	2	Output	Channel B differential output data D1 and D2 (multiplexed and true)
CHB4_P, CHB4_M	Refer to Figure 2	2	Output	Channel B differential output data D3 and D4 (multiplexed and true)
CHB6_P, CHB6_M	Refer to Figure 2	2	Output	Channel B differential output data D5 and D6 (multiplexed and true)
CHB8_P, CHB8_M	Refer to Figure 2	2	Output	Channel B differential output data D7 and D8 (multiplexed and true)
CHB10_P, CHB10_M	Refer to Figure 2	2	Output	Channel B differential output data D9 and D10 (multiplexed and true)
DRVDD	1, 48	2	Input	Output buffer supply
DRGND	49, PAD	2	Input	Output buffer ground
NC	Refer to Figure 2	1	—	Do not connect

PIN CONFIGURATION (CMOS MODE)

RGC PACKAGE(3)
QFN-64
(TOP VIEW)



(4) The PowerPAD is connected to DRGND.

(5) NC = no connection.

Figure 3. ADS58C28 CMOS Pinout

Pin Assignments (CMOS Mode)

PIN NAME	PIN NUMBER	# OF PINS	FUNCTION	DESCRIPTION
AVDD	16, 22, 33, 34	4	Input	Analog power supply
AGND	17, 18, 21, 24, 27, 28, 31, 32	8	Input	Analog ground
CLK_P	25	1	Input	Differential clock positive input
CLK_M	26	1	Input	Differential clock negative input
INA_P	29	1	Input	Differential analog positive input, channel A
INA_M	30	1	Input	Differential analog negative input, channel A
INB_P	19	1	Input	Differential analog positive input, channel B
INB_M	20	1	Input	Differential analog negative input, channel B
CM	23	1	Output	This pin outputs the common-mode voltage (0.95V) that can be used externally to bias the analog input pins

Pin Assignments (CMOS Mode) (continued)

PIN NAME	PIN NUMBER	# OF PINS	FUNCTION	DESCRIPTION
RESET	12	1	Input	Serial interface RESET input. When using the serial interface mode, the internal registers must be initialized through a hardware RESET by applying a high pulse on this pin or by using the software reset option; refer to the *Serial Interface Configuration* section. In parallel interface mode, the RESET pin must be permanently tied high. SDATA and SEN are used as parallel control pins in this mode. This pin has an internal 100kΩ pull-down resistor.
SCLK	13	1	Input	This pin functions as a serial interface clock input when RESET is low. It controls the low-speed mode when RESET is tied high; see Table 6 for detailed information. This pin has an internal 100kΩ pull-down resistor.
SDATA	14	1	Input	Serial interface data input; this pin has an internal 100kΩ pull-down resistor.
SEN	15	1	Input	This pin functions as a serial interface enable input when RESET is low. It controls the output interface and data format selection when RESET is tied high; see Table 7 for detailed information. This pin has an internal 150kΩ pull-up resistor to AVDD.
SDOUT	64	1	Output	This pin functions as a serial interface register readout when the READOUT bit is enabled. When READOUT = 0, this pin forces a logic low and is not put in 3-state.
CTRL1	35	1	Input	Digital control input pins. Together, they control various power-down modes.
CTRL2	36	1	Input	Digital control input pins. Together, they control various power-down modes.
CTRL3	37	1	Input	Digital control input pins. Together, they control various power-down modes.
CLKOUT	57	1	Output	CMOS output clock
CHA_D0 to CHA_D10	Refer to Figure 3	11	Output	Channel A ADC output data bits, CMOS levels
CHB_D0 to CHB_D10	Refer to Figure 3	11	Output	Channel B ADC output data bits, CMOS levels
DRVDD	1, 48	2	Input	Output buffer supply
DRGND	49, PAD	2	Input	Output buffer ground
NC	Refer to Figure 3	1	—	Do not connect
UNUSED	56	1	—	This pin is not used in the CMOS interface

FUNCTIONAL BLOCK DIAGRAM

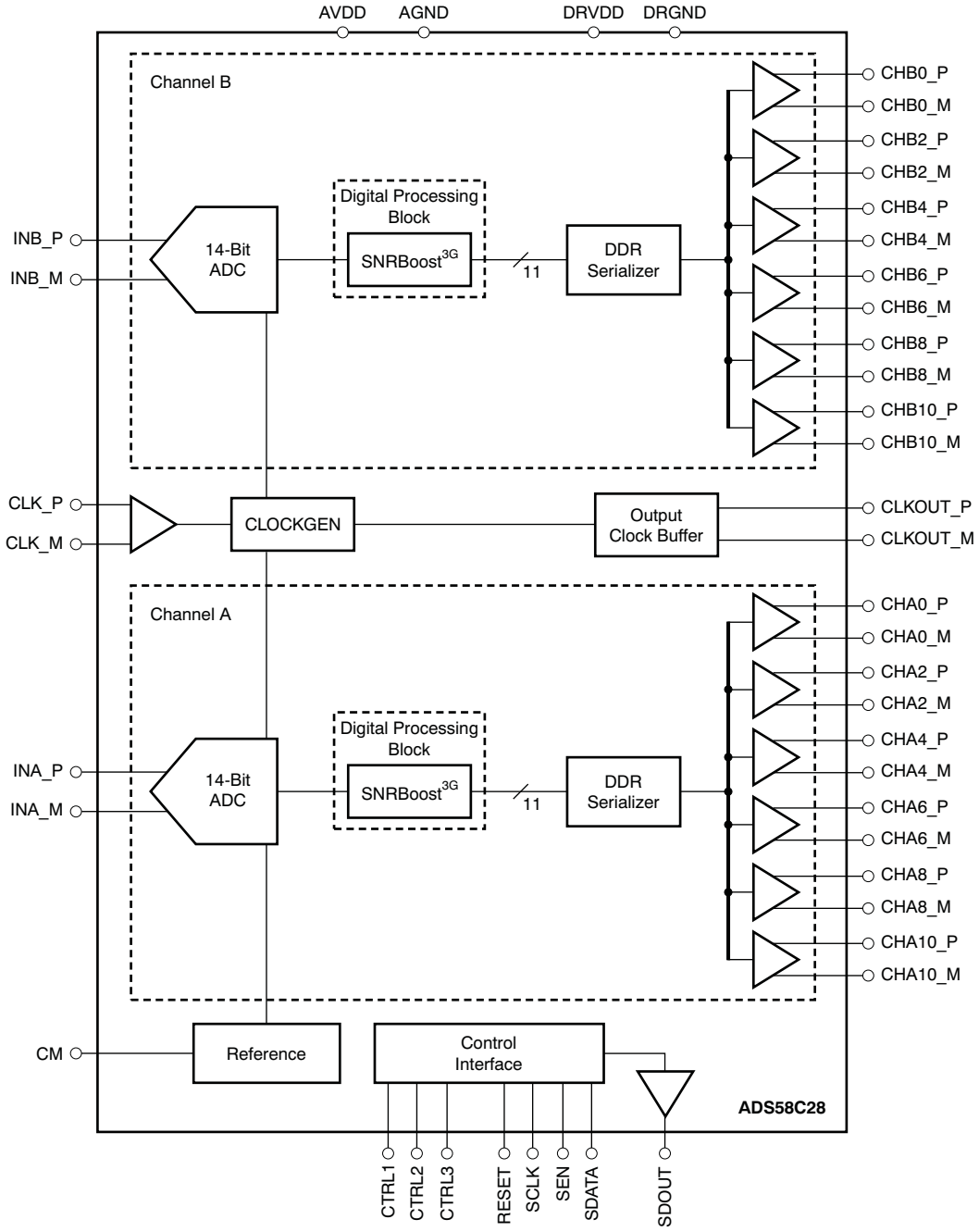


Figure 4. ADS58C28 Block Diagram (LVDS Interface)

TIMING CHARACTERISTICS: LVDS AND CMOS MODES(1)

Typical values are at +25°C, AVDD = 1.8 V, DRVDD = 1.8 V, sampling frequency = 200MSPS, sine wave input clock, C_{LOAD} = 5pF(2), and R_{LOAD} = 100Ω(3), unless otherwise noted.
Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8V, and DRVDD = 1.7V to 1.9V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_A	Aperture delay		0.5	0.8	1.1	ns
	Aperture delay matching	Between the two channels of the same device		±70		ps
	Variation of aperture delay	Between two devices at the same temperature and DRVDD supply		±150		ps
t_J	Aperture jitter			140		f_S rms
	Wakeup time	Time to valid data after coming out of STANDBY mode		50	100	µs
		Time to valid data after coming out of GLOBAL power-down mode		100	500	µs
	ADC latency(4)	Default latency after reset, DIGITAL MODE1 = 0, DIGITAL MODE2 = 0		16		Clock cycles
		SNRBoost3G only enabled, DIGITAL MODE1 = 0, DIGITAL MODE2 = 1		17		Clock cycles
		SNRBoost3G, gain and offset corr enabled, DIGITAL MODE1 = 1, DIGITAL MODE2 = 0 or 1		24		Clock cycles
DDR LVDS MODE(5)						
t_{SU}	Data setup time(6)	Data valid(6) to zero-crossing of CLKOUTP	1.05	1.5		ns
t_H	Data hold time(6)	Zero-crossing of CLKOUTP to data becoming invalid(6)	0.35	0.6		ns
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over *1MSPS ≤ Sampling frequency ≤ 200MSPS*	5.1	6.4	7.7	ns
	LVDS bit clock duty cycle	Duty cycle of differential clock, (CLKOUTP-CLKOUTM) *1MSPS ≤ Sampling frequency ≤ 200MSPS*		50%		
t_{RISE}, t_{FALL}	Data rise time, Data fall time	Rise time measured from –100mV to +100mV Fall time measured from +100mV to –100mV *1MSPS ≤ Sampling frequency ≤ 200MSPS*		0.13		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from –100mV to +100mV Fall time measured from +100mV to –100mV *1MSPS ≤ Sampling frequency ≤ 200MSPS*		0.13		ns
PARALLEL CMOS MODE						
t_{START}	Input clock to data delay	Input clock rising edge crossover to start of data valid		0.06	1.5	ns
t_{DV}	Data valid time	Time interval of data valid	3.1	3.6		ns
	Output clock duty cycle	Duty cycle of output clock, CLKOUT *1MSPS ≤ Sampling frequency ≤ 150MSPS(7)*		44		%
t_{RISE} , t_{FALL}	Data rise time, Data fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD *1 ≤ Sampling frequency ≤ 200MSPS*		1		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time Output clock fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD *1 ≤ Sampling frequency ≤ 150MSPS*		1		ns

(1) Timing parameters are ensured by design and characterization and not tested in production.
(2) C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground
(3) R_{LOAD} is the differential load resistance between the LVDS output pair.
(4) At higher frequencies, t_{PDI} is greater than one clock period and overall latency = ADC latency + 1.
(5) Measurements are done with a transmission line of 100Ω characteristic impedance between the device and the load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(6) Data valid refers to a logic high of +100mV and a logic low of –100mV.
(7) In CMOS mode, the output clock should be used only up to 150MSPS. See Figure 69 for a simple capture scheme above 150MSPS.

Table 3. LVDS Timings at Lower Sampling Frequencies

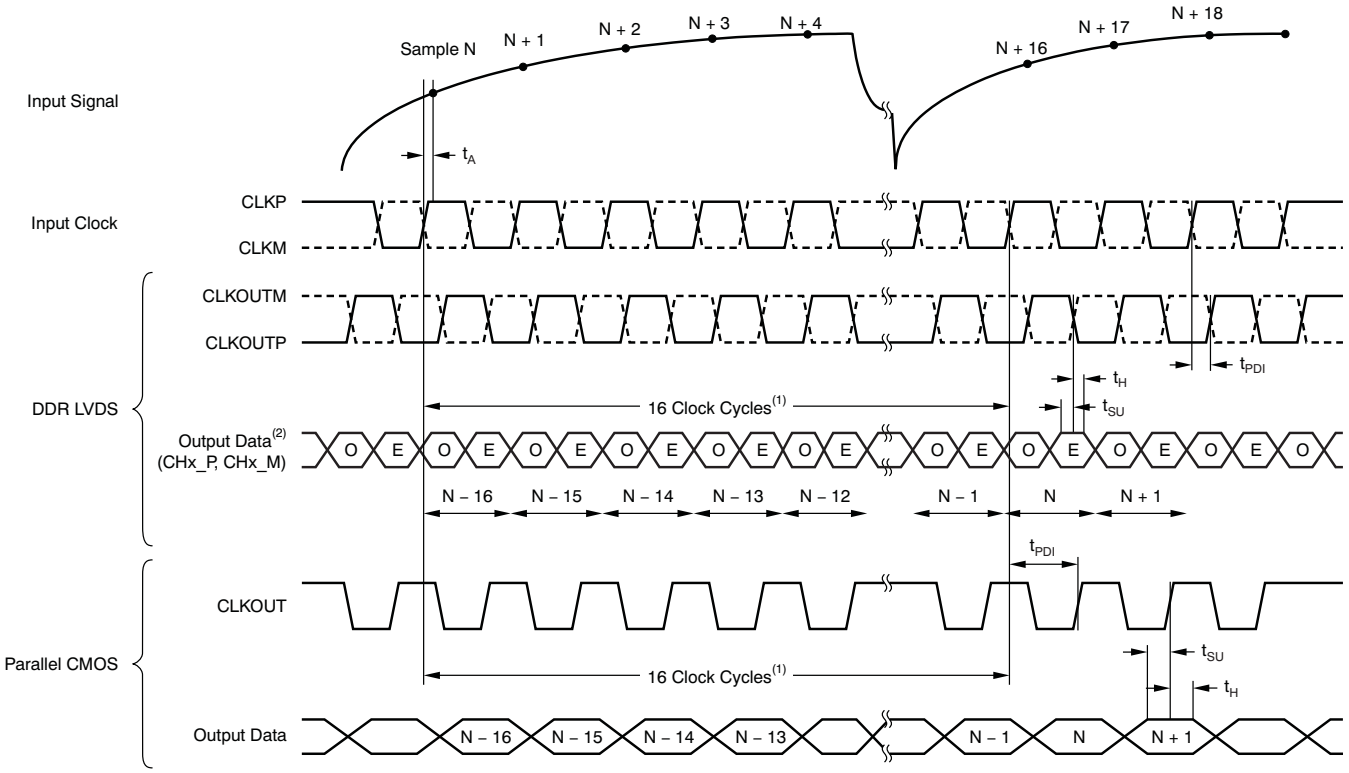
SAMPLING FREQUENCY (MSPS)	SETUP TIME (ns)			HOLD TIME (ns)			t_{PDI}, CLOCK PROPAGATION DELAY (ns)(1)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
185	1.1	1.7		0.35	0.6		5.1	6.4	7.7
170	1.3	1.9		0.35	0.6		5.1	6.4	7.7
150	1.7	2.3		0.35	0.6		5.1	6.4	7.7
125	2.3	3		0.35	0.6		5.1	6.4	7.7

(1) At higher frequencies, t_{PDI} is greater than one clock period and overall latency = ADC latency + 1.

Table 4. CMOS Timings at Lower Sampling Frequencies

SAMPLING FREQUENCY (MSPS)	TIMINGS SPECIFIED WITH RESPECT TO CLKOUT								
	SETUP TIME (ns)			HOLD TIME (ns)			t_{PDI}, CLOCK PROPAGATION DELAY (ns)(1)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
150	1.2	2.6		2.1	2.8		5.5	7	8.5
125	2	3.2		2.8	3.5		5.5	7	8.5
105	2.8	4		3.5	4.2		5.5	7	8.5
80	4.3	5.5		5	5.7		5.5	7	8.5

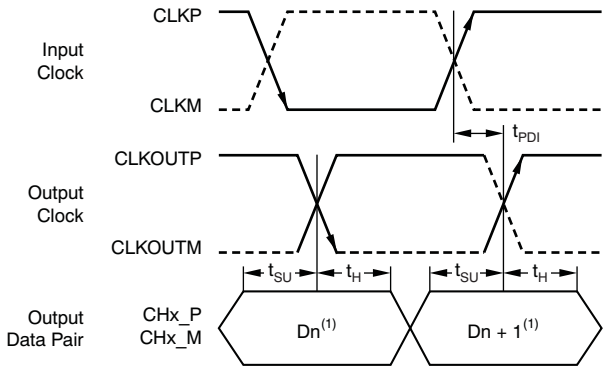
(1) At higher frequencies, t_{PDI} is greater than one clock period and overall latency = ADC latency + 1.



(1) ADC latency after reset; at higher frequencies, t_{PDI} is greater than one clock period and overall latency = ADC latency + 1.

(2) E = even bits (D0, D2, D4, etc.); O = odd bits (D1, D3, D5, etc.).

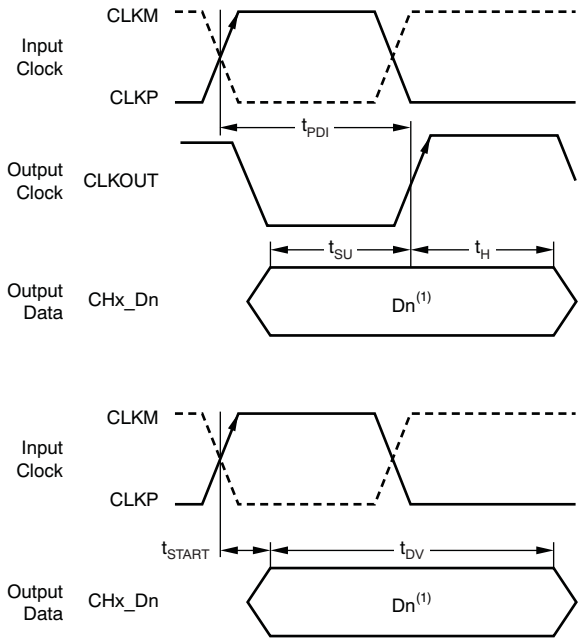
Figure 5. Latency Diagram



(1) Dn = bits D0, D2, D4, etc.

(2) Dn + 1 = bits D1, D3, D5, etc.

Figure 6. LVDS Mode Timing



(1) Dn = bits D0, D1, D2, etc. of channels A and B.

Figure 7. CMOS Mode Timing

DEVICE CONFIGURATION

The ADS58C28 can be configured independently using either parallel interface control or serial interface programming.

PARALLEL CONFIGURATION ONLY

To put the device into parallel configuration mode, keep RESET tied high (AVDD). Then, use the SEN, SCLK, CTRL1, CTRL2, and CTRL3 pins to directly control certain modes of the ADC. The device can be easily configured by connecting the parallel pins to the correct voltage levels (as described in Table 5 to Table 8). There is no need to apply a reset and SDATA can be connected to ground.

In this mode, SEN and SCLK function as parallel interface control pins. Some frequently-used functions can be controlled using these pins. Table 5 describes the modes controlled by the parallel pins.

Table 5. Parallel Pin Definition

PIN	CONTROL MODE
SCLK	Low-speed mode selection
SEN	Output data format and output interface selection
CTRL1	Together, these pins control the SNRBoost^{3G} and power-down modes.
CTRL2	
CTRL3	

SERIAL INTERFACE CONFIGURATION ONLY

To exercise this mode, the serial registers must first be reset to the default values and the RESET pin must be kept low. SEN, SDATA, and SCLK function as serial interface pins in this mode and can be used to access the internal registers of the ADC. The registers can be reset either by applying a pulse on the RESET pin or by setting the RESET bit high. The *Serial Register Map* section describes the register programming and the register reset process in more detail.

USING BOTH SERIAL INTERFACE AND PARALLEL CONTROLS

For increased flexibility, a combination of serial interface registers and parallel pin controls (CTRL1 to CTRL3) can also be used to configure the device. To enable this flexibility, keep RESET low. The parallel interface control pins CTRL1 to CTRL3 are available. After power-up, the device is automatically configured according to the voltage settings on these pins (see Table 8). SEN, SDATA, and SCLK function as serial interface digital pins and are used to access the internal registers of the ADC. The registers must first be reset to the default values either by applying a pulse on the RESET pin or by setting the RESET bit to '1'. After reset, the RESET pin must be kept low. The *Serial Register Map* section describes register programming and the register reset process in more detail.

DETAILS OF PARALLEL CONFIGURATION ONLY

The functions controlled by each parallel pin are described in Table 6, Table 7, and Table 8. A simple way of configuring the parallel pins is shown in Figure 8.

Table 6. SCLK Control Pin

VOLTAGE APPLIED ON SCLK	DESCRIPTION
0V to 0.9V	Low-speed mode is disabled
0.9V to AVDD	Low-speed mode is enabled

Table 7. SEN Control Pin

VOLTAGE APPLIED ON SEN	DESCRIPTION
0 (+50mV/–0mV)	Twos complement and parallel CMOS output
(3/8) AVDD (±50mV)	Offset binary and parallel CMOS output
(5/8) 2AVDD (±50mV)	Offset binary and DDR LVDS output
AVDD (+0mV/–50mV)	Twos complement and DDR LVDS output

Table 8. CTRL1, CTRL2, and CTRL3 Pins

CTRL1	CTRL2	CTRL3	DESCRIPTION
Low	Low	Low	Normal operation; SNRBoost^{3G} disabled for both channels
Low	Low	High	SNRBoost^{3G} enabled for channel B
Low	High	Low	SNRBoost^{3G} enabled for channel A
Low	High	High	SNRBoost^{3G} enabled for channel A and B
High	Low	Low	Global power-down
High	Low	High	Channel A powered down, channel B is active
High	High	Low	Do not use
High	High	High	MUX mode of operation, channel A and B data are multiplexed and output on the CHB_D[10:0] pins.

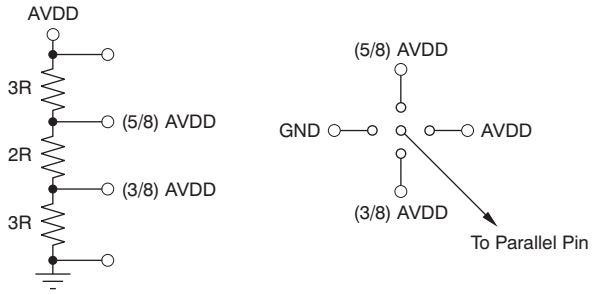


Figure 8. Simple Scheme to Configure the Parallel Pins

DETAILS OF SERIAL INTERFACE

The ADC has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), and SDATA (serial interface data) pins. Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA are latched at every SCLK falling edge when SEN is active (low). The serial data are loaded into the register at every 16th SCLK falling edge when SEN is low. When the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse. The first eight bits form the register address and the remaining eight bits are the register data. The interface can work with SCLK frequencies from 20MHz down to very low speeds (of a few hertz) and also with non-50% SCLK duty cycle.

Register Initialization

After power-up, the internal registers must be initialized to the default values. This initialization can be accomplished in one of two ways:

1. Either through hardware reset by applying a high pulse on the RESET pin (of width greater than 10ns), as shown in Figure 9; or
2. By applying a software reset. When using the serial interface, set the RESET bit (D7 in register 00h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

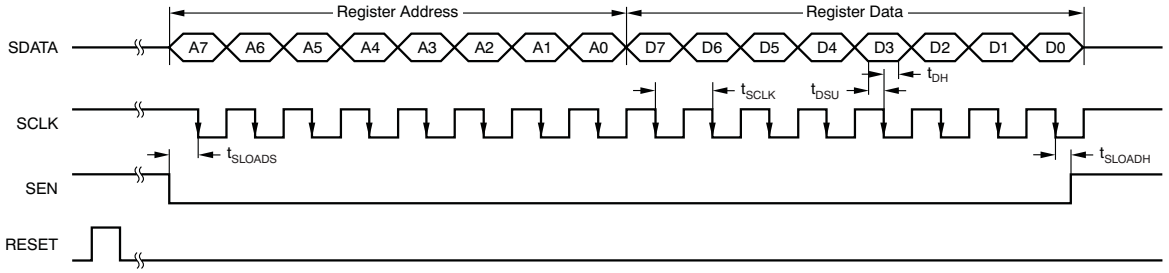


Figure 9. Serial Interface Timing

Table 9. Serial Interface Timing Characteristics(1)

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to $1/t_{SCLK}$)	> DC		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DSU}	SDATA setup time	25			ns
t_{DH}	SDATA hold time	25			ns

(1) Typical values at +25°C; minimum and maximum values across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8V, and DRVDD = 1.8V, unless otherwise noted.

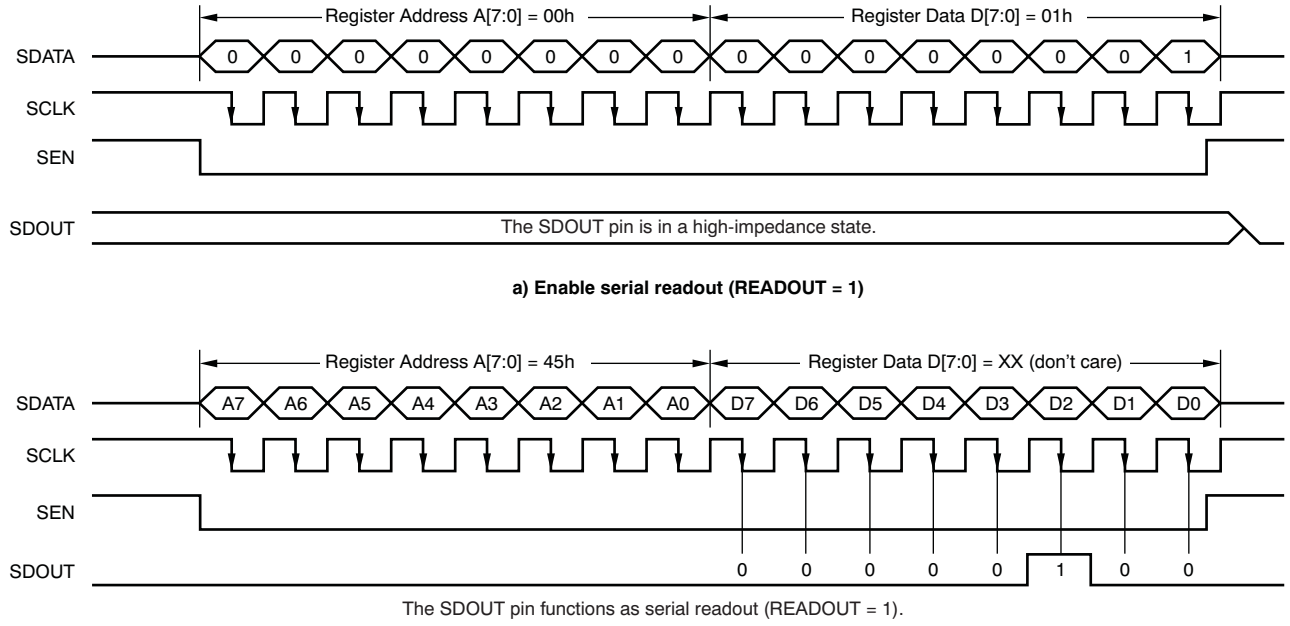
Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back. This readback mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

1. Set the READOUT register bit to '1'. This setting disables any further writes to the registers.
2. Initiate a serial interface cycle specifying the address of the register (A7 to A0) whose content has to be read.
3. The device outputs the contents (D7 to D0) of the selected register on the SDOUT pin (pin 64).
4. The external controller can latch the contents at the SCLK falling edge.
5. To enable register writes, reset the READOUT register bit to '0'.

The serial register readout works with both CMOS and LVDS interfaces on pin 64.

When READOUT is disabled, the SDOUT pin is in a high-impedance mode. If serial readout is not used, the SDOUT pin must float.



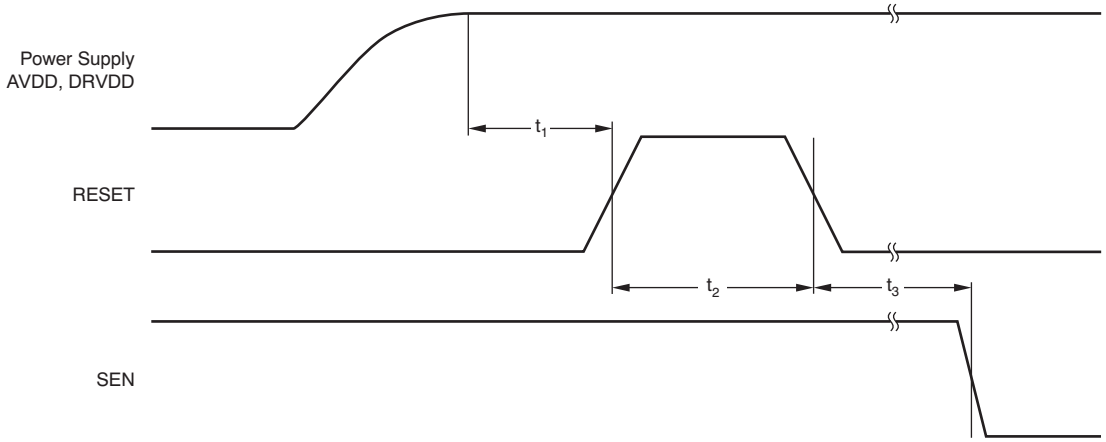
(1) The SDOUT pin functions as a serial readout (READOUT = 1).

Figure 10. Serial Readout Timing Diagram

Table 10. Reset Timing (Only when Serial Interface is Used)(1)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from AVDD and DRVDD power-up to active RESET pulse	1			ms
t_2	Reset pulse width	Active RESET signal pulse width	10			ns
					1	µs
t_3	Register write delay	Delay from RESET disable to SEN active	100			ns

(1) Typical values at +25°C; minimum and maximum values across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, unless otherwise noted.



NOTE: A high pulse on the RESET pin is required in the serial interface mode when initialized through a hardware reset. For parallel interface operation, RESET must be permanently tied high.

Figure 11. Reset Timing Diagram

SERIAL REGISTER MAP

Table 11 summarizes the functions supported by the serial interface.

Table 11. Serial Interface Register Map(1)

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
00	0	0	0	0	0	0	RESET	READOUT
01	LVDS SWING						0	0
03	0	0	0	0	0	0	HIGH PERF MODE	
25	CH A GAIN				0	CH A TEST PATTERNS		
26	0	CH A SNRBoost3G FILTER NUMBER						
28	0	CH A SNRBoost3G ON	0	0	0	0	0	0
29	0	0	0	DATA FORMAT		0	0	0
2B	CH B GAIN				0	CH B TEST PATTERNS		
2D	0	CH B SNRBoost3G FILTER NUMBER						
2E	0	CH B SNRBoost3G ON	0	0	0	0	0	0
3D	0	0	ENABLE OFFSET CORR	0	0	0	0	0
3F	0	0	CUSTOM PATTERN D[10:5]					
40	CUSTOM PATTERN D[4:0]					0	0	0
41	LVDS CMOS		CMOS CLKOUT STRENGTH		0	0	0	0
42	0	0	0	0	DIGITAL MODE 1	0	0	0
44	0	0	0	0	0	0	0	DIGITAL MODE 2
45	STBY	LVDS CLKOUT STRENGTH	LVDS DATA STRENGTH	0	0	PDN GLOBAL	0	0
4A	0	0	0	0	0	0	0	HIGH FREQ MODE CH B
58	0	0	0	0	0	0	0	HIGH FREQ MODE CH A
BF	CH A OFFSET PEDESTAL			0	0	0	0	0
C1	CH B OFFSET PEDESTAL			0	0	0	0	0
CF	FREEZE OFFSET CORR	0	OFFSET CORR TIME CONSTANT				0	0
DB	0	0	0	0	0	0	0	LOW SPEED MODE CH B
EA	OVERRIDE SNRBoost3G PINS	0	0	0	0	0	0	0
EF	0	0	0	EN LOW SPEED MODE	0	0	0	0
F1	0	0	0	0	0	0	EN LVDS SWING	
F2	0	0	0	0	LOW SPEED MODE CH A	0	0	0

(1) All registers default to '0' after reset.

DESCRIPTION OF SERIAL REGISTERS

Register Address 00h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	RESET	READOUT

Bits[7:2] **Always write '0'**

Bit 1 **RESET: Software reset applied**

This bit resets all internal registers to the default values and self-clears to 0 (default = 1).

Bit 0 **READOUT: Serial readout**

This bit sets the serial readout of the registers.
0 = Serial readout of registers disabled; the SDOUT pin is placed in a high-impedance state.
1 = Serial readout enabled; the SDOUT pin functions as a serial data readout with CMOS logic levels running from the DRVDD supply. See the *Serial Register Readout* section.

Register Address 01h (Default = 00h)

7	6	5	4	3	2	1	0
LVDS SWING						0	0

Bits[7:2] **LVDS SWING: LVDS swing programmability**

These bits program the LVDS swing. Set the EN LVDS SWING bit to '1' before programming swing.
000000 = Default LVDS swing; ±350mV with external 100Ω termination
011011 = LVDS swing increases to ±410mV
110010 = LVDS swing increases to ±465mV
010100 = LVDS swing increases to ±570mV
111110 = LVDS swing increases to ±200mV
001111 = LVDS swing increases to ±125mV

Bits[1:0] **Always write '0'**

Register Address 03h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	HIGH PERF MODE	

Bits[7:2] **Always write '0'**

Bits[1:0] **HIGH PERF MODE: High-performance mode**

These bits enable LVDS swing control using the LVDS SWING register bits.
00 = Default performance
01 = Do not use
10 = Do not use
11 = Obtain best performance across sample clock and input signal frequencies

Register Address 25h (Default = 00h)

7	6	5	4	3	2	1	0
CH A GAIN				0	CH A TEST PATTERNS		

Bits[7:4] CH A GAIN: Channel A gain programmability

These bits set the gain programmability in 0.5dB steps for channel A.

0000 = 0dB gain (default after reset)
0001 = 0.5dB gain
0010 = 1dB gain
0011 = 1.5dB gain
0100 = 2dB gain
0101 = 2.5dB gain
0110 = 3dB gain
0111 = 3.5dB gain
1000 = 4dB gain
1001 = 4.5dB gain
1010 = 5dB gain
1011 = 5.5dB gain
1100 = 6dB gain

Bit 3 Always write '0'

Bits[2:0] CH A TEST PATTERNS: Channel A data capture

These bits verify data capture for channel A; see Table 12.
000 = Normal operation
001 = Outputs all 0s
010 = Outputs all 1s
011 = Outputs toggle pattern; D[10:0] output data are an alternating sequence of *10101010101* and *01010101010*
100 = Outputs digital ramp; output data increments by 1LSB (11 bits) every eighth clock cycle from code 0 to code 2047
101 = Outputs custom pattern; use registers 3Fh and 40h to set the custom pattern
110 = Unused
111 = Unused

Register Address 26h (Default = 00h)

7	6	5	4	3	2	1	0
0	CH A SNRBoost^{3G} FILTER NUMBER						

Bit 7 Always write '0'

Bits[6:0] CH A SNRBoost^{3G} FILTER NUMBER: Channel A SNRBoost^{3G} filter selection

These bits select any one of 55 SNRBoost^{3G} filters for channel A **only** after selecting the appropriate mode from Table 12; refer to the *SNR Enhancement Using SNRBoost* section.

Register Address 28h (Default = 00h)

7	6	5	4	3	2	1	0
0	CH A SNRBoost^{3G} ON	0	0	0	0	0	0

Bit 7 Always write '0'

Bit 6 CH A SNRBoost^{3G} ON: Channel A SNRBoost^{3G} setting

This bit sets the SNRBoost^{3G} for channel A
0 = SNRBoost^{3G} for channel A is off
1 = SNRBoost^{3G} for channel A is on

Bits[5:0] Always write '0'

Register Address 29h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	DATA FORMAT		0	0	0

Bits[7:5] Always write '0'

Bits[4:3] DATA FORMAT: Data format selection

00 = Twos complement
01 = Twos complement
10 = Twos complement
11 = Offset binary

Bits[2:0] Always write '0'

Register Address 2Bh (Default = 00h)

7	6	5	4	3	2	1	0
CH B GAIN				0	CH B TEST PATTERNS		

Bits[7:4] CH B GAIN: Channel B gain programmability

These bits set the gain programmability in 0.5dB steps for channel B.

0000 = 0dB gain (default after reset)
0001 = 0.5dB gain
0010 = 1dB gain
0011 = 1.5dB gain
0100 = 2dB gain
0101 = 2.5dB gain
0110 = 3dB gain
0111 = 3.5dB gain
1000 = 4dB gain
1001 = 4.5dB gain
1010 = 5dB gain
1011 = 5.5dB gain
1100 = 6dB gain

Bit 3 Always write '0'

Bits[2:0] CH B TEST PATTERNS: Channel B data capture

These bits verify data capture for channel B; see Table 12.
000 = Normal operation
001 = Outputs all 0s
010 = Outputs all 1s
011 = Outputs toggle pattern; D[10:0] output data are an alternating sequence of *10101010101* and *01010101010*
100 = Outputs digital ramp; output data increments by 1LSB (11 bits) every eighth clock cycle from code 0 to code 2047
101 = Outputs custom pattern; use registers 3Fh and 40h to set the custom pattern
110 = Unused
111 = Unused

Register Address 2Dh (Default = 00h)

7	6	5	4	3	2	1	0
0	CH B SNRBoost^{3G} FILTER NUMBER						

Bit 7 **Always write '0'**

Bits[6:0] **CH B SNRBoost^{3G} FILTER NUMBER: Channel B SNRBoost^{3G} filter selection**

These bits select any one of 55 SNRBoost^{3G} filters for channel B **only** after selecting the appropriate mode from Table 12; refer to the *SNR Enhancement Using SNRBoost* section.

Register Address 2Eh (Default = 00h)

7	6	5	4	3	2	1	0
0	CH B SNRBoost^{3G} ON	0	0	0	0	0	0

Bit 7 **Always write '0'**

Bit 6 **CH B SNRBoost^{3G} ON: Channel B SNRBoost^{3G} setting**

This bit sets the SNRBoost^{3G} for channel B
0 = SNRBoost^{3G} for channel B is off
1 = SNRBoost^{3G} for channel B is on

Bits[5:0] **Always write '0'**

Register Address 3Dh (Default = 00h)

7	6	5	4	3	2	1	0
0	0	ENABLE OFFSET CORR	0	0	0	0	0

Bits[7:6] **Always write '0'**

Bit 5 **ENABLE OFFSET CORR: Offset correction setting**

This bit sets the offset correction; see Table 12.
0 = Offset correction disabled
1 = Offset correction enabled

Bits[4:0] **Always write '0'**

Register Address 3Fh (Default = 00h)

7	6	5	4	3	2	1	0
0	0	CUSTOM PATTERN D10	CUSTOM PATTERN D9	CUSTOM PATTERN D8	CUSTOM PATTERN D7	CUSTOM PATTERN D6	CUSTOM PATTERN D5

Bits[7:6] **Always write '0'**

Bits[7:0] **CUSTOM PATTERN D[10:5]**

These are the six custom pattern upper bits available at output instead of ADC data.

Register Address 40h (Default = 00h)

7	6	5	4	3	2	1	0
CUSTOM PATTERN D4	CUSTOM PATTERN D3	CUSTOM PATTERN D2	CUSTOM PATTERN D1	CUSTOM PATTERN D0	0	0	0

Bits[7:3] **CUSTOM PATTERN D[4:0]**

These are the five lower custom pattern bits available at output instead of ADC data.

Bits[2:0] **Always write '0'**

Register Address 41h (Default = 00h)

7	6	5	4	3	2	1	0
LVDS CMOS		CMOS CLKOUT STRENGTH		0	0	0	0

Bits[7:6] LVDS CMOS: Interface selection

These bits select the interface.
00 = DDR LVDS interface
01 = Parallel CMOS interface
10 = Parallel CMOS interface
11 = Parallel CMOS interface

Bits[5:4] CMOS CLKOUT STRENGTH

These bits control the strength of the CMOS output clock.
00 = Maximum strength (recommended)
01 = Medium strength
10 = Low strength
11 = Very low strength

Bits[3:0] Always write '0'

Register Address 42h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	DIGITAL MODE 1	0	0	0

Bits[7:4] Always write '0'

Bit 3 DIGITAL MODE 1

See Table 12.

Bits[2:0] Always write '0'

Register Address 44h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DIGITAL MODE 2

Bits[7:1] Always write '0'

Bit 0 DIGITAL MODE 2

Refer to the *Digital Functions* section.

Register Address 45h (Default = 00h)

7	6	5	4	3	2	1	0
STBY	LVDS CLKOUT STRENGTH	LVDS DATA STRENGTH	0	0	PDN GLOBAL	0	0

Bit 7 **STBY: Standby setting**

0 = Normal operation
1 = Both channels are put in standby; wakeup time from this mode is fast (typically 50µs).

Bit 6 **LVDS CLKOUT STRENGTH: LVDS output clock buffer strength setting**

0 = LVDS output clock buffer at default strength to be used with 100Ω external termination
1 = LVDS output clock buffer has double strength to be used with 50Ω external termination

Bit 5 **LVDS DATA STRENGTH**

0 = All LVDS data buffers at default strength to be used with 100Ω external termination
1 = All LVDS data buffers have double strength to be used with 50Ω external termination

Bits[4:3] **Always write '0'**

Bit 2 **PDN GLOBAL**

0 = Normal operation
1 = Total power down; all ADC channels, internal references, and output buffers are powered down. Wakeup time from this mode is slow (typically 100µs).

Bits[1:0] **Always write '0'**

Register Address 4Ah (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	HIGH FREQ MODE CH B

Bits[7:1] **Always write '0'**

Bit 0 **HIGH FREQ MODE CH B: Channel B high-frequency mode selection**

This bit configures the high-frequency mode for channel B. This bit is recommended for high input signal frequencies greater than 200MHz.
0 = Default performance after reset
1 = Set this bit for each channel for high input frequencies

Register Address 58h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	HIGH FREQ MODE CH A

Bits[7:1] **Always write '0'**

Bit 0 **HIGH FREQ MODE CH A: Channel A high-frequency mode selection**

This bit configures the high-frequency mode for channel A. This bit is recommended for high input signal frequencies greater than 200MHz.
0 = Default performance after reset
1 = Set this bit for each channel for high input frequencies

Register Address BFh (Default = 00h)

7	6	5	4	3	2	1	0
CH A OFFSET PEDESTAL			0	0	0	0	0

Bits[7:5] CH A OFFSET PEDESTAL: Channel A offset pedestal selection

When the offset correction is enabled, the final converged value after the offset is corrected is the ADC midcode value. A pedestal can be added to the final converged value by programming these bits. See the *Offset Correction* section. Channels can be independently programmed for different offset pedestals by choosing the relevant register address.

100 = Pedestal is 4LSB
011 = Pedestal is 3LSB
010 = Pedestal is 2LSB
001 = Pedestal is 1LSB
000 = Pedestal is 0LSB
111 = Pedestal is –1LSB
110 = Pedestal is –2LSB
101 = Pedestal is –3LSB

Bits[4:0] Always write '0'

Register Address C1h (Default = 00h)

7	6	5	4	3	2	1	0
CH B OFFSET PEDESTAL			0	0	0	0	0

Bits[7:5] CH B OFFSET PEDESTAL: Channel B offset pedestal selection

When the offset correction is enabled, the final converged value after the offset is corrected is the ADC midcode value. A pedestal can be added to the final converged value by programming these bits. See the *Offset Correction* section. Channels can be independently programmed for different offset pedestals by choosing the relevant register address.

100 = Pedestal is 4LSB
011 = Pedestal is 3LSB
010 = Pedestal is 2LSB
001 = Pedestal is 1LSB
000 = Pedestal is 0LSB
111 = Pedestal is –1LSB
110 = Pedestal is –2LSB
101 = Pedestal is –3LSB

Bits[4:0] Always write '0'

Register Address CFh (Default = 00h)

7	6	5	4	3	2	1	0
FREEZE OFFSET CORR	0	OFFSET CORR TIME CONSTANT				0	0

Bit 7 **FREEZE OFFSET CORR: Freeze offset correction setting**

This bit sets the freeze offset correction estimation.
0 = Estimation of offset correction is not frozen (the EN OFFSET CORR bit must be set)
1 = Estimation of offset correction is frozen (the EN OFFSET CORR bit must be set); when frozen, the last estimated value is used for offset correction of every clock cycle. See the *Offset Correction* section.

Bit 6 **Always write '0'**

Bits[5:2] **OFFSET CORR TIME CONSTANT**

The offset correction loop time constant in number of clock cycles. Refer to the *Offset Correction* section.

Bits[1:0] **Always write '0'**

Register Address DBh (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	LOW SPEED MODE CH B

Bits[7:1] **Always write '0'**

Bit 0 **LOW SPEED MODE CH B: Channel B low-speed mode enable**

This bit enables the low-speed mode for channel B. Set the EN LOW SPEED MODE bit to '1' before using this bit.
0 = Low-speed mode is disabled for channel B
1 = Low-speed mode is enabled for channel B

Register Address EAh (Default = 00h)

7	6	5	4	3	2	1	0
OVERRIDE SNRBoost^{3G} PINS	0	0	0	0	0	0	0

Bit 7 **OVERRIDE SNRBoost^{3G} PINS**

Refer to the *SNR Enhancement Using SNRBoost* section.

Bits[6:0] **Always write '0'**

Register Address EFh (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	EN LOW SPEED MODE	0	0	0	0

Bits[7:5] **Always write '0'**

Bit 4 **EN LOW SPEED MODE: Enable control of low-speed mode through serial register bits**

This bit enables the control of the low-speed mode using the ENABLE LOW SPEED MODE CH B and ENABLE LOW SPEED MODE CH A register bits.
0 = Low-speed mode is controlled by dc voltage on the SCLK pin
1 = Low-speed mode is controlled by serial register bits

Bits[3:0] **Always write '0'**

Register Address F1h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	EN LVDS SWING	

Bits[7:2] **Always write '0'**

Bits[1:0] **EN LVDS SWING: LVDS swing enable**

These bits enable LVDS swing control using the LVDS SWING register bits.
00 = LVDS swing control using the LVDS SWING register bits is disabled
01 = Do not use
10 = Do not use
11 = LVDS swing control using the LVDS SWING register bits is enabled

Register Address F2h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	LOW SPEED MODE CH A	0	0	0

Bits[7:4] **Always write '0'**

Bit 3 **LOW SPEED MODE CH A: Channel A low-speed mode enable**

This bit enables the low-speed mode for channel A. Set the EN LOW SPEED MODE bit to '1' before using this bit.
0 = Low-speed mode is disabled for channel A
1 = Low-speed mode is enabled for channel A

Bits[2:0] **Always write '0'**

TYPICAL CHARACTERISTICS

All graphs are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock. 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High Perf Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

FFT FOR 20MHz INPUT SIGNAL

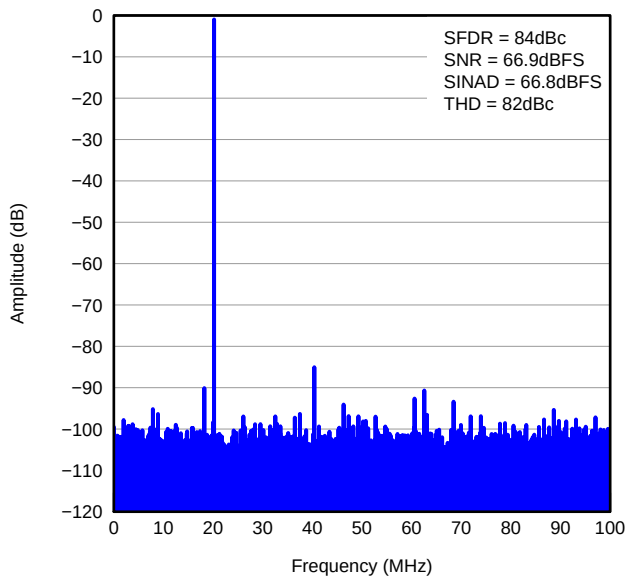


Figure 12.

FFT FOR 170MHz INPUT SIGNAL

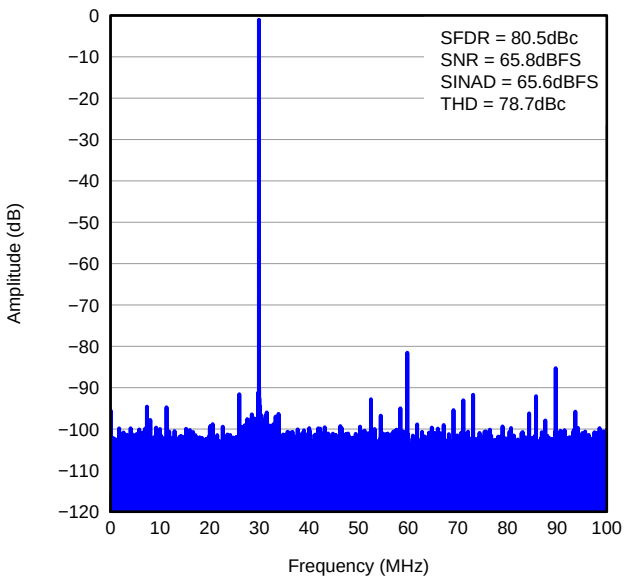


Figure 13.

FFT FOR 270MHz INPUT SIGNAL

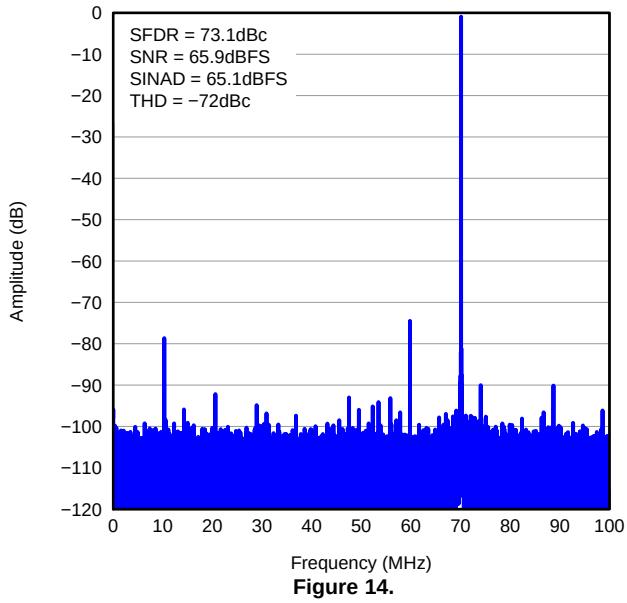


Figure 14.

TYPICAL CHARACTERISTICS (continued)

All graphs are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock. $1.5V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High Perf Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

FFT FOR TWO-TONE INPUT SIGNAL

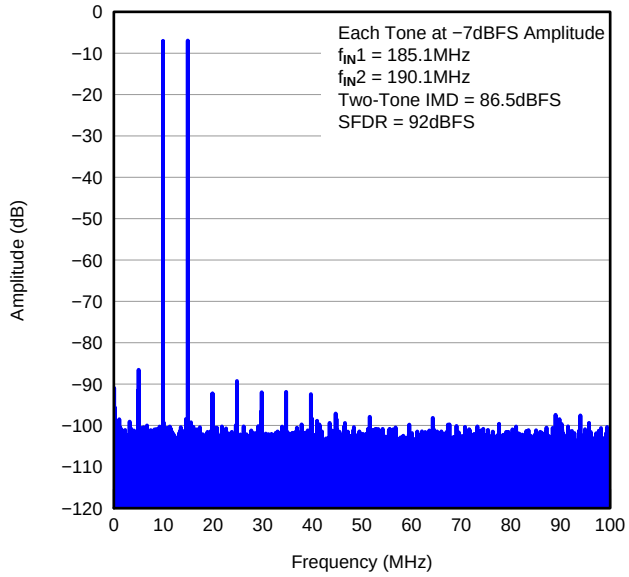


Figure 15.

FFT FOR TWO-TONE INPUT SIGNAL

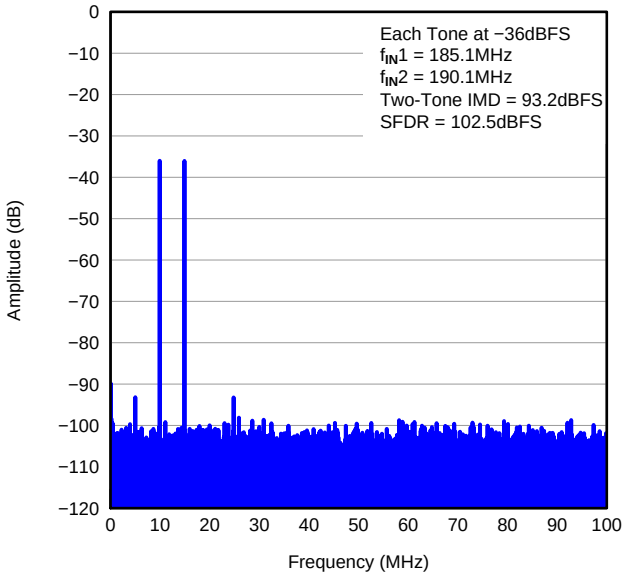


Figure 16.

FFT WITH SNRBoost^{3G} ENABLED (60MHz Bandwidth)

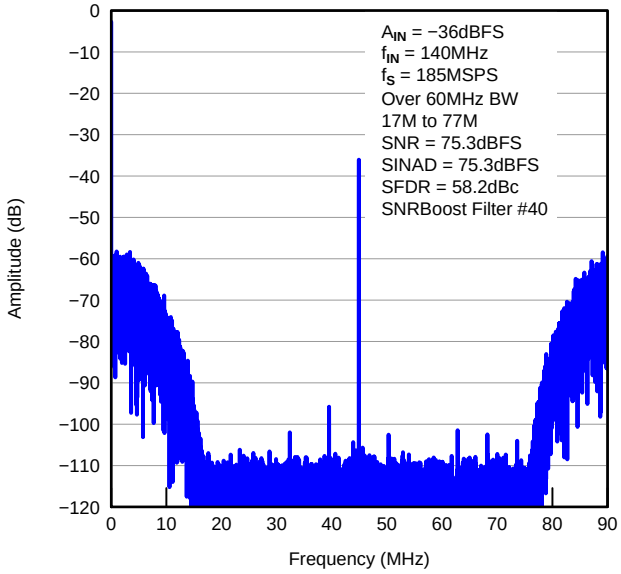


Figure 17.

FFT WITH SNRBoost^{3G} ENABLED (60MHz Bandwidth)

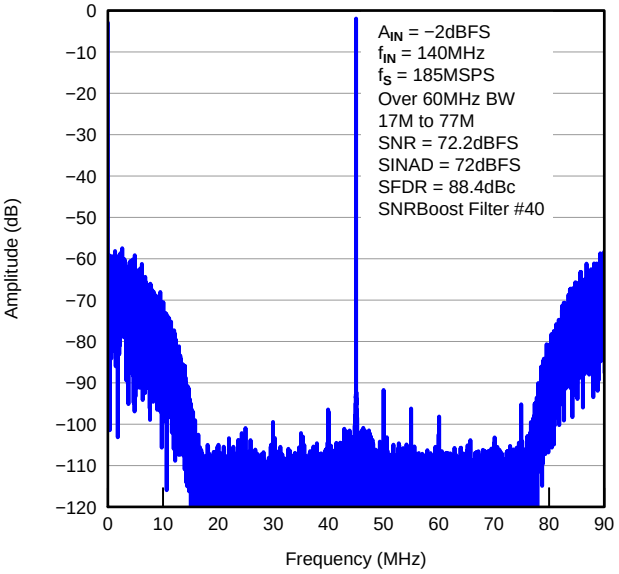


Figure 18.

TYPICAL CHARACTERISTICS (continued)

All graphs are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock. $1.5V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High Perf Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

FFT WITH SNRBoost^{3G} ENABLED (40MHz Bandwidth)

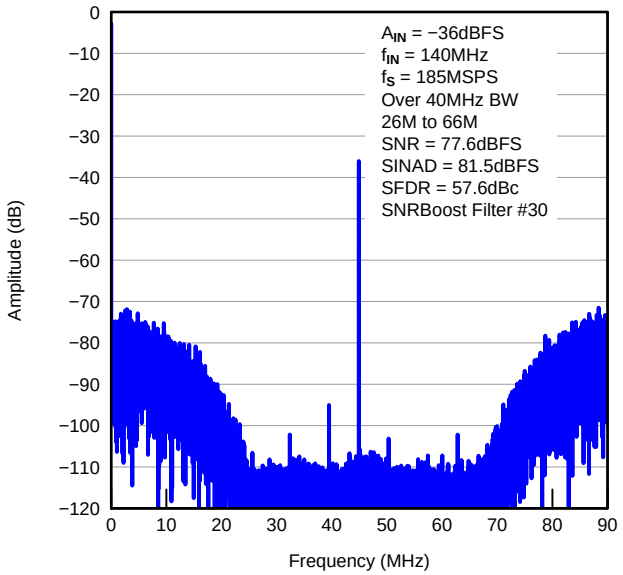


Figure 19.

FFT WITH SNRBoost^{3G} ENABLED (40MHz Bandwidth)

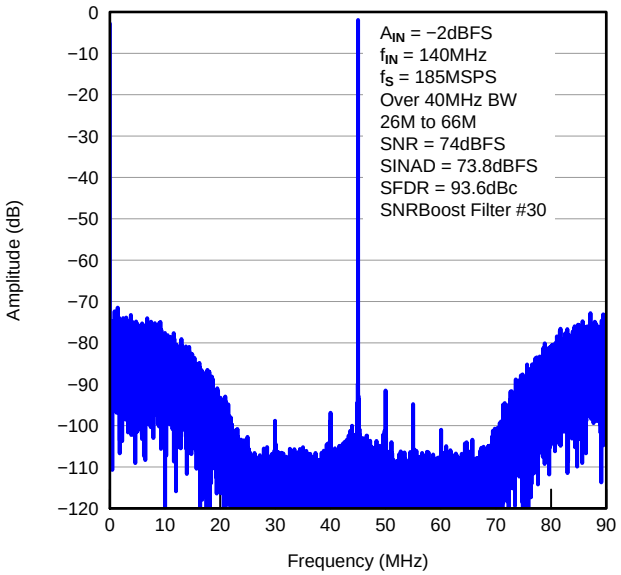


Figure 20.

FFT WITH SNRBoost^{3G} ENABLED (30MHz Bandwidth)

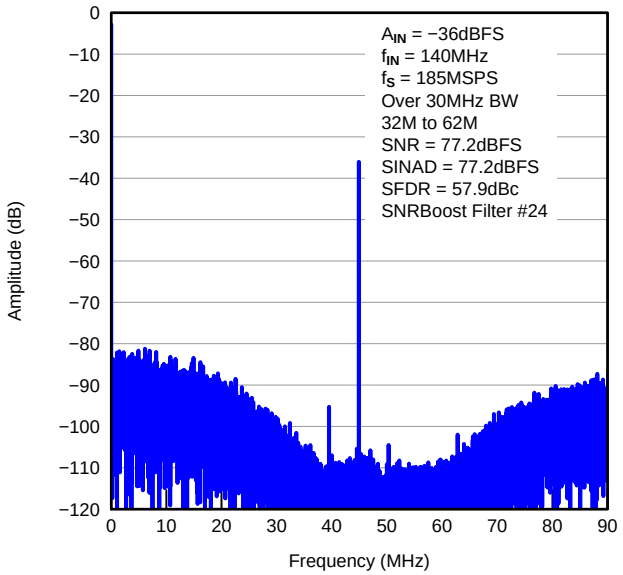


Figure 21.

FFT WITH SNRBoost^{3G} ENABLED (30MHz Bandwidth)

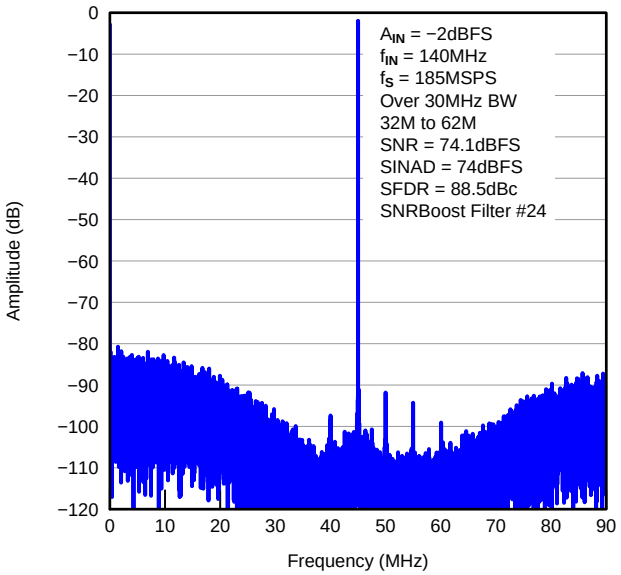


Figure 22.

TYPICAL CHARACTERISTICS (continued)

All graphs are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock. 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High Perf Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

FFT WITH SNRBoost^{3G} ENABLED (20MHz Bandwidth)

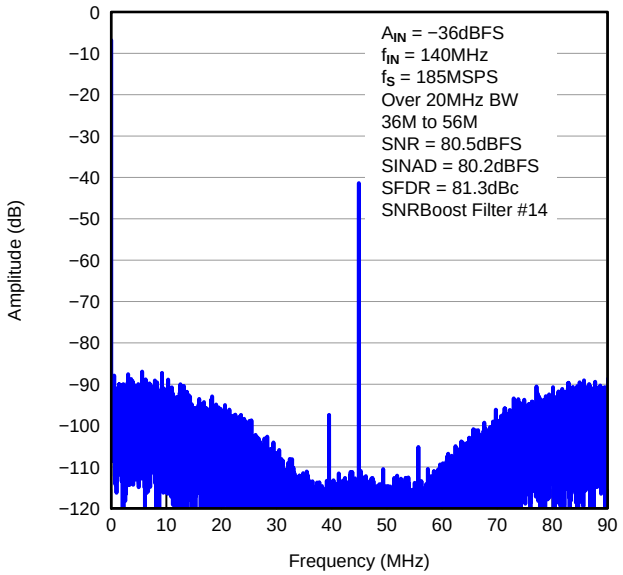


Figure 23.

FFT WITH SNRBoost^{3G} ENABLED (20MHz Bandwidth)

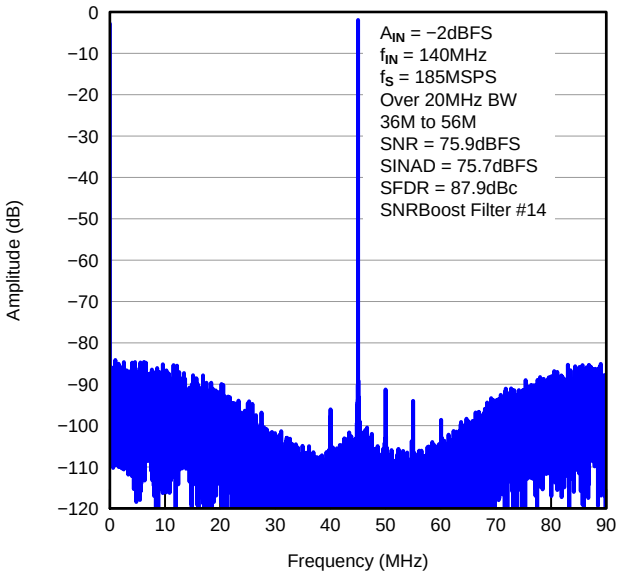


Figure 24.

TIME DOMAIN WAVEFORM OF UNWRAP SIGNAL DISABLED

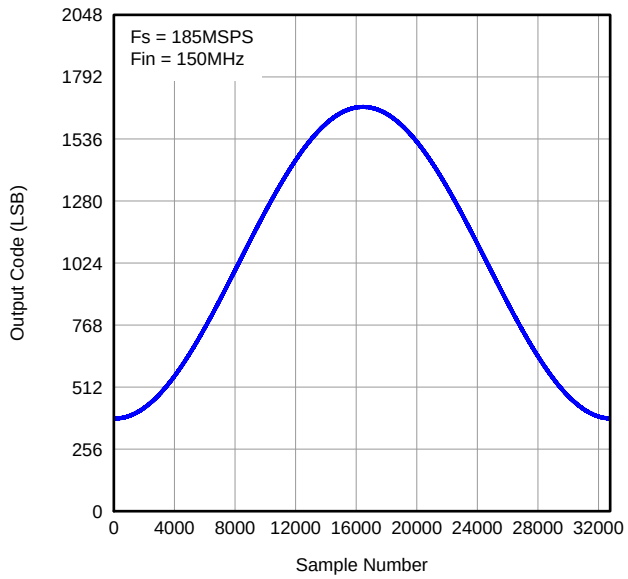


Figure 25.

TIME DOMAIN WAVEFORM OF UNWRAP SIGNAL ENABLED

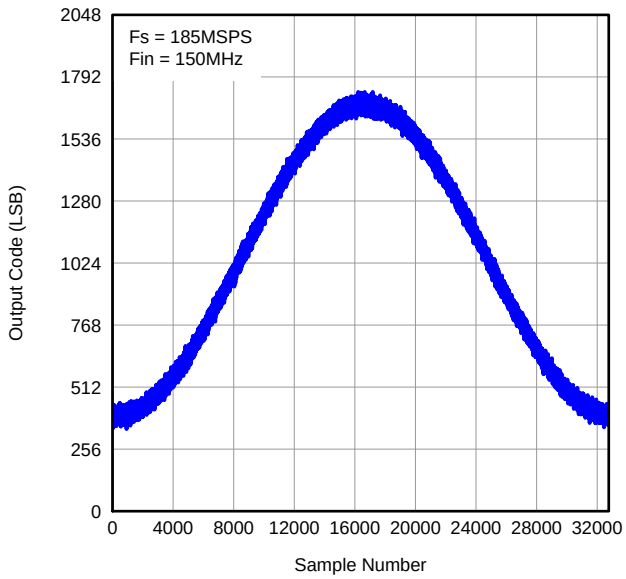


Figure 26.

TYPICAL CHARACTERISTICS (continued)

All graphs are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock. 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High Perf Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

SFDR vs INPUT FREQUENCY

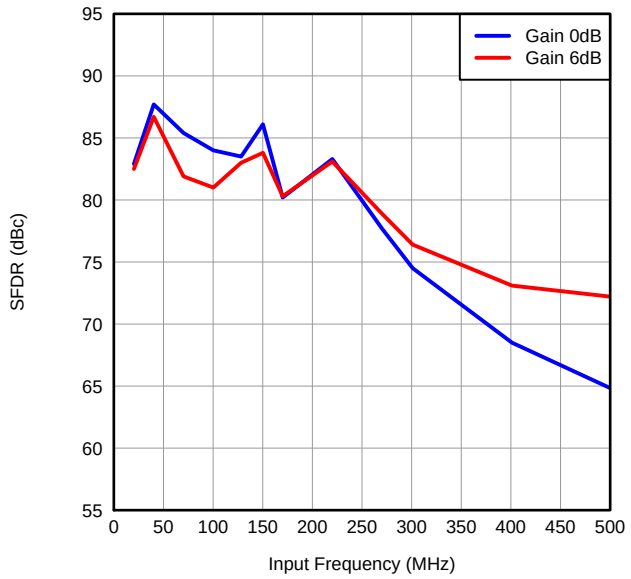


Figure 27.

SNR vs INPUT FREQUENCY

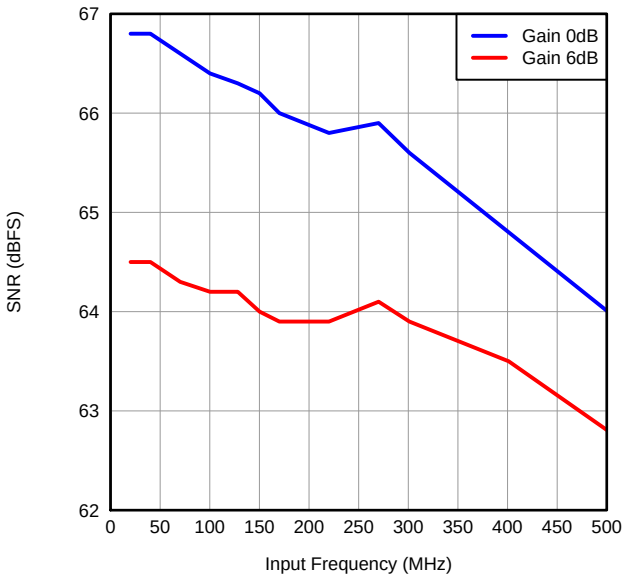


Figure 28.

SFDR ACROSS GAIN AND INPUT FREQUENCY

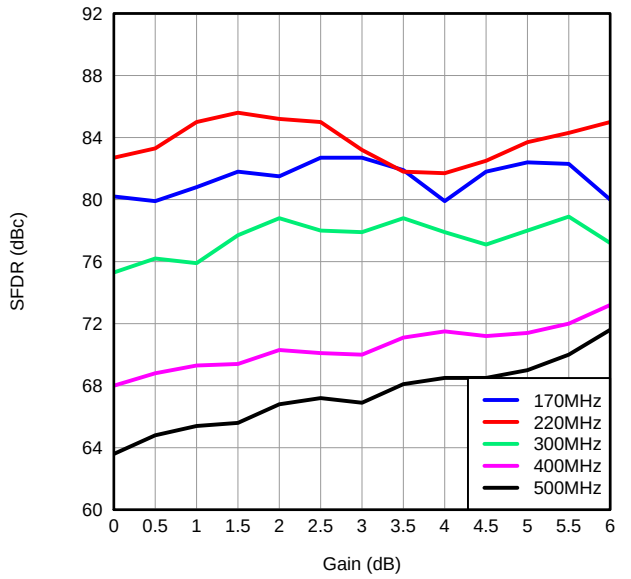


Figure 29.

SINAD ACROSS GAIN AND INPUT FREQUENCY

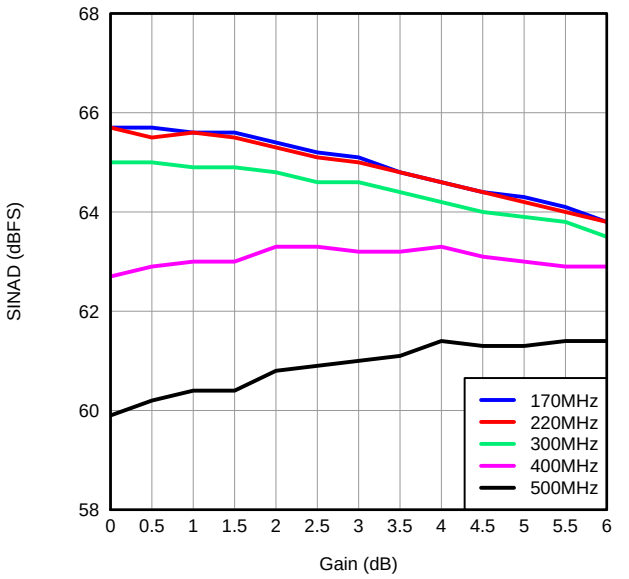


Figure 30.

TYPICAL CHARACTERISTICS (continued)

All graphs are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock. 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High Perf Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

PERFORMANCE ACROSS INPUT AMPLITUDE WITH SNRBoost^{3G} DISABLED

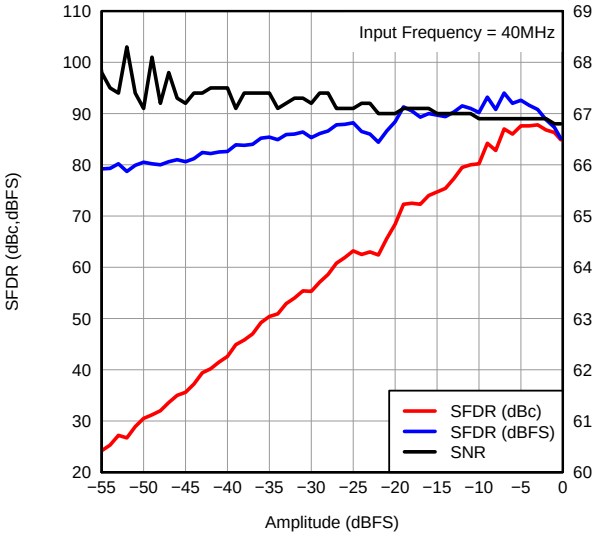


Figure 31.

PERFORMANCE ACROSS INPUT AMPLITUDE WITH SNRBoost^{3G} ENABLED

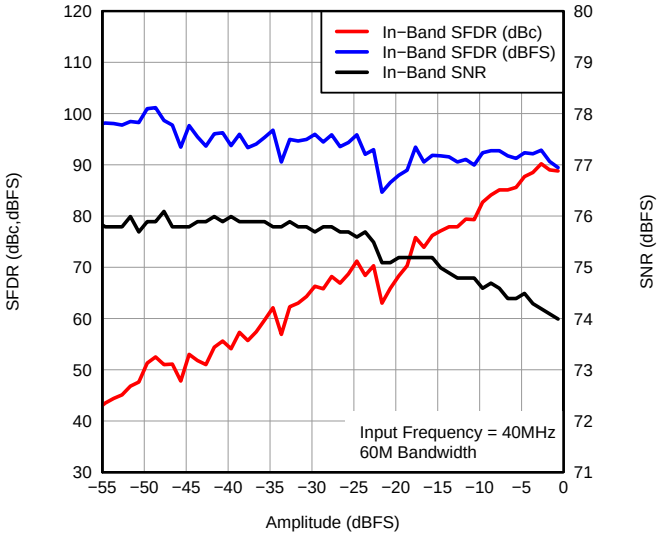


Figure 32.

PERFORMANCE ACROSS INPUT AMPLITUDE WITH SNRBoost^{3G} DISABLED

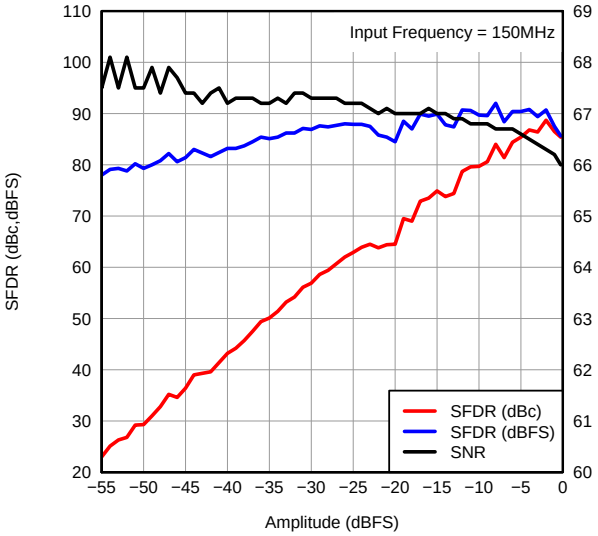


Figure 33.

PERFORMANCE ACROSS INPUT AMPLITUDE WITH SNRBoost^{3G} ENABLED

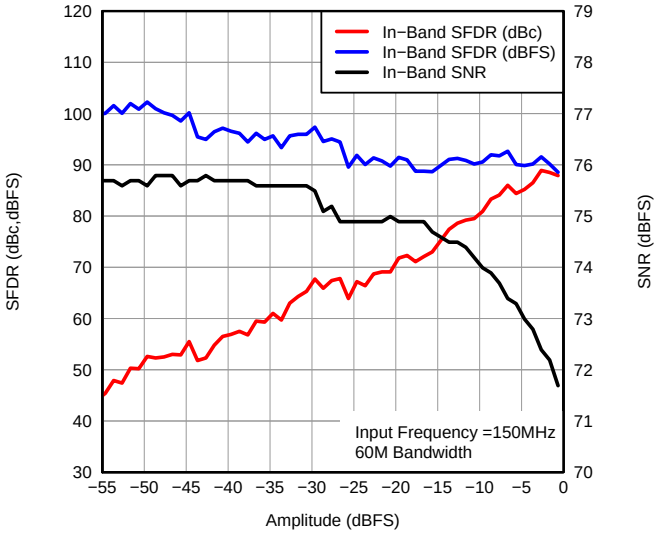


Figure 34.

TYPICAL CHARACTERISTICS (continued)

All graphs are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock. $1.5V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High Perf Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

PERFORMANCE vs INPUT COMMON-MODE VOLTAGE

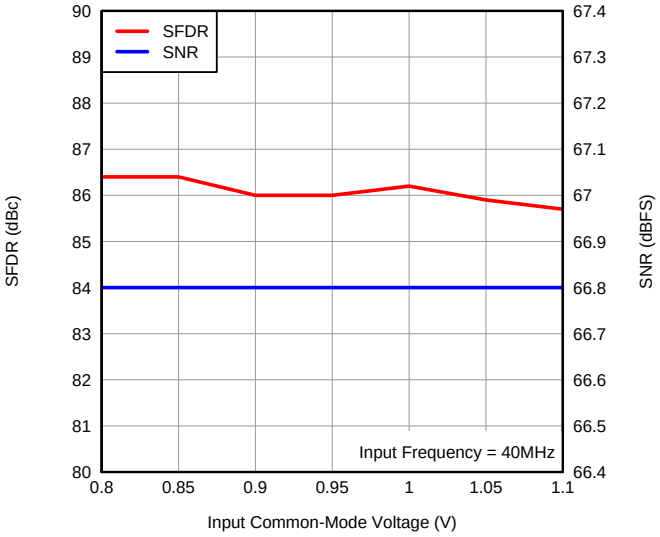


Figure 35.

PERFORMANCE vs INPUT COMMON-MODE VOLTAGE

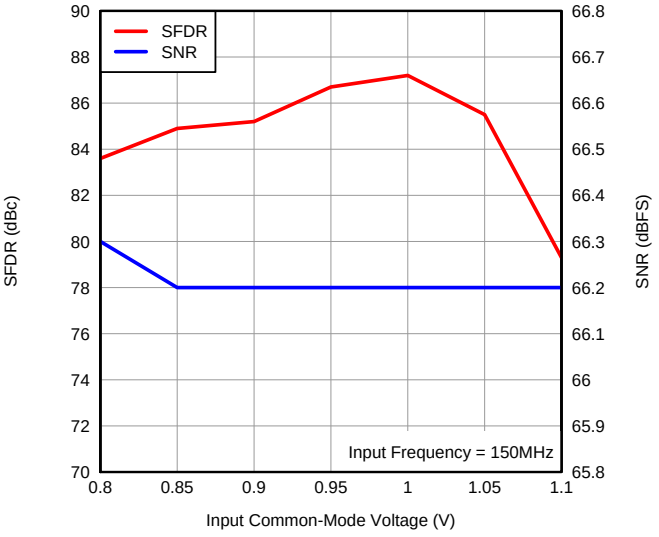


Figure 36.

SFDR ACROSS TEMPERATURE vs AVDD SUPPLY

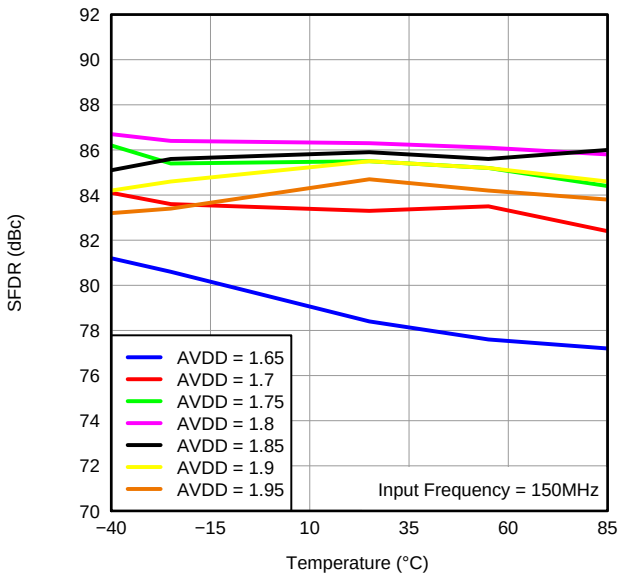


Figure 37.

SNR ACROSS TEMPERATURE vs AVDD SUPPLY

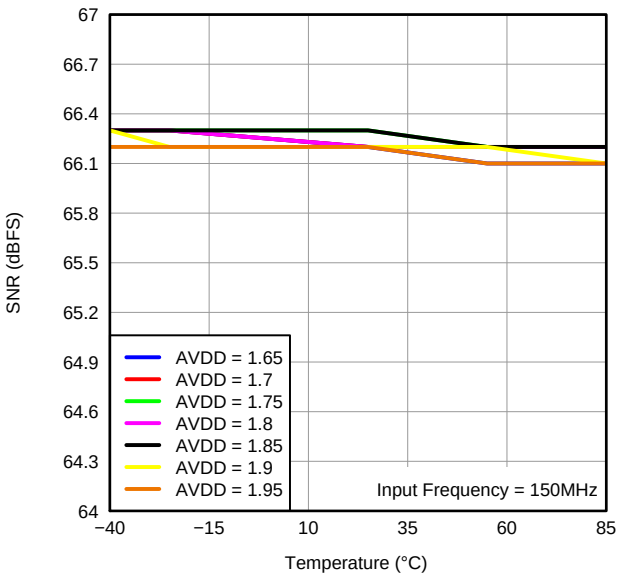


Figure 38.

TYPICAL CHARACTERISTICS (continued)

All graphs are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock. 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High Perf Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

PERFORMANCE ACROSS DRVDD SUPPLY VOLTAGE

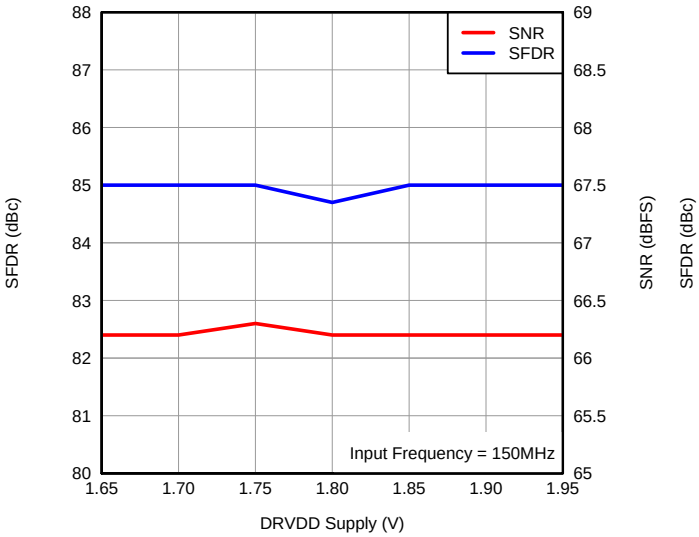


Figure 39.

PERFORMANCE ACROSS INPUT CLOCK AMPLITUDE

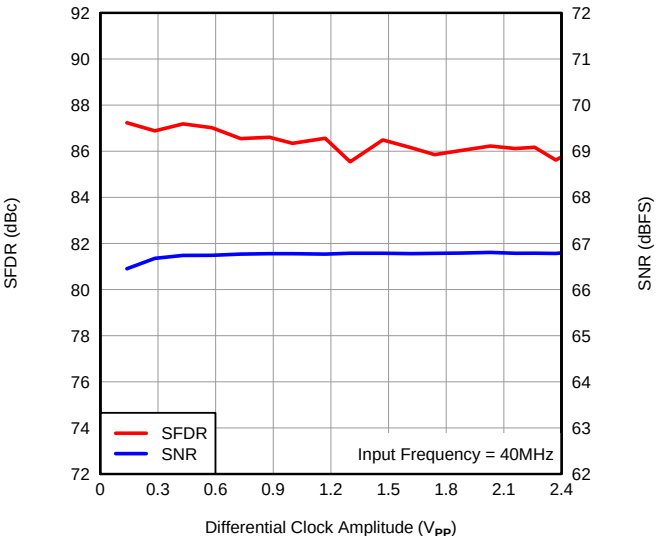


Figure 40.

PERFORMANCE ACROSS INPUT CLOCK AMPLITUDE

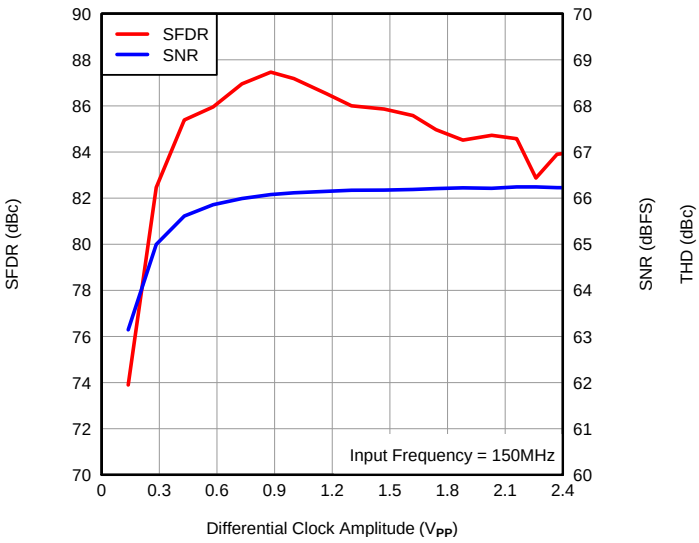


Figure 41.

PERFORMANCE ACROSS INPUT CLOCK DUTY CYCLE

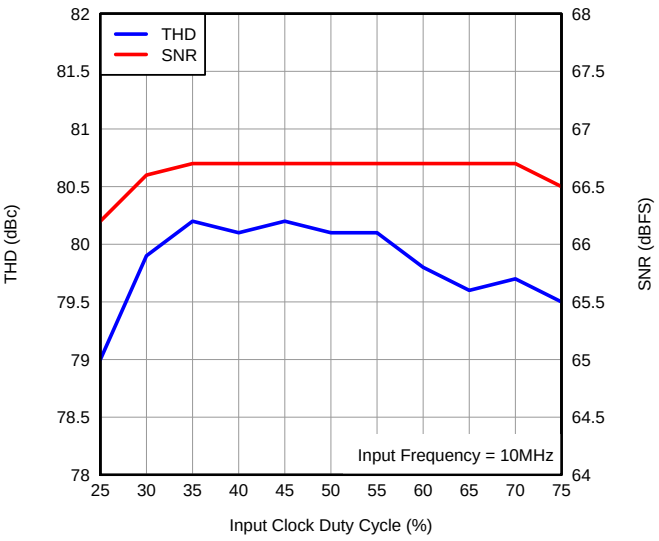


Figure 42.

TYPICAL CHARACTERISTICS (continued)

All graphs are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock. 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High Perf Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

ANALOG POWER vs SAMPLING FREQUENCY

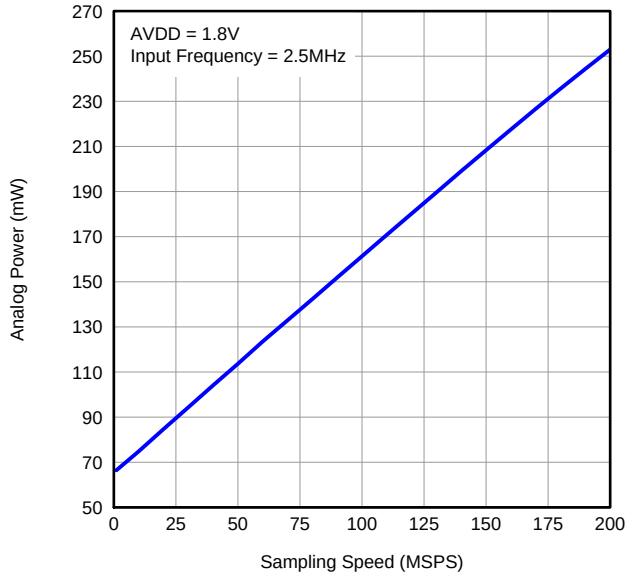


Figure 43.

DIGITAL POWER vs SAMPLING FREQUENCY

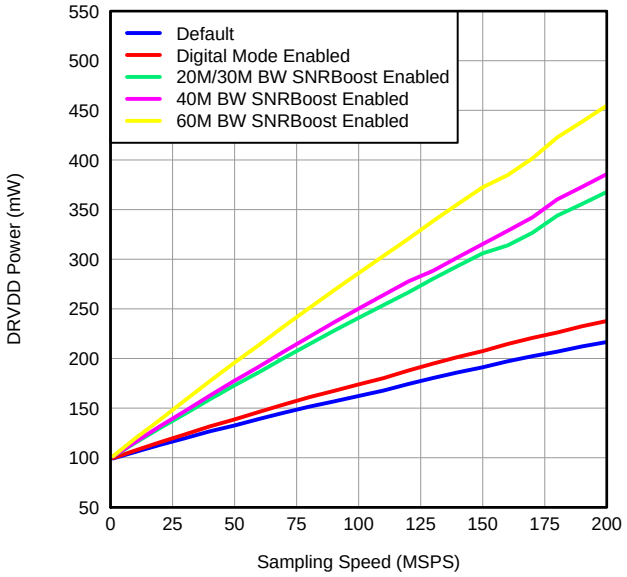


Figure 44.

CMRR OVER FREQUENCY

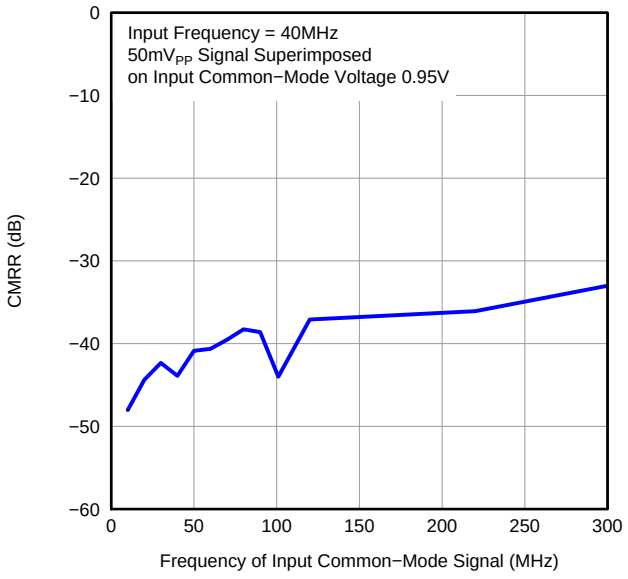


Figure 45.

CMRR SPECTRUM

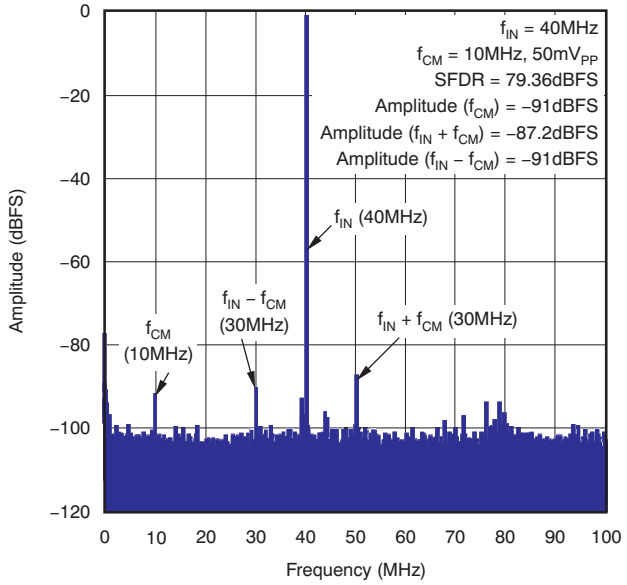


Figure 46.

TYPICAL CHARACTERISTICS (continued)

All graphs are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock. 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High Perf Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

PSRR OVER FREQUENCY

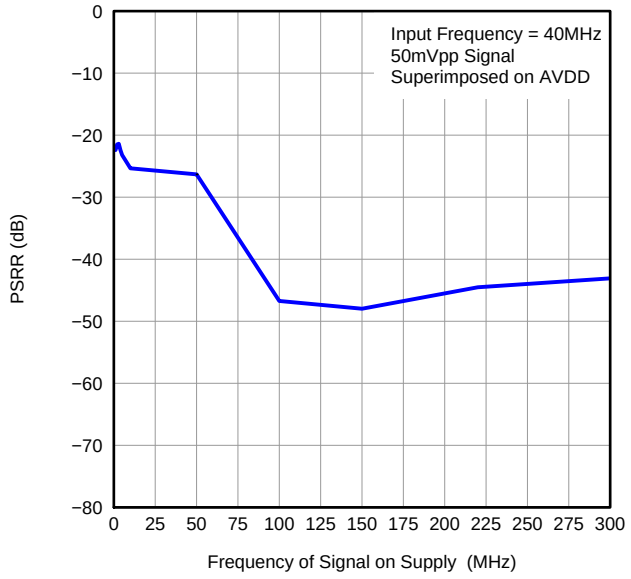


Figure 47.

ZOOMED VIEW OF PSRR SPECTRUM

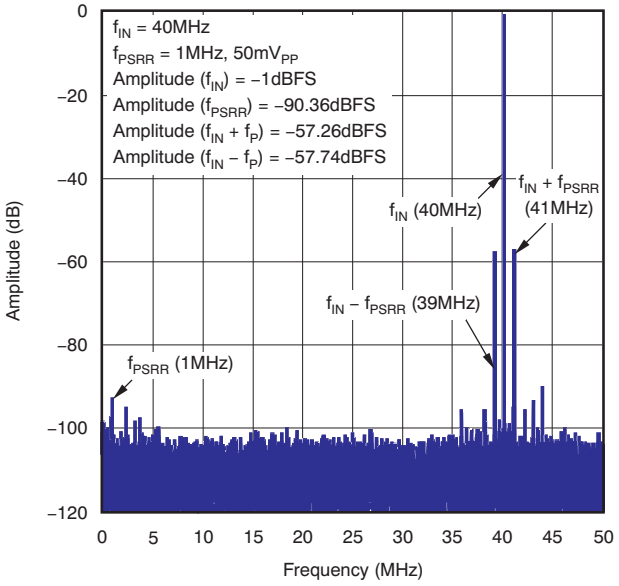


Figure 48.

CROSSTALK

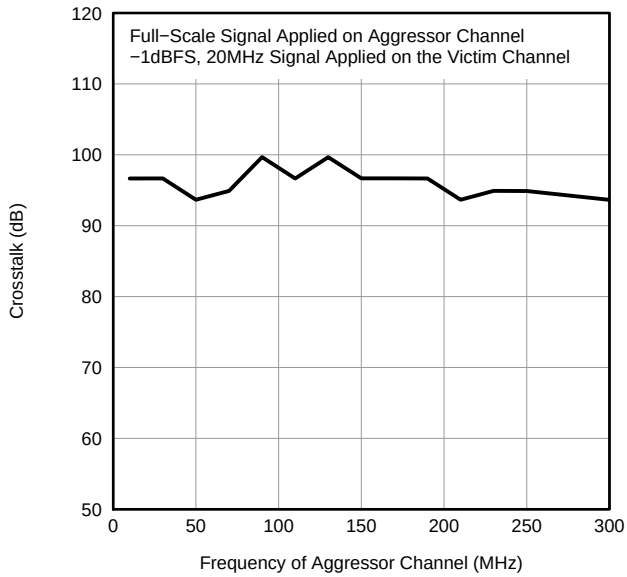


Figure 49.

TYPICAL CHARACTERISTICS: Contour

All graphs are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock. 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High Perf Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

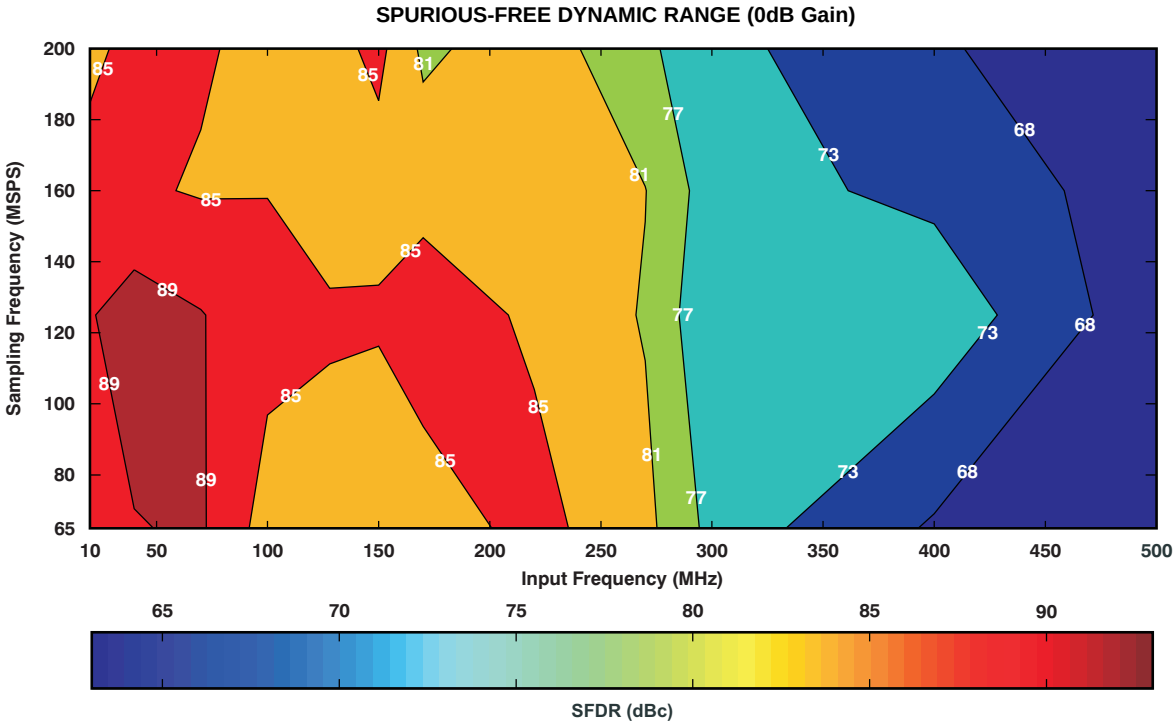


Figure 50.

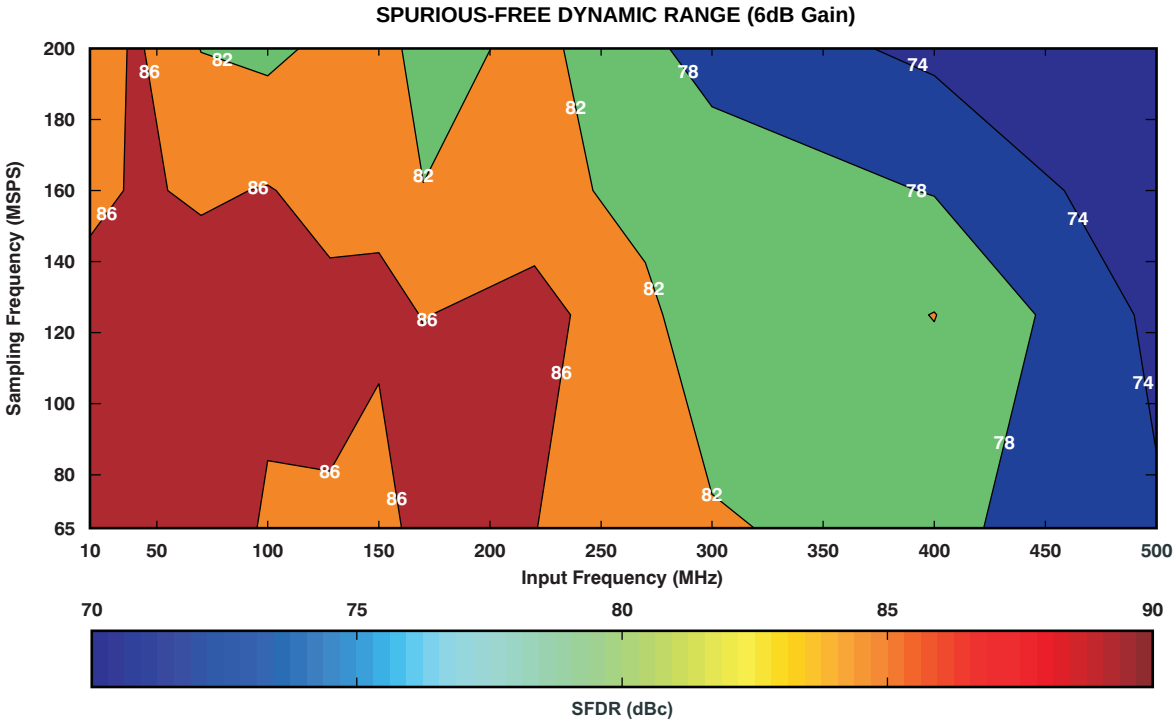


Figure 51.

TYPICAL CHARACTERISTICS: Contour (continued)

All graphs are at +25°C, AVDD = 1.8V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock. 1.5V_{PP} differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, High Perf Mode disabled, 0dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

SIGNAL-TO-NOISE RATIO (0dB Gain)

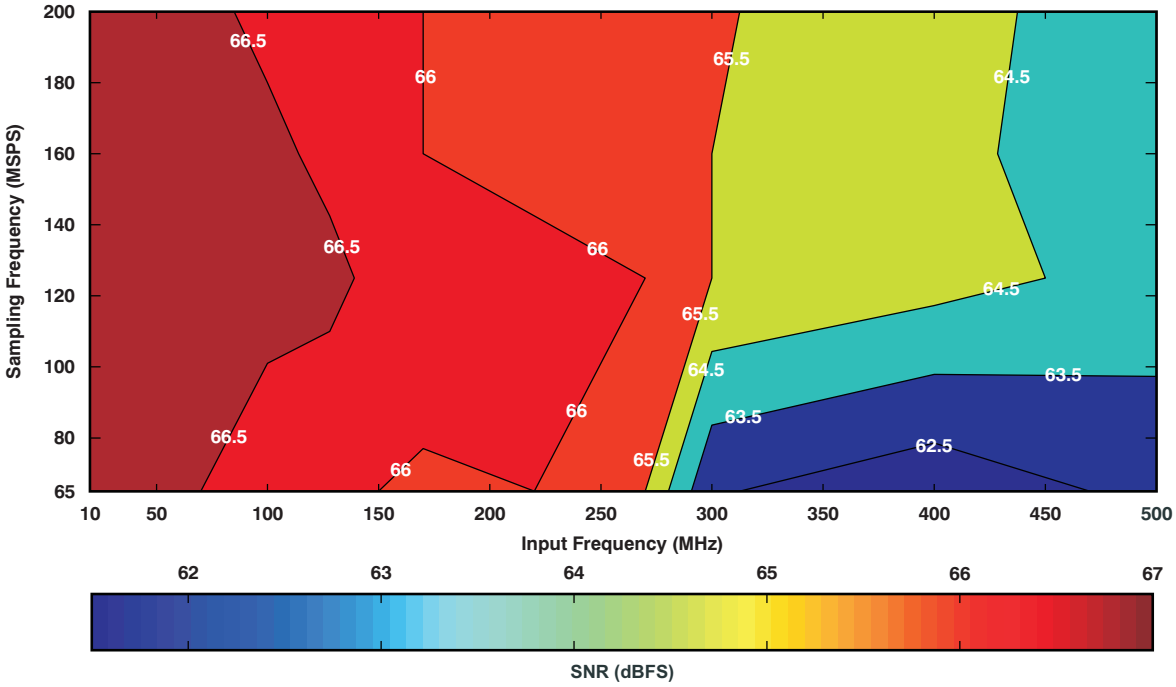


Figure 52.

SIGNAL-TO-NOISE RATIO (6dB Gain)

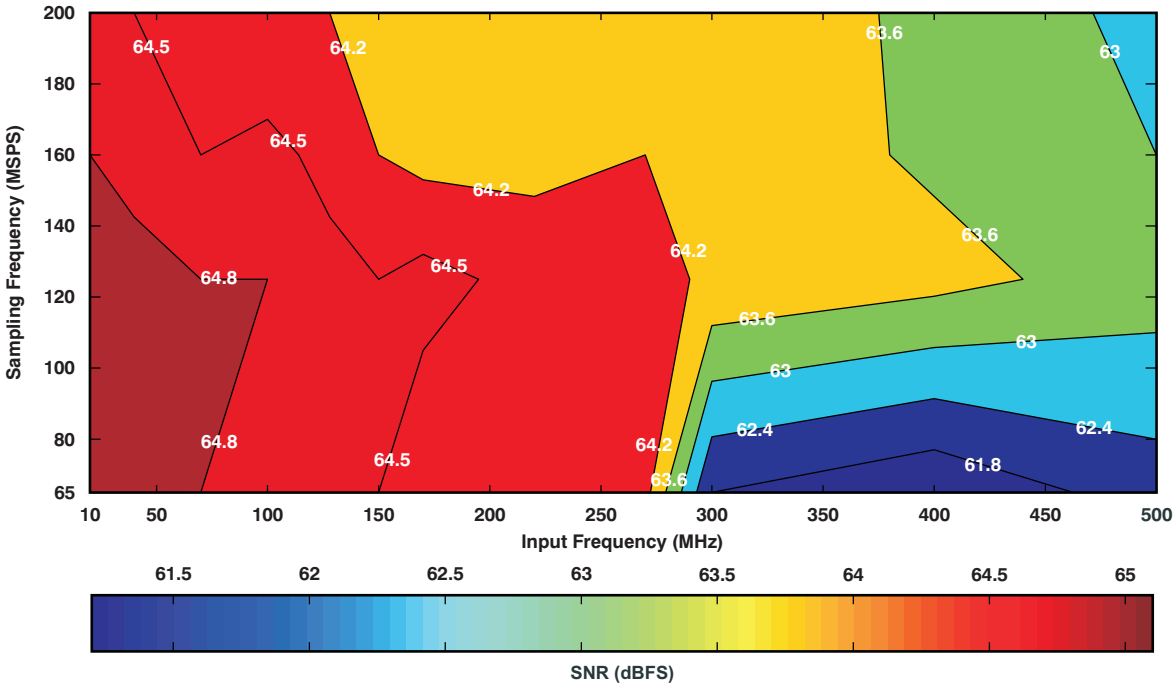


Figure 53.

APPLICATION INFORMATION

THEORY OF OPERATION

The ADS58C28 is a dual-channel, 11-bit, analog-to-digital converter (ADC) with sampling rates up to 200MSPS. At every rising edge of the input clock, the analog input signal of each channel is simultaneously sampled. The sampled signal in each channel is converted by a pipeline of low-resolution stages. In each stage, the sampled and held signal is converted by a high-speed, low-resolution, flash sub-ADC. The difference (residue) between the stage input and the quantized equivalent is gained and propagates to the next stage. At every clock, each succeeding stage resolves the sampled input with greater accuracy. The digital outputs from all stages are combined in a digital correction logic block and are processed digitally to create the final code, after a data latency of 16 clock cycles. The digital output is available as either DDR LVDS or parallel CMOS and coded in either straight offset binary or binary twos complement format.

ANALOG INPUT

The analog input consists of a switched-capacitor based, differential sample-and-hold architecture. This differential topology results in very good ac performance even for high input frequencies at high sampling rates. The IN_P and IN_M pins must be externally biased around a common-mode voltage of 0.95V, available on the VCM pin. For a full-scale differential input, each input pin (IN_P and IN_M) must swing symmetrically between VCM + 0.5V and VCM – 0.5V, resulting in a $2V_{PP}$ differential input swing. The input sampling circuit has a high 3dB bandwidth that extends up to 550MHz (measured from the input pins to the sampled voltage).

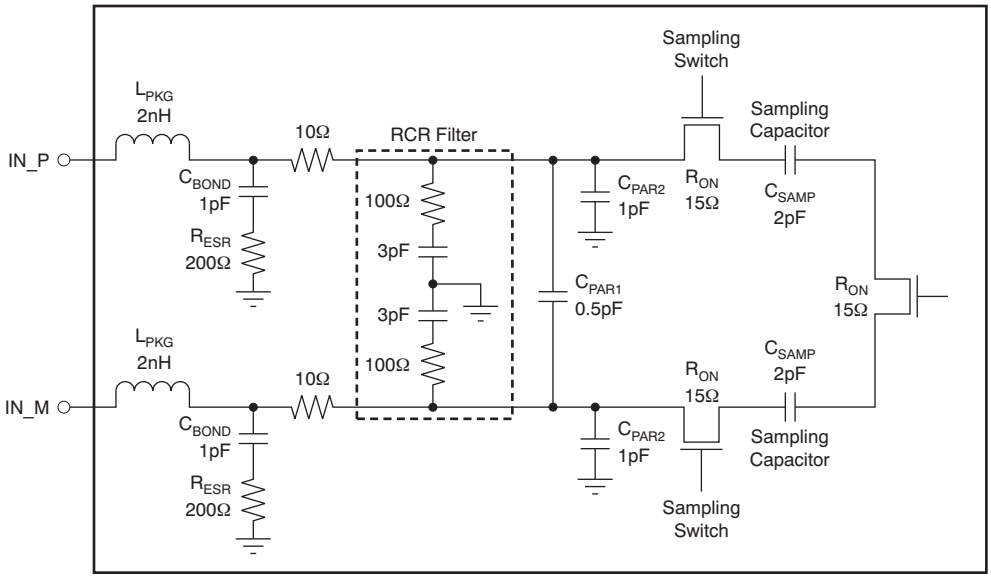


Figure 54. Analog Input Equivalent Circuit

Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This operation improves the common-mode noise immunity and even-order harmonic rejection. A 5Ω to 15Ω resistor in series with each input pin is recommended to damp out ringing caused by package parasitics.

SFDR performance can be limited as a result of several reasons, including the effects of sampling glitches; nonlinearity of the sampling circuit; and nonlinearity of the quantizer that follows the sampling circuit. Depending on the input frequency, sample rate, and input amplitude, one of these factors plays a dominant part in limiting performance. At very high input frequencies (greater than approximately 300MHz), SFDR is determined largely by the device sampling circuit nonlinearity. At low input amplitudes, the quantizer nonlinearity usually limits performance.

Glitches are caused by the opening and closing of the sampling switches. The driving circuit should present a low source impedance to absorb these glitches. Otherwise, glitches could limit performance, primarily at low input frequencies (up to approximately 200MHz). It is also necessary to present low impedance (less than 50Ω) for the common-mode switching currents. This configuration can be achieved by using two resistors from each input terminated to the common-mode voltage (VCM).

The device includes an internal R-C filter from each input to ground. The purpose of this filter is to absorb the sampling glitches inside the device itself. The cutoff frequency of the R-C filter involves a trade-off. A lower cutoff frequency (larger C) absorbs glitches better, but it reduces the input bandwidth. On the other hand, with a higher cutoff frequency (smaller C), bandwidth support is maximized. However, the sampling glitches now must be supplied by the external drive circuit. This tradeoff has limitations as a result of the presence of the package bond-wire inductance.

In the ADS58C28, the R-C component values have been optimized while supporting high input bandwidth (up to 550MHz). However, in applications with input frequencies up to 200MHz to 300MHz, the filtering of the glitches can be improved further using an external R-C-R filter; see Figure 57 and Figure 58.

In addition, the drive circuit may have to be designed to provide a low insertion loss over the desired frequency range and matched impedance to the source. Furthermore, the ADC input impedance must be considered. Figure 55 and Figure 56 show the impedance ($Z_{IN} = R_{IN} \parallel C_{IN}$) looking into the ADC input pins.

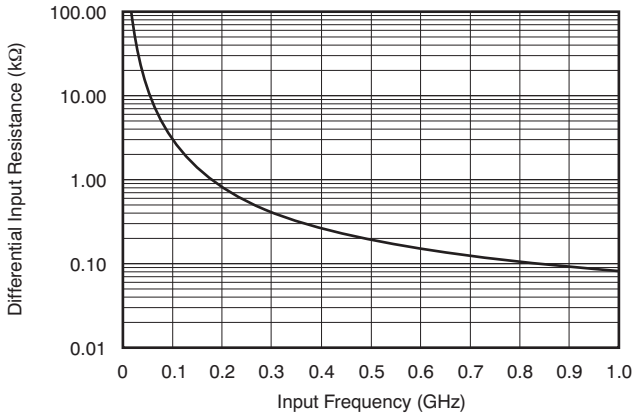


Figure 55. ADC Analog Input Resistance (R_{IN}) Across Frequency

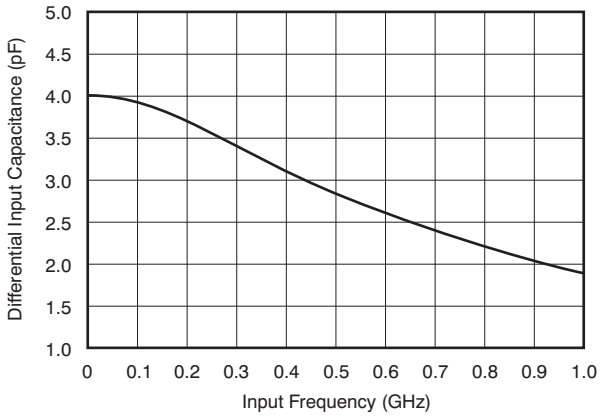


Figure 56. ADC Analog Input Capacitance (C_{IN}) Across Frequency

Driving Circuit

Two example driving circuit configurations are shown in Figure 57 and Figure 58—one optimized for low bandwidth (low input frequencies) and the other one for high bandwidth to support higher input frequencies. Note that both of the drive circuits have been terminated by 50Ω near the ADC side. The termination is accomplished by a 25Ω resistor from each input to the 0.95V common-mode (VCM) from the device. This allows the analog inputs to be biased around the required common-mode voltage.

The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch; good performance is obtained for high-frequency input signals. An additional termination resistor pair may be required between the two transformers, as shown in Figure 57, Figure 58, and Figure 59. The center point of this termination is connected to ground to improve the balance between the P and M sides. The values of the terminations between the transformers and on the secondary side must be chosen to obtain an effective 50Ω (in the case of 50Ω source impedance).

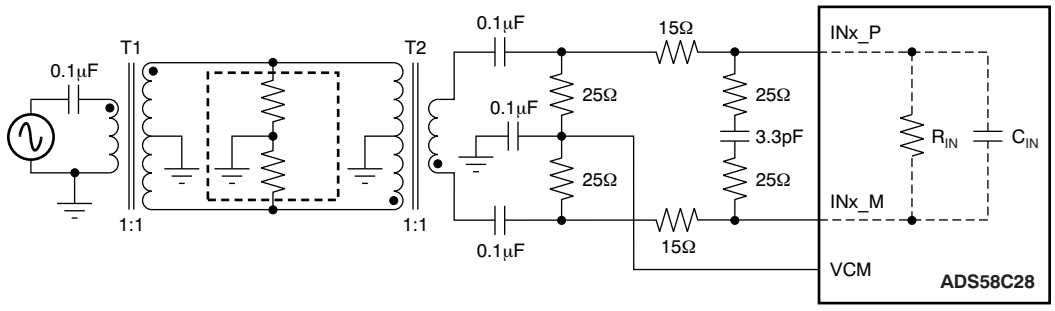


Figure 57. Drive Circuit with Low Bandwidth (for Low Input Frequencies)

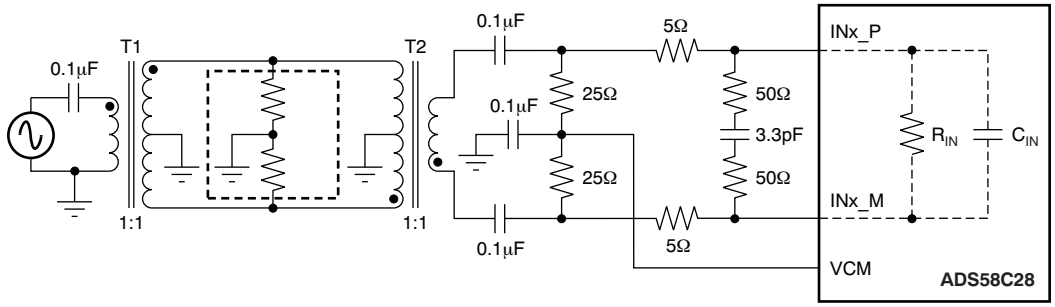


Figure 58. Drive Circuit with High Bandwidth (for High Input Frequencies)

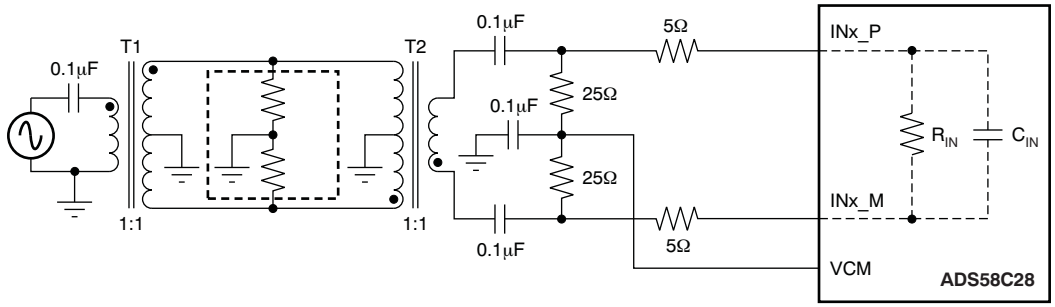


Figure 59. Drive Circuit with Very High Bandwidth (Greater than 300MHz)

All of these examples show 1:1 transformers being used with a 50Ω source. As explained in the *Drive Circuit Requirements* section, this configuration helps to present a low source impedance to absorb the sampling glitches. With a 1:4 transformer, the source impedance is 200Ω. Higher impedance can lead to degradation in performance, compared to the case with 1:1 transformers. For applications where only a band of frequencies are used, the drive circuit can be tuned to present a low impedance for the sampling glitches. Figure 60 shows an example with a 1:4 transformer, tuned for a band of approximately 150MHz.

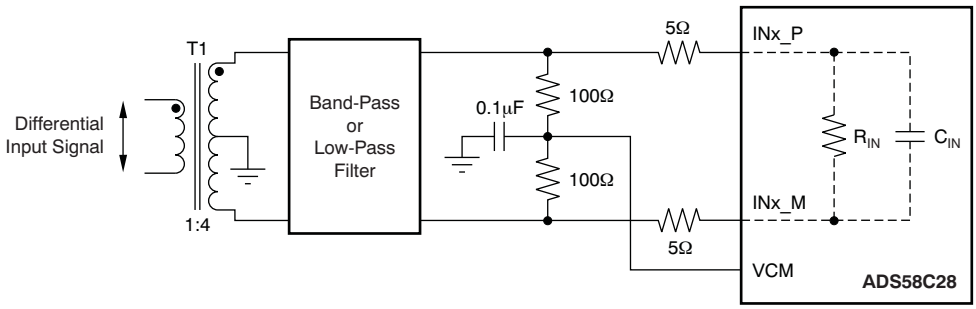
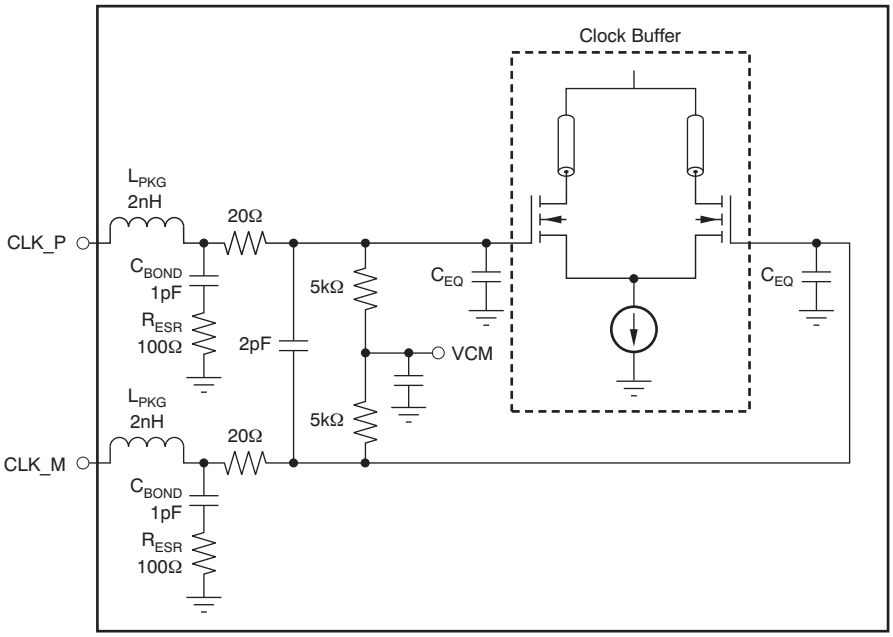


Figure 60. Drive Circuit with a 1:4 Transformer

CLOCK INPUT

The ADS58C28 clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to VCM using internal 5kΩ resistors. This setting allows the use of transformer-coupled drive circuits for sine-wave clock or ac-coupling for LVPECL and LVDS clock sources. Figure 61 shows a circuit for the internal clock buffer.



NOTE: C_{EQ} is 1pF to 3pF and is the equivalent input capacitance of the clock buffer.

Figure 61. Internal Clock Buffer

A single-ended CMOS clock can be ac-coupled to the CLK_P input, with CLK_M connected to ground with a 0.1μF capacitor, as shown in Figure 62. For best performance, the clock inputs must be driven differentially, thereby reducing susceptibility to common-mode noise. For high input frequency sampling, it is recommended to use a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input. Figure 63 shows a differential circuit.

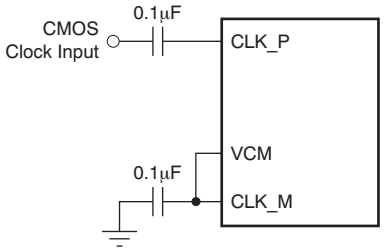


Figure 62. Single-Ended Clock Driving Circuit

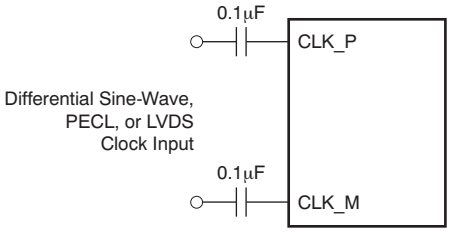


Figure 63. Differential Clock Driving Circuit

DIGITAL FUNCTIONS

The device has several useful digital functions such as test patterns, gain, offset correction, and SNRBoost^{3G}. All of these functions can be controlled using two control bits (DIGITAL MODE 1 and DIGITAL MODE 2), as shown in Table 12.

Table 12. Digital Functions Control Bits

DIGITAL MODE 1	DIGITAL MODE 2	DESCRIPTION
0	0	Default
0	1	SNRBoost^{3G} enabled, test patterns, gain, and offset correction disabled
1	0	SNRBoost^{3G}, test patterns, gain, and offset correction enabled
1	1	SNRBoost^{3G}, test patterns, gain, and offset correction enabled

SNR ENHANCEMENT USING SNRBoost^{3G}

SNRBoost^{3G} technology makes it possible to overcome SNR limitations resulting from quantization noise. Using SNRBoost^{3G}, enhanced SNR can be obtained for any bandwidth (less than Nyquist or $f_S/2$; see Table 5). SNR improvement is achieved without affecting the default harmonic performance.

The ADS58C28 uses third-generation SNRBoost technology (SNRBoost^{3G}) to achieve SNR enhancement over very wide bandwidths (up to 60MHz). When SNRBoost^{3G} is enabled, the noise floor in the spectrum acquires a typical bathtub shape. The special feature of SNRBoost^{3G} is the nearly flat noise floor within the entire band of the bathtub.

The position of the center of the bathtub and its bandwidth are programmable; the available bandwidths are 60MHz, 40MHz, 30MHz, and 20MHz. Several center frequency options are available for each bandwidth. The ADS58C28 includes 55 pre-programmed combinations of center frequency and bandwidth. Any one of these combinations can be selected by programming the Ch SNRBoost^{3G} Filter Number register bits. Each channel can be programmed with independent center frequency and bandwidths.

One of the characteristics of SNRBoost^{3G} is that the bandwidth scales with the sampling frequency. 60MHz and 40MHz bandwidths are achieved at a sampling rate of 184MHz; at higher sample rates, even higher bandwidths are possible. The lower 30MHz and 20MHz bandwidths are achieved at a sample rate of 200MHz; at lower sample rates, the achieved bandwidth is lower. Table 14 shows all combinations of center frequency for each bandwidth, specified as fractions of the sample rate. By positioning the bathtub within the desired signal band, SNR improvement can be achieved. Note that as the bandwidth increases, the amount of SNR improvement reduces. After reset, the SNRBoost^{3G} function is disabled.

To use SNRBoost^{3G} with control pins, follow this exact sequence:

Select and Enable the SNRBoost^{3G} Filter

1. First, disable the DIGITAL MODE 1 and DIGITAL MODE 2 bits (set to '0').
2. Next, select the appropriate SNRBoost^{3G} filter, using the Ch SNRBoost^{3G} Filter number register bits.
3. Finally, set the DIGITAL MODE 2 bit (set to '1').

Turn On/Off SNRBoost^{3G}

1. Use the CTRL1, CTRL2, and CTRL3 pins to dynamically turn on/off the SNRBoost^{3G} for each pair of channels.

To use SNRBoost^{3G} without using control pins follow this exact sequence:

Select and Enable the SNRBoost^{3G} Filter

1. First, disable the DIGITAL MODE 1 and DIGITAL MODE 2 bits (set to '0').
2. Next, select the appropriate SNRBoost^{3G} filter using the Ch SNRBoost Filter number register bits.
3. Then set the DIGITAL MODE 2 bit (set to '1').
4. Finally, set the SNRBoost^{3G} pin override bit (OVERRIDE SNRBoost PINS).

Turn On/Off SNRBoost^{3G}

1. Turn on and off the SNRBoost^{3G} for each channel using the SNRBoost CH A ON and SNRBoost CH B ON register bits.

NOTE

To use a different SNRBoost^{3G} filter, it is required to follow all the above steps in the exact order specified. Not following this order can result in incorrect operation of the SNRBoost^{3G} filter. To turn on and off the filter without changing the filter number, simply follow the steps under the Turn On/Off SNRBoost^{3G} outline.

Table 13 describes the SNRBoost^{3G} control when used with the CTRL pins.

Table 13. SNRBoost^{3G} Control Using Pins CTRL1, CTRL2, and CTRL3

CTRL1	CTRL2	CTRL3	DESCRIPTION
Low	Low	Low	Normal operation; SNRBoost^{3G} disabled for both channels
Low	Low	High	SNRBoost^{3G} enabled for channel B
Low	High	Low	SNRBoost^{3G} enabled for channel A
Low	High	High	SNRBoost^{3G} enabled for channels A and B
High	Low	Low	Global power-down
High	Low	High	Channel A standby
High	High	Low	Do not use
High	High	High	MUX mode of operation, channels A and B data are multiplexed and output on pins CHB_D[10:0].

Table 14. Complete List of SNRBoost^{3G} Modes (f_S = Sampling Frequency in MSPS)

SNRBoost^{3G} FILTER NUMBER	BANDWIDTH OF THE BATHTUB (MHz)	CENTER FREQUENCY OF THE BATHTUB (MHz)
0	25 × (f_S/200)	15 × (f_S/200)
1	20 × (f_S/200)	30 × (f_S/200)
2	20 × (f_S/200)	35 × (f_S/200)
3	20 × (f_S/200)	42 × (f_S/200)
4	20 × (f_S/200)	50 × (f_S/200)
5	20 × (f_S/200)	58 × (f_S/200)
6	20 × (f_S/200)	65 × (f_S/200)
7	20 × (f_S/200)	75 × (f_S/200)
8	20 × (f_S/200)	85 × (f_S/200)
9	25 × (f_S/200)	87.5 × (f_S/200)
10	25 × (f_S/200)	15 × (f_S/200)
11	20 × (f_S/200)	25 × (f_S/200)
12	20 × (f_S/200)	35 × (f_S/200)
13	20 × (f_S/200)	42 × (f_S/200)
14	20 × (f_S/200)	50 × (f_S/200)
15	20 × (f_S/200)	58 × (f_S/200)
16	20 × (f_S/200)	65 × (f_S/200)
17	20 × (f_S/200)	75 × (f_S/200)
18	25 × (f_S/200)	82.5 × (f_S/200)
19	25 × (f_S/200)	87.5 × (f_S/200)
20	25 × (f_S/200)	15 × (f_S/200)
21	30 × (f_S/200)	30 × (f_S/200)
22	30 × (f_S/200)	35 × (f_S/200)
23	30 × (f_S/200)	45 × (f_S/200)
24	30 × (f_S/200)	55 × (f_S/200)
25	30 × (f_S/200)	65 × (f_S/200)
26	30 × (f_S/200)	70 × (f_S/200)
27	30 × (f_S/200)	80 × (f_S/200)
28	30 × (f_S/200)	85 × (f_S/200)
29	25 × (f_S/200)	87.5 × (f_S/200)
30	40 × (f_S/184)	46 × (f_S/184)
31	40 × (f_S/184)	72 × (f_S/184)
32	40 × (f_S/184)	20 × (f_S/184)
33	40 × (f_S/184)	40 × (f_S/184)
34	40 × (f_S/184)	39.5 × (f_S/184)
35	40 × (f_S/184)	33.5 × (f_S/184)
36	40 × (f_S/184)	27 × (f_S/184)
37	40 × (f_S/184)	53 × (f_S/184)
38	40 × (f_S/184)	59 × (f_S/184)
39	40 × (f_S/184)	65.5 × (f_S/184)

Table 14. Complete List of SNRBoost^{3G} Modes (f_S = Sampling Frequency in MSPS) (continued)

SNRBoost^{3G} FILTER NUMBER	BANDWIDTH OF THE BATHTUB (MHz)	CENTER FREQUENCY OF THE BATHTUB (MHz)
40	60 × (f_S/184)	46 × (f_S/184)
41	60 × (f_S/184)	46 × (f_S/184)
42	60 × (f_S/184)	30 × (f_S/184)
43	60 × (f_S/184)	30 × (f_S/184)
44	60 × (f_S/184)	62 × (f_S/184)
45	60 × (f_S/184)	62 × (f_S/184)
46	60 × (f_S/184)	40.5 × (f_S/184)
47	60 × (f_S/184)	40.5 × (f_S/184)
48	60 × (f_S/184)	37 × (f_S/184)
49	60 × (f_S/184)	37 × (f_S/184)
50	60 × (f_S/184)	53 × (f_S/184)
51	60 × (f_S/184)	50 × (f_S/184)
52	60 × (f_S/184)	54 × (f_S/184)
53	58 × (f_S/184)	58 × (f_S/184)
54	60 × (f_S/184)	62 × (f_S/184)

GAIN FOR SFDR/SNR TRADE-OFF

The ADS58C28 includes gain settings that can be used to get improved SFDR performance. The gain is programmable from 0dB to 6dB (in 0.5dB steps) using the GAIN register bits. For each gain setting, the analog input full-scale range scales proportionally, as shown in Table 15.

The SFDR improvement is achieved at the expense of SNR; for each gain setting, the SNR degrades approximately between 0.5dB and 1dB. The SNR degradation is reduced at high input frequencies. As a result, the gain is very useful at high input frequencies because the SFDR improvement is significant with marginal degradation in SNR. Therefore, the gain can be used as a trade-off between SFDR and SNR.

After a reset, the gain function is disabled. To use gain:

- First, program the DIGITAL MODE 1 and DIGITAL MODE 2 bits (see Table 12) to enable the gain function.
- This setting enables the gain and puts the device in a 0dB gain mode.
- For other gain settings, program the GAIN register bits.

Table 15. Full-Scale Range Across Gains

GAIN (dB)	TYPE	FULL-SCALE (V_{PP})
0	Default after reset	2
1	Fine adjust, programmable	1.78
2	Fine adjust, programmable	1.59
3	Fine adjust, programmable	1.42
4	Fine adjust, programmable	1.26
5	Fine adjust, programmable	1.12
6	Fine adjust, programmable	1

OFFSET CORRECTION

The ADS58C28 has an internal offset corretion algorithm that estimates and corrects dc offset up to ±10mV. The correction can be enabled using the ENABLE OFFSET CORR serial register bit. Once enabled, the algorithm estimates the channel offset and applies the correction every clock cycle. The time constant of the correction loop is a function of the sampling clock frequency. The time constant can be controlled using the OFFSET CORR TIME CONSTANT register bits, as described in Table 16.

Table 16. Time Constant of Offset Correction Algorithm

OFFSET CORR TIME CONSTANT	TIME CONSTANT, TC_{CLK} (Number of Clock Cycles)	TIME CONSTANT, $TC_{CLK} \times 1/f_S$ (sec)(1)
0000	1M	5ms
0001	2M	10ms
0010	4M	21ms
0011	8M	42ms
0100	16M	84ms
0101	32M	168ms
0110	64M	336ms
0111	128M	671ms
1000	256M	1.3s
1001	512M	2.7s
1010	1024M	5.4s
1011	2048M	10.7s
1100	Reserved	—
1101	Reserved	—
1110	Reserved	—
1111	Reserved	—

(1) Sampling frequency, f_S = 200MSPS.

After the offset is estimated, the correction can be frozen by setting FREEZE OFFSET CORR = 1. Once frozen, the last estimated value is used for the offset correction of every clock cycle. Note that offset correction is disabled by default after reset.

After a reset, the offset correction is disabled. To use offset correction:

- First, program the DIGITAL MODE 1 and DIGITAL MODE 2 bits (see Table 12) to enable the correction.
- Then set ENABLE OFFSET CORR to '1' and program the required time constant.

DIGITAL OUTPUT INFORMATION

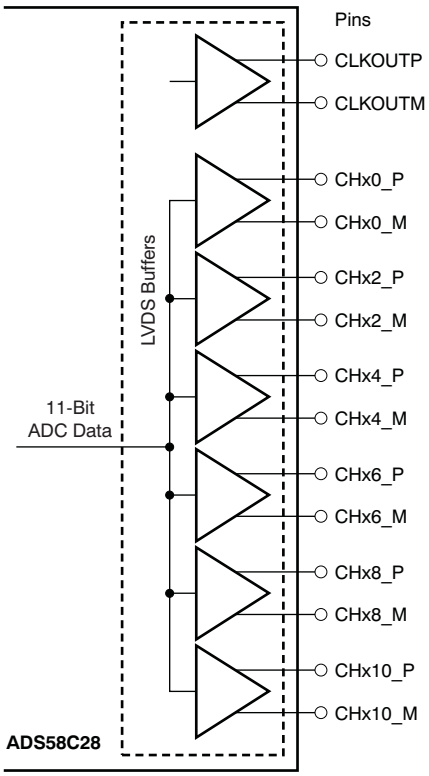
The ADS58C28 provides 11-bit digital data for each channel and a common output clock synchronized with the data.

Output Interface

Two output interface options are available: double data rate (DDR) LVDS and parallel CMOS. They can be selected using the LVDS CMOS serial interface register bit .

DDR LVDS Outputs

In this mode, the data bits and clock are output using low-voltage differential signal (LVDS) levels. Two data bits are multiplexed and output on each LVDS differential pair.



NOTE: X = channels A and B.

Figure 64. DDR LVDS Interface

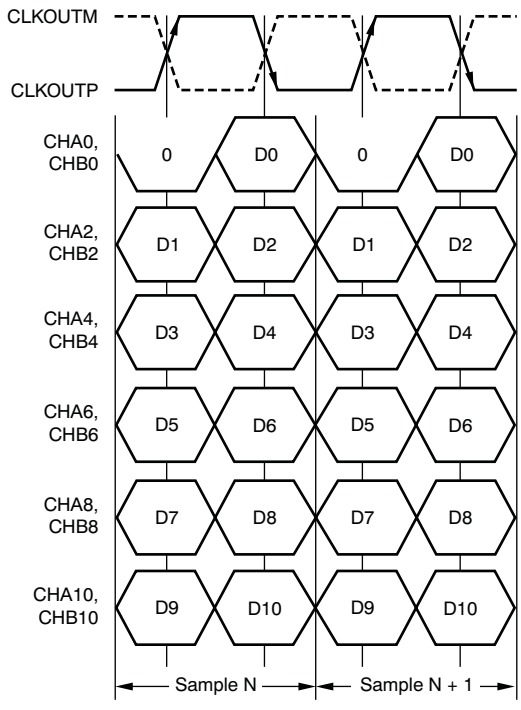


Figure 65. DDR LVDS Interface Timing Diagram

LVDS Output Data and Clock Buffers

The equivalent circuit of each LVDS output buffer is shown in Figure 66. After reset, the buffer presents an output impedance of 100Ω to match with the external 100Ω termination.

The V_{DIFF} voltage is nominally 350mV, resulting in an output swing of ±350mV with 100Ω external termination. The V_{DIFF} voltage is programmable using the LVDS SWING register bits from ±125mV to ±570mV.

Additionally, a mode exists to double the strength of the LVDS buffer to support 50Ω differential termination. This mode can be used when the output LVDS signal is routed to two separate receiver chips, each using a 100Ω termination. The mode can be enabled using the LVDS DATA STRENGTH and LVDS CLKOUT STRENGTH register bits for data and output clock buffers, respectively.

The buffer output impedance behaves in the same way as a source-side series termination. By absorbing reflections from the receiver end, it helps to improve signal integrity.

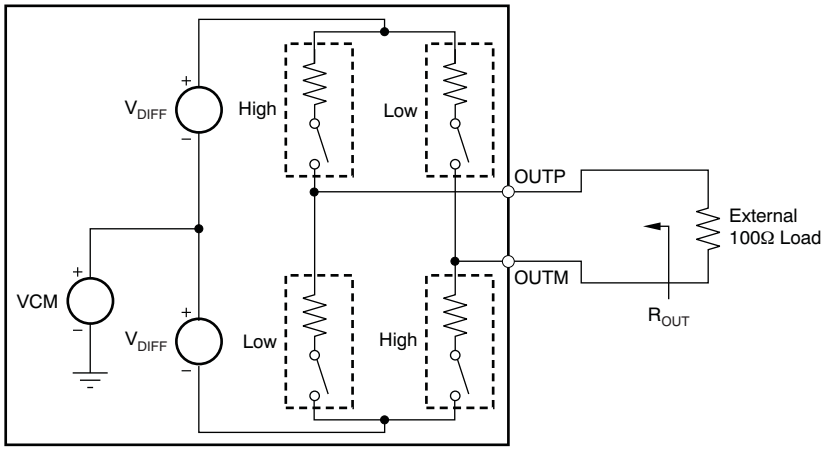
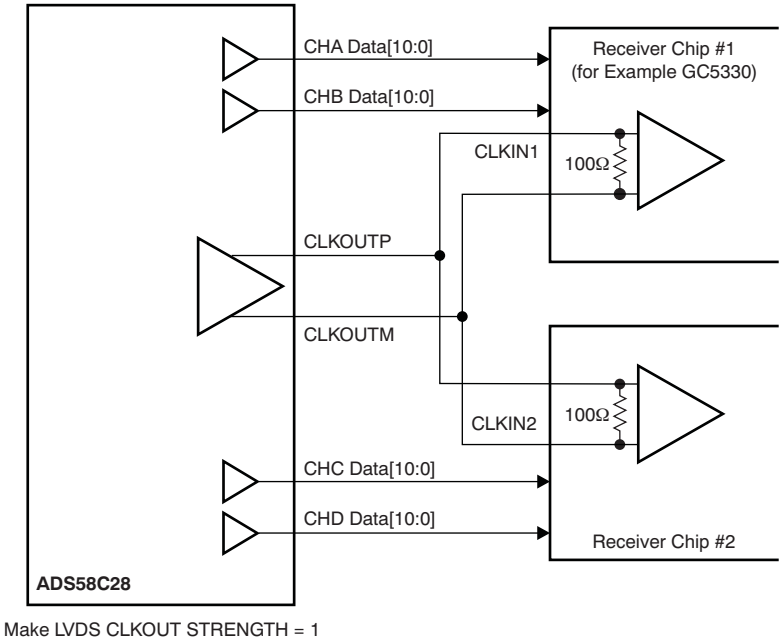


Figure 66. LVDS Buffer Equivalent Circuit



Make LVDS CLKOUT STRENGTH = 1

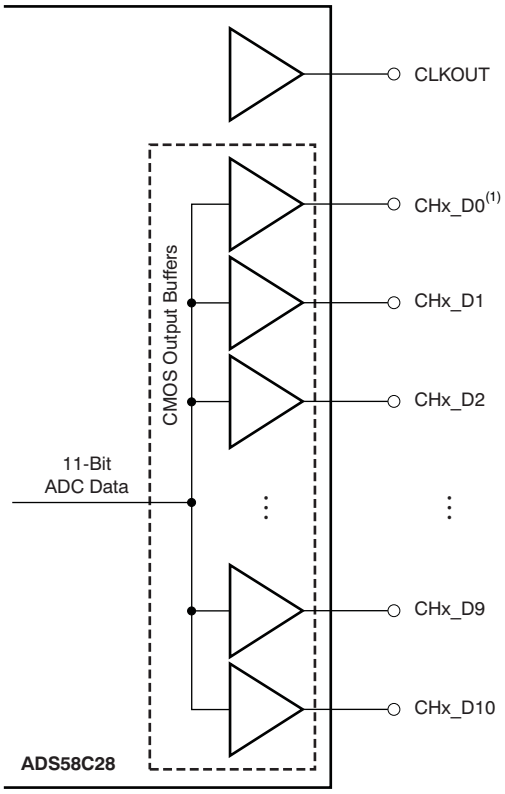
Figure 67. LVDS Strength Doubling (Example Application)

Parallel CMOS Interface

In the CMOS mode, each data bit is output on separate pins as CMOS voltage level, every clock cycle. The rising edge of the output clock CLKOUT can be used to latch data in the receiver.

Switching noise (caused by CMOS output data transitions) can couple into the analog inputs and degrade the SNR. The coupling and SNR degradation increases as the output buffer drive is made stronger. To minimize this effect, the CMOS output buffers are designed with controlled drive strength. The default drive strength ensures wide data stable window provided the data outputs have minimal load capacitance. It is recommended to use short traces (1 to 2 inches or 25,4mm to 50,8mm) terminated with not more than 5pF load capacitance.

For sampling frequencies greater than 150MSPS, it is recommended to use an external clock to capture data. The delay from input clock to output data and the data valid times are specified for the higher sampling frequencies. These timings can be used to delay the input clock appropriately and use it to capture the data.



NOTE: X = channels A and B.

Figure 68. CMOS Interface

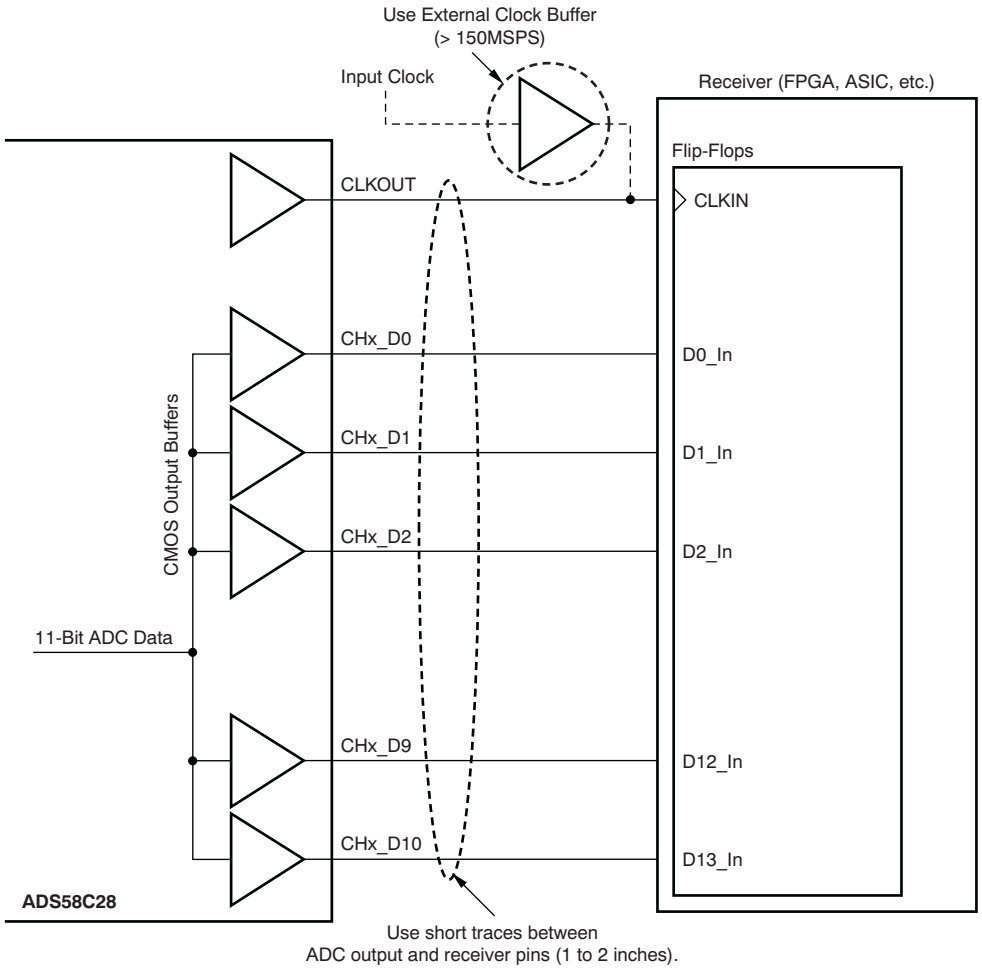


Figure 69. Data Capture with CMOS Interface

CMOS Interface Power Dissipation

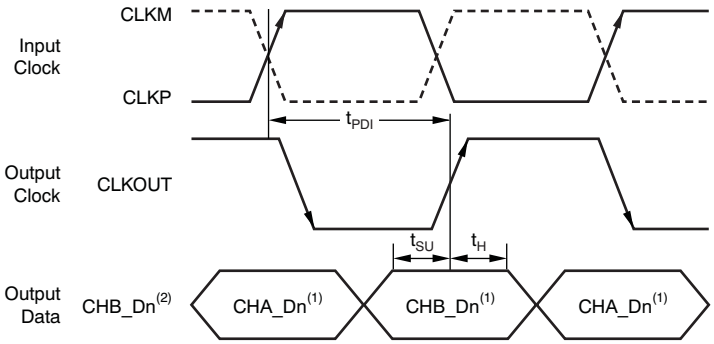
With CMOS outputs, the DRVDD current scales with the sampling frequency and the load capacitance on every output pin. The maximum DRVDD current occurs when each output bit toggles between 0 and 1 every clock cycle. In actual applications, this condition is unlikely to occur. The actual DRVDD current would be determined by the average number of output bits switching, which is a function of the sampling frequency and the nature of the analog input signal.

Digital current as a result of CMOS output switching = $C_L \times DRVDD \times (N \times F_{AVG})$,

where C_L = load capacitance, $N \times F_{AVG}$ = average number of output bits switching.

Multiplexed Mode of Operation

In this mode, the digital outputs of both channels are multiplexed and output on a single bus (CHB_D[10:0] pins), as shown in Figure 70. Any unused channel output pins (CHA_Dn) are forced low and are not put in a high-impedance state. Because the output data rate on the channel B bus is effectively doubled, this mode is recommended only for low sampling frequencies (< 75MSPS). This mode can be enabled using the POWER-DOWN MODE register bits or using the CTRL[3:1] parallel pins. Note that setup and hold timings in this mode are different compared to the default CMOS mode.



(1) Dn = Bits D0, D1, D2, etc.

(2) In multiplexed mode, both channel outputs come on channel B output pins.

Figure 70. ADS58C28 MUX Mode Timing Diagram

Output Data Format

Two output data formats are supported: twos complement and offset binary. They can be selected using the DATA FORMAT CHx serial interface register bit.

In the event of an input voltage overdrive, the digital outputs go to the appropriate full-scale level. For a positive overdrive, the output code is 7FFh in offset binary output format, and 3FFh in twos complement output format. For a negative input overdrive, the output code is 0000h in offset binary output format and 400h in twos complement output format.

BOARD DESIGN CONSIDERATIONS

Grounding

A single ground plane is sufficient to give good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. See the *EVM User Guide* for details on layout and grounding.

Exposed Pad

In addition to providing a path for heat dissipation, the PowerPAD is also electrically internally connected to the digital ground. Therefore, it is necessary to solder the exposed pad to the ground plane for best thermal and electrical performance. For detailed information, see application notes.

DEFINITION OF SPECIFICATIONS

Analog Bandwidth – The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value.

Aperture Delay – The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs. This delay is different across channels. The maximum variation is specified as aperture delay variation (channel-to-channel).

Aperture Uncertainty (Jitter) – The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle – The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum Conversion Rate – The maximum sampling rate at which specified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate – The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL) – An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral Nonlinearity (INL) – The INL is the deviation of the ADC transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error – Gain error is the deviation of the ADC actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error as a result of reference inaccuracy and error as a result of the channel. Both errors are specified independently as E_{GREF} and E_{GCHAN}.

To a first-order approximation, the total gain error is $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$.

For example, if $E_{TOTAL} = \pm 0.5\%$, the full-scale input varies from $(1 - 0.5/100) \times FS_{ideal}$ to $(1 + 0.5/100) \times FS_{ideal}$.

Offset Error – The offset error is the difference, given in number of LSBs, between the ADC actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into millivolts.

Temperature Drift – The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}. It is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference $T_{MAX} – T_{MIN}$.

Signal-to-Noise Ratio – SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and the first nine harmonics.

$$SNR = 10Log^{10} \frac{P_S}{P_N} \quad (1)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Signal-to-Noise and Distortion (SINAD) – SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10Log^{10} \frac{P_S}{P_N + P_D} \quad (2)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Effective Number of Bits (ENOB) – ENOB is a measure of the converter performance as compared to the theoretical limit based on quantization noise.

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02} \tag{3}$$

Total Harmonic Distortion (THD) – THD is the ratio of the power of the fundamental (P_S) to the power of the first nine harmonics (P_D).

$$\text{THD} = 10\text{Log}^{10}\ \frac{P_S}{P_N} \tag{4}$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR) – The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion – IMD3 is the ratio of the power of the fundamental (at frequencies f_1 and f_2) to the power of the worst spectral component at either frequency $2f_1 – f_2$ or $2f_2 – f_1$. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

DC Power-Supply Rejection Ratio (DC PSRR) – DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. The dc PSRR is typically given in units of mV/V.

AC Power-Supply Rejection Ratio (AC PSRR) – AC PSRR is the measure of rejection of variations in the supply voltage by the ADC. If ΔV_{SUP} is the change in supply voltage and ΔV_{OUT} is the resultant change of the ADC output code (referred to the input), then:

$$\text{PSRR} = 20\text{Log}^{10}\ \frac{\Delta V_{OUT}}{\Delta V_{SUP}}\ \text{(Expressed in dBc)} \tag{5}$$

Voltage Overload Recovery – The number of clock cycles taken to recover to less than 1% error after an overload on the analog inputs. This is tested by separately applying a sine wave signal with 6 dB positive and negative overload. The deviation of the first few samples after the overload (from the expected values) is noted.

Common-Mode Rejection Ratio (CMRR) – CMRR is the measure of rejection of variation in the analog input common-mode by the ADC. If ΔV_{CM_IN} is the change in the common-mode voltage of the input pins and ΔV_{OUT} is the resulting change of the ADC output code (referred to the input), then:

$$\text{CMRR} = 20\text{Log}^{10}\ \frac{\Delta V_{OUT}}{\Delta V_{CM}}\ \text{(Expressed in dBc)} \tag{6}$$

Crosstalk (only for multi-channel ADCs) – This is a measure of the internal coupling of a signal from an adjacent channel into the channel of interest. It is specified separately for coupling from the immediate neighboring channel (near-channel) and for coupling from channel across the package (far-channel). It is usually measured by applying a full-scale signal in the adjacent channel. Crosstalk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. It is typically expressed in dBc.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2010) to Revision B	Page
• Updated Figure 44	40

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS58C28IRGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ58C28
ADS58C28IRGCR.A	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ58C28
ADS58C28IRGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ58C28
ADS58C28IRGCT.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ58C28

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

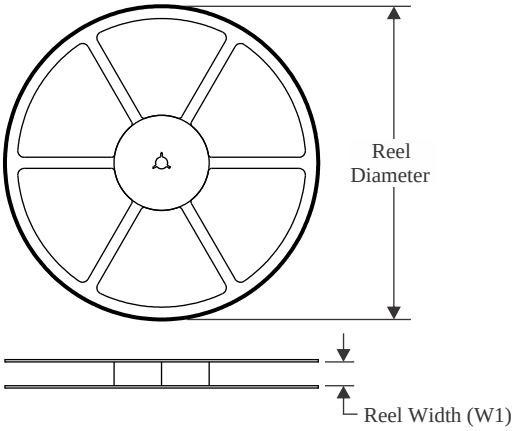
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

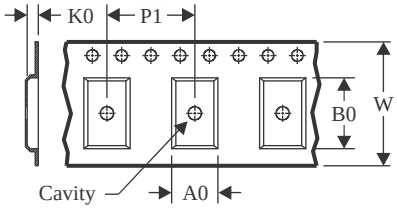
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

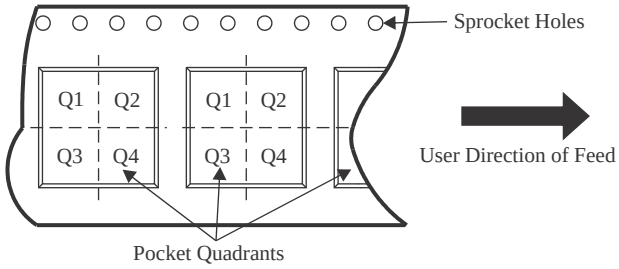


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

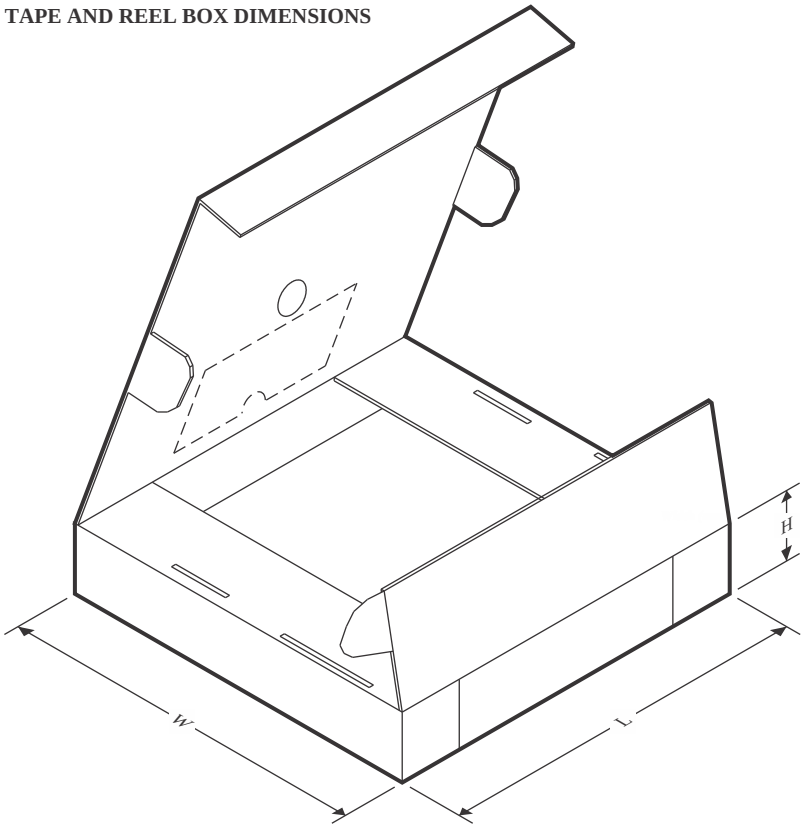
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS58C28IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS58C28IRGCR	VQFN	RGC	64	2000	350.0	350.0	43.0

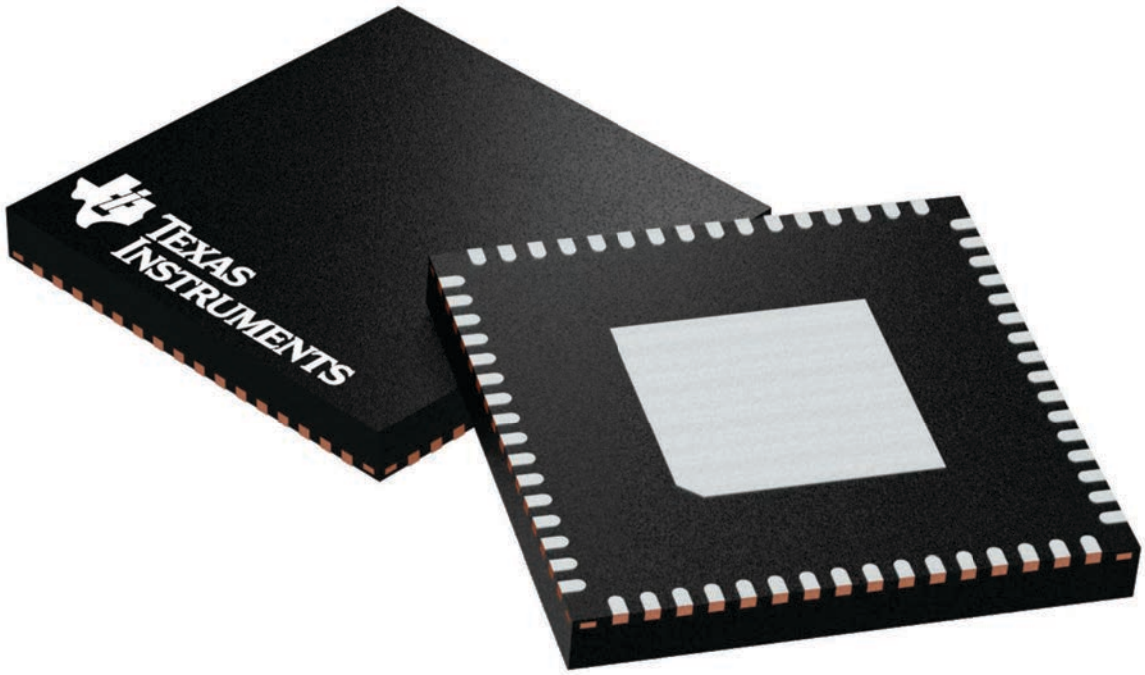
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

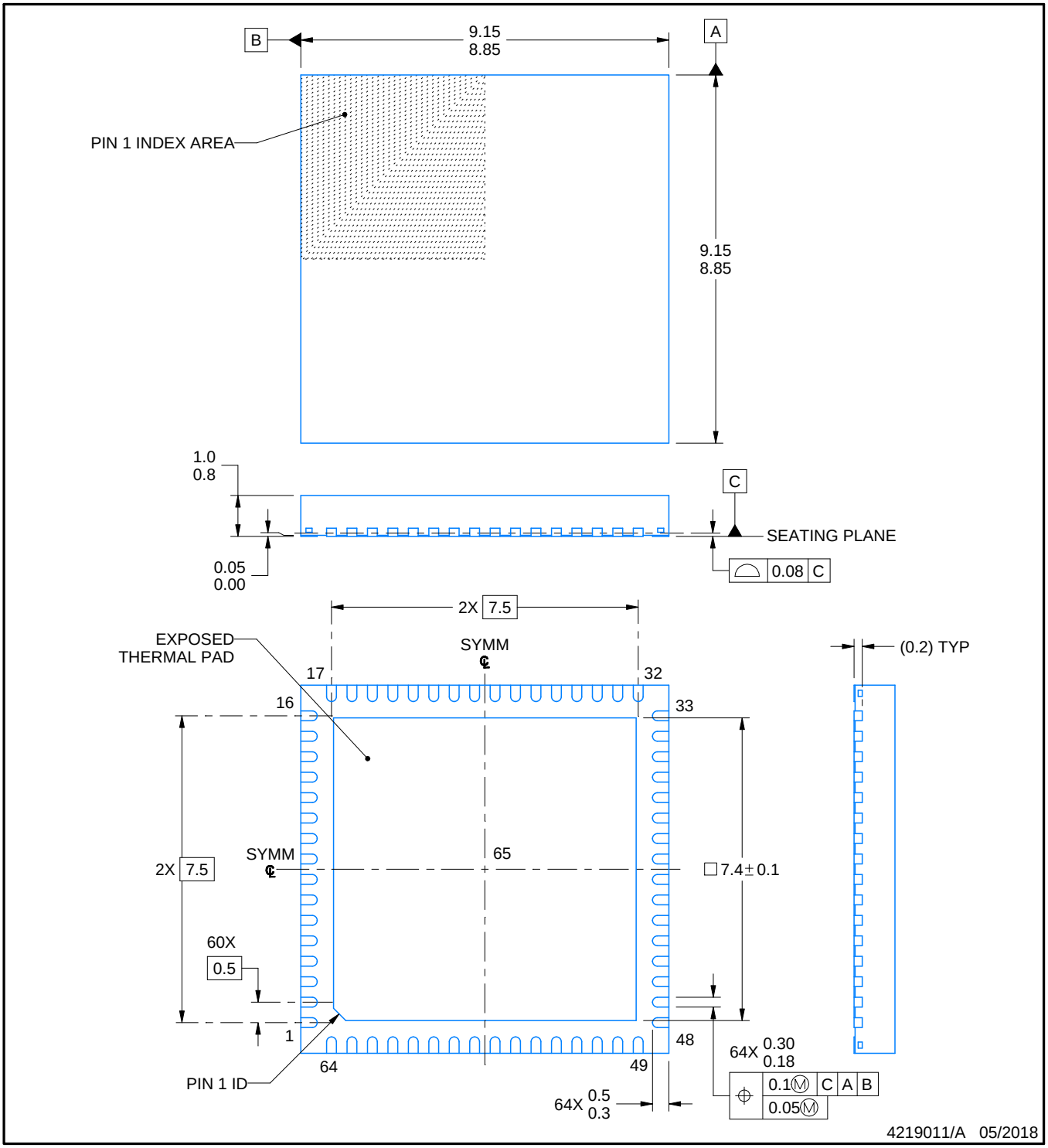
4224597/A

RGC0064H

PACKAGE OUTLINE

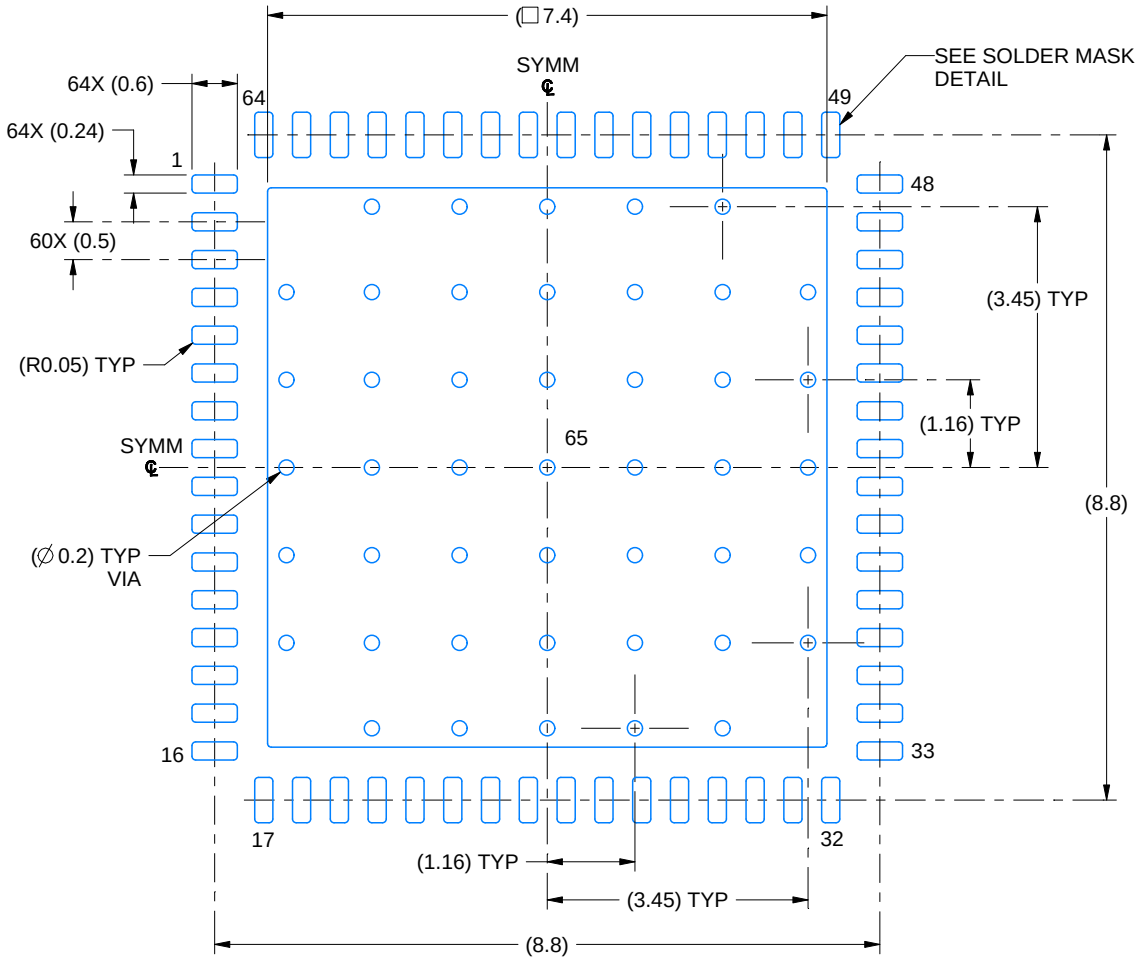
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

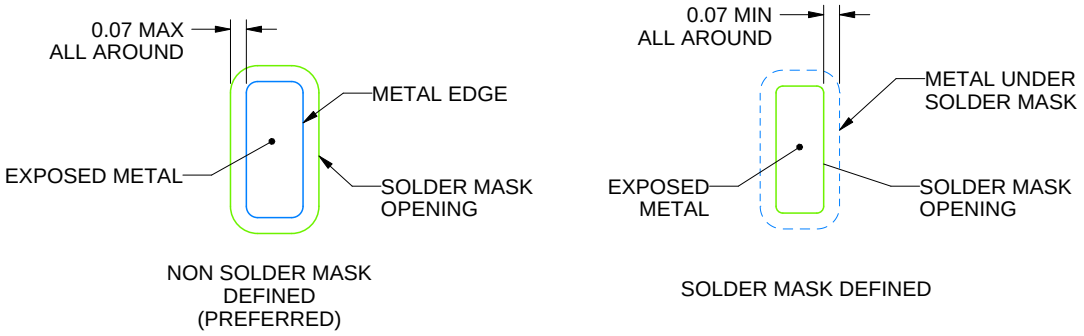


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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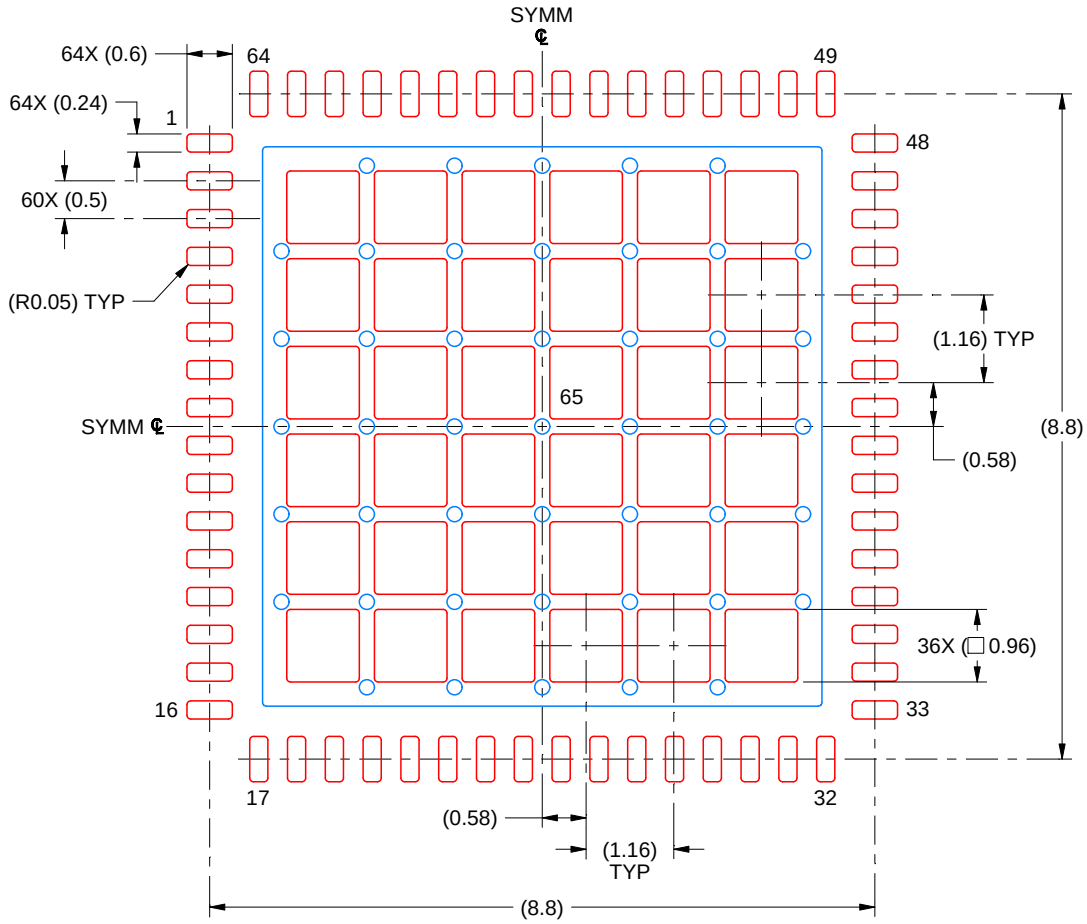
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
61% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219011/A 05/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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