ADS54J69 双通道、16 位、500MSPS 模数转换器

1 特性

- 16 位分辨率、双通道、500 MSPS 模数转换器 (DAC)
- 空闲通道噪底：-159dBFS/Hz
- 频谱性能（–1dBFS 时的 f_{IN} = 170MHz）：
  - 信噪比 (SNR)：73dBFS
  - 噪声频谱密度 (NSD)：–157dBFS/Hz
  - 无杂散动态范围 (SFDR)：93dBc
  - SFDR：94dBc（不包括 HD2、HD3 和交错音调）
- 频谱性能（–1dBFS 时的 f_{IN} = 310MHz）：
  - SNR：71.7dBFS
  - NSD：–155.7dBFS/Hz
  - SFDR：81dBc
  - SFDR：94dBc（不包括 HD2、HD3 和交错音调）
- 通道隔离：f_{IN} = 170MHz 时为 100dBc
- 输入满量程：1.9 V_{PP}
- 输入带宽 (3dB)：1.2GHz
- 片上抖动
- 集成 2 倍抽取率滤波器
- 支持 JESD204B 子类 1 接口：
  - 10.0Gbps 时每个 ADC 1 条通道
  - 5.0Gbps 时每个 ADC 2 条通道
  - 支持多芯片同步
- 功耗：500MSPS 时为 1.35W/通道
- 72 引脚超薄型四方扁平无引线 (VQFN) 封装 (10mm × 10mm)

2 应用

- 雷达和天线阵列
- 无线宽带
- 电缆 CMTS、DOCSIS 3.1 接收器
- 通信测试设备
- 微波接收器
- 软件定义无线电 (SDR)
- 数字转换器
- 医疗成像和诊断功能

3 说明

ADS54J69 是一款低功耗、高带宽 16 位、500MSPS 双通道模数转换器 (ADC)。该器件经设计具有高信噪比 (SNR)，可提供 -159dBFS/Hz 的噪底，从而 协助应用在宽瞬时带宽内 实现最高动态范围。该器件支持 JESD204B 串行接口，数据传输速率高达 10Gbps，每个 ADC 可支持 1 或 2 条通道。经缓冲的模拟输入可在较宽频率范围内提供统一输入阻抗并最大程度地降低采样和保持毛刺脉冲能量。可选择将每条 ADC 通道直接与宽带数字下变频器 (DDC) 模块相连。ADS54J69 以超低功耗在宽输入频率范围内提供出色的无杂散动态范围 (SFDR)。

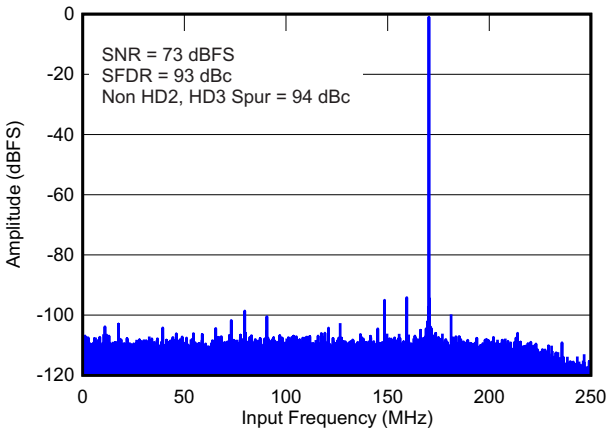
JESD204B 接口减少了接口线路数，从而实现高系统集成度。内部锁相环 (PLL) 会将 ADC 采样时钟加倍，以获得串行化各通道的 16 位数据时所使用的位时钟。

器件信息

器件编号	封装	封装尺寸（标称值）
ADS54J69	VQFNP (72)	10.00mm x 10.00mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

170MHz 中频 (IF) 时的频谱



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (February 2016) to Revision C — **Page**

- Added *Device Comparison Table* ... 5
- Added the FOVR latency parameter to the *Timing Characteristics* table ... 12
- Added *SYSREF Not Present (Subclass 0, 2)* section ... 27
- Changed the number of clock cycles in the *Fast OVR* section ... 28
- Changed the *Register Map* ... 40
- Deleted register 39h, 3Ah, and 56h ... 40
- Changed the *SNR versus Input Frequency and External Clock Jitter* figure ... 67
- Changed *Power Supply Recommendations* section ... 70
- Added the *Power Sequencing and Initialization* section ... 71
- 已添加 *文档支持*和*接收文档更新通知*部分 ... 74
- 已添加 *接收文档更新通知*部分 ... 74

Changes from Revision A (January 2016) to Revision B — **Page**

- Changed Sample Timing, *Aperture jitter* parameter in *Timing Characteristics* table ... 12
- Changed Table 35 ... 51
- Changed Table 42 ... 54
- Changed Table 44 ... 55
- Changed *SNR and Clock Jitter* section: changed Figure 130 and last sentence of section ... 67
- Changed *Application Curves* section ... 70

Changes from Original (May 2015) to Revision A **Page**

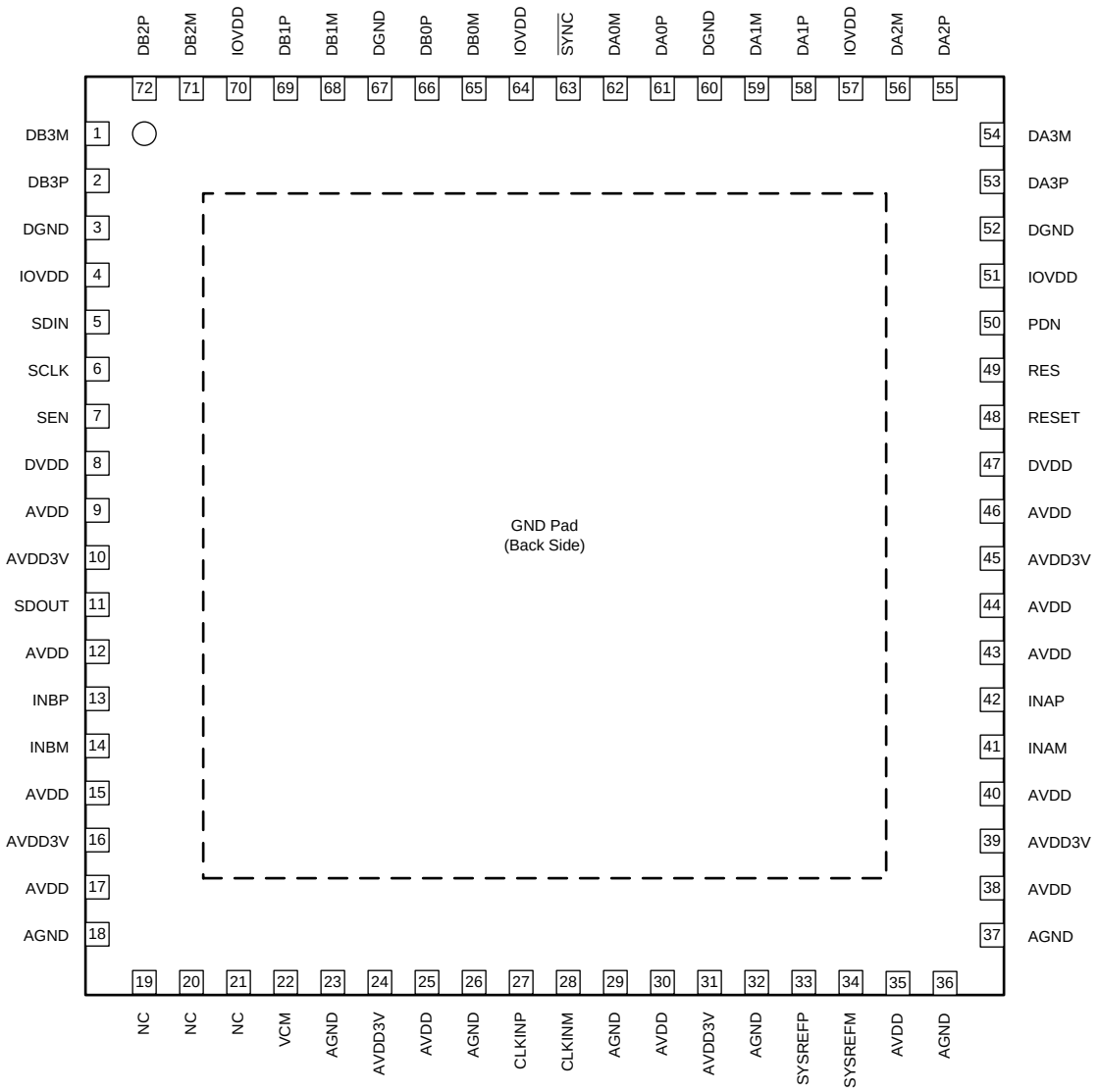
- 已发布为“量产数据”..... 1

5 Device Comparison Table

PART NUMBER	SPEED GRADE (MSPS)	RESOLUTION (Bits)	CHANNEL
ADS54J20	1000	12	2
ADS54J42	625	14	2
ADS54J40	1000	14	2
ADS54J60	1000	16	2
ADS54J66	500	14	4
ADS54J69	500	16	2

6 Pin Configuration and Functions

RMP Package
72-Pin VQFNP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CLOCK, SYSREF			
CLKINM	28	I	Negative differential clock input for the ADC
CLKINP	27	I	Positive differential clock input for the ADC
SYSREFM	34	I	Negative external SYSREF input
SYSREFP	33	I	Positive external SYSREF input
CONTROL, SERIAL INTERFACE			
PDN	50	I/O	Power-down. Can be configured via an SPI register setting. Can be configured to fast overrange output for channel A via the SPI.
RESET	48	I	Hardware reset; active high. This pin has an internal 20-kΩ pulldown resistor.
SCLK	6	I	Serial interface clock input
SDIN	5	I	Serial interface data input
SDOUT	11	O	Serial interface data output. Can be configured to fast overrange output for channel B via the SPI.
SEN	7	I	Serial interface enable
DATA INTERFACE			
DA0M	62	O	JESD204B serial data negative outputs for channel A
DA1M	59		
DA2M	56		
DA3M	54		
DA0P	61	O	JESD204B serial data positive outputs for channel A
DA1P	58		
DA2P	55		
DA3P	53		
DB0M	65	O	JESD204B serial data negative outputs for channel B
DB1M	68		
DB2M	71		
DB3M	1		
DB0P	66	O	JESD204B serial data positive outputs for channel B
DB1P	69		
DB2P	72		
DB3P	2		
$\overline{\text{SYNC}}$	63	I	Synchronization input for JESD204B port
INPUT, COMMON MODE			
INAM	41	I	Differential analog negative input for channel A
INAP	42	I	Differential analog positive input for channel A
INBM	14	I	Differential analog negative input for channel B
INBP	13	I	Differential analog positive input for channel B
VCM	22	O	Common-mode voltage, 2.1 V. Note that analog inputs are internally biased to this pin through 600 Ω (effective), no external connection from the VCM pin to the INxP or INxM pin is required.
POWER SUPPLY			
AGND	18, 23, 26, 29, 32, 36, 37	I	Analog ground
AVDD	9, 12, 15, 17, 25, 30, 35, 38, 40, 43, 44, 46	I	Analog 1.9-V power supply
AVDD3V	10, 16, 24, 31, 39, 45	I	Analog 3.0-V power supply for the analog buffer
DGND	3, 52, 60, 67	I	Digital ground
DVDD	8, 47	I	Digital 1.9-V power supply
IOVDD	4, 51, 57, 64, 70	I	Digital 1.15-V power supply for the JESD204B transmitter
NC, RES			
NC	19, 20, 21	—	Unused pins, do not connect
RES	49	I	Reserved pin. Connect to DGND.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range	AVDD3V	–0.3	3.6	V
	AVDD	–0.3	2.1	
	DVDD	–0.3	2.1	
	IOVDD	–0.2	1.4	
Voltage between AGND and DGND		–0.3	0.3	V
Voltage applied to input pins	INAP, INBP, INAM, INBM	–0.3	3	V
	CLKINP, CLKINM	–0.3	AVDD + 0.3	
	SYSREFP, SYSREFM	–0.3	AVDD + 0.3	
	SCLK, SEN, SDIN, RESET, $\overline{\text{SYNC}}$, PDN	–0.2	2.1	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	NOM	MAX	UNIT
Supply voltage range	AVDD3V		2.85	3.0	3.6	V
	AVDD		1.8	1.9	2.0	
	DVDD		1.7	1.9	2.0	
	IOVDD		1.1	1.15	1.2	
Analog inputs	Differential input voltage range			1.9		V_{PP}
	Input common-mode voltage			2.0		V
	Maximum analog input frequency for 1.9-V_{PP} input amplitude(3)(4)			400		MHz
Clock inputs	Input clock frequency, device clock frequency		500		1000	MHz
	Input clock amplitude differential ($V_{CLKP} - V_{CLKM}$)	Sine wave, ac-coupled	0.75	1.5		V_{PP}
		LVPECL, ac-coupled	0.8	1.6		
		LVDS, ac-coupled		0.7		
	Input device clock duty cycle		45%	50%	55%	
Temperature	Operating free-air, T_A		–40		85	°C
	Operating junction, T_J			105(5)	125	

(1) SYSREF must be applied for the device to initialize; see the *SYSREF Signal* section for details.
(2) After power-up, always use a hardware reset to reset the device for the first time; see Table 60 for details.
(3) Operating 0.5 dB below the maximum-supported amplitude is recommended to accommodate gain mismatch in interleaving ADCs.
(4) At high frequencies, the maximum supported input amplitude reduces; see Figure 51 for details.
(5) Prolonged use above the nominal junction temperature can increase the device failure-in-time (FIT) rate.

7.4 Thermal Information

THERMAL METRIC(1)		ADS54J69 RMP (VQFNP) 72 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	22.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	5.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	2.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	2.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, device clock frequency = 1 GSPS, output sampling rate = 500 MSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, –1-dBFS differential input, and 0-dB digital gain (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
	Device clock frequency				1000	MSPS
	Output sample rate				500	MSPS
	Resolution		16			Bits
POWER SUPPLIES						
AVDD3V	3.0-V analog supply		2.85	3.0	3.6	V
AVDD	1.9-V analog supply		1.8	1.9	2.0	V
DVDD	1.9-V digital supply		1.7	1.9	2.0	V
IOVDD	1.15-V SERDES supply		1.1	1.15	1.2	V
I_{AVDD3V}	3.0-V analog supply current	V_{IN} = full-scale on both channels		293	360	mA
I_{AVDD}	1.9-V analog supply current	V_{IN} = full-scale on both channels		354	510	mA
I_{DVDD}	1.9-V digital supply current	Four-lane output mode (default after reset)		188	260	mA
I_{IOVDD}	1.15-V SERDES supply current			512	920	mA
P_{dis}	Total power dissipation			2.66	3.1	W
I_{DVDD}	1.9-V digital supply current	Two-lane output mode		195		mA
I_{IOVDD}	1.15-V SERDES supply current			559		mA
P_{dis}	Total power dissipation			2.73		W
	Global power-down power dissipation	Using the GLOBAL PDN register bit in the master page		204	315	mW

7.6 AC Characteristics

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, device clock frequency = 1 GSPS, output sampling rate = 500 MSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, –1-dBFS differential input, and 0-dB digital gain (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz, A_{IN} = –1 dBFS		74.2		dBFS
		f_{IN} = 140 MHz, A_{IN} = –1 dBFS		73.4		
		f_{IN} = 170 MHz, A_{IN} = –1 dBFS	71.3	73		
		f_{IN} = 210 MHz, A_{IN} = –1 dBFS		72.7		
		f_{IN} = 310 MHz, A_{IN} = –1 dBFS		71.7		
		f_{IN} = 370 MHz, A_{IN} = –1 dBFS		70.3		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS		70.5		
NSD	Noise spectral density	f_{IN} = 10 MHz, A_{IN} = –1 dBFS		158.2		dBFS/Hz
		f_{IN} = 140 MHz, A_{IN} = –1 dBFS		157.4		
		f_{IN} = 170 MHz, A_{IN} = –1 dBFS	155.3	157.0		
		f_{IN} = 210 MHz, A_{IN} = –1 dBFS		156.7		
		f_{IN} = 310 MHz, A_{IN} = –1 dBFS		155.7		
		f_{IN} = 370 MHz, A_{IN} = –1 dBFS		154.3		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS		154.5		
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz, A_{IN} = –1 dBFS		73.8		dBFS
		f_{IN} = 140 MHz, A_{IN} = –1 dBFS		73.3		
		f_{IN} = 170 MHz, A_{IN} = –1 dBFS	69.8	72.9		
		f_{IN} = 210 MHz, A_{IN} = –1 dBFS		72.5		
		f_{IN} = 310 MHz, A_{IN} = –1 dBFS		71.2		
		f_{IN} = 370 MHz, A_{IN} = –1 dBFS		70.2		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS		69.4		
SFDR	Spurious free dynamic range (excluding IL spurs)	f_{IN} = 10 MHz, A_{IN} = –1 dBFS		86		dBc
		f_{IN} = 140 MHz, A_{IN} = –1 dBFS		95		
		f_{IN} = 170 MHz, A_{IN} = –1 dBFS	79	94		
		f_{IN} = 210 MHz, A_{IN} = –1 dBFS		89		
		f_{IN} = 310 MHz, A_{IN} = –1 dBFS		81		
		f_{IN} = 370 MHz, A_{IN} = –1 dBFS		87		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS		73		
HD2	Second-order harmonic distortion	f_{IN} = 10 MHz, A_{IN} = –1 dBFS		86		dBc
		f_{IN} = 140 MHz, A_{IN} = –1 dBFS		104		
		f_{IN} = 170 MHz, A_{IN} = –1 dBFS	85	102		
		f_{IN} = 210 MHz, A_{IN} = –1 dBFS		95		
		f_{IN} = 310 MHz, A_{IN} = –1 dBFS		81		
		f_{IN} = 370 MHz, A_{IN} = –1 dBFS		87		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS		96		
HD3	Third-order harmonic distortion	f_{IN} = 10 MHz, A_{IN} = –1 dBFS		89		dBc
		f_{IN} = 140 MHz, A_{IN} = –1 dBFS		103		
		f_{IN} = 170 MHz, A_{IN} = –1 dBFS	86	101		
		f_{IN} = 210 MHz, A_{IN} = –1 dBFS		100		
		f_{IN} = 310 MHz, A_{IN} = –1 dBFS		98		
		f_{IN} = 370 MHz, A_{IN} = –1 dBFS		95		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS		73		

AC Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, device clock frequency = 1 GSPS, output sampling rate = 500 MSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, –1-dBFS differential input, and 0-dB digital gain (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3, and IL spur)	f_{IN} = 10 MHz, A_{IN} = –1 dBFS		98		dBc
		f_{IN} = 140 MHz, A_{IN} = –1 dBFS		95		
		f_{IN} = 170 MHz, A_{IN} = –1 dBFS	84	94		
		f_{IN} = 210 MHz, A_{IN} = –1 dBFS		89		
		f_{IN} = 310 MHz, A_{IN} = –1 dBFS		92		
		f_{IN} = 370 MHz, A_{IN} = –1 dBFS		97		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS		92		
ENOB	Effective number of bits	f_{IN} = 10 MHz, A_{IN} = –1 dBFS		12		Bits
		f_{IN} = 140 MHz, A_{IN} = –1 dBFS		11.9		
		f_{IN} = 170 MHz, A_{IN} = –1 dBFS	11.3	11.9		
		f_{IN} = 210 MHz, A_{IN} = –1 dBFS		11.8		
		f_{IN} = 310 MHz, A_{IN} = –1 dBFS		11.5		
		f_{IN} = 370 MHz, A_{IN} = –1 dBFS		11.4		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS		11.2		
THD	Total harmonic distortion	f_{IN} = 10 MHz, A_{IN} = –1 dBFS		84		dBc
		f_{IN} = 140 MHz, A_{IN} = –1 dBFS		95		
		f_{IN} = 170 MHz, A_{IN} = –1 dBFS	79	89		
		f_{IN} = 210 MHz, A_{IN} = –1 dBFS		85		
		f_{IN} = 310 MHz, A_{IN} = –1 dBFS		80		
		f_{IN} = 370 MHz, A_{IN} = –1 dBFS		85		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS		72		
SFDR_IL	Interleaving spur	f_{IN} = 10 MHz, A_{IN} = –1 dBFS		90		dBc
		f_{IN} = 140 MHz, A_{IN} = –1 dBFS		90		
		f_{IN} = 170 MHz, A_{IN} = –1 dBFS	75	87		
		f_{IN} = 210 MHz, A_{IN} = –1 dBFS		85		
		f_{IN} = 310 MHz, A_{IN} = –1 dBFS		85		
		f_{IN} = 370 MHz, A_{IN} = –1 dBFS		86		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS		82		
IMD3	Two-tone, third-order intermodulation distortion	f_{IN1} = 185 MHz, f_{IN2} = 190 MHz, A_{IN} = –7 dBFS		86		dBFS
		f_{IN1} = 365 MHz, f_{IN2} = 370 MHz, A_{IN} = –7 dBFS		79		
		f_{IN1} = 465 MHz, f_{IN2} = 470 MHz, A_{IN} = –10 dBFS		78		

7.7 Digital Characteristics

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, device clock frequency = 1 GSPS, output sampling rate = 500 MSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, –1-dBFS differential input, and 0-dB digital gain (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (RESET, SCLK, SEN, SDIN, $\overline{\text{SYNC}}$, PDN)(1)						
V_{IH}	High-level input voltage	All digital inputs support 1.2-V and 1.8-V logic levels	0.8			V
V_{IL}	Low-level input voltage	All digital inputs support 1.2-V and 1.8-V logic levels			0.4	V
I_{IH}	High-level input current	SEN		0		µA
		RESET, SCLK, SDIN, PDN, $\overline{\text{SYNC}}$		50		
I_{IL}	Low-level input current	SEN		50		µA
		RESET, SCLK, SDIN, PDN, $\overline{\text{SYNC}}$		0		
DIGITAL INPUTS (SYSREFP, SYSREFM)						
V_D	Differential input voltage		0.35	0.45	1.4	V
$V_{(CM\_DIG)}$	Common-mode voltage for SYSREF(2)			1.3		V
DIGITAL OUTPUTS (SDOUT, PDN(3))						
V_{OH}	High-level output voltage		DVDD – 0.1	DVDD		V
V_{OL}	Low-level output voltage				0.1	V
DIGITAL OUTPUTS (JESD204B Interface: DxP, DxM)(4)						
V_{OD}	Output differential voltage	With default swing setting		700		mV_{PP}
V_{OC}	Output common-mode voltage			450		mV
	Transmitter short-circuit current	Transmitter pins shorted to any voltage between –0.25 V and 1.45 V	–100		100	mA
z_{os}	Single-ended output impedance			50		Ω
	Output capacitance	Output capacitance inside the device, from either output to ground		2		pF

(1) The RESET, SCLK, SDIN, and PDN pins have a 20-kΩ (typical) internal pulldown resistor to ground, and the SEN pin has a 20-kΩ (typical) pullup resistor to IOVDD.
(2) The SYSREFP and SYSREFM pins are internally biased to the 1.3-V common-mode voltage through a 5-kΩ resistor.
(3) When functioning as an OVR pin for channel B.
(4) 100-Ω differential termination.

7.8 Timing Characteristics

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, device clock frequency = 1 GSPS, output sampling rate = 500 MSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input (unless otherwise noted)

			MIN	TYP	MAX	UNITS
SAMPLE TIMING						
	Aperture delay		0.75		1.6	ns
	Aperture delay matching between two channels on the same device			±70		ps
	Aperture delay matching between two devices at the same temperature and supply voltage			±270		ps
	Aperture jitter	Actual jitter of sampling clock buffer		145		f_S rms
		Effective jitter after decimation filtering		102		
WAKE-UP TIMING						
	Wake-up time to valid data after coming out of global power-down			150		µs
LATENCY						
	Data latency(1): ADC sample to digital output			134(2)		Input clock cycles
	OVR latency: ADC sample to OVR bit			62		Input clock cycles
	FOVR latency: ADC sample to FOVR signal on pin			18 + 4 ns		Input clock cycles
t_{PD}	Propagation delay: logic gates and output buffers delay (does not change with f_S)			4		ns
SYSREF TIMING						
t_{SU_SYSREF}	Setup time for SYSREF, referenced to the input clock falling edge		300		900	ps
t_{H_SYSREF}	Hold time for SYSREF, referenced to the input clock falling edge		100			ps
JESD OUTPUT INTERFACE TIMING CHARACTERISTICS						
	Unit interval		100		400	ps
	Serial output data rate		2.5		10	Gbps
	Total jitter for BER of 1E-15 and lane rate = 10 Gbps			26		ps
	Random jitter for BER of 1E-15 and lane rate = 10 Gbps			0.75		ps rms
	Deterministic jitter for BER of 1E-15 and lane rate = 10 Gbps			12		ps, pk-pk
t_R, t_F	Data rise time, data fall time: rise and fall times are measured from 20% to 80%, differential output waveform, 2.5 Gbps ≤ bit rate ≤ 10 Gbps			35		ps

(1) Overall latency = data latency + decimation filter delay + t_{PDI}.
(2) Decimation filter latency is not included in this specification.

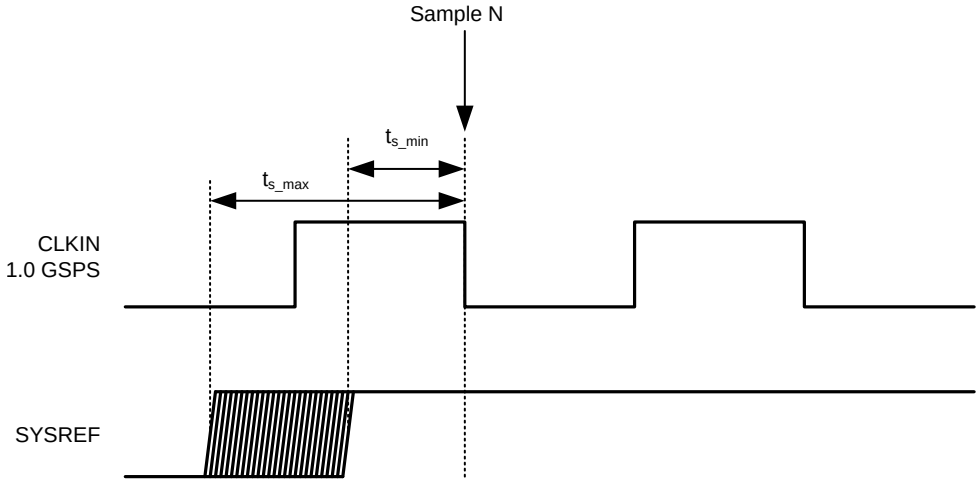


Figure 1. SYSREF Timing

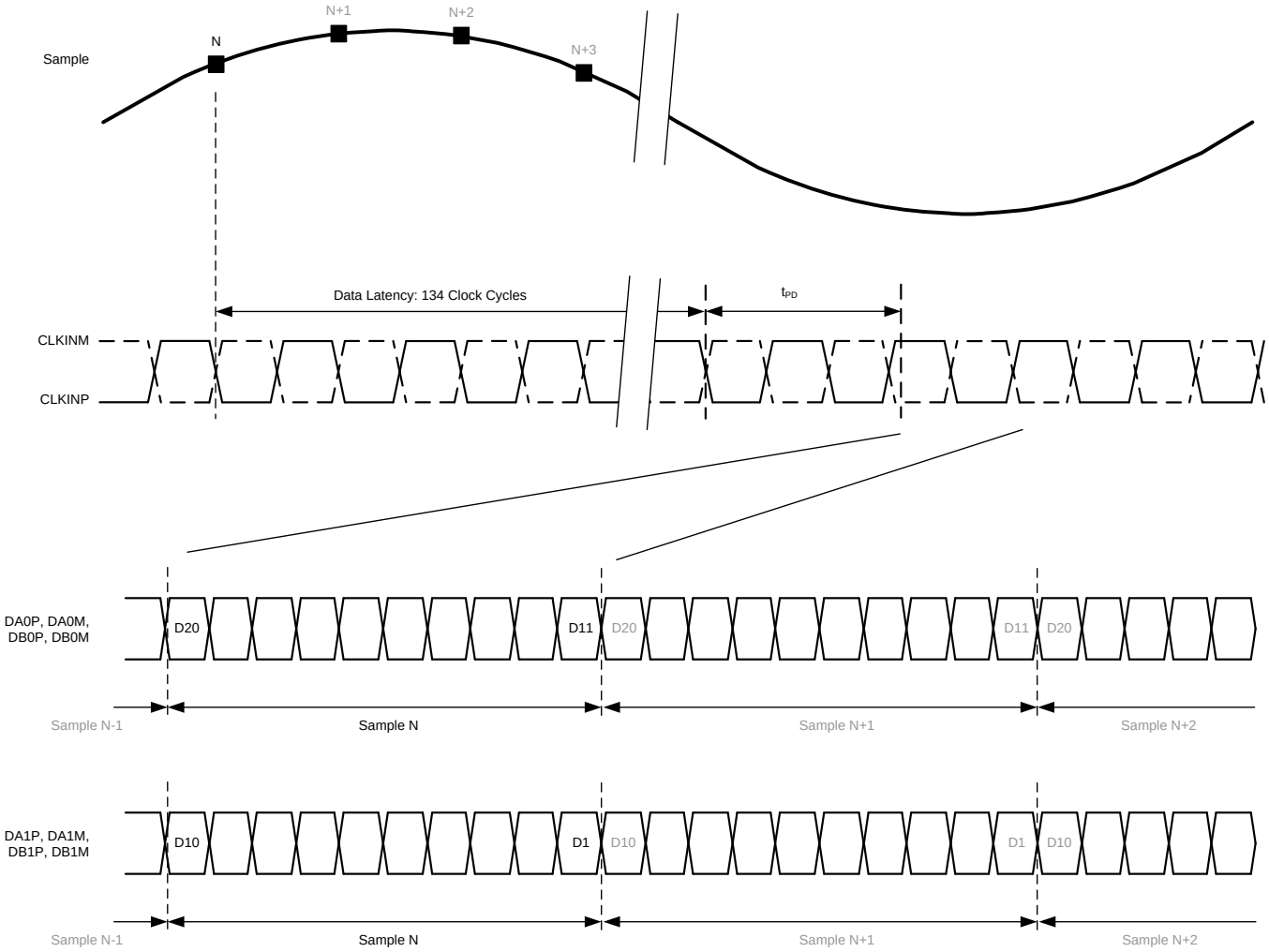
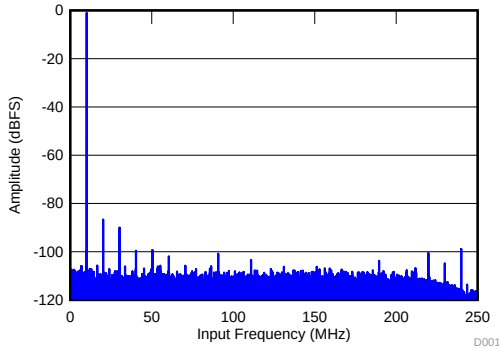


Figure 2. Sample Timing Requirements

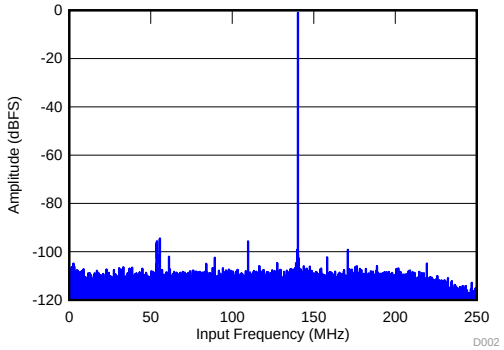
7.9 Typical Characteristics

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, device clock frequency = 1 GSPS, output sampling rate = 500 MSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input (unless otherwise noted)



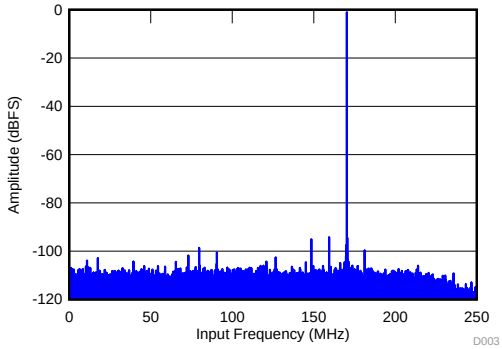
SNR = 74.2 dBFS; SFDR = 86 dBc; SINAD = 73.8 dBFS;
THD = 83 dBc; HD2 = 86 dBc; HD3 = 89 dBc;
IL spur = 99 dBc; non HD2, HD3 spur = 98 dBc

Figure 3. FFT for 10-MHz Input Signal



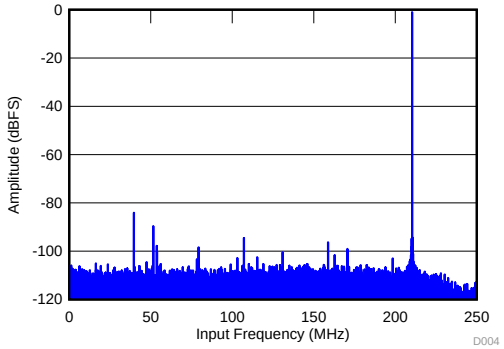
SNR = 73.3 dBFS; SFDR = 94 dBc; SINAD = 73.25 dBFS;
THD = 93 dBc; HD2 = 104 dBc; HD3 = 111 dBc;
IL spur = 95 dBc; non HD2, HD3 spur = 94 dBc

Figure 4. FFT for 140-MHz Input Signal



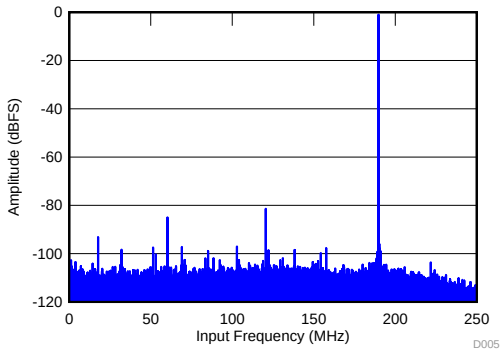
SNR = 73 dBFS; SFDR = 93 dBc; SINAD = 73.18 dBFS;
THD = 89 dBc; HD2 = 93 dBc; HD3 = 103 dBc;
IL spur = 99 dBc; non HD2, HD3 spur = 94 dBc

Figure 5. FFT for 170-MHz Input Signal



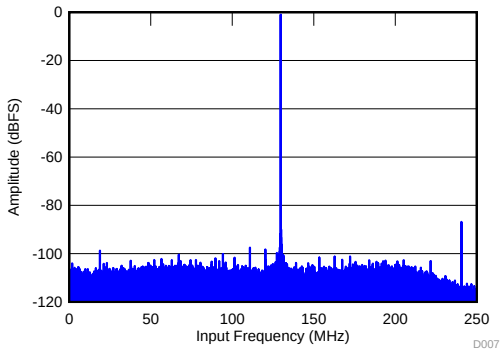
SNR = 72.8 dBFS; SFDR = 89 dBc; SINAD = 72.63 dBFS;
THD = 86 dBc; HD2 = 97 dBc; HD3 = 99 dBc;
IL spur = 84 dBc; non HD2, HD3 spur = 89 dBc

Figure 6. FFT for 210-MHz Input Signal



SNR = 71.6 dBFS; SFDR = 80 dBc; SINAD = 71 dBFS;
THD = 79 dBc; HD2 = –80 dBc; HD3 = –96 dBc;
IL spur = 85 dBc; non HD2, HD3 spur = 92 dBc

Figure 7. FFT for 310-MHz Input Signal

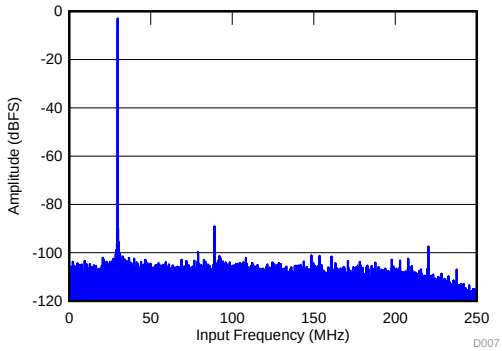


SNR = 70.5 dBFS; SFDR = 86 dBc; SINAD = 70.4 dBFS;
THD = 85 dBc; HD2 = –86 dBc; HD3 = –96 dBc;
IL spur = 98 dBc; non HD2, HD3 spur = 98 dBc

Figure 8. FFT for 370-MHz Input Signal

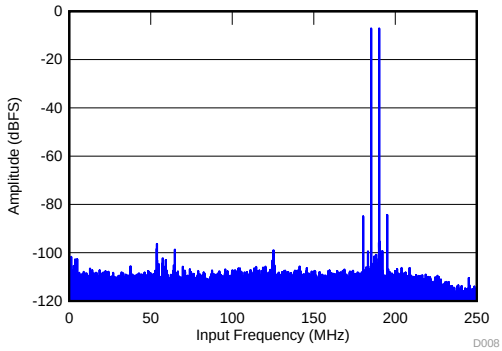
Typical Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, device clock frequency = 1 GSPS, output sampling rate = 500 MSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input (unless otherwise noted)



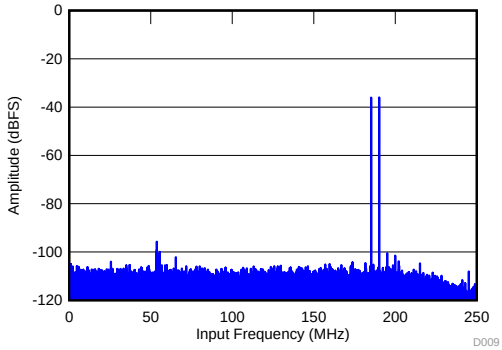
SNR = 70.6 dBFS; SFDR = 86 dBc; SINAD = 70.55 dBFS; THD = 85 dBc; tone at –3 dBFS; HD2 = 102 dBc; HD3 = 86 dBc; IL spur = 97 dBc; non HD2, HD3 spur = 96 dBc

Figure 9. FFT for 470-MHz Input Signal



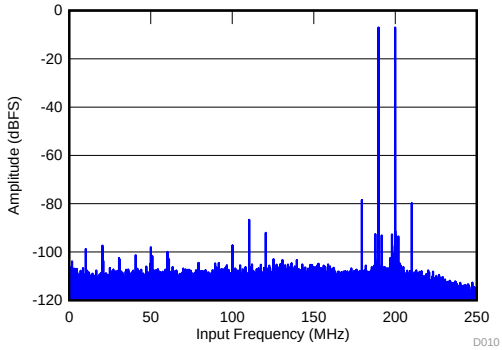
f_{IN1} = 185 MHz, f_{IN2} = 190 MHz, each tone at –7 dBFS, IMD = 86 dBFS

Figure 10. FFT for Two-Tone Input Signal (–7 dBFS)



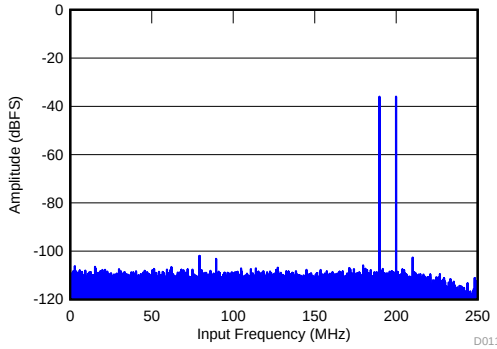
f_{IN1} = 185 MHz, f_{IN2} = 190 MHz, each tone at –36 dBFS, IMD = 101 dBFS

Figure 11. FFT for Two-Tone Input Signal (–36 dBFS)



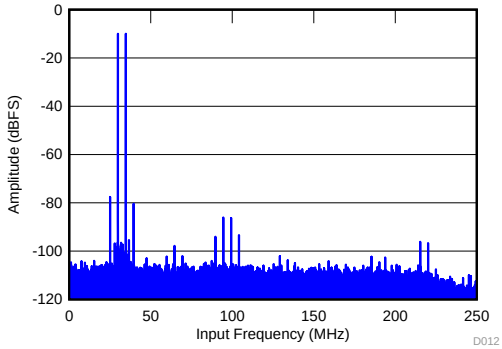
f_{IN1} = 300 MHz, f_{IN2} = 310 MHz, each tone at –7 dBFS, IMD = 79 dBFS

Figure 12. FFT for Two-Tone Input Signal (–7 dBFS)



f_{IN1} = 300 MHz, f_{IN2} = 310 MHz, each tone at –36 dBFS, IMD3 = 102 dBFS

Figure 13. FFT for Two-Tone Input Signal (–36 dBFS)

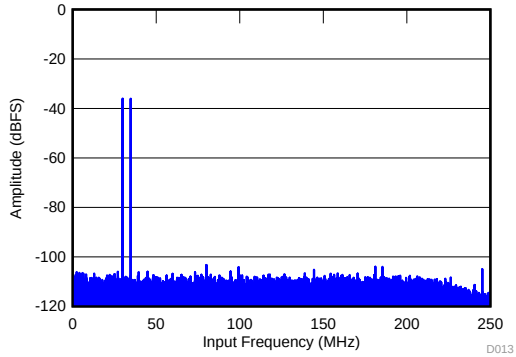


f_{IN1} = 470 MHz, f_{IN2} = 465 MHz, each tone at –10 dBFS, IMD = 78 dBFS

Figure 14. FFT for Two-Tone Input Signal (–10 dBFS)

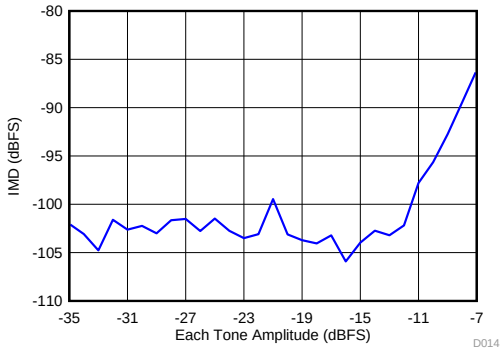
Typical Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, device clock frequency = 1 GSPS, output sampling rate = 500 MSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input (unless otherwise noted)



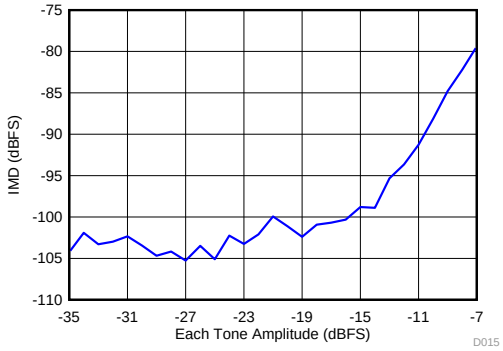
f_{IN1} = 470 MHz, f_{IN2} = 465 MHz, each tone at –36 dBFS, IMD3 = 104 dBFS

Figure 15. FFT for Two-Tone Input Signal (–36 dBFS)



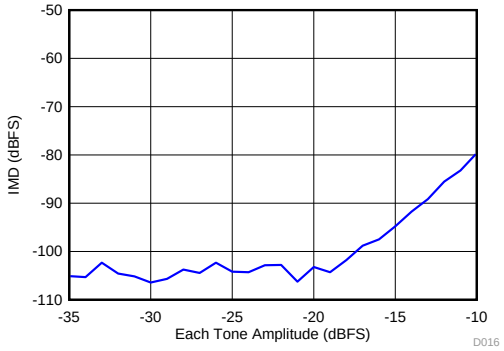
f_{IN1} = 185 MHz, f_{IN2} = 190 MHz

Figure 16. Intermodulation Distortion vs Input Amplitude (185 MHz and 190 MHz)



f_{IN1} = 300 MHz, f_{IN2} = 310 MHz

Figure 17. Intermodulation Distortion vs Input Amplitude (365 MHz and 370 MHz)



f_{IN1} = 465 MHz, f_{IN2} = 470 MHz

Figure 18. Intermodulation Distortion vs Input Amplitude (465 MHz and 470 MHz)

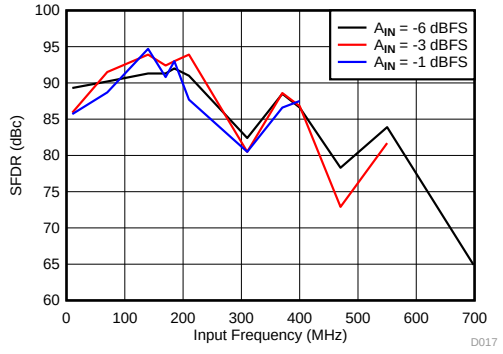


Figure 19. Spurious-Free Dynamic Range vs Input Frequency

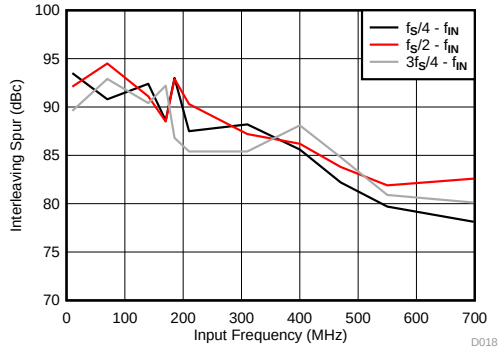


Figure 20. IL Spur vs Input Frequency

Typical Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, device clock frequency = 1 GSPS, output sampling rate = 500 MSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input (unless otherwise noted)

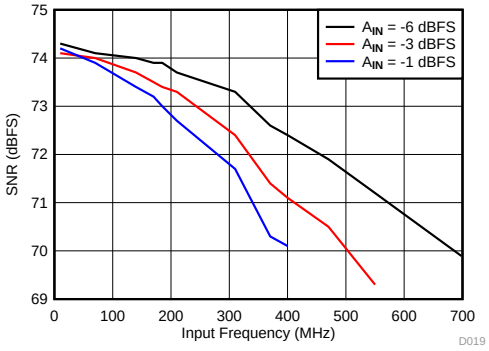
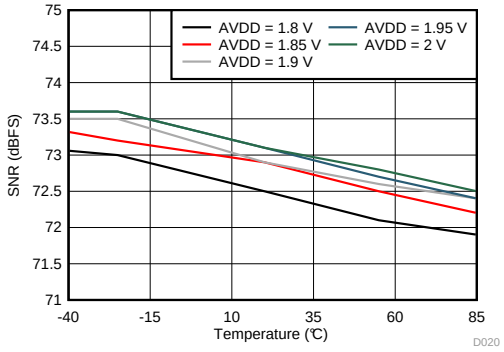
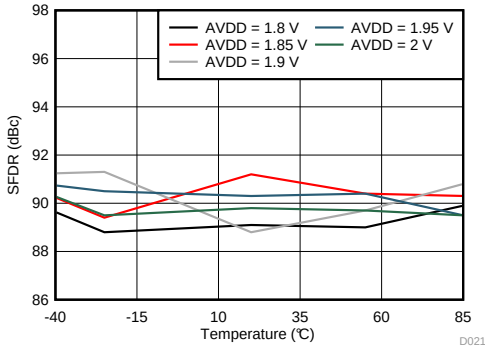


Figure 21. Signal-to-Noise Ratio vs Input Frequency



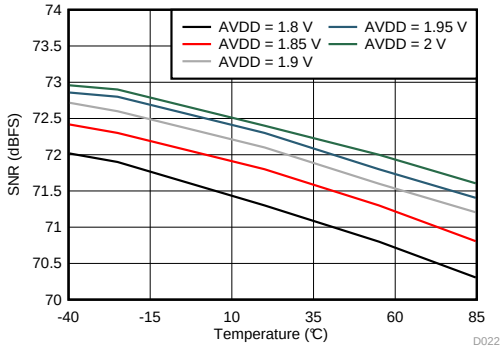
f_{IN} = 185 MHz

Figure 22. Signal-to-Noise Ratio vs AVDD Supply and Temperature



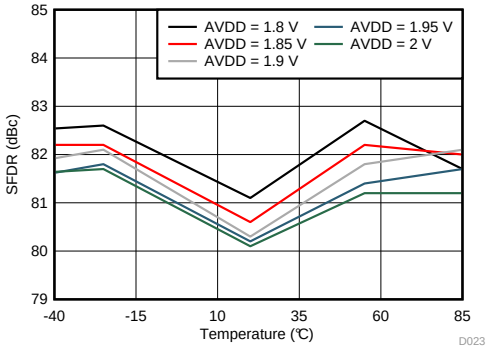
f_{IN} = 185 MHz

Figure 23. Spurious-Free Dynamic Range vs AVDD Supply and Temperature



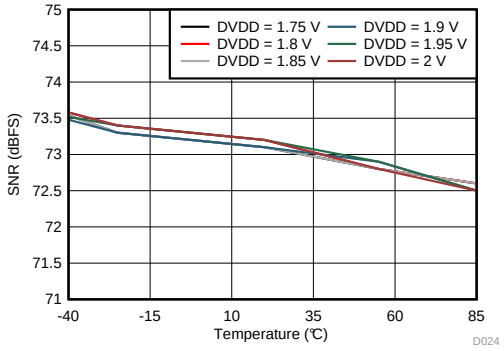
f_{IN} = 300 MHz

Figure 24. Signal-to-Noise Ratio vs AVDD Supply and Temperature



f_{IN} = 300 MHz

Figure 25. Spurious-Free Dynamic Range vs AVDD Supply and Temperature

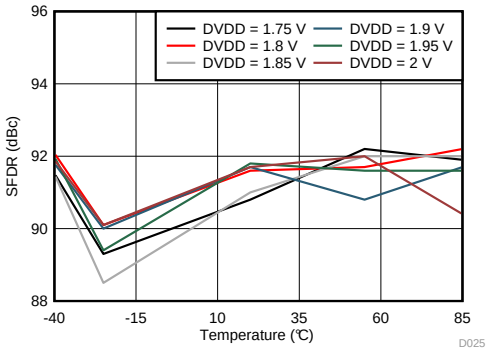


f_{IN} = 185 MHz

Figure 26. Signal-to-Noise Ratio vs DVDD Supply and Temperature

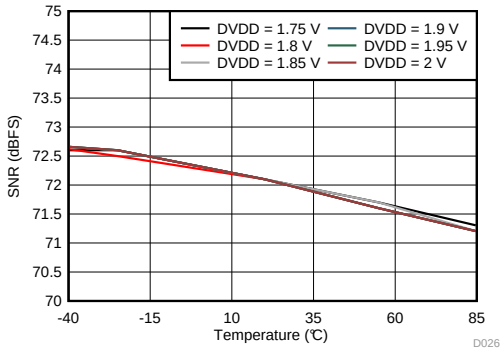
Typical Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, device clock frequency = 1 GSPS, output sampling rate = 500 MSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input (unless otherwise noted)



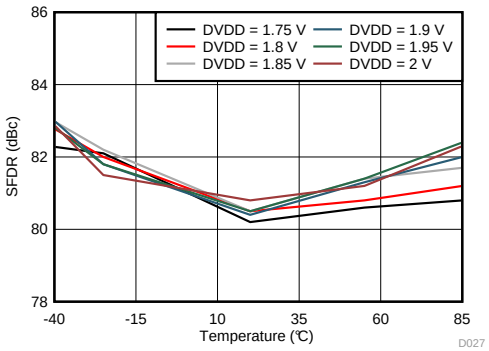
f_{IN} = 185 MHz

Figure 27. Spurious-Free Dynamic Range vs DVDD Supply and Temperature



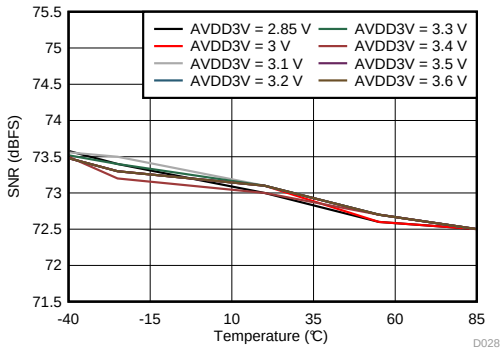
f_{IN} = 300 MHz

Figure 28. Signal-to-Noise Ratio vs DVDD Supply and Temperature



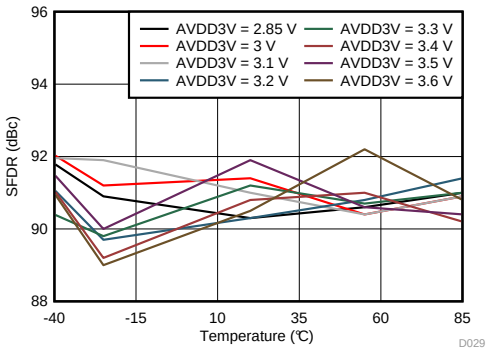
f_{IN} = 300 MHz

Figure 29. Spurious-Free Dynamic Range vs DVDD Supply and Temperature



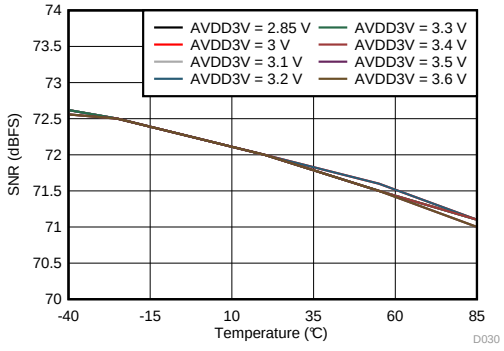
f_{IN} = 185 MHz

Figure 30. Signal-to-Noise Ratio vs AVDD3V Supply and Temperature



f_{IN} = 185 MHz

Figure 31. Spurious-Free Dynamic Range vs AVDD3V Supply and Temperature

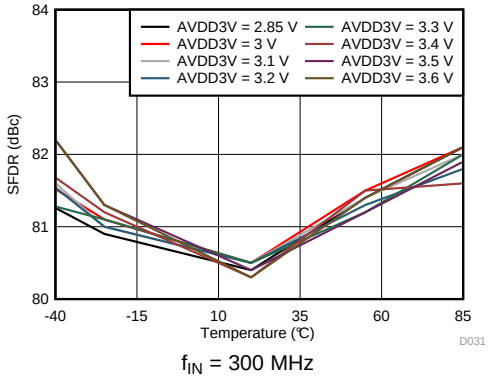


f_{IN} = 300 MHz

Figure 32. Signal-to-Noise Ratio vs AVDD3V Supply and Temperature

Typical Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, device clock frequency = 1 GSPS, output sampling rate = 500 MSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input (unless otherwise noted)



f_{IN} = 300 MHz

Figure 33. Spurious-Free Dynamic Range vs AVDD3V Supply and Temperature

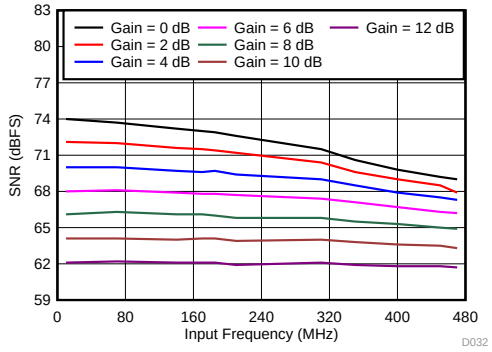


Figure 34. Signal-to-Noise Ratio vs Gain and Input Frequency

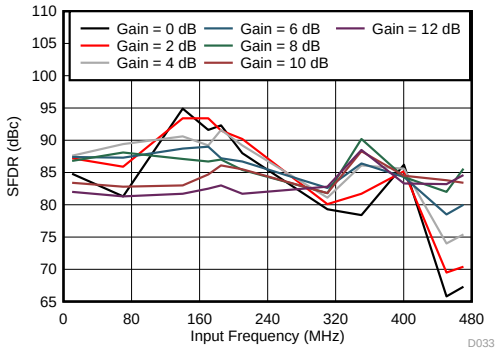


Figure 35. Spurious-Free Dynamic Range vs Gain and Input Frequency

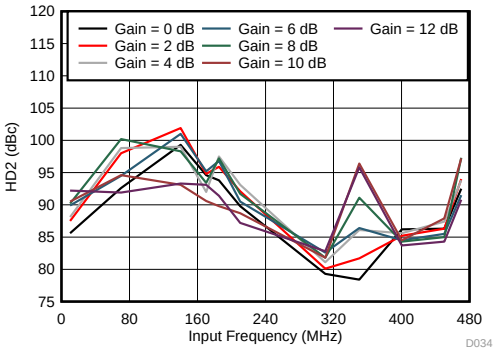


Figure 36. Second-Order Harmonic Distortion vs Gain and Input Frequency

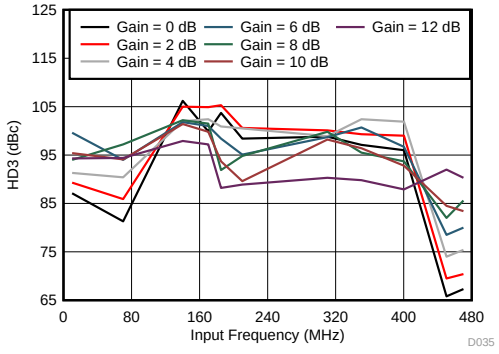


Figure 37. Third-Order Harmonic Distortion vs Gain and Input Frequency

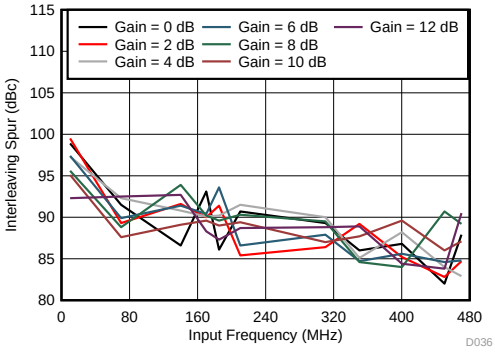
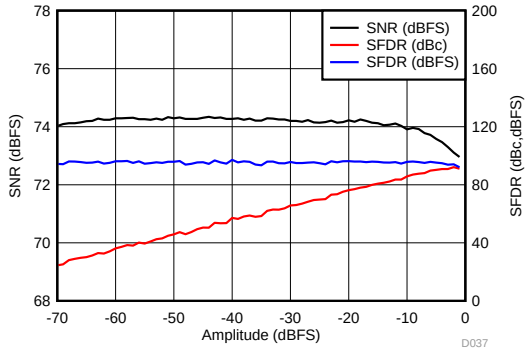


Figure 38. IL Spur vs Gain and Input Frequency

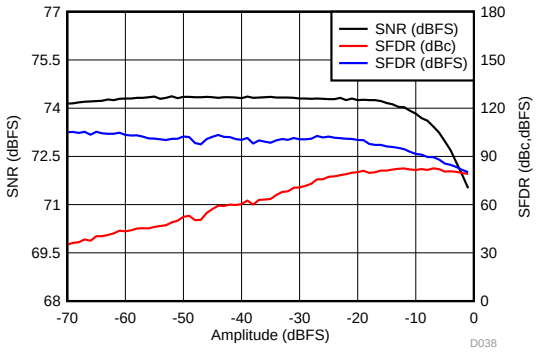
Typical Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, device clock frequency = 1 GSPS, output sampling rate = 500 MSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input (unless otherwise noted)



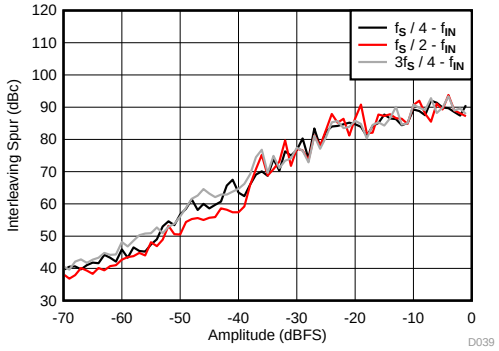
f_{IN} = 185 MHz

Figure 39. Performance vs Amplitude



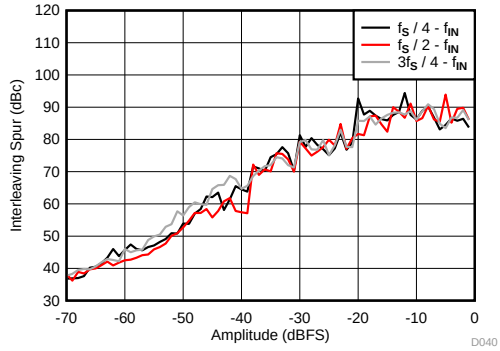
f_{IN} = 310 MHz

Figure 40. Performance vs Amplitude



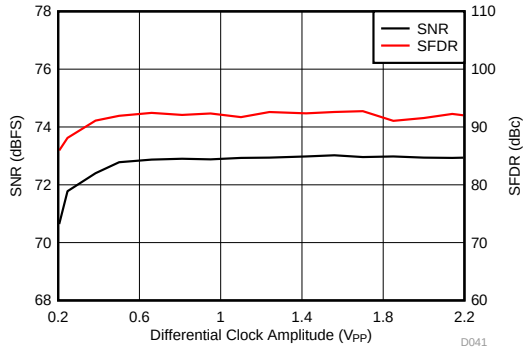
f_{IN} = 185 MHz

Figure 41. IL Spur vs Amplitude



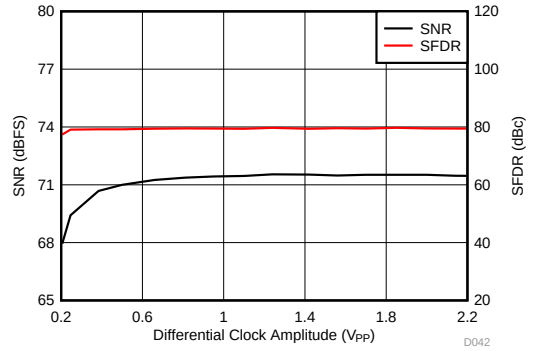
f_{IN} = 310 MHz

Figure 42. IL Spur vs Amplitude



f_{IN} = 185 MHz

Figure 43. Performance vs Differential Clock Amplitude

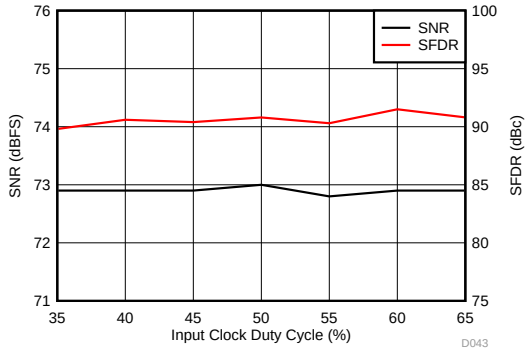


f_{IN} = 310 MHz

Figure 44. Performance vs Differential Clock Amplitude

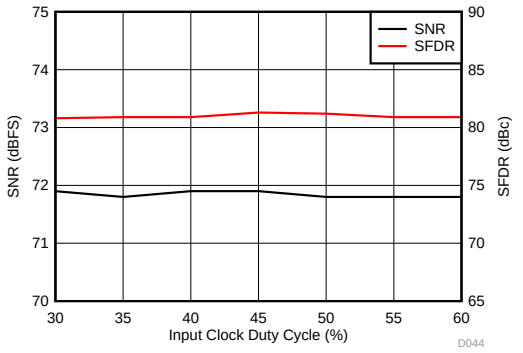
Typical Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, device clock frequency = 1 GSPS, output sampling rate = 500 MSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input (unless otherwise noted)



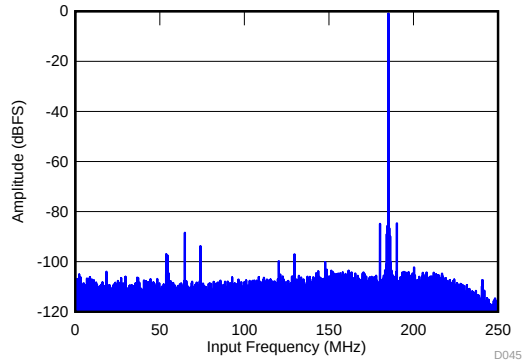
f_{IN} = 185 MHz

Figure 45. Performance vs Input Clock Duty Cycle



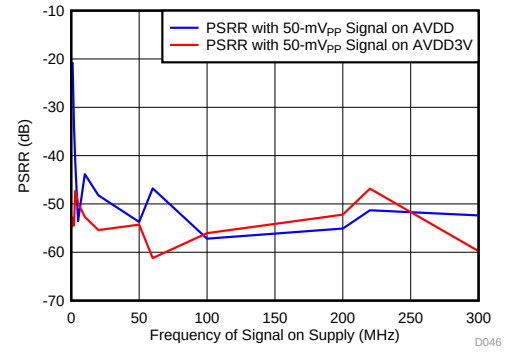
f_{IN} = 300 MHz

Figure 46. Performance vs Input Clock Duty Cycle



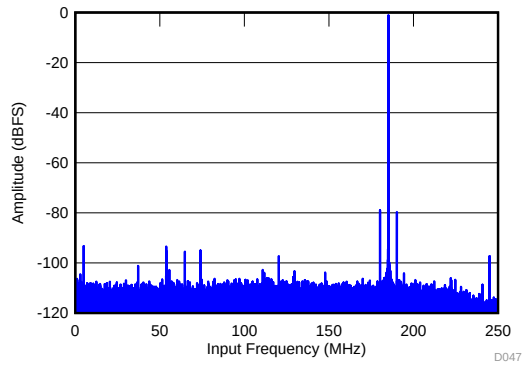
A_{IN} = –1 dBFS, SFDR = 84 dBc, SINAD = 70 dBFS, f_{PSRR} = 5 MHz, A_{PSRR} = 50 mV_{PP}, f_{IN} = 185 MHz, amplitude: $f_{IN} - f_{PSRR}$ = 85 dBc, $f_{IN} + f_{PSRR}$ = 84 dBc

Figure 47. Power-Supply Rejection Ratio FFT for AVDD Supply



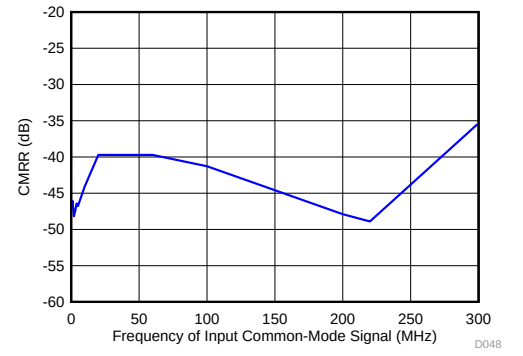
f_{IN} = 185 MHz

Figure 48. Power-Supply Rejection Ratio vs Noise Signal Frequency



A_{IN} = –1 dBFS, SFDR = 78 dBc, SINAD = 71 dBFS, f_{CMRR} = 5 MHz, A_{CMRR} = 50 mV_{PP}, f_{IN} = 185 MHz, amplitude: $f_{IN} - f_{CMRR}$ = 79 dBc, $f_{IN} + f_{CMRR}$ = 80 dBc

Figure 49. Common-Mode Rejection Ratio FFT



f_{IN} = 185 MHz

Figure 50. Common-Mode Rejection Ratio vs Common-Mode Signal Frequency

Typical Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, device clock frequency = 1 GSPS, output sampling rate = 500 MSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input (unless otherwise noted)

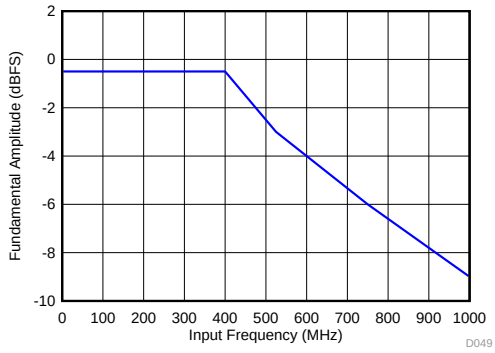


Figure 51. Maximum-Supported Amplitude vs Input Frequency

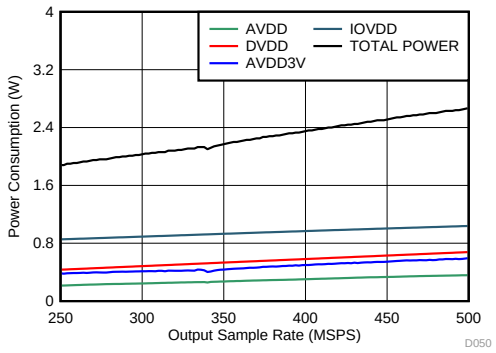


Figure 52. Power Consumption vs Sampling Speed

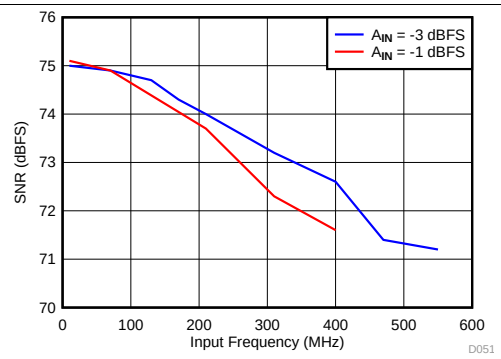


Figure 53. Signal-to-Noise Ratio vs Input Frequency (Output Sample Rate = 300 MSPS)

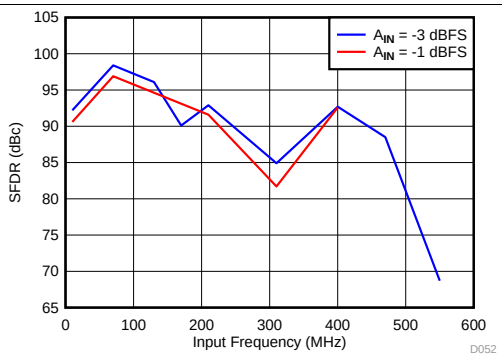


Figure 54. Spurious-Free Dynamic Range vs Input Frequency (Output Sample Rate = 300 MSPS)

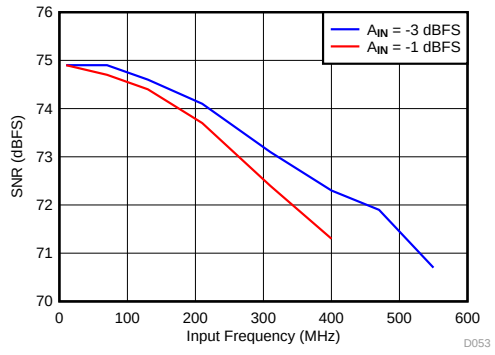


Figure 55. Signal-to-Noise Ratio vs Input Frequency (Output Sample Rate = 350 MSPS)

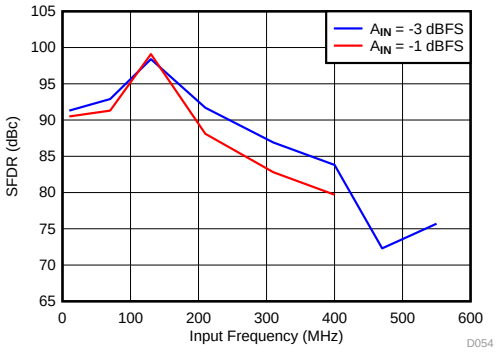


Figure 56. Spurious-Free Dynamic Range vs Input Frequency (Output Sample Rate = 350 MSPS)

Typical Characteristics (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, device clock frequency = 1 GSPS, output sampling rate = 500 MSPS, 50% clock duty cycle, AVDD3V = 3.0 V, AVDD = DVDD = 1.9 V, IOVDD = 1.15 V, and –1-dBFS differential input (unless otherwise noted)

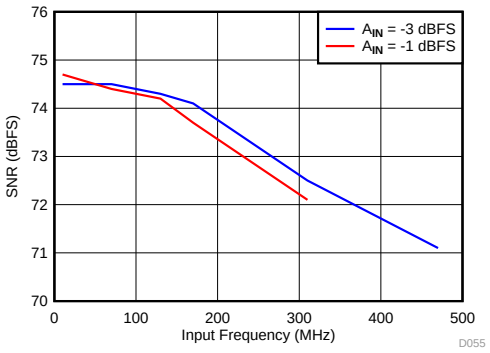


Figure 57. Signal-to-Noise Ratio vs Input Frequency (Output Sample Rate = 400 MSPS)

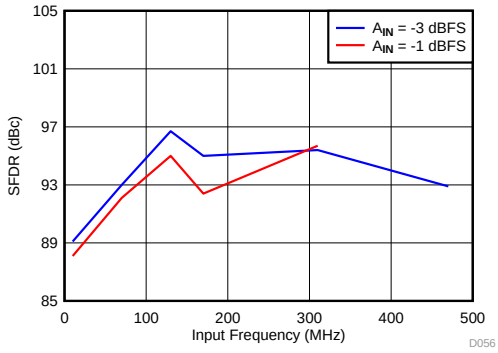


Figure 58. Spurious-Free Dynamic Range vs Input Frequency (Output Sample Rate = 400 MSPS)

8 Detailed Description

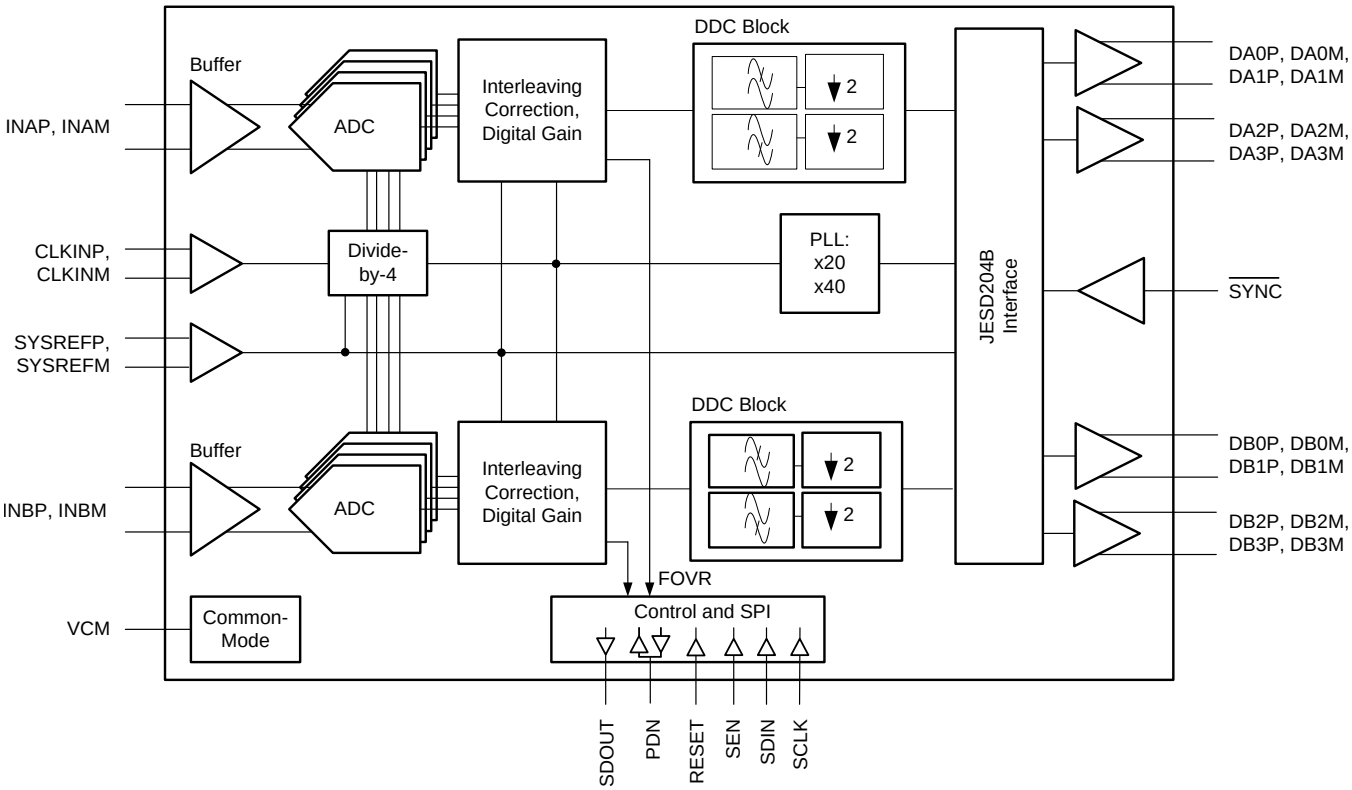
8.1 Overview

The ADS54J69 is a low-power, wide-bandwidth, 16-bit, 500-MSPS, dual-channel, analog-to-digital converter (ADC). The ADS54J69 employs four interleaving ADCs for each channel to achieve a noise floor of –159 dBFS/Hz.

The ADS54J69 uses TI's proprietary interleaving and dither algorithms to achieve a clean spectrum with high spurious-free dynamic range (SFDR). Built-in, half-band, decimate-by-2 filters further enhance the capability of the ADS54J69 to deliver excellent signal-to-noise ratio (SNR) and SFDR over a wide range of frequencies. Analog input buffers isolate the ADC driver from glitch energy generated from sampling process, thereby simplify the driving network on-board.

The JESD204B interface reduces the number of interface lines with two-lane and four-lane options, allowing a high system integration density. The JESD204B interface operates in subclass-1, enabling multi-chip synchronization with the SYSREF input.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Analog Inputs

The ADS54J69 analog signal inputs are designed to be driven differentially. The analog input pins have internal analog buffers that drive the sampling circuit. As a result of the analog buffer, the input pins present a high impedance input across a very wide frequency range to the external driving source that enables great flexibility in the external analog filter design as well as excellent 50-Ω matching for RF applications. The buffer also helps isolate the external driving circuit from the internal switching currents of the sampling circuit, resulting in a more constant SFDR performance across input frequencies.

The common-mode voltage of the signal inputs is internally biased to VCM using 600-Ω resistors, allowing for ac-coupling of the input drive network. Each input pin (INP, INM) must swing symmetrically between (VCM + 0.475 V) and (VCM – 0.475 V), resulting in a 1.9-V_{PP} (default) differential input swing. The input sampling circuit has a 3-dB bandwidth that extends up to 1.2 GHz. An equivalent analog input network diagram is shown in Figure 59.

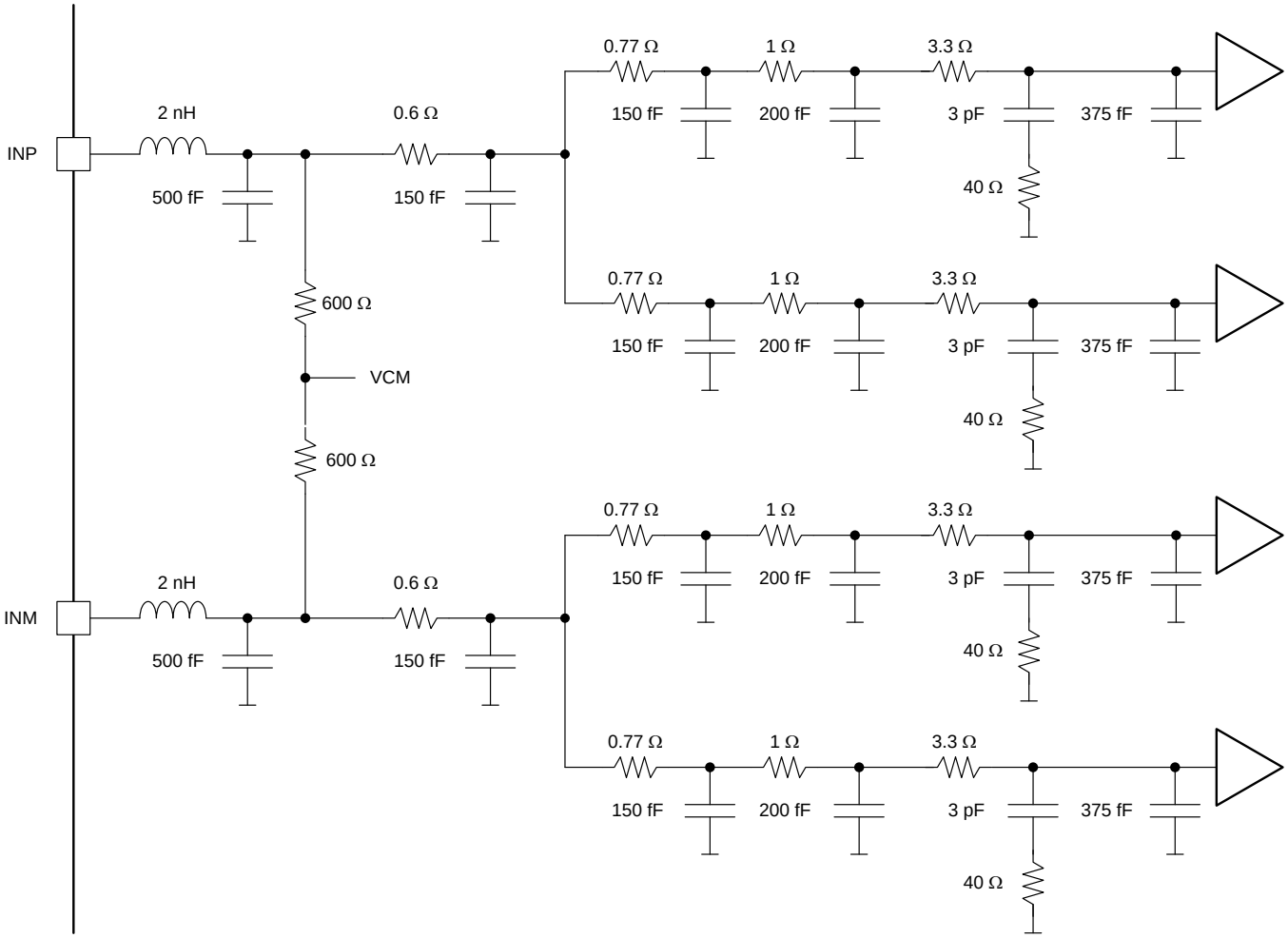


Figure 59. Analog Input Network

Feature Description (continued)

The input bandwidth shown in Figure 60 is measured with respect to a 50-Ω differential input termination at the ADC input pins.

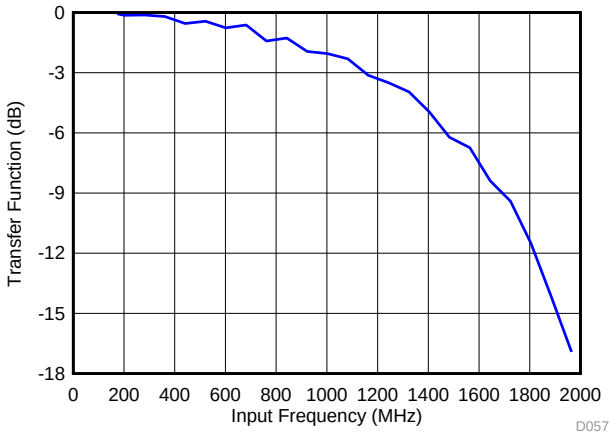


Figure 60. Transfer Function versus Frequency

8.3.2 DDC Block

The ADS54J69 has an optional DDC block that can be enabled via an SPI register write. Each ADC channel is followed by a DDC block consisting of a decimate-by-2, half-band, finite impulse response (FIR) filter with low-pass and high-pass options programmable via the SPI interface.

8.3.2.1 Decimate-by-2 Filter

This decimation filter has 41 taps. The stop-band attenuation is approximately 90 dB and the pass-band flatness is ±0.05 dB. Table 1 shows corner frequencies for the low-pass and high-pass filter options.

Table 1. Corner Frequencies for the Decimate-by-2 Filter

CORNERS (dB)	LOW PASS	HIGH PASS
–0.1	0.202 × f_S	0.298 × f_S
–0.5	0.210 × f_S	0.290 × f_S
–1	0.215 × f_S	0.285 × f_S
–3	0.227 × f_S	0.273 × f_S

Figure 61 and Figure 62 show the frequency response of the decimate-by-2 filter from dc to f_S / 2.

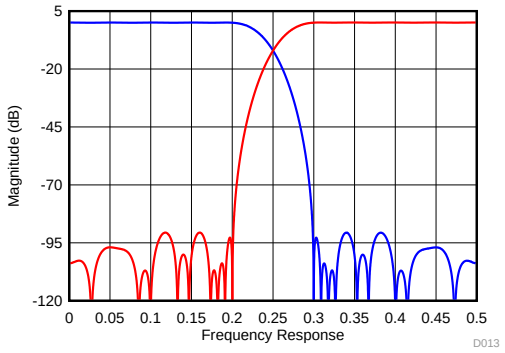


Figure 61. Decimate-by-2 Filter Response

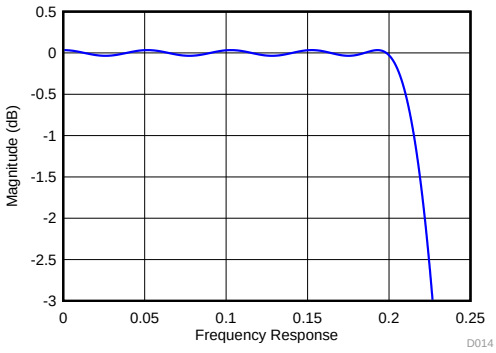


Figure 62. Decimate-by-2 Filter Response (Zoomed)

8.3.3 SYSREF Signal

The SYSREF signal is a periodic signal that is sampled by the ADS54J69 device clock and used to align the boundary of the local multi-frame clock inside the data converter. SYSREF is required to be a sub-harmonic of the local multi-frame clock (LMFC) internal timing. To meet this requirement, the timing of SYSREF is dependent on the device clock frequency and the LMFC frequency, as determined by the selected DDC decimation and frames per multi-frame settings. The SYSREF signal is recommended be a low-frequency signal in the range of 1 MHz to 5 MHz in order to reduce coupling to the signal path both on the printed circuit board (PCB) as well as internal in the device.

The external SYSREF signal must be a sub-harmonic of the internal LMFC clock, as shown in Equation 1 and Table 2.

$$SYSREF = LMFC / 2^N \quad (1)$$

where

- N = 0, 1, 2, and so forth

Table 2. LMFC Clock Frequency

LMFS CONFIGURATION	DECIMATION	LMFC CLOCK(1)(2)
4222	2X	(f_S / 4) / k
2242	2X	(f_S / 4) / k

(1) K = Number of frames per multi-frame (JESD digital page 6900h, address 06h, bits 4-0).
(2) f_S = sampling (device) clock frequency.

8.3.3.1 SYSREF Not Present (Subclass 0, 2)

A SYSREF pulse is required by the ADS54J69 to reset internal counters. If SYSREF is not present, as can be the case in subclass 0 or 2, this pulse can be done by doing the following register writes shown in Table 3.

Table 3. Internally Pulsing SYSREF Twice Using Register Writes

ADDRESS (Hex)	DATA (Hex)	COMMENT
0-011h	80h	Set the master page
0-054h	80h	Enable manual SYSREF
0-053h	01h	Set SYSREF high
0-053h	00h	Set SYSREF low
0-053h	01h	Set SYSREF high
0-053h	00h	Set SYSREF low

8.3.4 Overrange Indication

The ADS54J69 provides a fast overrange indication that can be presented in the digital output data stream via an SPI configuration. Alternatively, if not used, the SDOUT (pin 11) and PDN (pin 50) pins can be configured via the SPI to output the fast overrange (FOVR) indicator.

When the FOVR indication is embedded in the output data stream, the FOVR replaces the LSB of the 16-bit data stream going to the 8b/10b encoder, as shown in Figure 63.

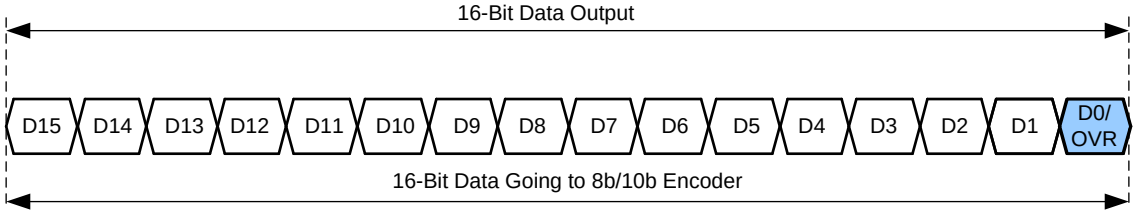


Figure 63. Overrange Indication in a Data Stream

8.3.4.1 Fast OVR

The fast OVR is triggered if the input voltage exceeds the programmable overrange threshold and is presented after only 18 clock cycles + t_{PD} (t_{PD} of the gates and buffers is approximately 4 ns), thus enabling a quicker reaction to an overrange event.

The input voltage level at which the overload is detected is referred to as the *threshold*. The threshold is programmable using the FOVR THRESHOLD bits, as shown in Figure 64. The FOVR is triggered 18 clock cycles + t_{PD} (t_{PD} of the gates and buffers is approximately 4 ns) after the overload condition occurs.

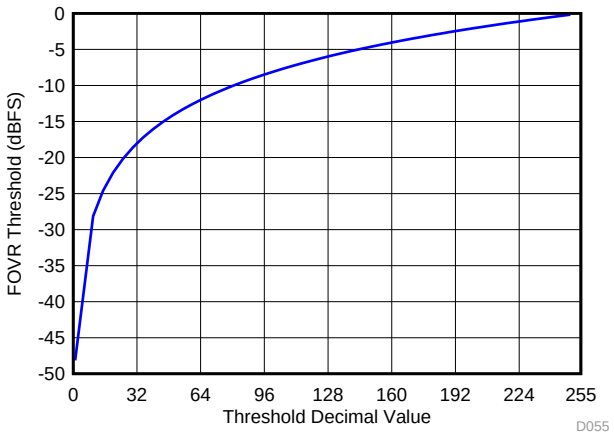


Figure 64. Programming Fast OVR Thresholds

The input voltage level at which the fast OVR is triggered is defined by Equation 2:

Full-Scale × [Decimal Value of the FOVR Threshold Bits] / 255) (2)

The default threshold is E3h (227d), corresponding to a threshold of –1 dBFS.

In terms of full-scale input, the fast OVR threshold can be calculated as Equation 3:

20log (FOVR Threshold / 255) (3)

8.3.5 Power-Down Mode

The ADS54J69 provides a highly-configurable power-down mode. Power-down can be enabled by using the PDN pin or via SPI register writes.

A power-down mask can be configured that allows a trade-off between wake-up time and power consumption in power-down mode. Two independent power-down masks can be configured: MASK 1 and MASK 2, as shown in Table 4. See the master page registers in Table 10 for further details.

Table 4. Register Address for Power-Down Modes

REGISTER ADDRESS A[7:0] (Hex)	COMMENT	REGISTER DATA							
		7	6	5	4	3	2	1	0
MASTER PAGE (80h)									
20	MASK 1	PDN ADC CHA				PDN ADC CHB			
21		PDN BUFFER CHB		PDN BUFFER CHA		0	0	0	0
23	MASK 2	PDN ADC CHA				PDN ADC CHB			
24		PDN BUFFER CHB		PDN BUFFER CHA		0	0	0	0
26	CONFIG	GLOBAL PDN	OVERRIDE PDN PIN	PDN MASK SEL	0	0	0	0	0
53		0	MASK SYSREF	0	0	0	0	0	0
55		0	0	0	PDN MASK	0	0	0	0

To save power, the device can be put in complete power-down by using the GLOBAL PDN register bit. However, when the JESD link is required to be active during power-down, the ADC and analog buffer can be selectively powered down by using the PDN ADC CHx and PDN BUFFER CHx register bits after enabling the PDN MASK register bit. The PDN MASK SEL register bit can be used to select between MASK 1 or MASK 2. Table 5 shows power consumption for different combinations of the GLOBAL PDN, PDN ADC CHx, and PDN BUFF CHx register bits.

Table 5. Power Consumption in Different Power-Down Settings

REGISTER BIT	COMMENT	I_{AVDD3V} (mA)	I_{AVDD} (mA)	I_{DVDD} (mA)	I_{IOVDD} (mA)	TOTAL POWER (W)
Default	After reset, with a full-scale input signal to both channels	346	354	188	512	2.66
GBL PDN = 1	The device is in a complete power-down state	3	6	21	127	0.2
GBL PDN = 0, PDN ADC CHx = 1 (x = A or B)	The ADC of one channel is powered down	284	221	130	461	2.05
GBL PDN = 0, PDN BUFF CHx = 1 (x = A or B)	The input buffer of one channel is powered down	270	352	188	516	2.43
GBL PDN = 0, PDN ADC CHx = 1, PDN BUFF CHx = 1 (x = A or B)	The ADC and input buffer of one channel are powered down	206	220	129	465	1.82
GBL PDN = 0, PDN ADC CHx = 1, PDN BUFF CHx = 1 (x = A and B)	The ADC and input buffer of both channels are powered down	64	84	67	389	0.93

8.4 Device Functional Modes

8.4.1 Device Configuration

The ADS54J69 can be configured by using a serial programming interface, as described in the *Serial Interface* section. In addition, the device has one dedicated parallel pin (PDN) for controlling the power-down mode.

The ADS54J69 supports a 24-bit (16-bit address, 8-bit data) SPI operation and uses paging (see the *Register Maps* section) to access all register bits.

8.4.1.1 Serial Interface

The ADC has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), and SDIN (serial interface data) pins, as shown in Figure 65. Legends used in Figure 65 are explained in Table 6. Serially shifting bits into the device is enabled when SEN is low. Serial data on SDIN are latched at every SCLK rising edge when SEN is active (low). The interface can function with SCLK frequencies from 2 MHz down to very low speeds (of a few Hertz) and also with a non-50% SCLK duty cycle.

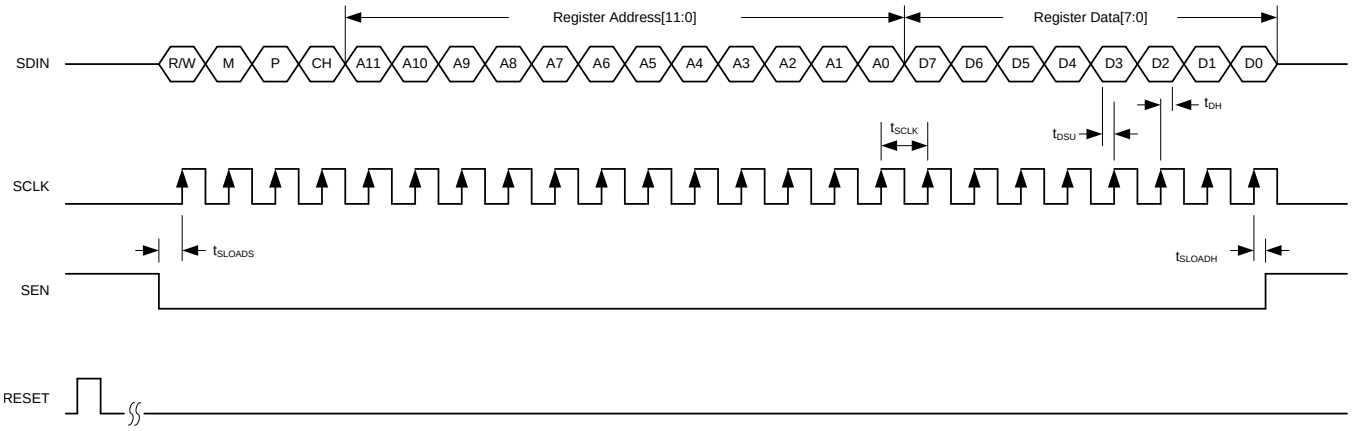


Figure 65. SPI Timing Diagram

Table 6. SPI Timing Diagram Legend

SPI BITS	DESCRIPTION	BIT SETTINGS
R/W	Read/write bit	0 = SPI write 1 = SPI read back
M	SPI bank access	0 = Analog SPI bank (master and ADC pages) 1 = JESD SPI bank (main digital, analog JESD, and digital JESD pages)
P	JESD page selection bit	0 = Page access 1 = Register access
CH	SPI access for a specific channel of the JESD SPI bank	0 = Channel A 1 = Channel B By default, both channels are being addressed.
A[11:0]	SPI address bits	—
D[7:0]	SPI data bits	—

Table 7 shows the timing requirements for the serial interface signals in Figure 65.

Table 7. SPI Timing Requirements

		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to 1 / t_{SCLK})	> dc		2	MHz
t_{SLOADS}	SEN to SCLK setup time	100			ns
t_{SLOADH}	SCLK to SEN hold time	100			ns
t_{DSU}	SDIN setup time	100			ns
t_{DH}	SDIN hold time	100			ns

8.4.1.2 Serial Register Write: Analog Bank

The analog SPI bank contains two pages (the master and ADC page). The internal register of the ADS54J69 analog SPI bank can be programmed by:

1. Driving the SEN pin low.
2. Initiating a serial interface cycle specifying the page address of the register whose content must be written.
   - Master page: write address 0011h with 80h.
   - ADC page: write address 0011h with 0Fh.
3. Writing the register content, as shown in Figure 66. When a page is selected, multiple writes into the same page can be done.

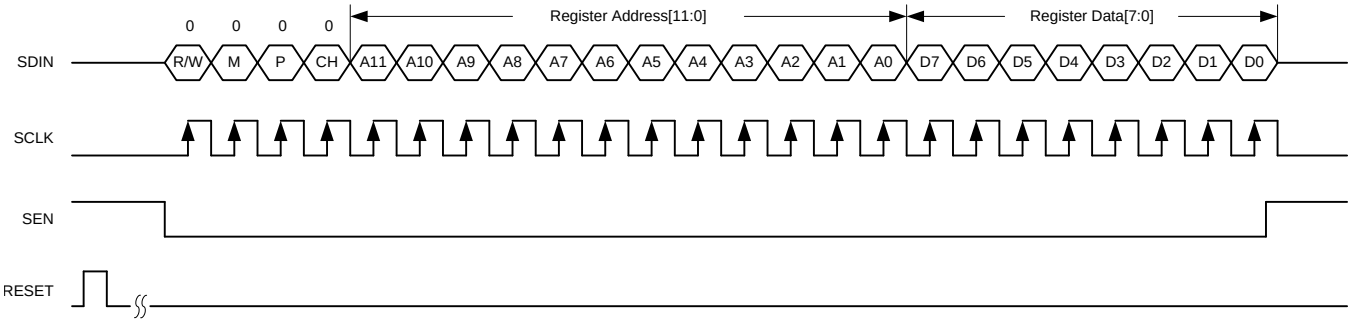


Figure 66. Serial Register Write Timing Diagram

8.4.1.3 Serial Register Readout: Analog Bank

The content from one of the two analog banks can be read out by:

1. Driving the SEN pin low.
2. Selecting the page address of the register whose content must be read.
   - Master page: write address 0011h with 80h.
   - ADC page: write address 0011h with 0Fh.
3. Setting the R/W bit to 1 and writing the address to be read back.
4. Reading back the register content on the SDOUT pin, as shown in Figure 67. When a page is selected, multiple read backs from the same page can be done.

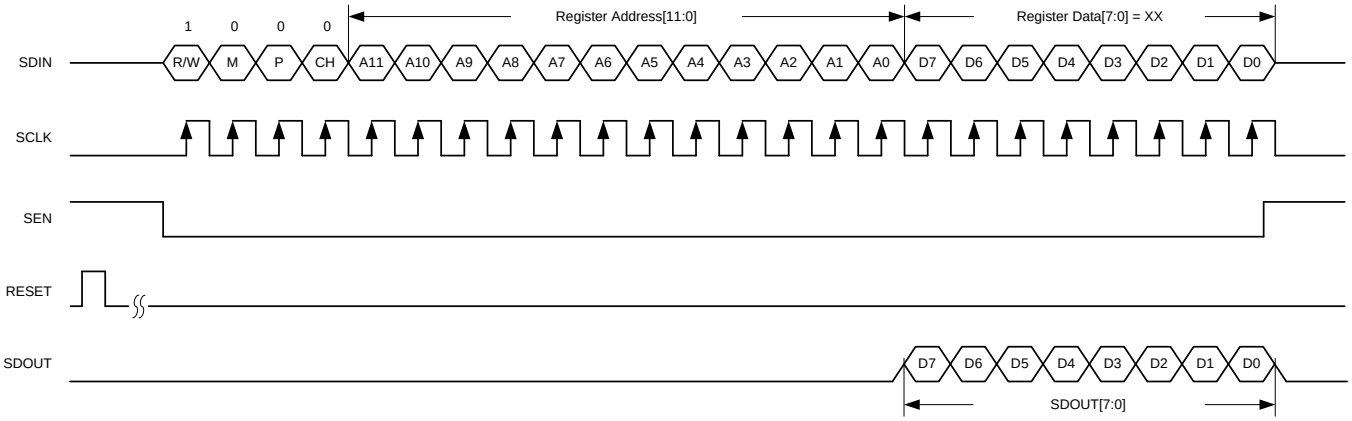


Figure 67. Serial Register Read Timing Diagram

8.4.1.4 JESD Bank SPI Page Selection

The JESD SPI bank contains four pages (main digital, digital, and analog JESD pages). The individual pages can be selected by:

1. Driving the SEN pin low.
2. Setting the M bit to 1 and specifying the page with two register writes. Note that the P bit must be set to 0, as shown in Figure 68.
   - Write address 4003h with 00h (LSB byte of page address).
   - Write address 4004h with the MSB byte of the page address.
     - For the main digital page: write address 4004h with 68h.
     - For the digital JESD page: write address 4004h with 69h.
     - For the analog JESD page: write address 4004h with 6Ah.

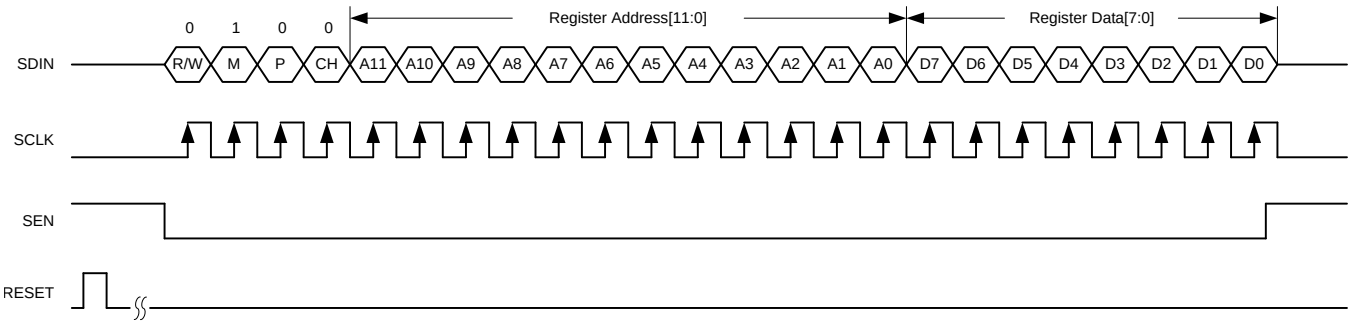


Figure 68. SPI Page Selection

8.4.1.5 Serial Register Write: JESD Bank

The ADS54J69 is a dual-channel device and the JESD204B portion is configured individually for each channel by using the CH bit. Note that the P bit must be set to 1 for register writes.

1. Drive the SEN pin low.
2. Select the JESD bank page. Note that the M bit = 1 and the P bit = 0.
   - Write address 4003h with 00h.
   - If separate control for both channels is desired, write address 4005h with 01h.
   - For the main digital page: write address 4004h with 68h.
   - For the digital JESD page: write address 4004h with 69h.
   - For the analog JESD page: write address 4004h with 6Ah.
3. Set the M and P bits to 1, select channel A (CH = 0) or channel B (CH = 1), and write the register content as shown in Figure 69. When a page is selected, multiple writes into the same page can be done.

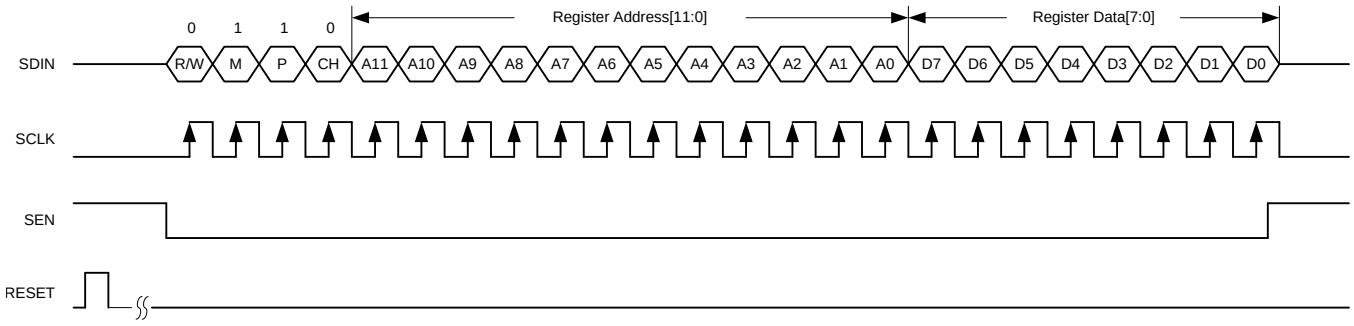


Figure 69. JESD Serial Register Write Timing Diagram

8.4.1.5.1 Individual Channel Programming

By default, register writes are applied to both channels. To enable individual channel writes, write address 4005h with 01h (default is 00h).

8.4.1.6 Serial Register Readout: JESD Bank

The content from one of the pages of the JESD bank can be read out by:

1. Driving the SEN pin low.
2. Select the JESD bank page. Note that the M bit = 1 and the P bit = 0.
   - Write address 4003h with 00h.
   - If separate control for both channels is desired, write address 4005h with 01h.
   - For the main digital page: write address 4004h with 68h.
   - For the digital JESD page: write address 4004h with 69h.
   - For the analog JESD page: write address 4004h with 6Ah.
3. Setting the R/W, M, and P bits to 1, selecting channel A or channel B, and writing the address to be read back.
4. Reading back the register content on the SDOUT pin; see Figure 70. When a page is selected, multiple read backs from the same page can be done.

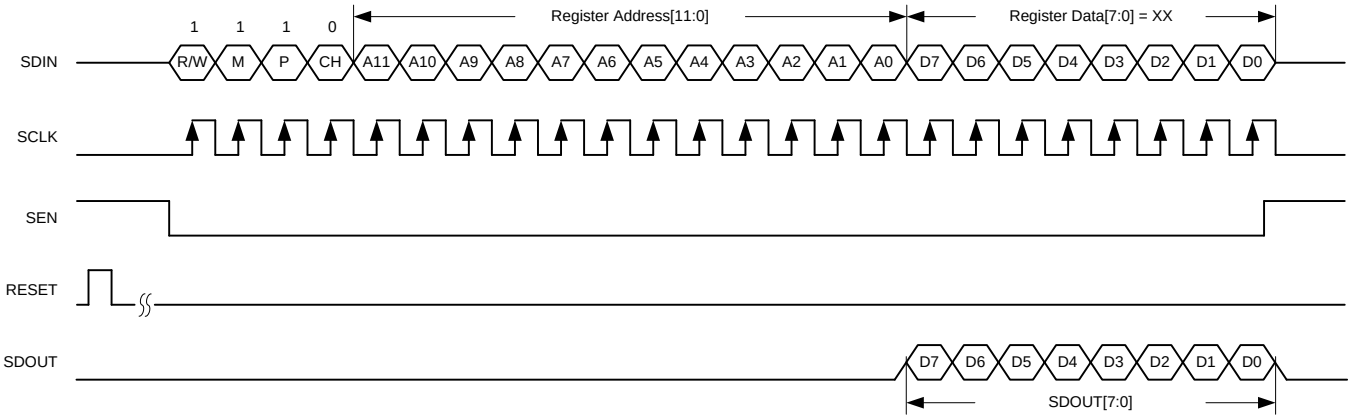


Figure 70. JESD Serial Register Read Timing Diagram

8.4.2 JESD204B Interface

The ADS54J69 supports device subclass 1 with a maximum output data rate of 10.0 Gbps for each serial transmitter.

An external SYSREF signal is used to align all internal clock phases and the local multi-frame clock to a specific sampling clock edge, allowing synchronization of multiple devices in a system and minimizing timing and alignment uncertainty. The $\overline{\text{SYNC}}$ input is used to control the JESD204B SERDES blocks.

Depending on the ADC output data rate, the JESD204B output interface can be operated with either two or four active lanes (out of total 8 lanes), as shown in Figure 71. The JESD204B setup and configuration of the frame assembly parameters is controlled via the SPI interface.

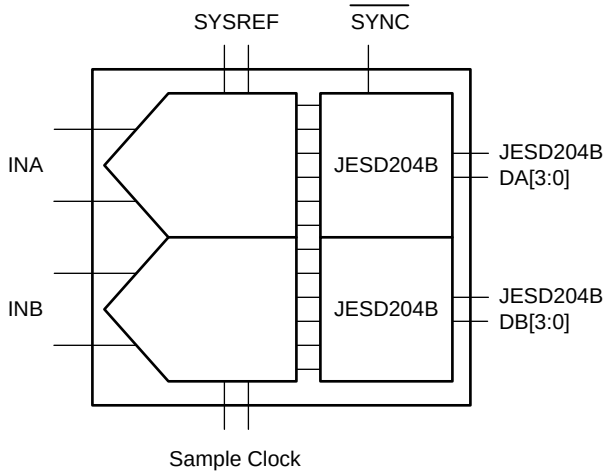


Figure 71. ADS54J69 Block Diagram

The JESD204B transmitter block shown in Figure 72 consists of the transport layer, the data scrambler, and the link layer. The transport layer maps the ADC output data into the selected JESD204B frame data format. The link layer performs the 8b/10b data encoding as well as the synchronization and initial lane alignment using the SYNC input signal. Optionally, data from the transport layer can be scrambled.

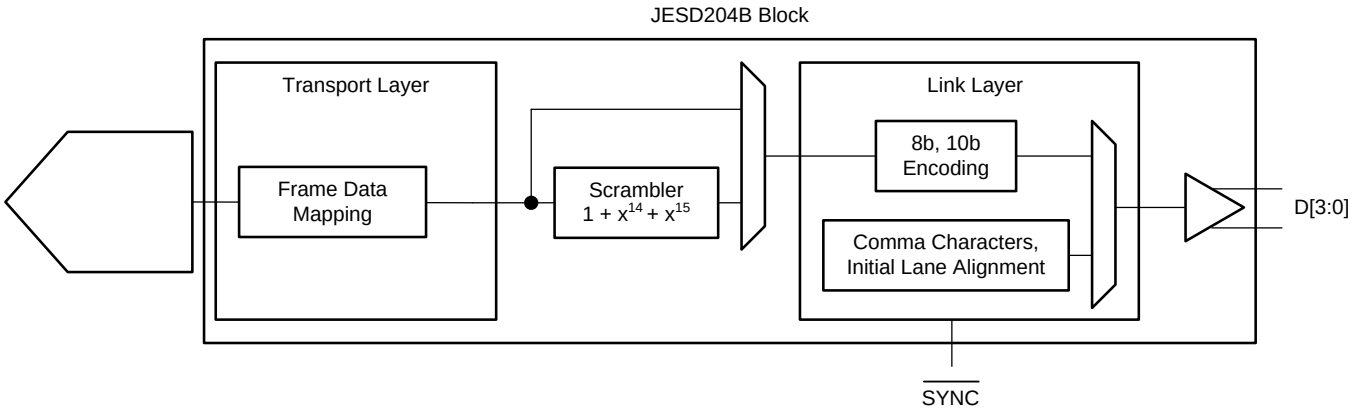


Figure 72. JESD204B Transmitter Block

8.4.2.1 JESD204B Initial Lane Alignment (ILA)

The initial lane alignment process is started when the receiving device de-asserts the SYNC signal, as shown in Figure 73. When a logic low is detected on the SYNC input pin, the ADS54J69 starts transmitting comma (K28.5) characters to establish a code group synchronization.

When synchronization is complete, the receiving device asserts the SYNC signal and the ADS54J69 starts the initial lane alignment sequence with the next local multi-frame clock boundary. The ADS54J69 transmits four multi-frames, each containing K frames (K is SPI programmable). Each of the multi-frames contains the frame start and end symbols and the second multi-frame also contains the JESD204 link configuration data.

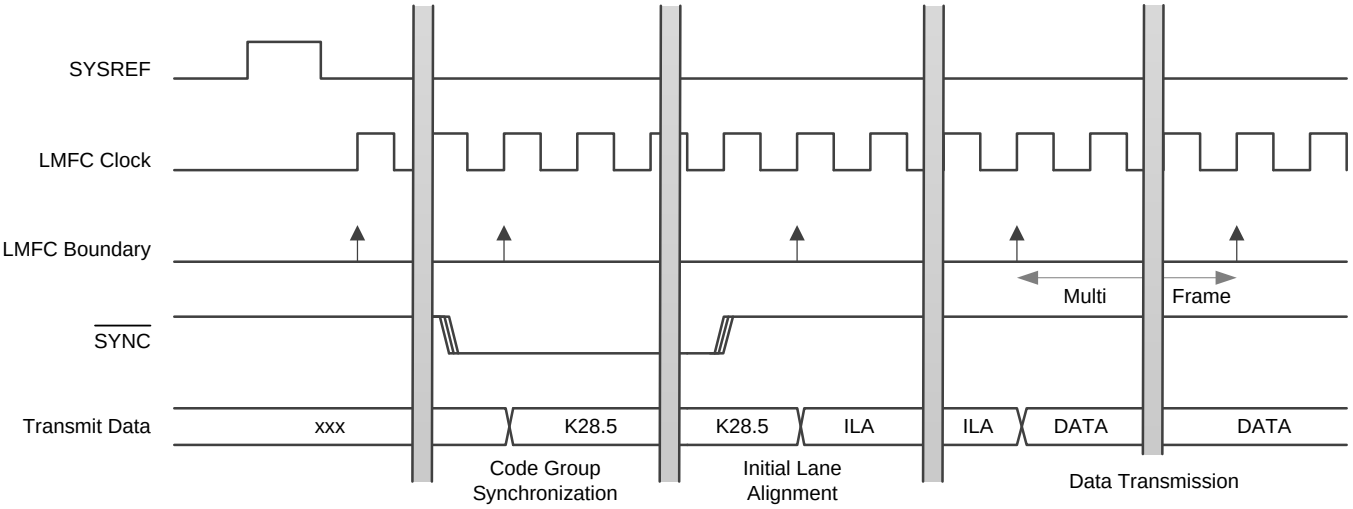


Figure 73. Lane Alignment Sequence

8.4.2.2 JESD204B Test Patterns

There are three different test patterns available in the transport layer of the JESD204B interface. The ADS54J69 supports a clock output, encoded, and a PRBS ($2^{15} – 1$) pattern. These test patterns can be enabled via an SPI register write and are located in the JESD digital page of the JESD bank.

8.4.2.3 JESD204B Frame

The JESD204B standard defines the following parameters:

- L is the number of lanes per link
- M is the number of converters per device
- F is the number of octets per frame clock period, per lane
- S is the number of samples per frame per converter

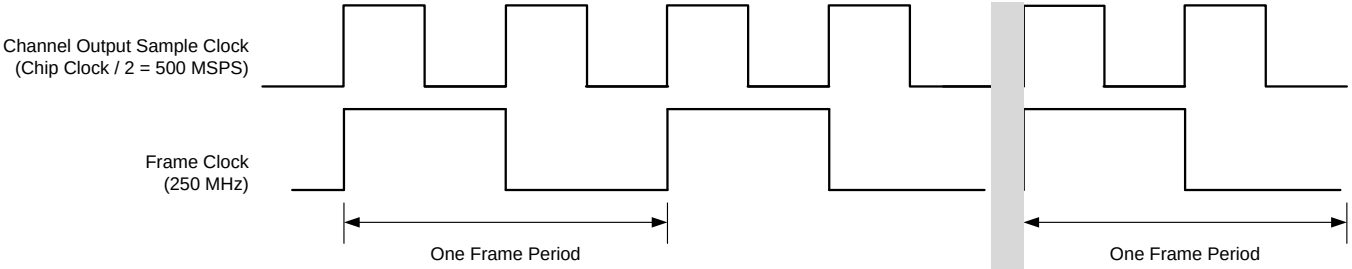
8.4.2.4 JESD204B Frame Assembly with Decimation

Table 8 lists the available JESD204B formats and interface rate at maximum sampling frequency. At lower sampling frequencies, interface rates scale down proportionally.

Figure 74 shows the detailed frame assembly for the decimated output.

Table 8. Interface Rates with Decimation Filter

L	M	F	S	JESD MODE REGISTER BIT	JESD PLL MODE SETTING	DECIMATION	MAX ADC OUTPUT RATE (MSPS)	MAX f_{SERDES} (Gbps)
4	2	2	2	001	20x	2X	500	5.0
2	2	4	2	010	40x	2X	500	10.0



PIN	LMFS = 4222, 2X DECIMATION				LMFS = 2242, 2X DECIMATION			
DA0	A1[15:8]	A1[7:0]	A3[15:8]	A3[7:0]	Lane DA0 is Unused			
DA1	A0[15:8]	A0[7:0]	A2[15:8]	A2[7:0]	A0[15:8]	A0[7:0]	A1[15:8]	A1[7:0]
DA2	Lane DA2 is Unused				Lane DA2 is Unused			
DA3	Lane DA3 is Unused				Lane DA3 is Unused			
DB0	B1[15:8]	B1[7:0]	B3[15:8]	B3[7:0]	Lane DB0 is Unused			
DB1	B0[15:8]	B0[7:0]	B2[15:8]	B2[7:0]	B0[15:8]	B0[7:0]	B1[15:8]	B1[7:0]
DB2	Lane DB2 is Unused				Lane DB2 is Unused			
DB3	Lane DB3 is Unused				Lane DB3 is Unused			

Figure 74. Frame Assembly with Decimation Filter

Note that after power-up, the JESD output bus must be reordered to obtain correct link parameters in the ILA sequence. Table 9 shows the required register writes to reorder the JESD output bus.

Table 9. Configuring LMFS for the JESD Link

L	M	F	S	DECIMATION	JESD PLL MODE (In JESD Analog Page)	JESD MODE REGISTER BIT (In JESD Digital Page)	DA_BUS_REORDER REGISTER BIT (In JESD Digital Page)	DB_BUS_REORDER REGISTER BIT (In JESD Digital Page)	REGISTER 52 (In Main Digital Page)	REGISTER 72 (In Main Digital Page)
4	2	2	2	2X	00h	01h	0Ah	0Ah	80h	08h
2	2	4	2	2X	10h	02h	0Ah	0Ah	80h	08h

8.4.2.4.1 JESD Transmitter Interface

Each of the 10.0-Gbps SERDES JESD transmitter outputs requires ac-coupling between the transmitter and receiver. The differential pair must be terminated with 100-Ω resistors as close to the receiving device as possible to avoid unwanted reflections and signal degradation, as shown in Figure 75.

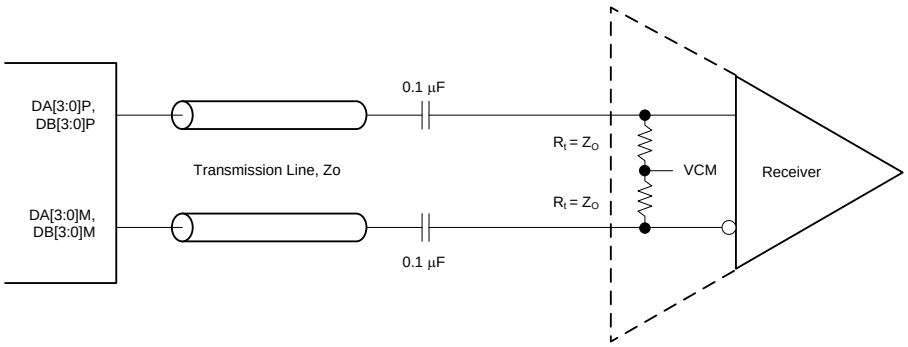


Figure 75. Output Connection to Receiver

8.4.2.4.2 Eye Diagrams

Figure 76 to Figure 79 show the serial output eye diagrams of the ADS54J69 at 5.0 Gbps and 10 Gbps with default and increased output voltage swing against the JESD204B mask.

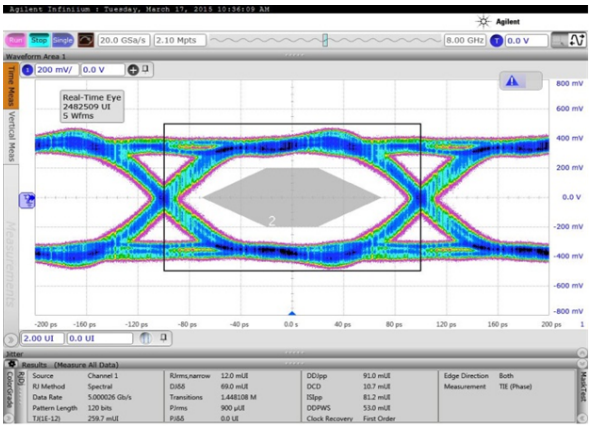


Figure 76. Eye Diagram at 5-Gbps Bit Rate with Default Output Swing

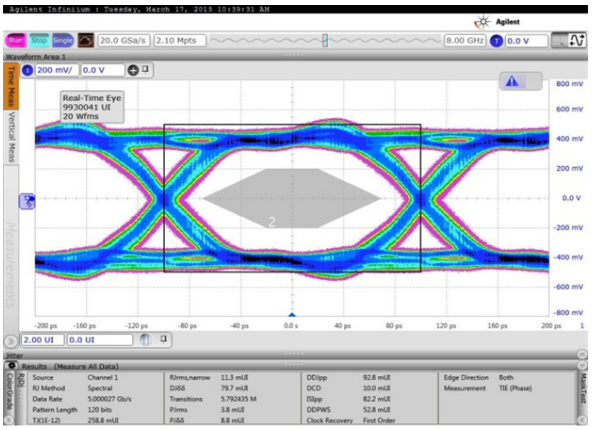


Figure 77. Eye Diagram at 5-Gbps Bit Rate with Increased Output Swing

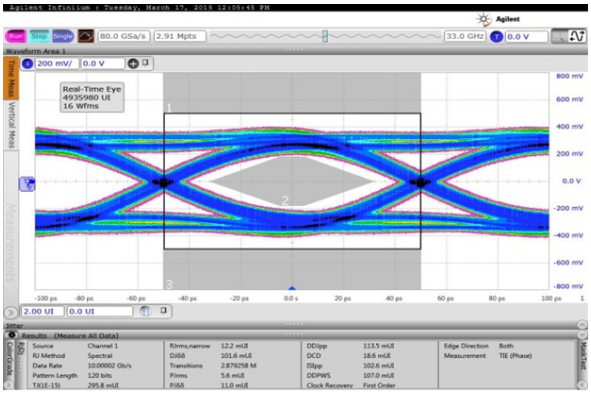


Figure 78. Eye Diagram at 10-Gbps Bit Rate with Default Output Swing

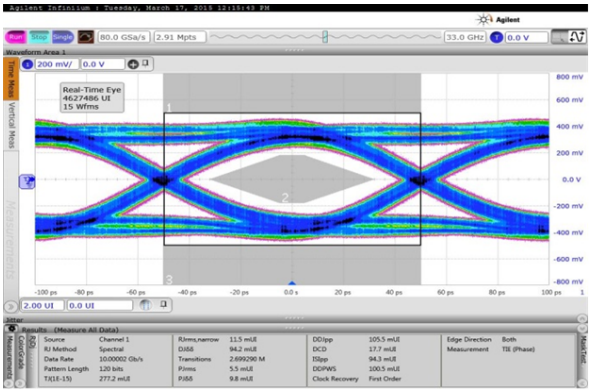


Figure 79. Eye Diagram at 10-Gbps Bit Rate with Increased Output Swing

8.5 Register Maps

Figure 80 shows a conceptual diagram of the serial registers.

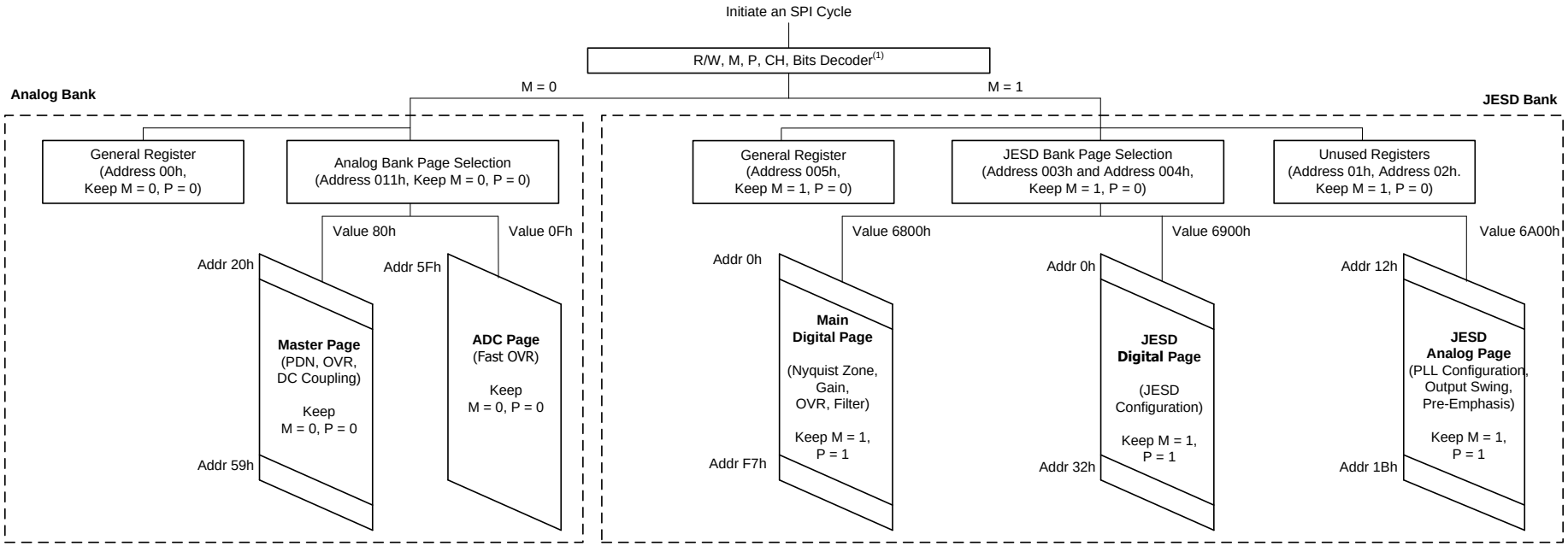


Figure 80. Serial Interface Registers

8.5.1 Detailed Register Info

The ADS54J69 contains two main SPI banks: the analog SPI bank and the digital SPI bank. The analog SPI bank gives access to the ADC analog blocks and the JESD SPI bank controls the digital features and anything related to the JESD204B serial interface. The analog SPI bank is divided into two pages (master and ADC) and the JESD SPI bank is divided into three pages (main digital, JESD digital, and JESD analog). Table 10 lists a register map for the ADS54J69.

Register Maps (continued)

Table 10. Register Map

REGISTER ADDRESS	REGISTER DATA							
A[11:0] (Hex)	7	6	5	4	3	2	1	0
GENERAL REGISTERS								
0	RESET	0	0	0	0	0	0	RESET
3	JESD BANK PAGE SEL[7:0]							
4	JESD BANK PAGE SEL[15:8]							
5	0	0	0	0	0	0	0	DISABLE BROADCAST
11	ANALOG BANK PAGE SEL							
MASTER PAGE (80h)								
20	PDN ADC CHA				PDN ADC CHB			
21	PDN BUFFER CHB		PDN BUFFER CHA		0	0	0	0
23	PDN ADC CHA				PDN ADC CHB			
24	PDN BUFFER CHB		PDN BUFFER CHA		0	0	0	0
26	GLOBAL PDN	OVERRIDE PDN PIN	PDN MASK SEL	0	0	0	0	0
4F	0	0	0	0	0	0	0	EN INPUT DC COUPLING
53	0	MASK SYSREF	0	0	0	0	EN SYSREF DC COUPLING	SET SYSREF
54	ENABLE MANUAL SYSREF	0	0	0	0	0	0	0
55	0	0	0	PDN MASK	0	0	0	0
59	FOVR CHB	0	ALWAYS WRITE 1	0	0	0	0	0
ADC PAGE (0Fh)								
5F	FOVR THRESHOLD PROG							
MAIN DIGITAL PAGE (6800h)								
0	0	0	0	0	0	0	0	PULSE RESET
41	0	0	0	DECFIL MODE[3]	0	DECFIL MODE[2:0]		
42	0	0	0	0	0	NYQUIST ZONE		
43	0	0	0	0	0	0	0	FORMAT SEL
44	0	DIGITAL GAIN						
4B	0	0	FORMAT EN	0	0	0	0	0
MAIN DIGITAL PAGE (6800h) (continued)								

Register Maps (continued)

Table 10. Register Map (continued)

REGISTER ADDRESS A[11:0] (Hex)	REGISTER DATA							
	7	6	5	4	3	2	1	0
4D	0	0	0	0	DEC MODE EN	0	0	0
4E	CTRL NYQUIST	0	0	0	0	0	0	0
52	ALWAYS WRITE 1	0	0	0	0	0	0	DIG GAIN EN
72	0	0	0	0	ALWAYS WRITE 1	0	0	0
AB	0	0	0	0	0	0	0	LSB SEL EN
AD	0	0	0	0	0	0	LSB SELECT	
F7	0	0	0	0	0	0	0	DIG RESET
JESD DIGITAL PAGE (6900h)								
0	CTRL K	0	0	TESTMODE EN	FLIP ADC DATA	LANE ALIGN	FRAME ALIGN	TX LINK DIS
1	SYNC REG	SYNC REG EN	0	0	0	JESD MODE		
2	LINK LAYER TESTMODE			LINK LAYER RPAT	LMFC MASK RESET	0	0	0
3	FORCE LMFC COUNT	LMFC COUNT INIT					RELEASE ILANE SEQ	
5	SCRAMBLE EN	0	0	0	0	0	0	0
6	0	0	0	FRAMES PER MULTI FRAME (K)				
7	0	0	0	0	SUBCLASS	0	0	0
31	DA_BUS_REORDER[7:0]							
32	DB_BUS_REORDER[7:0]							
JESD ANALOG PAGE (6A00h)								
12	SEL EMP LANE 1						0	0
13	SEL EMP LANE 0						0	0
14	SEL EMP LANE 2						0	0
15	SEL EMP LANE 3						0	0
16	0	0	0	0	0	0	JESD PLL MODE	
1A	0	0	0	0	0	0	FOVR CHA	0
1B	JESD SWING			0	FOVR CHA EN	0	0	0

8.5.2 Example Register Writes

This section provides three different example register writes. Table 11 describes a global power-down register write, Table 12 describes the register writes to enable the high-pass filter in the default four-lane output mode (LMFS = 4222), and Table 13 describes the register writes to enable the high-pass filter in the two-lane output mode (LMFS = 2242).

Note that by default after reset, the low-pass filter and four-lane output mode are enabled and register writes are applied to both channels together.

Table 11. Global Power-Down

ADDRESS (Hex)	DATA (Hex)	COMMENT
11h	80h	Set the master page
26h	C0h	Set the global power-down

Table 12. Selecting 2X Decimation with Four-Lane Mode (LMFS = 4222)

ADDRESS (Hex)	DATA (Hex)	COMMENT
4-004h	68h	Select the main digital page (6800h)
4-003h	00h	
6-041h	16h	Set decimate-by-2 (high-pass filter)
6-04Dh	08h	Enable decimation filter control
6-072h	08h	Enable the ALWAYS WRITE 1 register bit (for output bus reorder)
6-052h	80h	Enable the ALWAYS WRITE 1 register bit (for output bus reorder)
6-000h	01h	Pulse the PULSE RESET register bit so that registers programmed in the main digital page (6800h) become effective.
6-000h	00h	
4-004h	69h	Select the JESD digital page (6900h)
4-003h	00h	
6-031h	0Ah	Output bus reorder for channel A
6-032h	0Ah	Output bus reorder for channel B
6-001h	01h	JESD filter mode + 4-lanes output selection

Table 13. Selecting 2X Decimation with Two-Lane Mode (LMFS = 2242)

ADDRESS (Hex)	DATA (Hex)	COMMENT
4-004h	68h	Select the main digital page (6800h)
4-003h	00h	
6-041h	16h	Set decimate-by-2 (high-pass filter)
6-04Dh	08h	Enable decimation filter control
6-072h	08h	Set the ALWAYS WRITE 1 register bit (for output bus reorder)
6-052h	80h	Set the ALWAYS WRITE 1 register bit (for output bus reorder)
6-000h	01h	Pulse the PULSE RESET register bit so that registers programmed in the main digital page (6800h) become effective.
6-000h	00h	
4-004h	69h	Select the JESD digital page (6900h)
4-003h	00h	
6-031h	0Ah	Output bus reorder for channel A
6-032h	0Ah	Output bus reorder for channel B
6-001h	02h	JESD filter mode + 2-lanes output selection
4-004h	6Ah	Select the JESD analog page (6A00h)
4-003h	00h	
6-016h	02h	JESD PLL MODE 40x selection in the analog page

8.5.3 Register Descriptions

8.5.3.1 General Registers

8.5.3.1.1 Register 0h (address = 0h)

Figure 81. Register 0h

7	6	5	4	3	2	1	0
RESET	0	0	0	0	0	0	RESET
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: W = Write only; -n = value after reset

Table 14. Register 0h Field Descriptions

Bit	Field	Type	Reset	Description
7	RESET	W	0h	0 = Normal operation 1 = Internal software reset, clears back to 0
6-1	0	W	0h	Must write 0
0	RESET	W	0h	0 = Normal operation 1 = Internal software reset, clears back to 0

8.5.3.1.2 Register 3h (address = 3h)

Figure 82. Register 3h

7	6	5	4	3	2	1	0
JESD BANK PAGE SEL[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15. Register 3h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	JESD BANK PAGE SEL[7:0]	R/W	0h	Program these bits to access the desired page in the JESD bank. 6800h = Main digital page selected 6900h = JESD digital page selected 6A00h = JESD analog page selected

8.5.3.1.3 Register 4h (address = 4h)

Figure 83. Register 4h

7	6	5	4	3	2	1	0
JESD BANK PAGE SEL[15:8]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 16. Register 4h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	JESD BANK PAGE SEL[15:8]	R/W	0h	Program these bits to access the desired page in the JESD bank. 6800h = Main digital page selected 6900h = JESD digital page selected 6A00h = JESD analog page selected

8.5.3.1.4 Register 5h (address = 5h)

Figure 84. Register 5h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DISABLE BROADCAST
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 17. Register 5h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	DISABLE BROADCAST	R/W	0h	0 = Normal operation; channel A and B are programmed as a pair 1 = Channel A and B can be individually programmed based on the CH bit (keep CH = 0 for channel A, CH = 1 for channel B).

8.5.3.1.5 Register 11h (address = 11h)

Figure 85. Register 11h

7	6	5	4	3	2	1	0
ANALOG PAGE SELECTION							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 18. Register 11h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ANALOG BANK PAGE SEL	R/W	0h	Program these bits to access the desired page in the analog bank. Master page = 80h ADC page = 0Fh

8.5.3.2 Master Page (080h) Registers

8.5.3.2.1 Register 20h (address = 20h), Master Page (080h)

Figure 86. Register 20h

7	6	5	4	3	2	1	0
PDN ADC CHA				PDN ADC CHB			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 19. Registers 20h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	PDN ADC CHA	R/W	0h	There are two power-down masks that are controlled via the PDN mask register bit in address 55h. Power-down mask 1 or mask 2 are selected via register bit 5 in address 26h. Power-down mask 1: addresses 20h and 21h. Power-down mask 2: addresses 23h and 24h. 0Fh = Power-down CHB only. F0h = Power-down CHA only. FFh = Power-down both.
3-0	PDN ADC CHB	R/W	0h	

8.5.3.2.2 Register 21h (address = 21h), Master Page (080h)

Figure 87. Register 21h

7	6	5	4	3	2	1	0
PDN BUFFER CHB		PDN BUFFER CHA		0	0	0	0
R/W-0h		R/W-0h		W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 20. Register 21h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PDN BUFFER CHB	R/W	0h	There are two power-down masks that are controlled via the PDN mask register bit in address 55h. Power-down mask 1 or mask 2 are selected via register address 26h, bit 5. Power-down mask 1: addresses 20h and 21h. Power-down mask 2: addresses 23h and 24h. There are two buffers per channel. One buffer drives two ADC cores. PDN BUFFER CHx: 00 = Both buffers of a channel are active. 11 = Both buffers are powered down. 01–10 = Do not use.
5-4	PDN BUFFER CHA	R/W	0h	
3-0	0	W	0h	Must write 0

8.5.3.2.3 Register 23h (address = 23h), Master Page (080h)

Figure 88. Register 23h

7	6	5	4	3	2	1	0
PDN ADC CHA				PDN ADC CHB			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 21. Register 23h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	PDN ADC CHA	R/W	0h	There are two power-down masks that are controlled via the PDN mask register bit in address 55h. Power-down mask 1 or mask 2 are selected via register address 26h, bit 5. Power-down mask 1: addresses 20h and 21h. Power-down mask 2: addresses 23h and 24h. 0Fh = Power-down CHB only. F0h = Power-down CHA only. FFh = Power-down both.
3-0	PDN ADC CHB	R/W	0h	

8.5.3.2.4 Register 24h (address = 24h), Master Page (080h)

Figure 89. Register 24h

7	6	5	4	3	2	1	0
PDN BUFFER CHB		PDN BUFFER CHA		0	0	0	0
R/W-0h		R/W-0h		W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 22. Register 24h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PDN BUFFER CHB	R/W	0h	There are two power-down masks that are controlled via the PDN mask register bit in address 55h. Power-down mask 1 or mask 2 are selected via register address 26h, bit 5. Power-down mask 1: addresses 20h and 21h. Power-down mask 2: addresses 23h and 24h. Power-down mask 2: addresses 23h and 24h. There are two buffers per channel. One buffer drives two ADC cores. PDN BUFFER CHx: 00 = Both buffers of a channel are active. 11 = Both buffers are powered down. 01–10 = Do not use.
5-4	PDN BUFFER CHA	R/W	0h	
3-0	0	W	0h	Must write 0

8.5.3.2.5 Register 26h (address = 26h), Master Page (080h)

Figure 90. Register 26h

7	6	5	4	3	2	1	0
GLOBAL PDN	OVERRIDE PDN PIN	PDN MASK SEL	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 23. Register 26h Field Descriptions

Bit	Field	Type	Reset	Description
7	GLOBAL PDN	R/W	0h	Bit 6 (OVERRIDE PDN PIN) must be set before this bit can be programmed. 0 = Normal operation 1 = Global power-down via the SPI
6	OVERRIDE PDN PIN	R/W	0h	This bit ignores the power-down pin control. 0 = Normal operation 1 = Ignores inputs on the power-down pin
5	PDN MASK SEL	R/W	0h	This bit selects power-down mask 1 or mask 2. 0 = Power-down mask 1 1 = Power-down mask 2
4-0	0	W	0h	Must write 0

8.5.3.2.6 Register 39h (address = 39h), Master Page (080h)

Figure 91. Register 39h

7	6	5	4	3	2	1	0
PERF MODE[1:0]		0	0	0	0	0	0
R/W-0h		W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 24. Register 39h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PERF MODE[1:0]	R/W	0h	Set all four PERF MODE[3:0] bits together. Bits are located in register address 39h, 3Ah, and 56h in the master page.
5-0	0	W	0h	Must write 0

8.5.3.2.7 Register 3Ah (address = 3Ah), Master Page (080h)

Figure 92. Register 3Ah

7	6	5	4	3	2	1	0
0	PERF MODE[2]	0	0	0	0	0	0
W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 25. Register 3Ah Field Descriptions

Bit	Field	Type	Reset	Description
7	0	W	0h	Must write 0
6	PERF MODE[2]	R/W	0h	Set all four PERF MODE[3:0] bits together. Bits are located in register address 39h, 3Ah, and 56h in the master page.
5-0	0	W	0h	Must write 0

8.5.3.2.8 Register 4Fh (address = 4Fh), Master Page (080h)

Figure 93. Register 4Fh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	EN INPUT DC COUPLING
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 26. Register 4Fh Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	EN INPUT DC COUPLING	R/W	0h	Enables dc-coupling between the analog inputs and driver by changing the internal biasing resistor between the analog inputs and VCM from 600 Ω to 5 kΩ. 0 = Disable dc-coupling support 1 = Enable dc-coupling support

8.5.3.2.9 Register 53h (address = 53h), Master Page (080h)

Figure 94. Register 53h

7	6	5	4	3	2	1	0
0	MASK SYSREF	0	0	0	0	EN SYSREF DC COUPLING	SET SYSREF
W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 27. Register 53h Field Descriptions

Bit	Field	Type	Reset	Description
7	0	W	0h	Must write 0
6	MASK SYSREF	R/W	0h	0 = Normal operation 1 = Ignores the SYSREF input
5-2	0	W	0h	Must write 0
1	EN SYSREF DC COUPLING	R/W	0h	Enables a higher common-mode voltage input on the SYSREF signal (up to 1.6 V). 0 = Normal operation 1 = Enables a higher SYSREF common-mode voltage support
0	SET SYSREF	R/W	0h	0 = Set SYSREF low 1 = Set SYSREF high

8.5.3.2.10 Register 54h (address = 54h), Master Page (080h)

Figure 95. Register 54h

7	6	5	4	3	2	1	0
ENABLE MANUAL SYSREF	0	0	0	0	0	0	0
R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 28. Register 54h Field Descriptions

Bit	Field	Type	Reset	Description
7	ENABLE MANUAL SYSREF	R/W	0h	This bit enables manual SYSREF
6-0	0	W	0h	Must write 0

8.5.3.2.11 Register 55h (address = 55h), Master Page (080h)

Figure 96. Register 55h

7	6	5	4	3	2	1	0
0	0	0	PDN MASK	0	0	0	0
W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 29. Register 55h Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	W	0h	Must write 0
4	PDN MASK	R/W	0h	This bit enables power-down via a register bit. 0 = Normal operation 1 = Power-down is enabled by powering down internal blocks as specified in the selected power-down mask
3-0	0	W	0h	Must write 0

8.5.3.2.12 Register 56h (address = 56h), Master Page (080h)

Figure 97. Register 56h

7	6	5	4	3	2	1	0
0	0	0	0	0	PERF MODE[3]	0	0
W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: W = Write only; -n = value after reset

Table 30. Register 56h Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	W	0h	Must write 0
2	PERF MODE[3]	W	0h	Set all four PERF MODE[3:0] bits together. Bits are located in register address 39h, 3Ah, and 56h in the master page.
1-0	0	W	0h	Must write 0

8.5.3.2.13 Register 59h (address = 59h), Master Page (080h)

Figure 98. Register 59h

7	6	5	4	3	2	1	0
FOVR CHB	0	ALWAYS WRITE 1	0	0	0	0	0
W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 31. Register 59h Field Descriptions

Bit	Field	Type	Reset	Description
7	FOVR CHB	W	0h	Outputs the FOVR signal for channel B on the SDOUT pin. 0 = Normal operation 1 = Outputs FOVR on the SDOUT pin
6	0	W	0h	Must write 0
5	ALWAYS WRITE 1	R/W	0h	Must write 1
4-0	0	W	0h	Must write 0

8.5.3.3 ADC Page (0Fh) Registers

8.5.3.3.1 Registers 5F (addresses = 5F), ADC Page (0Fh)

Figure 99. Register 5F

7	6	5	4	3	2	1	0
FOVR THRESHOLD PROG							
R/W-E3h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 32. Registers 5F Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FOVR THRESHOLD PROG	R/W	E3h	Program the fast OVR thresholds together for channel A and B, as described in the *Overrange Indication* section.

8.5.3.4 Main Digital Page (6800h) Registers

8.5.3.4.1 Register 0h (address = 0h), Main Digital Page (6800h)

Figure 100. Register 0h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	PULSE RESET
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 33. Register 0h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	PULSE RESET	R/W	0h	Must be pulsed after power-up or after configuring registers in the main digital page of the JESD bank. Any register bits in the main digital page (6800h) take effect only after this bit is pulsed; see the *Start-Up Sequence* section for the correct sequence. 0 = Normal operation 0 → 1 → 0 = Bit is pulsed

8.5.3.4.2 Register 41h (address = 41h), Main Digital Page (6800h)

Figure 101. Register 41h

7	6	5	4	3	2	1	0
0	0	0	DECFIL MODE[3]	0	DECFIL MODE[2:0]		
W-0h	W-0h	W-0h	R/W-0h	W-0h	R/W-0h		

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 34. Register 41h Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	W	0h	Must write 0
4	DECFIL MODE[3]	R/W	0h	Refer Table 35.
3	0	W	0h	Must write 0
2-0	DECFIL MODE[2:0]	R/W	2h	These bits select the decimation filter mode. Table 35 lists the bit settings. Register bit DEC MODE EN (register 4Dh, bit 3) must also be enabled.

Table 35. DECFIL MODE Bit Settings

DEC MODE EN (REGISTER 4Dh, BIT 3)	BITS (4, 2-0)	FILTER MODE	DECIMATION
0	XXXX	Low-pass filter	2X
1	1010	Low-pass filter	2X
1	1110	High-pass filter	2X
1	Others	Do not use	—

8.5.3.4.3 Register 42h (address = 42h), Main Digital Page (6800h)

Figure 102. Register 42h

7	6	5	4	3	2	1	0
0	0	0	0	0	NYQUIST ZONE		
W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h		

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 36. Register 42h Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	W	0h	Must write 0
2-0	NYQUIST ZONE	R/W	0h	The Nyquist zone must be selected for proper interleaving correction. Here Nyquist refers to Device Clock/2. For 1 GSPS Device clock, Nyquist frequency is 500 MHz. Also set register bit CTRL NYQUIST (4Eh, bit 7). 000 = 1st Nyquist zone (0 MHz to 500 MHz) 001 = 2nd Nyquist zone (500 MHz to 1000 MHz) 010 = 3rd Nyquist zone (1000 MHz to 1500 MHz) All others = Not used

8.5.3.4.4 Register 43h (address = 43h), Main Digital Page (6800h)

Figure 103. Register 43h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	FORMAT SEL
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 37. Register 43h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	FORMAT SEL	R/W	0h	Changes the output format. Set the FORMAT EN bit (register 4Bh, bit 5) to enable control using this bit. 0 = Twos complement 1 = Offset binary

8.5.3.4.5 Register 44h (address = 44h), Main Digital Page (6800h)

Figure 104. Register 44h

7	6	5	4	3	2	1	0
0	DIGITAL GAIN						
R/W-0h	R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 38. Register 44h Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R/W	0h	Must write 0
6-0	DIGITAL GAIN	R/W	0h	Digital gain setting. Digital gain must be enabled (register 52h, bit 0). Gain in dB = 20log (digital gain / 32). 7Fh = 127, equals digital gain of 9.5 dB.

8.5.3.4.6 Register 4Bh (address = 4Bh), Main Digital Page (6800h)

Figure 105. Register 4Bh

7	6	5	4	3	2	1	0
0	0	FORMAT EN	0	0	0	0	0
W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 39. Register 4Bh Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0
5	FORMAT EN	R/W	0h	This bit enables control for data format selection using the FORMAT SEL register bit. 0 = Default, output is in twos complement format 1 = Output is in offset binary format after the FORMAT SEL bit is set
4-0	0	W	0h	Must write 0

8.5.3.4.7 Register 4Dh (address = 4Dh), Main Digital Page (6800h)

Figure 106. Register 4Dh

7	6	5	4	3	2	1	0
0	0	0	0	DEC MOD EN	0	0	0
W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 40. Register 4Dh Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0
3	DEC MOD EN	R/W	0h	This bit enables control of decimation filter mode via the DECFIL MODE[3:0] register bits. 0 = Default 1 = Decimation modes control is enabled
2-0	0	W	0h	Must write 0

8.5.3.4.8 Register 4Eh (address = 4Eh), Main Digital Page (6800h)

Figure 107. Register 4Eh

7	6	5	4	3	2	1	0
CTRL NYQUIST	0	0	0	0	0	0	0
R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 41. Register 4Eh Field Descriptions

Bit	Field	Type	Reset	Description
7	CTRL NYQUIST	R/W	0h	This bit enables selecting the Nyquist zone using register 42h, bits 2-0. 0 = Selection disabled 1 = Selection enabled
6-0	0	W	0h	Must write 0

8.5.3.4.9 Register 52h (address = 52h), Main Digital Page (6800h)

Figure 108. Register 52h

7	6	5	4	3	2	1	0
ALWAYS WRITE 1	0	0	0	0	0	0	DIG GAIN EN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 42. Register 52h Field Descriptions

Bit	Field	Type	Reset	Description
7	ALWAYS WRITE 1	W	0h	This bit enables output bus reorder using the Dx_BUS_REORDER[7:0] bits. Set this bit along with register 72h, bit 3 in the main digital page.
6-1	0	W	0h	Must write 0
0	DIG GAIN EN	R/W	0h	Enables selecting the digital gain for register 44h. 0 = Digital gain disabled 1 = Digital gain enabled

8.5.3.4.10 Register 72h (address = 72h), Main Digital Page (6800h)

Figure 109. Register 72h

7	6	5	4	3	2	1	0
0	0	0	0	ALWAYS WRITE 1	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: W = Write only; -n = value after reset

Table 43. Register 72h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0
3	ALWAYS WRITE 1	W	0h	This bit enables output bus reorder using the Dx_BUS_REORDER[7:0] bits. Set this bit along with register 52h, bit 7 in the main digital page.
2-0	0	W	0h	Must write 0

8.5.3.4.11 Register ABh (address = ABh), Main Digital Page (6800h)

Figure 110. Register ABh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	LSB SEL EN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 44. Register ABh Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	LSB SEL EN	R/W	0h	Enables control for the LSB SELECT register bit. 0 = Default 1 = The LSB of the 16-bit ADC data can be programmed as fast OVR using the LSB SELECT bit

8.5.3.4.12 Register ADh (address = ADh), Main Digital Page (6800h)

Figure 111. Register ADh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LSB SELECT	
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 45. Register ADh Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0
1-0	LSB SELECT	R/W	0h	Enables output of the FOVR flag instead of the output data LSB. 00 = Output is 16-bit data 11 = Output data LSB is replaced by the FOVR information for each channel

8.5.3.4.13 Register F7h (address = F7h), Main Digital Page (6800h)

Figure 112. Register F7h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	DIG RESET
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: W = Write only; -n = value after reset

Table 46. Register F7h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0
0	DIG RESET	W	0h	Self-clearing reset for the digital block. Does not include the interleaving correction. 0 = Normal operation 1 = Digital reset

8.5.3.5 JESD Digital Page (6900h) Registers

8.5.3.5.1 Register 0h (address = 0h), JESD Digital Page (6900h)

Figure 113. Register 0h

7	6	5	4	3	2	1	0
CTRL K	0	0	TESTMODE EN	FLIP ADC DATA	LANE ALIGN	FRAME ALIGN	TX LINK DIS
R/W-0h	W-0h	W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 47. Register 0h Field Descriptions

Bit	Field	Type	Reset	Description
7	CTRL K	R/W	0h	Enable bit for a number of frames per multi-frame. 0 = Default is five frames per multi-frame 1 = Frames per multi-frame can be set in register 06h
6-5	0	W	0h	Must write 0
4	TESTMODE EN	R/W	0h	This bit generates the long transport layer test pattern mode, as per section 5.1.6.3 of the JESD204B specification. 0 = Test mode disabled 1 = Test mode enabled
3	FLIP ADC DATA	R/W	0h	0 = Normal operation 1 = Output data order is reversed: MSB to LSB
2	LANE ALIGN	R/W	0h	This bit inserts the lane alignment character (K28.3) for the receiver to align to the lane boundary, as per section 5.3.3.5 of the JESD204B specification. 0 = Normal operation 1 = Inserts lane alignment characters
1	FRAME ALIGN	R/W	0h	This bit inserts the lane alignment character (K28.7) for the receiver to align to the lane boundary, as per section 5.3.3.5 of the JESD204B specification. 0 = Normal operation 1 = Inserts frame alignment characters
0	TX LINK DIS	R/W	0h	This bit disables sending the initial link alignment (ILA) sequence when $\overline{\text{SYNC}}$ is de-asserted. 0 = Normal operation 1 = ILA disabled

8.5.3.5.2 Register 1h (address = 1h), JESD Digital Page (6900h)

Figure 114. Register 1h

7	6	5	4	3	2	1	0
SYNC REG	SYNC REG EN	0	0	0	JESD MODE		
R/W-0h	R/W-0h	W-0h	W-0h	W-0h	R/W-1h		

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 48. Register 1h Field Descriptions

Bit	Field	Type	Reset	Description
7	SYNC REG	R/W	0h	Register control for sync request. 0 = Normal operation 1 = ADC output data are replaced with K28.5 characters; the SYNC REG EN register bit must also be set to 1
6	SYNC REG EN	R/W	0h	Enables register control for sync request. 0 = Use the $\overline{\text{SYNC}}$ pin for sync requests 1 = Use the SYNC REG register bit for sync requests
5-3	0	W	0h	Must write 0
2-0	JESD MODE	R/W	1h	These bits select the number of active output lanes. The JESD PLL MODE register bit located in the JESD analog page must also be set accordingly. Active lanes carry serial JESD data whereas inactive lanes don't carry any data. 001 = 20X mode, four active lanes per device (default) 010 = 40X mode, two active lanes per device All others = Not used

8.5.3.5.3 Register 2h (address = 2h), JESD Digital Page (6900h)

Figure 115. Register 2h

7	6	5	4	3	2	1	0
LINK LAYER TESTMODE			LINK LAYER RPAT	LMFC MASK RESET	0	0	0
R/W-0h			R/W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 49. Register 2h Field Descriptions

Bit	Field	Type	Reset	Description
7-5	LINK LAYER TESTMODE	R/W	0h	These bits generate a pattern according to section 5.3.3.8.2 of the JESD204B document. 000 = Normal ADC data 001 = D21.5 (high-frequency jitter pattern) 010 = K28.5 (mixed-frequency jitter pattern) 011 = Repeat initial lane alignment (generates a K28.5 character and continuously repeats lane alignment sequences) 100 = 12-octet RPAT jitter pattern All others = Not used
4	LINK LAYER RPAT	R/W	0h	This bit changes the running disparity in the modified RPAT pattern test mode (only when the link layer test mode = 100). 0 = Normal operation 1 = Changes disparity
3	LMFC MASK RESET	R/W	0h	Masks the LMFC reset coming to the digital block. 0 = LMFC reset is not masked 1 = Ignore the LMFC reset request
2-0	0	W	0h	Must write 0

8.5.3.5.4 Register 3h (address = 3h), JESD Digital Page (6900h)

Figure 116. Register 3h

7	6	5	4	3	2	1	0
FORCE LMFC COUNT	LMFC COUNT INIT					RELEASE ILANE SEQ	
R/W-0h	R/W-0h					R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 50. Register 3h Field Descriptions

Bit	Field	Type	Reset	Description
7	FORCE LMFC COUNT	R/W	0h	This bit forces the LMFC count. 0 = Normal operation 1 = Enables using a different starting value for the LMFC counter
6-2	MASK SYSREF	R/W	0h	When SYSREF transmits to the digital block, the LMFC count resets to 0 and K28.5 stops transmitting when the LMFC count reaches 31. The initial value that the LMFC count resets to can be set using LMFC COUNT INIT. In this manner, the receiver can be synchronized early because the LANE ALIGNMENT SEQUENCE is received early. The FORCE LMFC COUNT register bit must be enabled.
1-0	RELEASE ILANE SEQ	R/W	0h	These bits delay the generation of the lane alignment sequence by 0, 1, 2 or 3 multi-frames after the code group synchronization. 00 = 0 01 = 1 10 = 2 11 = 3

8.5.3.5.5 Register 5h (address = 5h), JESD Digital Page (6900h)

Figure 117. Register 5h

7	6	5	4	3	2	1	0
SCRAMBLE EN	0	0	0	0	0	0	0
R/W-Undefined	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 51. Register 5h Field Descriptions

Bit	Field	Type	Reset	Description
7	SCRAMBLE EN	R/W	Undefined	Scrambles the enable bit in the JESD204B interface. 0 = Scrambling disabled 1 = Scrambling enabled
6-0	0	W	0h	Must write 0

8.5.3.5.6 Register 6h (address = 6h), JESD Digital Page (6900h)

Figure 118. Register 6h

7	6	5	4	3	2	1	0
0	0	0	FRAMES PER MULTI FRAME (K)				
W-0h	W-0h	W-0h	R/W-8h				

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 52. Register 6h Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	W	0h	Must write 0
4-0	FRAMES PER MULTI FRAME (K)	R/W	8h	These bits set the number of multi-frames. Actual K is the value in hex + 1 (that is, 0Fh is K = 16).

8.5.3.5.7 Register 7h (address = 7h), JESD Digital Page (6900h)

Figure 119. Register 7h

7	6	5	4	3	2	1	0
0	0	0	0	SUBCLASS	0	0	0
W-0h	W-0h	W-0h	W-0h	R/W-1h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 53. Register 7h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0
3	SUBCLASS	R/W	1h	This bit sets the JESD204B subclass. 000 = Subclass 0 is backward compatible with JESD204A 001 = Subclass 1 deterministic latency using the SYSREF signal
2-0	0	W	0h	Must write 0

8.5.3.5.8 Register 31h (address = 31h), JESD Digital Page (6900h)

Figure 120. Register 31h

7	6	5	4	3	2	1	0
DA_BUS_REORDER[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 54. Register 31h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DA_BUS_REORDER[7:0]	R/W	0h	Use these bits to program output connections between data streams and output lanes in decimate-by-2 mode. Table 12 lists the supported combinations of these bits.

8.5.3.5.9 Register 32h (address = 32h), JESD Digital Page (6900h)

Figure 121. Register 32h

7	6	5	4	3	2	1	0
DB_BUS_REORDER[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 55. Register 32h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DB_BUS_REORDER[7:0]	R/W	0h	Use these bits to program output connections between data streams and output lanes in decimate-by-2 mode. Table 12 lists the supported combinations of these bits.

8.5.3.6 JESD Analog Page (6A00h) Register

8.5.3.6.1 Registers 12h-5h (address = 12h-5h), JESD Analog Page (6A00h)

Figure 122. Register 12h

7	6	5	4	3	2	1	0
SEL EMP LANE 1						0	0
R/W-0h						W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 123. Register 13h

7	6	5	4	3	2	1	0
SEL EMP LANE 0						0	0
R/W-0h						W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 124. Register 14h

7	6	5	4	3	2	1	0
SEL EMP LANE 2						0	0
R/W-0h						W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Figure 125. Register 15h

7	6	5	4	3	2	1	0
SEL EMP LANE 3						0	0
R/W-0h						W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 56. Registers 12h-15h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	SEL EMP LANE 1, 0, 2, or 3	R/W	0h	Selects the amount of de-emphasis for the JESD output transmitter. The de-emphasis value in dB is measured as the ratio between the peak value after the signal transition to the settled value of the voltage in one bit period. 000000 = 0 dB 000001 = –1 dB 000011 = –2 dB 000111 = –4.1 dB 001111 = –6.2 dB 011111 = –8.2 dB 111111 = –11.5 dB
1-0	0	W-0h	0h	Must write 0

8.5.3.6.2 Register 16h (address = 16h), JESD Analog Page (6A00h)

Figure 126. Register 16h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	JESD PLL MODE	
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 57. Register 16h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0
1-0	JESD PLL MODE	R/W	0h	These bits select the JESD PLL multiplication factor and must match the JESD MODE setting. 00 = 20X mode, four active lanes per device 01 = Not used 10 = 40X mode, two active lanes per device 11 = Not used

8.5.3.6.3 Register 1Ah (address = 1Ah), JESD Analog Page (6A00h)

Figure 127. Register 1Ah

7	6	5	4	3	2	1	0
0	0	0	0	0	0	FOVR CHA	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 58. Register 1Ah Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0
1	FOVR CHA	R/W	0h	Outputs the FOVR signal for channel A on the PDN pin. FOVR CHA EN (register 1Bh, bit 3) must be enabled. 0 = Normal operation 1 = FOVR on the PDN pin
0	0	W	0h	Must write 0

8.5.3.6.4 Register 1Bh (address = 1Bh), JESD Analog Page (6A00h)

Figure 128. Register 1Bh

7	6	5	4	3	2	1	0
JESD SWING			0	FOVR CHA EN	0	0	0
R/W-0h			W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 59. Register 1Bh Field Descriptions

Bit	Field	Type	Reset	Description
7-5	JESD SWING	R/W	0h	Selects the output differential amplitude V_{OD} (mV_{PP}) of the JESD transmitter (for all lanes). 0 = 860 mV_{PP} 1 = 810 mV_{PP} 2 = 770 mV_{PP} 3 = 745 mV_{PP} 4 = 960 mV_{PP} 5 = 930 mV_{PP} 6 = 905 mV_{PP} 7 = 880 mV_{PP}
4	0	W	0h	Must write 0
3	FOVR CHA EN	R/W	0h	Enables overwriting the PDN pin with the FOVR signal from channel A. 0 = Normal operation 1 = PDN is overwritten
2-0	JESD PLL MODE	R/W	0h	Must write 0

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Start-Up Sequence

The steps described in Table 60 are the recommended power-up sequence with the ADS54J69 in 20X or 40X mode.

Table 60. Initialization Sequence

STEP	SEQUENCE	DESCRIPTION	PAGE BEING PROGRAMMED	COMMENT
1	Power-up the device	Bring up IOVDD to 1.15 V before applying power to DVDD. Bring up DVDD to 1.9 V, AVDD to 1.9 V, and AVDD3V to 3.0 V.	—	See the *Power Sequencing and Initialization* section for power sequence requirements.
2	Reset the device	**Hardware reset**		
		Apply a hardware reset by pulsing pin 48 (low->high->low).	—	A hardware reset clears all registers to their default values.
		Software reset: Register writes equivalent to a hardware reset are:		
		Write address 0-000h with 81h.	General register	Reset registers in the ADC page and master page of the analog bank This bit is a self-clearing bit.
				This bit is a self-clearing bit.
		Write address 4-001h with 00h and address 4-002h with 00h.	Unused page	Clear any unwanted content from the unused pages of the JESD bank.
		Write address 4-003h with 00h and address 4-004h with 68h.	—	Select the main digital page of the JESD bank.
		Write address 6-0F7h with 01h for channel A.	Main digital page (JESD bank)	Use the DIG RESET register bit to reset all pages in the JESD bank.
				This bit is a self-clearing bit.
		Write address 6-000h with 01h, then address 6-000h with 00h.		Pulse the PULSE RESET register bit for both channels.
3	Performance modes	Write address 0-011h with 80h.	—	Select the master page of the analog bank.
		Write address 0-059h with 20h.	Master page (analog bank)	Set the ALWAYS WRITE 1 bit.
4	Program registers for 20X or 40X serialization and program the HPF or LPF filter	**The JESD mode (in the JESD digital page) and JESD PLL mode (in the JESD analog page) register bits control 20X or 40X serialization. By default after reset, the device is in 20X serialization mode (4-lanes output).**		
		Write address 4-003h with 00h and address 4-004h with 69h.	—	Select the JESD digital page.
		Write address 6-000h with 80h.	JESD digital page (JESD bank)	Set the CTRL K bit for both channels to program K for the SYSREF signal frequency in step 5.
		Write address 6-001h with 01h.		Enable 20X serialization (4-lane output, default setting after reset).
		Write address 6-001h with 02h.		Enable 40X serialization (2-lane output).
		Write address 4-003h with 00h and address 4-004h with 6Ah.	JESD analog page (JESD bank)	Select the JESD analog page.
		Write address 6-016h with 00h		Enable 20X serialization (4-lane output, default setting after reset).
		Write address 6-016h with 02h		To enable 40X serialization (2-lane output).
		Write address 4-003h with 00h and address 4-004h with 68h.	Main digital page (JESD bank)	Select the main digital page.
		Write address 6-052h with 80h and address 6-072h with 08h.		Set the ALWAYS WRITE 1 bit (enables correct order of the JESD output lanes).
		Write address 6-04Dh with 08h		Enable the decimation filter programming.
		Write address 6-041h with 12h		Enable the low-pass filter (default setting after reset).
		Write address 6-041h with 16h		Enable the high-pass filter.
		Write address 6-000h with 01h and address 6-000h with 00h.		Pulse the PULSE RESET register bit. All settings programmed in the main digital page take effect only after this bit is pulsed.

Table 60. Initialization Sequence (continued)

STEP	SEQUENCE	DESCRIPTION	PAGE BEING PROGRAMMED	COMMENT
5	Set the value of K and the SYSREF signal frequency accordingly	Write address 4-003h with 00h and address 4-004h with 69h.	—	Select the JESD digital page.
		Write address 6-006h with XXh (choose the value of K).	JESD digital page (JESD bank)	Default value of K is 8 for 20X (4-lane) mode and 4 for 40X (2-lane) mode. However, K can be programmed for higher values than the default by using bits 4-0 of address 6-006 in the JESD digital page. For example, if K = 31 by writing address 6-006h with 1Fh in the JESD digital page, then the SYSREF signal frequency must be kept less than or equal to 250 MHz / 32 = 7.8125 MHz.
6	JESD lane alignment	Pull the $\overline{\text{SYNC}}$ pin (pin 63) low.	—	Transmit K28.5 characters.
		Pull the $\overline{\text{SYNC}}$ pin high.		After the receiver is synchronized, initiate an ILA phase and subsequent transmissions of ADC data.

9.1.2 Hardware Reset

Figure 129 and Table 61 show the timing for a hardware reset.

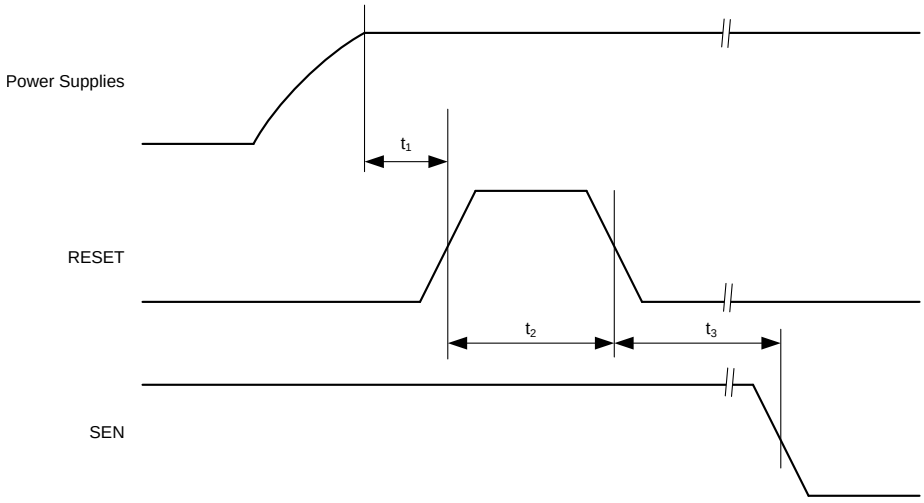


Figure 129. Hardware Reset Timing Diagram

Table 61. Timing Requirements for Figure 129

		MIN	TYP	MAX	UNIT
t_1	Power-on delay from power-up to active high RESET pulse	1			ms
t_2	Reset pulse duration: active high RESET pulse duration	10			ns
t_3	Register write delay: delay from RESET disable to SEN active	100			ns

9.1.3 SNR and Clock Jitter

The signal-to-noise ratio (SNR) of the ADC is limited by three different factors: quantization noise, thermal noise, and jitter, as shown in Equation 4. The quantization noise is typically not noticeable in pipeline converters and is 98 dB for a 16-bit ADC. The thermal noise limits SNR at low input frequencies and the clock jitter sets SNR for higher input frequencies. The decimation-by-2 process gives approximately an additional 3-dB improvement in SNR.

$$SNR_{ADC}[dBc] = -3 - 20log\sqrt{\left(10^{-\frac{SNR_{Quantization\ \ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Thermal\ \ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Jitter}}{20}}\right)^2} \quad (4)$$

The SNR limitation resulting from the sample clock jitter can be calculated by Equation 5:

$$SNR_{Jitter}[dBc] = -20log(2\pi \times f_{in} \times T_{Jitter}) \quad (5)$$

The total clock jitter (T_{Jitter}) has two components: the internal aperture jitter (145 f_S) is set by the noise of the clock input buffer and the external clock jitter. T_{Jitter} can be calculated by Equation 6:

$$T_{Jitter} = \sqrt{\left(T_{Jitter,\ Ext\_Clock\_Input}\right)^2 + \left(T_{Aperture\_ADC}\right)^2} \quad (6)$$

External clock jitter can be minimized by using high-quality clock sources and jitter cleaners as well as band-pass filters at the clock input. A faster clock slew rate also improves the ADC aperture jitter.

The ADS54J69 has a thermal noise of approximately 71.1 dBFS and an internal aperture jitter of 120 f_S. The SNR, depending on the amount of external jitter for different input frequencies, is shown in Figure 130.

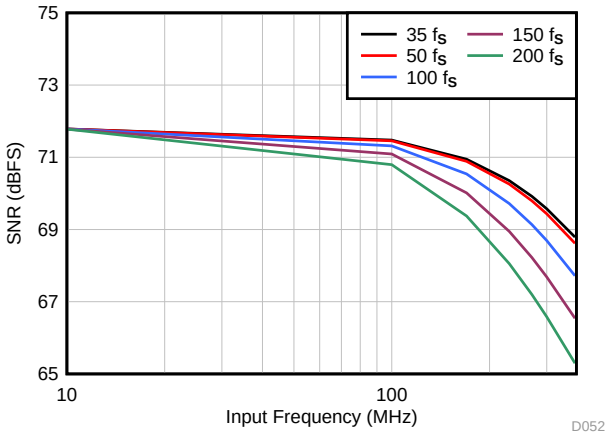


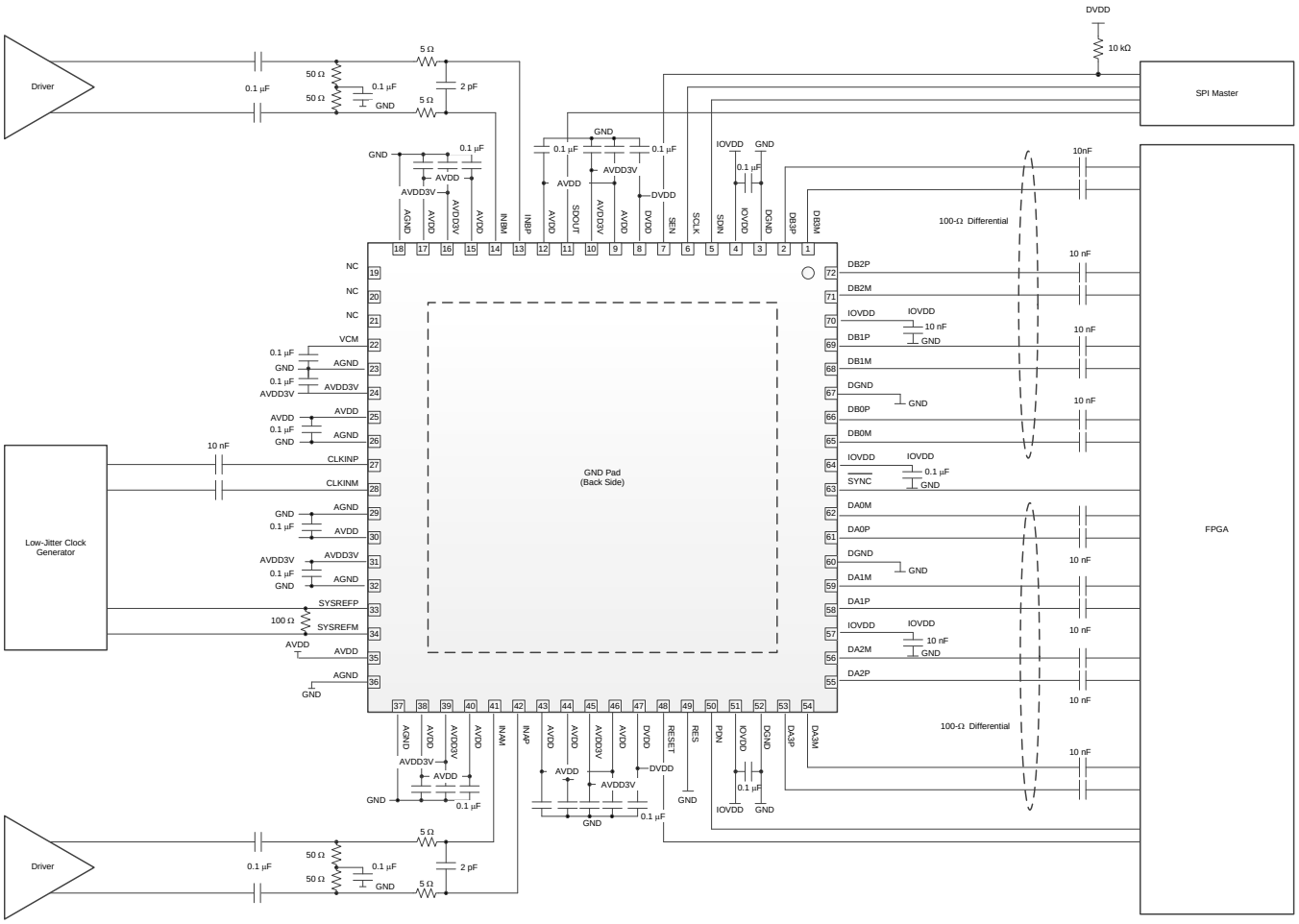
Figure 130. SNR versus Input Frequency and External Clock Jitter

Half-band decimation filtering employed by the ADS54J69 reduces the affect of all contributors to SNR by 3 dB. Filtering makes the SNR curve in Figure 130 start at 74 dBFS despite a thermal noise of 71.1 dBFS.

Decimation filtering also improves the affect of jitter noise by 3 dB, and is equivalent to having 102 f_S as the effective aperture jitter instead of 120 f_S.

9.2 Typical Application

The ADS54J69 is designed for wideband receiver applications demanding excellent dynamic range over a large input frequency range. A typical schematic for an ac-coupled receiver is shown in Figure 131.



NOTE: GND = AGND and DGND connected in the PCB layout.

Figure 131. AC-Coupled Receiver

Typical Application (continued)

9.2.1 Design Requirements

9.2.1.1 Transformer-Coupled Circuits

Typical applications involving transformer-coupled circuits are discussed in this section. Transformers (such as ADT1-1WT or WBC1-1) can be used up to 300 MHz to achieve good phase and amplitude balances at the ADC inputs. When designing dc driving circuits, the ADC input impedance must be considered. Figure 132 and Figure 133 show the impedance ($Z_{IN} = R_{IN} \parallel C_{IN}$) across the ADC input pins.

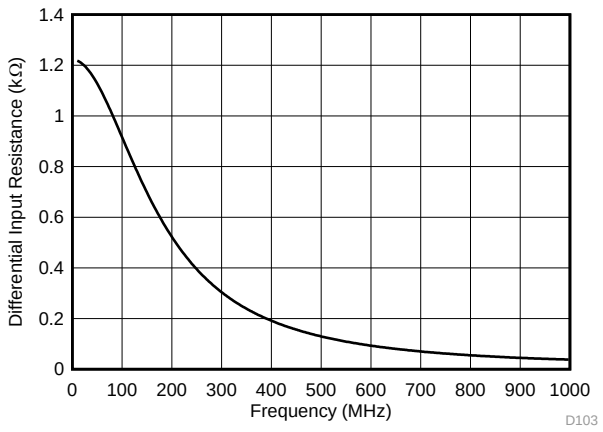


Figure 132. R_{IN} vs Input Frequency

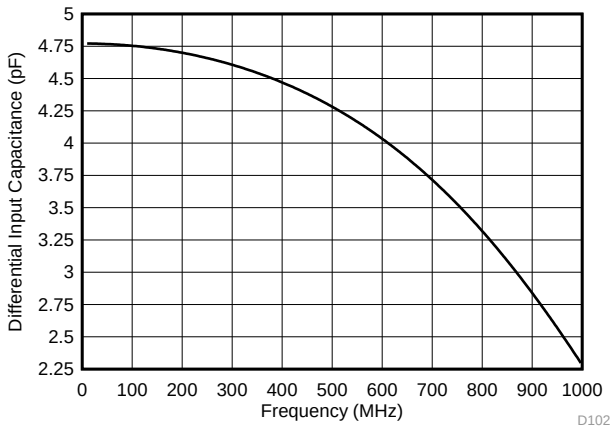


Figure 133. C_{IN} vs Input Frequency

By using the simple drive circuit of Figure 134, uniform performance can be obtained over a wide frequency range. The buffers present at the analog inputs of the device help isolate the external drive source from the switching currents of the sampling circuit.

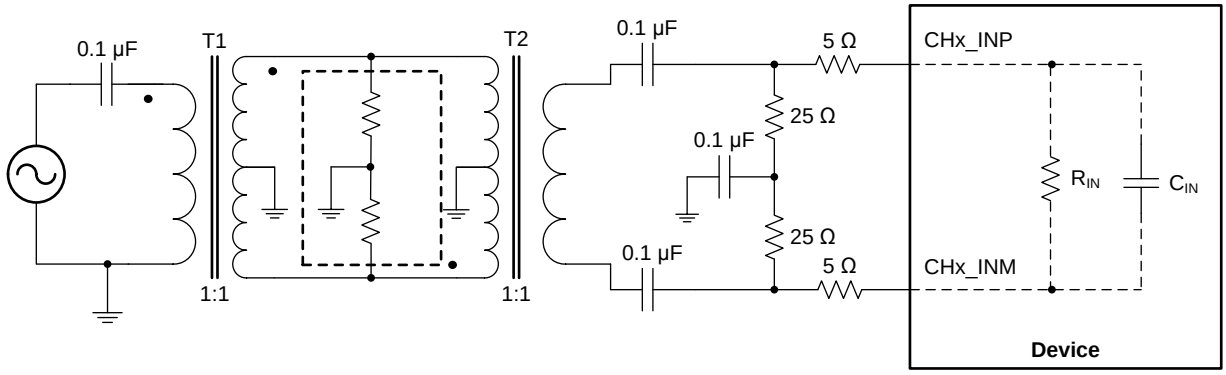


Figure 134. Input Drive Circuit

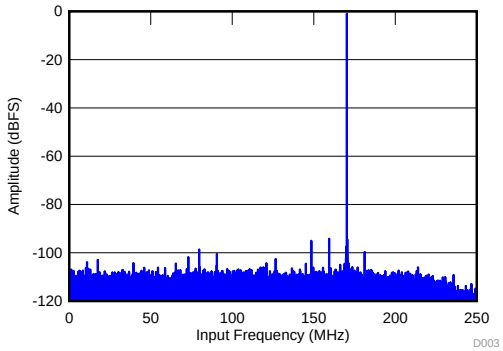
9.2.2 Detailed Design Procedure

For optimum performance, the analog inputs must be driven differentially. This architecture improves common-mode noise immunity and even-order harmonic rejection. A small resistor (5 Ω to 10 Ω) in series with each input pin is recommended to damp out ringing caused by package parasitics, as shown in Figure 134.

Typical Application (continued)

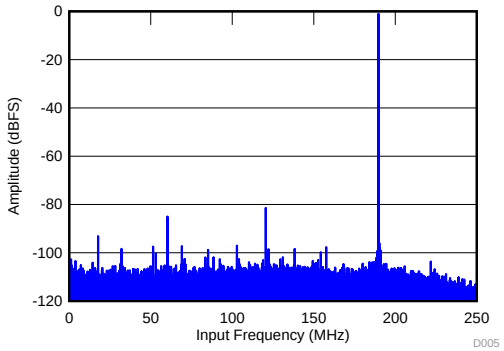
9.2.3 Application Curves

Figure 135 and Figure 136 show the typical performance at 170 MHz and 230 MHz, respectively.



SNR = 73 dBFS; SFDR = 93 dBc; SINAD = 73.18 dBFS;
THD = 89 dBc; HD2 = 93 dBc; HD3 = 103 dBc;
IL spur = 99 dBc; non HD2, HD3 spur = 94 dBc

Figure 135. FFT for 170-MHz Input Signal



SNR = 71.6 dBFS; SFDR = 80 dBc; SINAD = 71 dBFS;
THD = 79 dBc; HD2 = –80 dBc; HD3 = –96 dBc;
IL spur = 85 dBc; non HD2, HD3 spur = 92 dBc

Figure 136. FFT for 310-MHz Input Signal

10 Power Supply Recommendations

The device requires a 1.15-V nominal supply for IOVDD, a 1.9-V nominal supply for DVDD, a 1.9-V nominal supply for AVDD, and a 3.0-V nominal supply for AVDD3V. For detailed information regarding the operating voltage minimum and maximum specifications of different supplies, see the *Recommended Operating Conditions* table.

10.1 Power Sequencing and Initialization

Figure 137 shows the suggested power-up sequencing for the device. Note that the 1.15-V IOVDD supply must rise before the 1.9-V DVDD supply. If the 1.9-V DVDD supply rises before the 1.15-V IOVDD supply, then the internal default register settings may not load properly. The other supplies (the 3-V AVDD3V and the 1.9-V AVDD), can come up in any order during the power sequence. The power supplies can ramp up at any rate and there is no hard requirement for the time delay between IOVDD ramp up to DVDD ramp-up (can be in orders of microseconds but is recommend to be a few milliseconds).

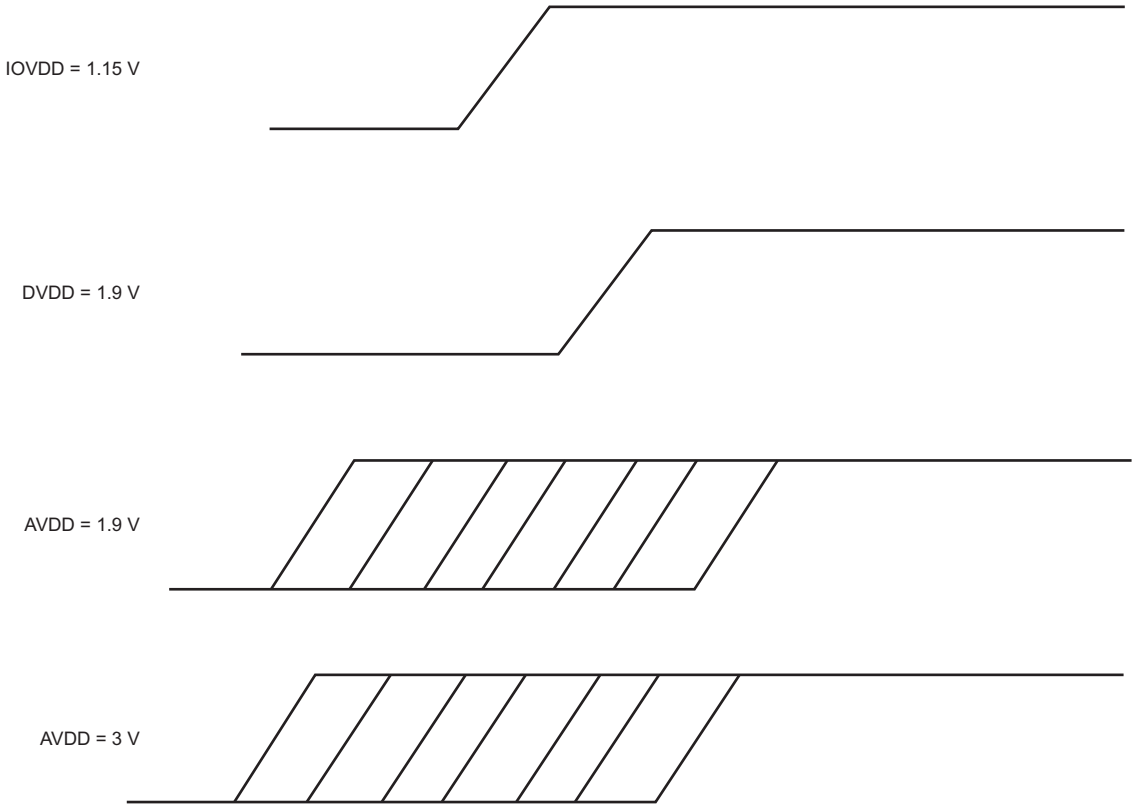


Figure 137. Power Sequencing for the ADS54Jxx Family of Devices

11 Layout

11.1 Layout Guidelines

The device evaluation module (EVM) layout can be used as a reference layout to obtain the best performance. A layout diagram of the EVM top layer is provided in Figure 138. A complete layout of the EVM is available from the ADS54J69EVM folder. Some important points to remember during board layout are:

- Analog inputs are located on opposite sides of the device pinout to ensure minimum crosstalk on the package level. To minimize crosstalk onboard, the analog inputs must exit the pinout in opposite directions, as illustrated in the reference layout of Figure 138 as much as possible.
- In the device pinout, the sampling clock is located on a side perpendicular to the analog inputs in order to minimize coupling between them. This configuration is also maintained on the reference layout of Figure 138 as much as possible.
- Keep digital outputs away from the analog inputs. When these digital outputs exit the pinout, the digital output traces must not be kept parallel to the analog input traces because this configuration can result in coupling from the digital outputs to the analog inputs and degrade performance. All digital output traces to the receiver [such as a field-programmable gate array (FPGA) or an application-specific integrated circuit (ASIC)] must be matched in length to avoid skew among outputs.
- At each power-supply pin (AVDD, DVDD, or AVDDD3V), keep a 0.1-µF decoupling capacitor close to the device. A separate decoupling capacitor group consisting of a parallel combination of 10-µF, 1-µF, and 0.1-µF capacitors can be kept close to the supply source.

11.2 Layout Example

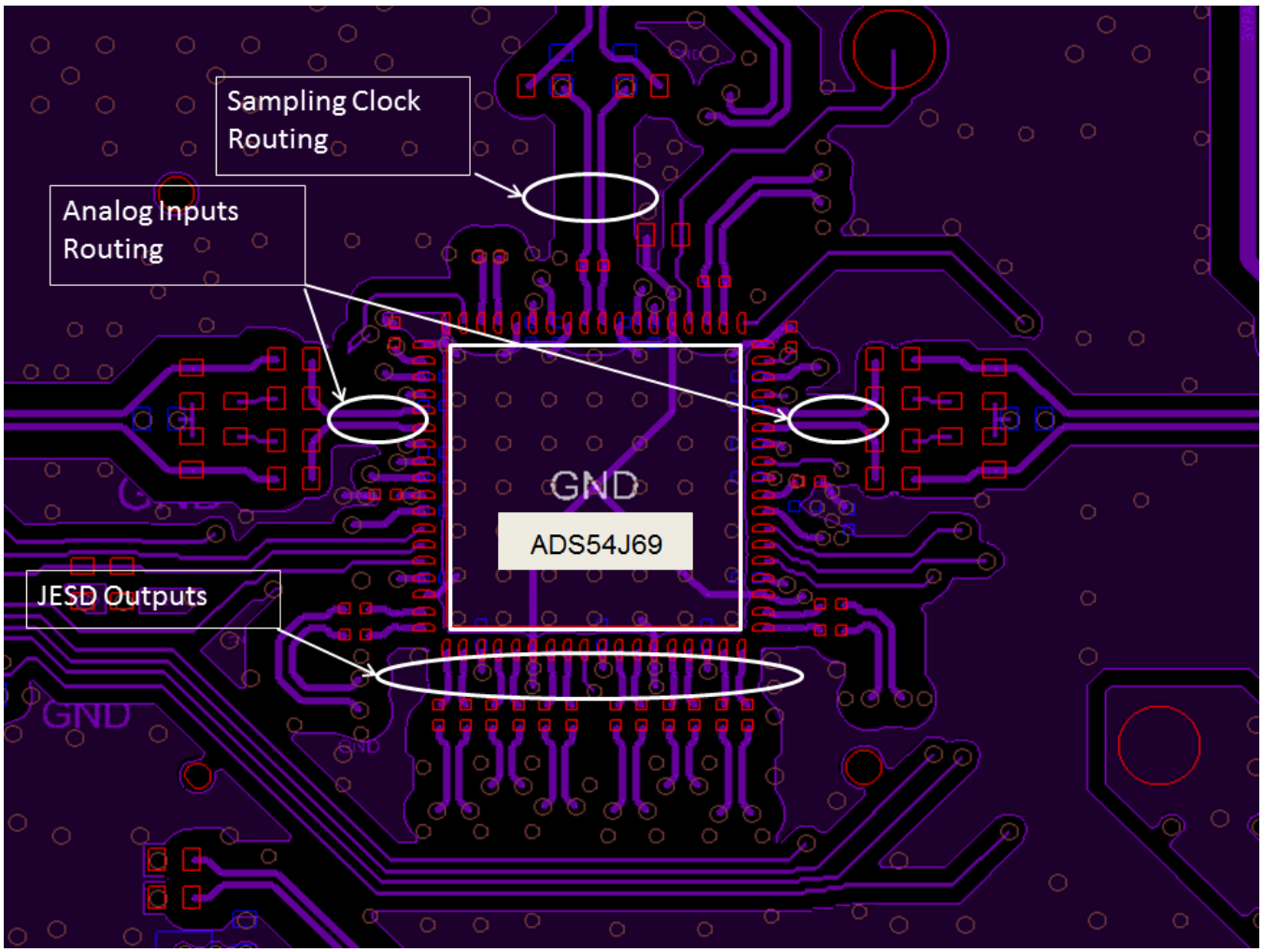


Figure 138. ADS54J69EVM layout

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

相关文档如下：

- *ADS54J20双通道 12 位 1.0GSPS 模数转换器*
- *ADS54J40 双通道 14 位 1.0GSPS 模数转换器*
- *ADS54J42 双通道、14 位、625MSPS 模数转换器*
- *ADS54J60 双通道 16 位 1.0GSPS 模数转换器*
- *ADS54J66 具有集成 DDC 的四通道、14 位、500MSPS ADC*
- 《ADS54J69EVM 用户指南》

12.2 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS54J69IRMP	Active	Production	VQFN (RMP) | 72	168 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ54J69
ADS54J69IRMP.A	Active	Production	VQFN (RMP) | 72	168 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ54J69
ADS54J69IRMPG4	Active	Production	VQFN (RMP) | 72	168 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ54J69
ADS54J69IRMPG4.A	Active	Production	VQFN (RMP) | 72	168 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ54J69
ADS54J69IRMPT	Active	Production	VQFN (RMP) | 72	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ54J69
ADS54J69IRMPT.A	Active	Production	VQFN (RMP) | 72	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ54J69

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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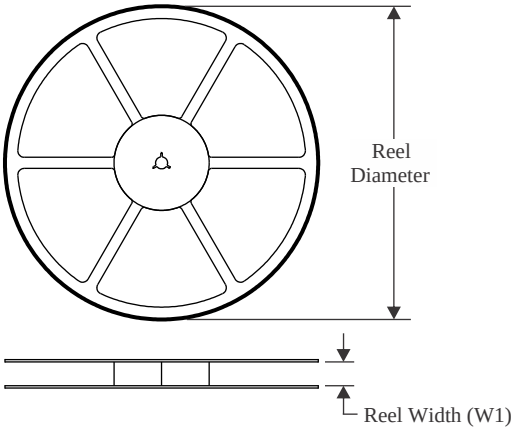
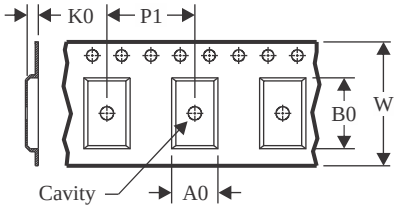
TAPE AND REEL INFORMATION

REEL DIMENSIONS

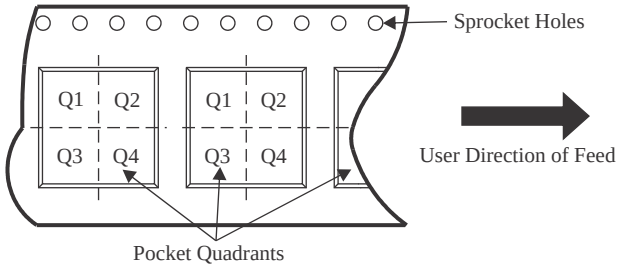


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

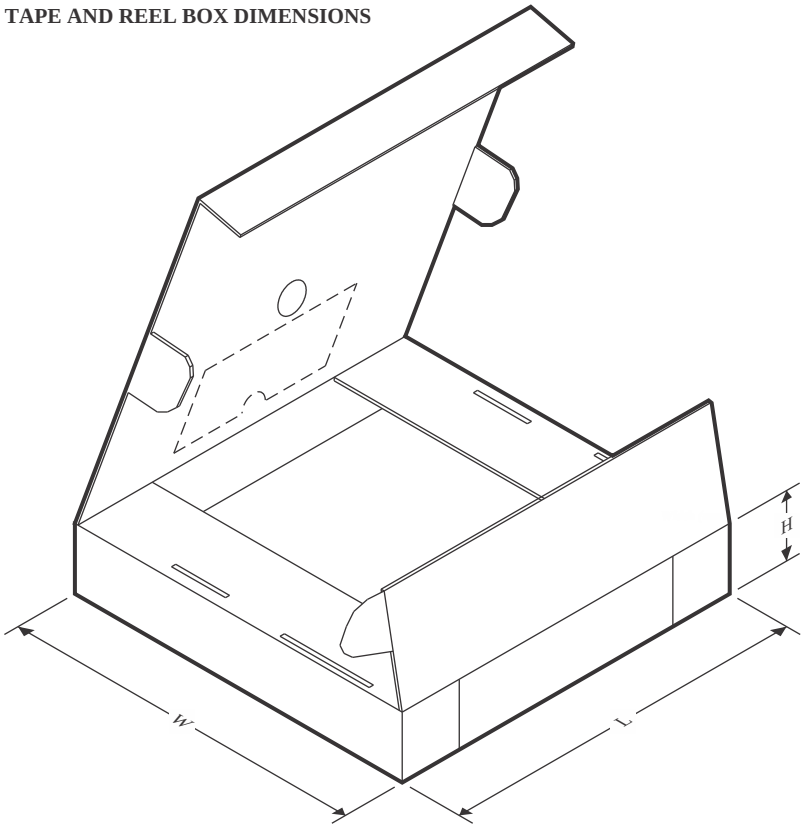
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS54J69IRMPT	VQFN	RMP	72	250	180.0	24.4	10.25	10.25	2.25	16.0	24.0	Q2

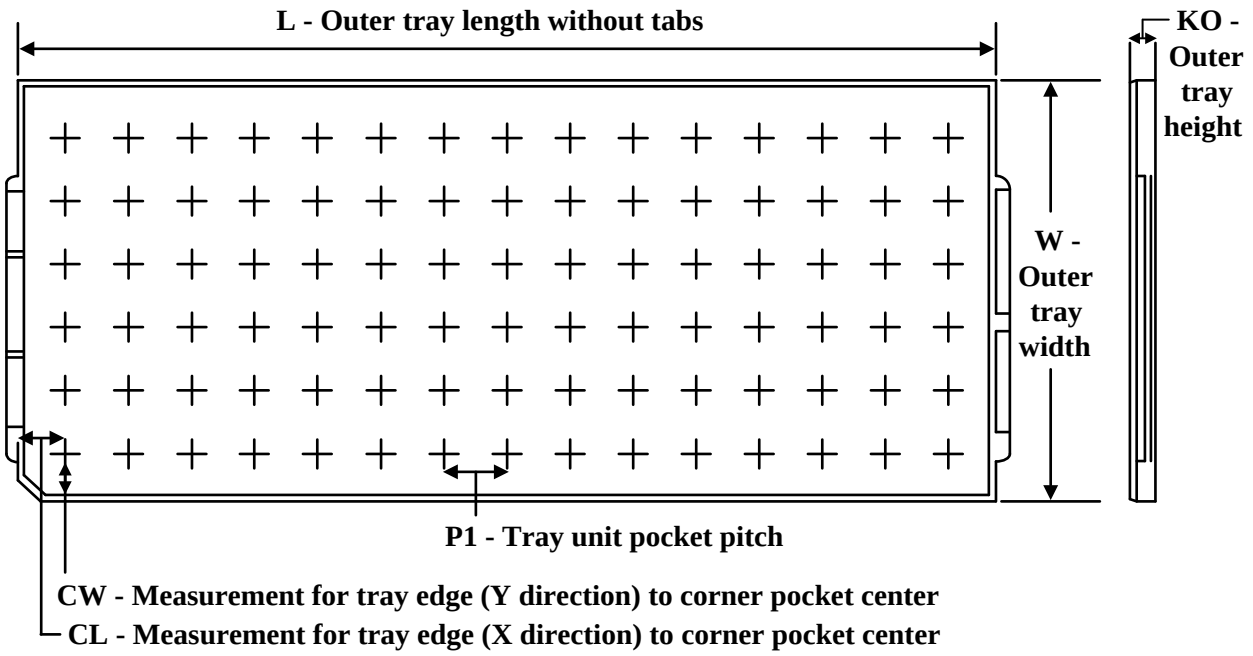
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS54J69IRMPT	VQFN	RMP	72	250	213.0	191.0	55.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

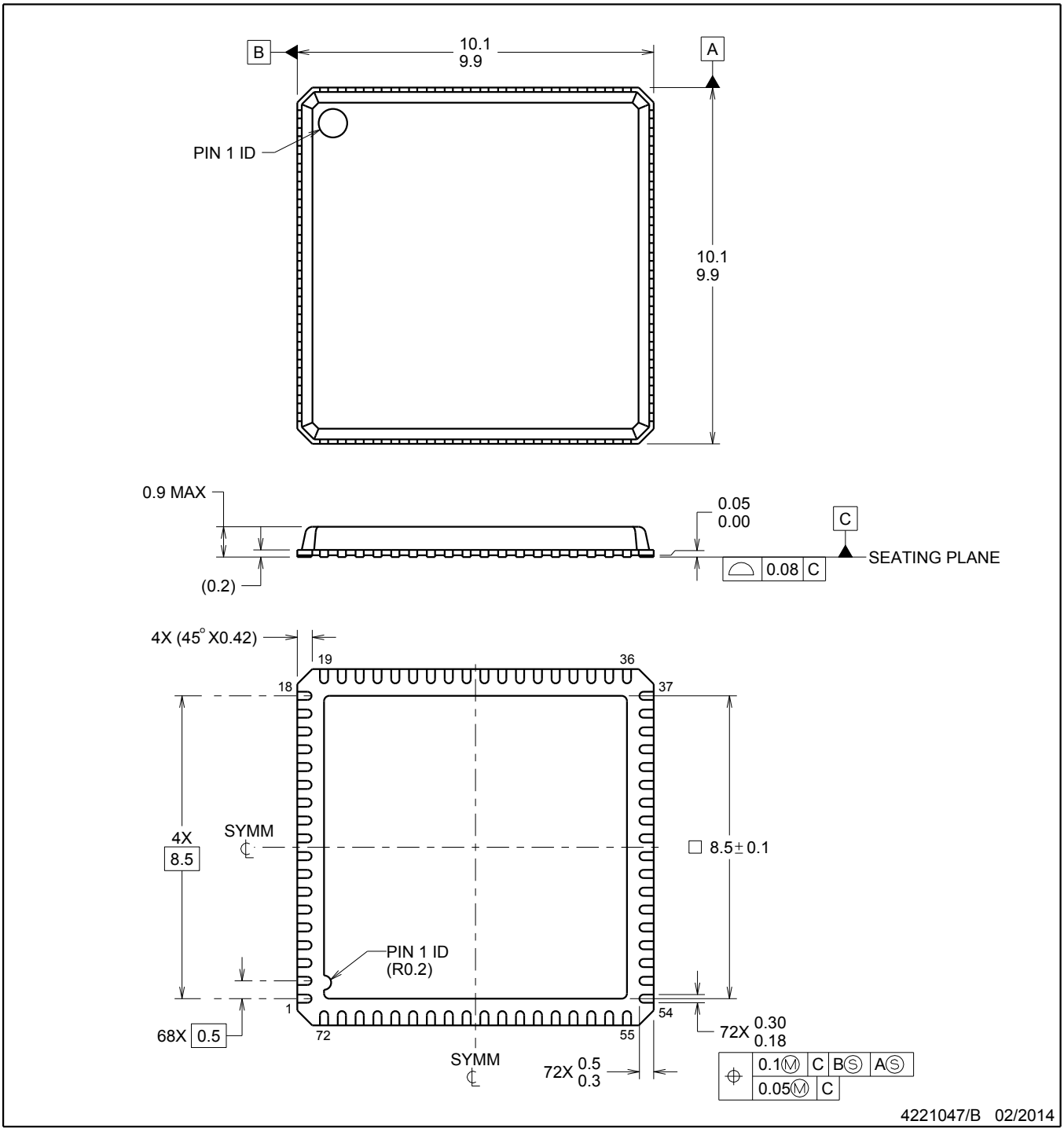
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADS54J69IRMP	RMP	VQFNP	72	168	8 X 21	150	315	135.9	7620	14.65	11	11.95
ADS54J69IRMP.A	RMP	VQFNP	72	168	8 X 21	150	315	135.9	7620	14.65	11	11.95
ADS54J69IRMPG4	RMP	VQFNP	72	168	8 X 21	150	315	135.9	7620	14.65	11	11.95
ADS54J69IRMPG4.A	RMP	VQFNP	72	168	8 X 21	150	315	135.9	7620	14.65	11	11.95

PACKAGE OUTLINE

RMP0072A

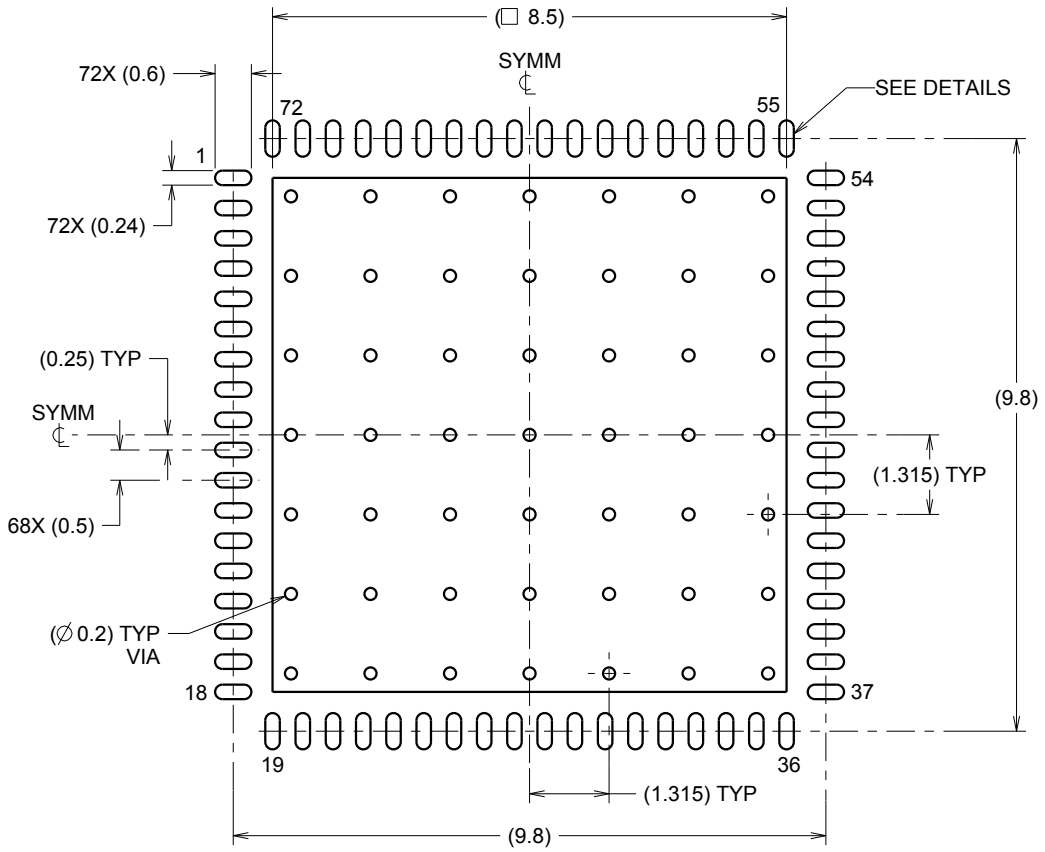
VQFN - 0.9 mm max height

VQFN

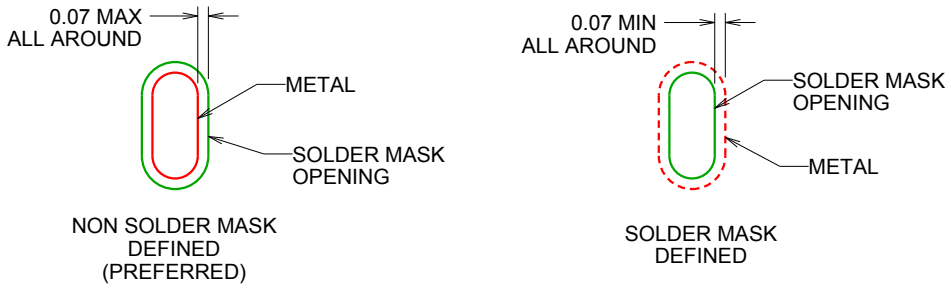


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:8X

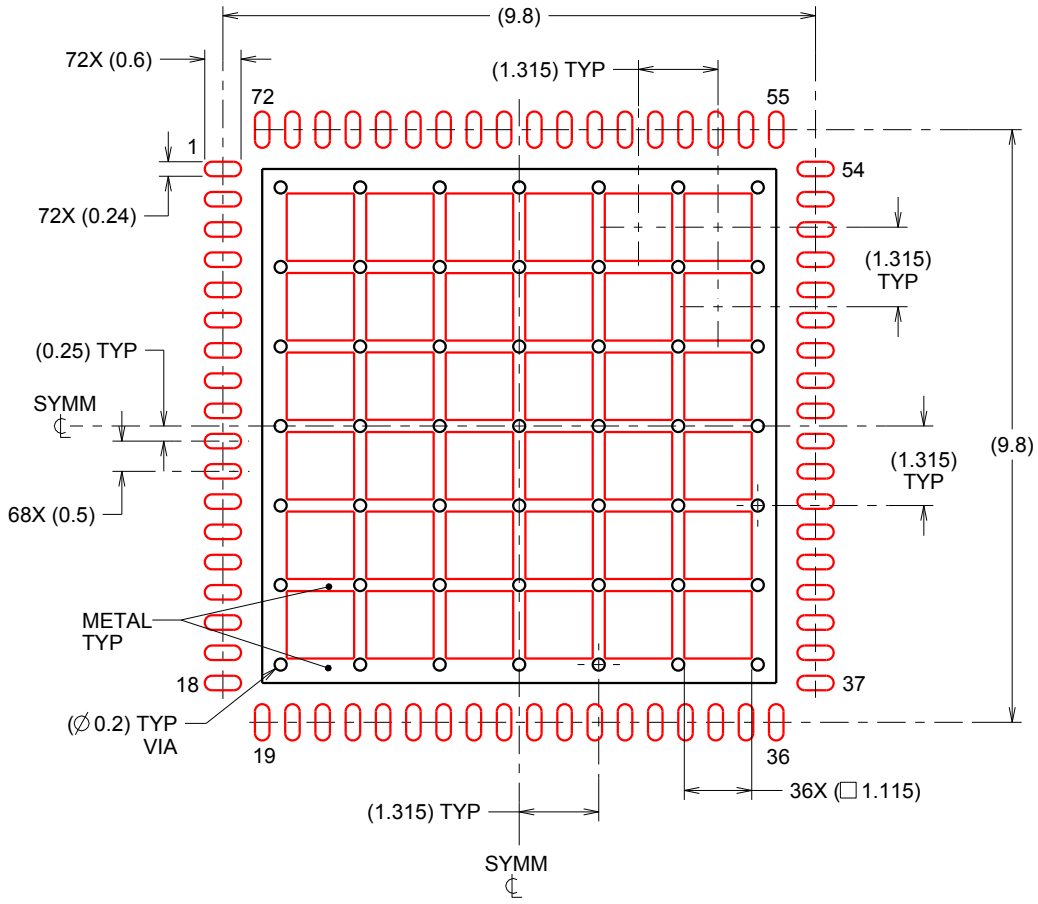


SOLDER MASK DETAILS

4221047/B 02/2014

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
62% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

4221047/B 02/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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