ADS42JBx9 双通道、14 和 16 位、250MSPS 模数转换器

1 特性

- 双通道 ADC
- 14 和 16 位分辨率
- 最大时钟速率：250MSPS
- JESD204B 串口
  - 与子类别 0，1，2 兼容
  - 高达 3.125Gbps
  - 支持两路和四路信道
- 具有高阻抗输入的模拟输入缓冲器
- 灵活的输入时钟缓冲器：
  1，2 和 4 分频
- 差分满量程输入：$2V_{PP}$和 $2.5V_{PP}$
  （寄存器可编程）
- 封装：9mm x 9mm 超薄四方扁平无引线 (VQFN)-64
- 功率耗散：每通道 850mW
- 间隙抖动：85 $f_s$rms
- 内部抖动
- 通道隔离：100dB
- 性能：
  - 2 V_{PP}，-1 dBFS 时，$f_{输入}$ = 170MHz
    - 信噪比 (SNR)：73.3dBFS
    - 无杂散动态范围 (SFRD)：对于二次谐波 (HD2)，三次谐波 (HD3) 为 93dBc
    - SFDR：对于非 HD2，HD3 为 100dBc
  - 2.5 V_{PP}，-1 dBFS 时，$f_{输入}$ = 170MHz
    - SNR：74.7dBFS
    - SFDR：对于 HD2，HD3 为 89dBc
      对于非 HD2，HD3 为 95dBc

2 应用

- 通信和线缆基础设施
- 多载波、多模蜂窝接收器
- 雷达和智能天线阵列
- 宽带无线
- 测试和测量仪器
- 软件定义的和多样性射频
- 微波和双通道 I/O 接收器
- 集线器
- 功率放大器线性化

3 说明

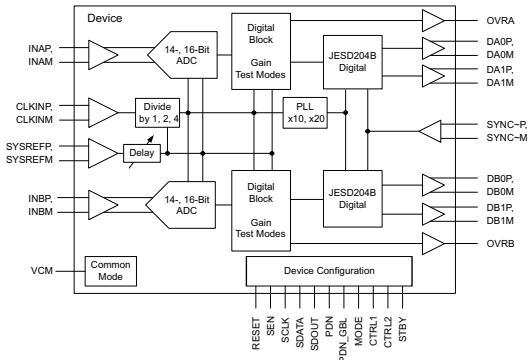
ADS42JB69 和 ADS42JB49 是高线性、双通道，16 和 14 位，250MSPS，模数转换器 (ADC)。 这些器件支持 JESD204B 串口，数据速率高达 3.125Gbps。 经缓冲的模拟输入在大大降低采样保持毛刺脉冲能量的同时，在宽频率范围内提供统一的输入阻抗，这使得它可以轻松地将模拟输入驱动至极高输入频率。 采样时钟分频器可实现更灵活的系统时钟架构设计。 此器件采用内部抖动算法以在宽输入频率范围内提供出色的无杂散动态范围 (SFDR)。

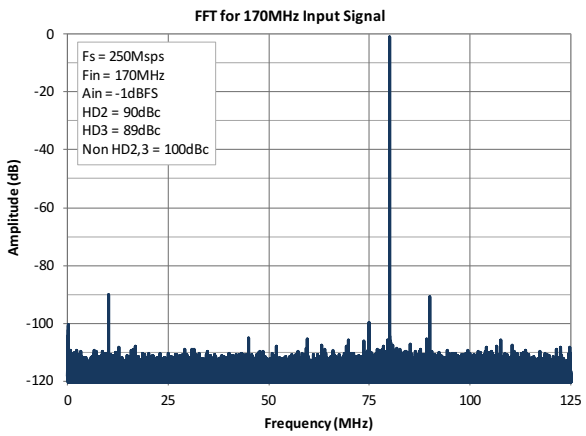
器件信息(1)

器件型号	封装	接口选项
ADS42JB49	VQFN (64)	14 位 DDR 或 QDR LVDS
		14 位 JESD204B
ADS42JB69	VQFN (64)	16 位 DDR 或 QDR LVDS
		16 位 JESD204B

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图





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4 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (August 2013) to Revision F — **Page**

- 已将格式更改为符合最新的数据表标准 ... 1
- 已添加 *ESD 额定值*表和*特性描述*、*器件功能模式*、*应用和实施*、*电源相关建议*、*布局*、*器件和文档支持*以及*机械、封装和可订购信息*部分 ... 1
- Changed title of Device Comparison Table ... 4
- Changed title of Pin Functions table ... 5
- Deleted Ordering Information table ... 6
- Corrected names of registers 10h, 11h, 12h, and 13h in Table 13 ... 41

Changes from Revision D (August 2013) to Revision E — **Page**

- 已更改 文档状态至生产数据 ... 1

Changes from Revision C (July 2013) to Revision D — **Page**

- 更新了首页方框图 ... 1
- Changed 2-V_{PP} Full-Scale *INL* maximum specification in ADS42JB49 Electrical Characteristics table ... 9

Changes from Revision B (July 2013) to Revision C — **Page**

- 已添加 特性部分中的内部抖动 ... 1
- 已更改 从“此器件提供出色的”改为“此器件采用内部抖动算法以提供” ... 1
- Changed 2-V_{PP} Full-Scale *INL* maximum specification in ADS42JB69 Electrical Characteristics table ... 8
- Deleted 2.5-V_{PP} Full-Scale *INL* maximum specification in ADS42JB69 Electrical Characteristics table ... 8

- Changed 2-V_{PP} Full-Scale *INL* maximum specification in ADS42JB49 Electrical Characteristics table 9
- Deleted 2.5-V_{PP} Full-Scale *INL* maximum specification in ADS42JB49 Electrical Characteristics table 9
- Changed E_{GREF} specifications in General Electrical Characteristics table 10

Changes from Revision A (November 2012) to Revision B **Page**

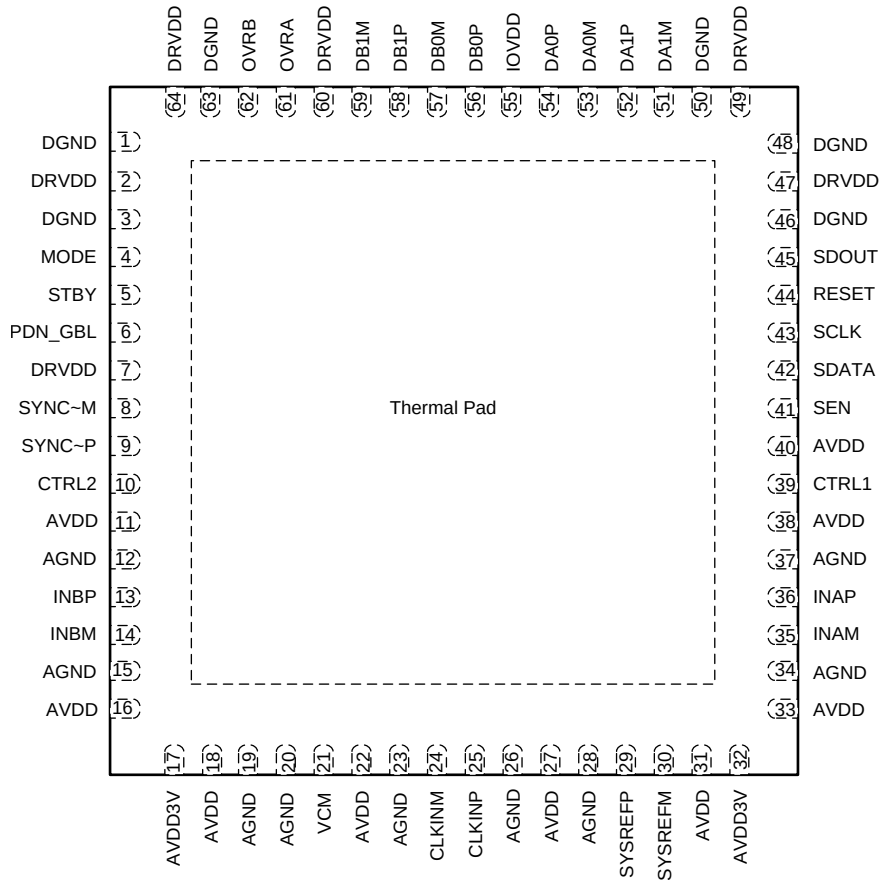
- 已更改 文档状态至混合状态..... 1

5 Device Comparison Table

INTERFACE OPTION	14-BIT, 160 MSPS	14-BIT, 250 MSPS	16-BIT, 250 MSPS
DDR or QDR LVDS	—	ADS42LB49	ADS42LB69
JESD204B	ADS42JB46	ADS42JB49	ADS42JB69

6 Pin Configuration and Functions

RGC Package
VQFN-64
(Top View)



Pin Functions: JESD204B Output Interface

PIN		I/O	FUNCTION	DESCRIPTION
NAME	NO.			
AGND	12, 15, 19, 20, 23, 26, 28, 34, 37	I	Supply	Analog ground
AVDD	11, 16, 18, 22, 27, 31, 33, 38, 40	I	Supply	1.8-V analog power supply
AVDD3V	17, 32	I	Supply	3.3-V analog supply for analog buffer
CLKINM	24	I	Clock	Differential ADC clock input
CLKINP	25	I	Clock	Differential ADC clock input
CTRL1	39	I	Control	Power-down control with an internal 150-kΩ pull-down resistor
CTRL2	10	I	Control	Power-down control with an internal 150-kΩ pull-down resistor
DA0P/M	54, 53	O	Interface	JESD204B serial data output for channel A, lane 0
DA1P/M	52,51	O	Interface	JESD204B serial data output for channel A, lane 1
DB0P/M	56,57	O	Interface	JESD204B serial data output for channel B, lane 0
DB1P/M	58,59	O	Interface	JESD204B serial data output for channel B, lane 1
DGND	1, 3, 46, 48, 50, 63	I	Supply	Digital ground
DRVDD	2, 7, 47, 49, 60, 64	I	Supply	Digital 1.8-V power supply
INAM	35	I	Input	Differential analog input for channel A
INAP	36	I	Input	Differential analog input for channel A
INBM	14	I	Input	Differential analog input for channel B
INBP	13	I	Input	Differential analog input for channel B
IOVDD	55	I	Supply	Digital 1.8-V power supply for the JESD204B transmitter
MODE	4	I	Control	Connect to GND
OVRA	61	O	Interface	Overrange indication channel A in CMOS output format.
OVRB	62	O	Interface	Overrange indication channel B in CMOS output format.
PDN_GBL	6	I	Control	Global power down. Active high with an internal 150-kΩ pull-down resistor.
RESET	44	I	Control	Hardware reset; active high. This pin has an internal 150-kΩ pull-down resistor.
SCLK	43	I	Control	Serial interface clock input. This pin has an internal 150-kΩ pull-down resistor.
SDATA	42	I	Control	Serial interface data input. This pin has an internal 150-kΩ pull-down resistor.
SDOUT	45	O	Control	Serial interface data output
SEN	41	I	Control	Serial interface enable. This pin has an internal 150-kΩ pull-up resistor.
STBY	5	I	Control	Standby. Active high with an internal 150-kΩ pull-down resistor.
SYNC~P	9	I	Interface	Synchronization input for JESD204B port
SYNC~M	8	I	Interface	Synchronization input for JESD204B port
SYSREFM	30	I	Clock	External SYSREF input (subclass 1)
SYSREFP	29	I	Clock	External SYSREF input (subclass 1)
VCM	21	O	Output	1.9-V common-mode output voltage for analog inputs
Thermal pad	—	GND	Ground	Connect to ground plane

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	AVDD3V	–0.3	3.6	V
	AVDD	–0.3	2.1	V
	DRVDD	–0.3	2.1	V
	IOVDD	–0.3	2.1	V
Voltage between AGND and DGND		–0.3	0.3	V
Voltage applied to input pins	INAP, INBP, INAM, INBM	–0.3	3	V
	CLKINP, CLKINM	–0.3	minimum (2.1, AVDD + 0.3)	V
	SYNC~P, SYNC~M	–0.3	minimum (2.1, AVDD + 0.3)	V
	SYSREFP, SYSREFM	–0.3	minimum (2.1, AVDD + 0.3)	V
	SCLK, SEN, SDATA, RESET, PDN_GBL, CTRL1, CTRL2, STBY, MODE	–0.3	3.9	V
Temperature	Operating free-air, T_A	–40	+85	°C
	Operating junction, T_J		+125	°C
	Storage, T_{stg}	–65	+150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
SUPPLIES						
AVDD	Analog supply voltage		1.7	1.8	1.9	V
AVDD3V	Analog buffer supply voltage		3.15	3.3	3.45	V
DRVDD	Digital supply voltage		1.7	1.8	1.9	V
IOVDD	Output buffer supply voltage		1.7	1.8	1.9	V
ANALOG INPUTS						
V_{ID}	Differential input voltage range	Default after reset		2		V_{PP}
		Register programmable(2)		2.5		V_{PP}
V_{ICR}	Input common-mode voltage			VCM ± 0.025		V
	Maximum analog input frequency with 2.5-V_{PP} input amplitude			250		MHz
	Maximum analog input frequency with 2-V_{PP} input amplitude			400		MHz
CLOCK INPUT						
	Input clock sample rate	10x mode	60		250	MSPS
		20x mode	40		156.25	MSPS
	Input clock amplitude differential ($V_{CLKP} - V_{CLKM}$)	Sine wave, ac-coupled	0.3(3)	1.5		V_{PP}
		LVPECL, ac-coupled		1.6		V_{PP}
		LVDS, ac-coupled		0.7		V_{PP}
		LVCMOS, single-ended, ac-coupled		1.5		V
	Input clock duty cycle		35%	50%	65%	
DIGITAL OUTPUTS						
C_{LOAD}	Maximum external load capacitance from each output pin to DRGND			3.3		pF
R_{LOAD}	Single-ended load resistance			+50		Ω
T_A	Operating free-air temperature		–40		+85	°C

(1) After power-up, to reset the device for the first time, use the RESET pin only. Refer to the *Register Initialization* section.
(2) For details, refer to the *Digital Gain* section.
(3) Refer to the *Performance vs Clock Amplitude* curves, Figure 28 and Figure 29.

7.4 Thermal Information

THERMAL METRIC(1)		ADS42JBx9 RGC (QFN) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	22.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	7.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	2.5	
ψ_{JT}	Junction-to-top characterization parameter	0.1	
ψ_{JB}	Junction-to-board characterization parameter	2.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics: ADS42JB69 (16-Bit)

Typical values are at T_A = +25°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, and sampling rate = 250 MSPS, unless otherwise noted. Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, and IOVDD = 1.8 V.

PARAMETER		TEST CONDITIONS	2-V_{PP} FULL-SCALE			2.5-V_{PP} FULL-SCALE			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz		74			75.9		dBFS
		f_{IN} = 70 MHz		73.8			75.6		dBFS
		f_{IN} = 170 MHz	70.8	73.3			74.7		dBFS
		f_{IN} = 230 MHz		72.6			74		dBFS
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		73.9			75.7		dBFS
		f_{IN} = 70 MHz		73.7			75.3		dBFS
		f_{IN} = 170 MHz	69.6	73.2			74.5		dBFS
		f_{IN} = 230 MHz		72.2			73.1		dBFS
SFDR	Spurious-free dynamic range (including second and third harmonic distortion)	f_{IN} = 10 MHz		95			90		dBc
		f_{IN} = 70 MHz		91			88		dBc
		f_{IN} = 170 MHz	81	93			89		dBc
		f_{IN} = 230 MHz		84			82		dBc
THD	Total harmonic distortion	f_{IN} = 10 MHz		92			88		dBc
		f_{IN} = 70 MHz		89			86		dBc
		f_{IN} = 170 MHz	78	91			86		dBc
		f_{IN} = 230 MHz		82			80		dBc
HD2	2nd-order harmonic distortion	f_{IN} = 10 MHz		95			95		dBc
		f_{IN} = 70 MHz		91			88		dBc
		f_{IN} = 170 MHz	81	93			94		dBc
		f_{IN} = 230 MHz		84			82		dBc
HD3	3rd-order harmonic distortion	f_{IN} = 10 MHz		95			90		dBc
		f_{IN} = 70 MHz		96			93		dBc
		f_{IN} = 170 MHz	81	94			89		dBc
		f_{IN} = 230 MHz		86			84		dBc
	Worst spur (other than second and third harmonics)	f_{IN} = 10 MHz		102			102		dBc
		f_{IN} = 70 MHz		103			103		dBc
		f_{IN} = 170 MHz	87	100			95		dBc
		f_{IN} = 230 MHz		99			93		dBc
IMD	Two-tone intermodulation distortion	f_1 = 46 MHz, f_2 = 50 MHz, each tone at –7 dBFS		97			95		dBFS
		f_1 = 185 MHz, f_2 = 190 MHz, each tone at –7 dBFS		90			89		dBFS
	Crosstalk	20-MHz, full-scale signal on channel under observation; 170-MHz, full-scale signal on other channel		100			100		dB
	Input overload recovery	Recovery to within 1% (of full-scale) for 6-dB overload with sine-wave input		1			1		Clock cycle
PSRR	AC power-supply rejection ratio	For 50-mV_{PP} signal on AVDD supply, up to 10 MHz		> 40			> 40		dB
ENOB	Effective number of bits	f_{IN} = 170 MHz		11.9			12.1		LSBs
DNL	Differential nonlinearity	f_{IN} = 170 MHz		±0.6			±0.6		LSBs
INL	Integrated nonlinearity	f_{IN} = 170 MHz		±3	±8		±3.5		LSBs

7.6 Electrical Characteristics: ADS42JB49 (14-Bit)

Typical values are at T_A = +25°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, and sampling rate = 250 MSPS, unless otherwise noted. Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, and IOVDD = 1.8 V.

PARAMETER		TEST CONDITIONS	2-V_{PP} FULL-SCALE			2.5-V_{PP} FULL-SCALE			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz		73.4			75		dBFS
		f_{IN} = 70 MHz		73.2			74.7		dBFS
		f_{IN} = 170 MHz	69.5	72.7			74		dBFS
		f_{IN} = 230 MHz		72.2			73.4		dBFS
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		73.3			74.8		dBFS
		f_{IN} = 70 MHz		73.1			74.5		dBFS
		f_{IN} = 170 MHz	68.5	72.7			73.8		dBFS
		f_{IN} = 230 MHz		71.8			72.6		dBFS
SFDR	Spurious-free dynamic range (including second and third harmonic distortion)	f_{IN} = 10 MHz		95			90		dBc
		f_{IN} = 70 MHz		91			88		dBc
		f_{IN} = 170 MHz	79	93			89		dBc
		f_{IN} = 230 MHz		84			82		dBc
THD	Total harmonic distortion	f_{IN} = 10 MHz		92			88		dBc
		f_{IN} = 70 MHz		89			86		dBc
		f_{IN} = 170 MHz	76	90			86		dBc
		f_{IN} = 230 MHz		82			80		dBc
HD2	2nd-order harmonic distortion	f_{IN} = 10 MHz		95			95		dBc
		f_{IN} = 70 MHz		91			88		dBc
		f_{IN} = 170 MHz	79	93			94		dBc
		f_{IN} = 230 MHz		84			82		dBc
HD3	3rd-order harmonic distortion	f_{IN} = 10 MHz		95			90		dBc
		f_{IN} = 70 MHz		96			93		dBc
		f_{IN} = 170 MHz	79	94			89		dBc
		f_{IN} = 230 MHz		86			84		dBc
	Worst spur (other than second and third harmonics)	f_{IN} = 10 MHz		102			102		dBc
		f_{IN} = 70 MHz		103			103		dBc
		f_{IN} = 170 MHz	87	101			95		dBc
		f_{IN} = 230 MHz		99			93		dBc
IMD	Two-tone intermodulation distortion	f_1 = 46 MHz, f_2 = 50 MHz, each tone at –7 dBFS		97			95		dBFS
		f_1 = 185 MHz, f_2 = 190 MHz, each tone at –7 dBFS		90			89		dBFS
	Crosstalk	20-MHz, full-scale signal on channel under observation; 170-MHz, full-scale signal on other channel		100			100		dB
	Input overload recovery	Recovery to within 1% (of full-scale) for 6-dB overload with sine-wave input		1			1		Clock cycle
PSRR	AC power-supply rejection ratio	For a 50-mV_{PP} signal on AVDD supply, up to 10 MHz		> 40			> 40		dB
ENOB	Effective number of bits	f_{IN} = 170 MHz		11.8			12		LSBs
DNL	Differential nonlinearity	f_{IN} = 170 MHz		±0.15			±0.15		LSBs
INL	Integrated nonlinearity	f_{IN} = 170 MHz		±0.75	±3		±0.9		LSBs

7.7 Electrical Characteristics: General

Typical values are at +25°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, and sampling rate = 250 MSPS, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, and IOVDD = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
V_{ID}	Differential input voltage range	Default (after reset)		2		V_{PP}
		Register programmed (1)		2.5		V_{PP}
		Differential input resistance (at 170 MHz)		1.2		kΩ
		Differential input capacitance (at 170 MHz)		4		pF
	Analog input bandwidth	With 50-Ω source impedance, and 50-Ω termination		900		MHz
VCM	Common-mode output voltage			1.9		V
	VCM output current capability			10		mA
DC ACCURACY						
	Offset error		–20		20	mV
E_{GREF}	Gain error as a result of internal reference inaccuracy alone			±2		%FS
E_{GCHAN}	Gain error of channel alone			–5		%FS
	Temperature coefficient of E_{GCHAN}			0.01		Δ%/°C
POWER SUPPLY						
IAVDD	Analog supply current			128	160	mA
IAVDD3V	Analog buffer supply current			290	330	mA
IDRVDD	Digital supply current			228	252	mA
IOVDD	Output buffer supply current	50-Ω external termination from pin to IOVDD, f_{IN} = 2.5 MHz		60	100	mA
	Analog power			231		mW
	Analog buffer power			957		mW
	Digital power			410		mW
	Power consumption by output buffer	50-Ω external termination from pin to IOVDD, f_{IN} = 2.5 MHz		109		mW
	Total power			1.7	1.96	W
	Global power-down				160	mW

(1) Refer to the *Serial Interface* section.

7.8 Digital Characteristics

The dc specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level '0' or '1'. AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, and IOVDD = 1.8 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS (RESET, SCLK, SEN, SDATA, PDN_GBL, STBY, CTRL1, CTRL2, MODE)(1)						
	High-level input voltage	All digital inputs support 1.8-V and 3.3-V logic levels	1.2			V
	Low-level input voltage	All digital inputs support 1.8-V and 3.3-V logic levels			0.4	V
	High-level input current	SEN		0		µA
		RESET, SCLK, SDATA, PDN_GBL, STBY, CTRL1, CTRL2, MODE		10		µA
	Low-level input current	SEN		10		µA
		RESET, SCLK, SDATA, PDN_GBL, STBY, CTRL1, CTRL2, MODE		0		µA
DIGITAL INPUTS (SYNC~P, SYNC~M, SYSREFP, SYSREFM)						
	High-level input voltage			1.3		V
	Low-level input voltage			0.5		V
V_{CM_DIG}	Input common-mode voltage			0.9		V
DIGITAL OUTPUTS (SDOUT, OVRA, OVRB)						
	High-level output voltage		DRVDD – 0.1	DRVDD		V
	Low-level output voltage				0.1	V
DIGITAL OUTPUTS (JESD204B Interface: DA[0,1], DB[0,1])(2)						
	High-level output voltage			IOVDD		V
	Low-level output voltage			IOVDD – 0.4		V
$\lvert V_{OD} \rvert$	Output differential voltage			0.4		V
V_{OCM}	Output common-mode voltage			IOVDD – 0.2		V
	Transmitter short-circuit current	Transmitter terminals shorted to any voltage between –0.25 V and 1.45 V	–100		100	mA
	Single-ended output impedance			50		Ω
	Output capacitance	Output capacitance inside the device, from either output to ground		2		pF

(1) RESET, SCLK, SDATA, PDN_GBL, STBY, CTRL1, CTRL2 and MODE pins have 150-kΩ (typical) internal pull-down resistor to ground, while SEN pin has 150-kΩ (typical) pull-up resistor to AVDD.
(2) 50-Ω, single-ended external termination to IOVDD.

7.9 Timing Characteristics

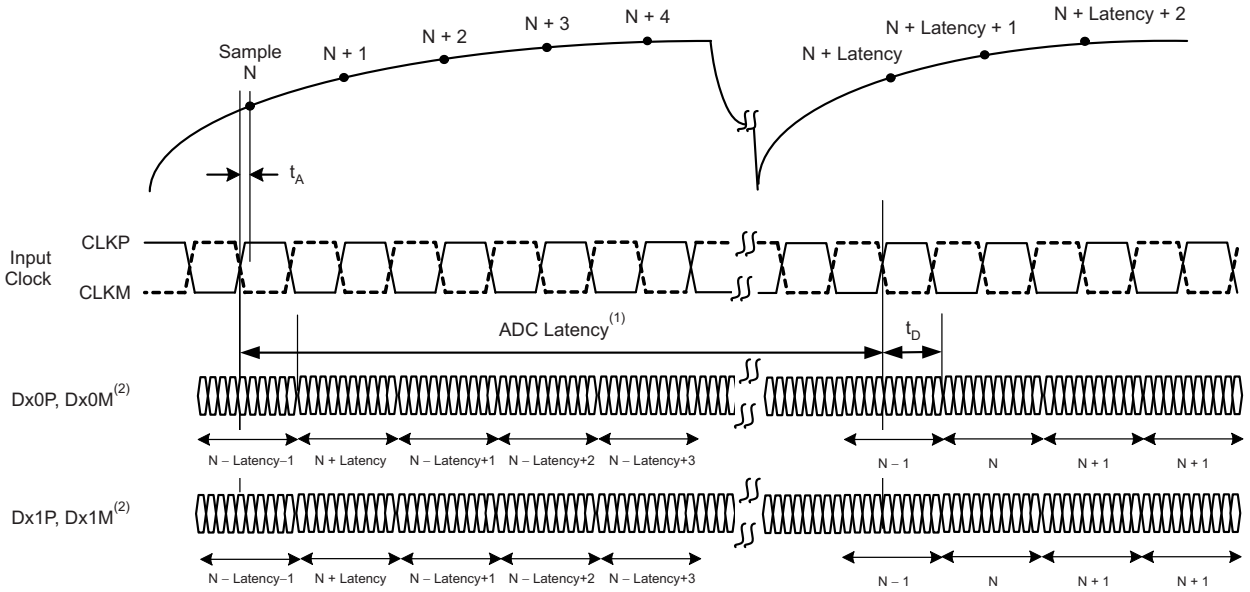
Typical values are at +25°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, and sampling rate = 250 MSPS, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, and IOVDD = 1.8 V. See Figure 1.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SAMPLE TIMING CHARACTERISTICS						
	Aperture delay		0.4	0.7	1.1	ns
	Aperture delay matching	Between two channels on the same device		±70		ps
		Between two devices at the same temperature and supply voltage		±150		ps
	Aperture jitter			85		f_S rms
	Wake-up time	Time to valid data after coming out of STANDBY mode		50	200	µs
		Time to valid data after coming out of global power-down		250	1000	µs
$t_{SU\_SYNC\sim}$	Setup time for SYNC~	Referenced to input clock rising edge	400			ps
$t_{H\_SYNC\sim}$	Hold time for SYNC~	Referenced to input clock rising edge	100			ps
t_{SU_SYSREF}	Setup time for SYSREF	Referenced to input clock rising edge	400			ps
t_{H_SYSREF}	Hold time for SYSREF	Referenced to input clock rising edge	100			ps
CML OUTPUT TIMING CHARACTERISTICS						
	Unit interval		320		1667	ps
	Serial output data rate				3.125	Gbps
	Total jitter	2.5 Gbps (10x mode, f_S = 250 MSPS)		0.28		$_{P-P}$UI
		3.125 Gbps (20x mode, f_S = 156.25 MSPS)		0.3		$_{P-P}$UI
t_R, t_F	Data rise time, data fall time	Rise and fall times measured from 20% to 80%, differential output waveform, 600 Mbps ≤ bit rate ≤ 3.125 Gbps		105		ps

Table 1. Latency in Different Modes(1)(2)

MODE	PARAMETER	LATENCY (N Cycles)	TYPICAL DATA DELAY (t_D, ns)
10x	ADC latency	23	0.65 × t_S + 3
	Normal OVR latency	14	6.7
	Fast OVR latency	9	6.7
	from SYNC~ falling edge to CGS phase(3)	16	0.65 × t_S + 3
	from SYNC~ rising edge to ILA sequence(4)	25	0.65 × t_S + 3
20x	ADC latency	22	0.85 × t_S + 3
	Normal OVR latency	14	6.7
	Fast OVR latency	9	6.7
	from SYNC~ falling edge to CGS phase(3)	15	0.85 × t_S + 3
	from SYNC~ rising edge to ILA sequence(4)	16	0.85 × t_S + 3

(1) Overall latency = latency + t_D.
(2) t_S is the time period of the ADC conversion clock.
(3) Latency is specified for subclass 2. In subclass 0, the SYNC~ falling edge to CGS phase latency is 16 clock cycles in 10x mode and 15 clock cycles in 20x mode.
(4) Latency is specified for subclass 2. In subclass 0, the SYNC~ rising edge to ILA sequence latency is 11 clock cycles in 10x mode and 11 clock cycles in 20x mode.



(1) Overall latency = ADC latency + t_D.

(2) x = A for channel A and B for channel B.

Figure 1. ADC Latency

7.10 Typical Characteristics: ADS42JB69

Typical values are at T_A = +25°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

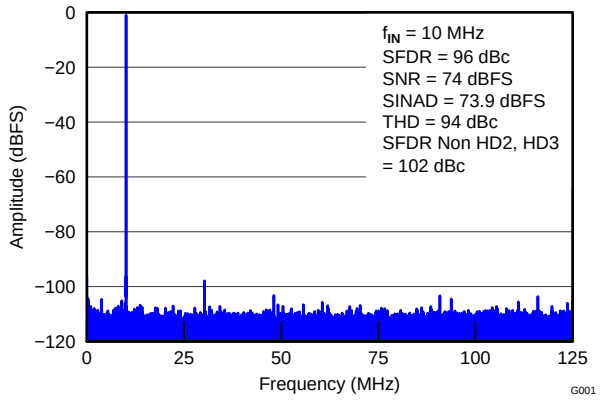


Figure 2. FFT for 10-MHz Input Signal

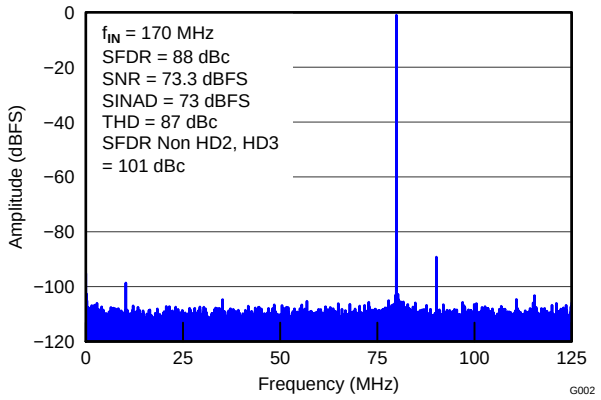


Figure 3. FFT for 170-MHz Input Signal

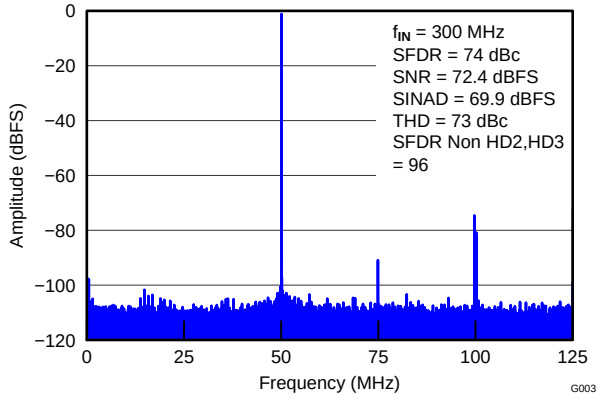


Figure 4. FFT for 300-MHz Input Signal

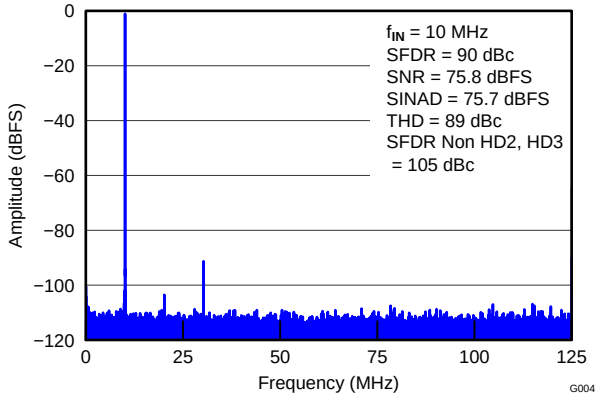


Figure 5. FFT for 10-MHz Input Signal (2.5-V_{PP} Full-Scale)

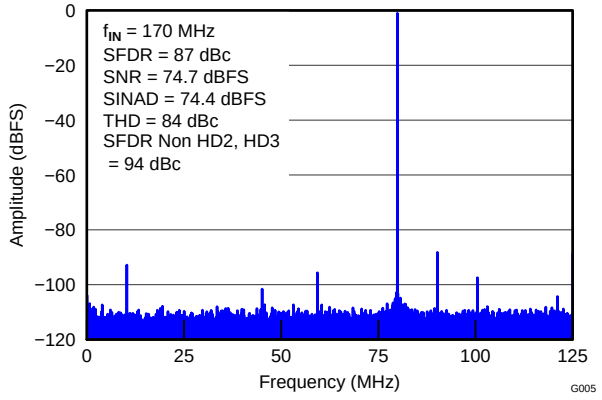


Figure 6. FFT for 170-MHz Input Signal (2.5-V_{PP} Full-Scale)

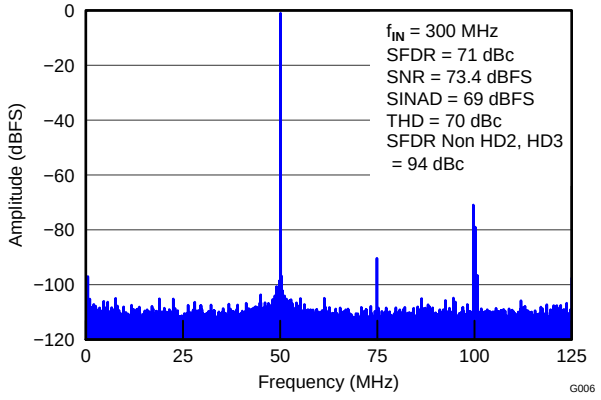


Figure 7. FFT for 300-MHz Input Signal (2.5-V_{PP} Full-Scale)

Typical Characteristics: ADS42JB69 (continued)

Typical values are at T_A = +25°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

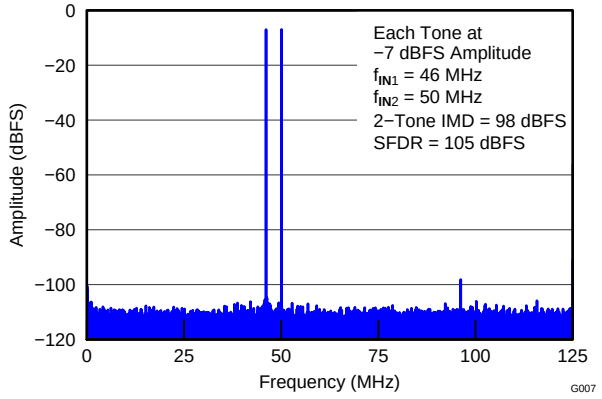


Figure 8. FFT for Two-Tone Input Signal (–7 dBFS at 46 MHz and 50 MHz)

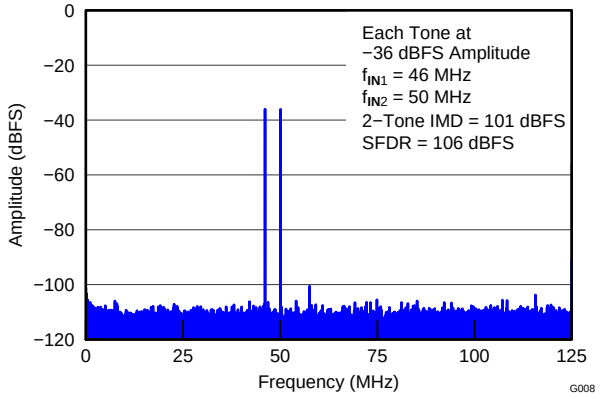


Figure 9. FFT for Two-Tone Input Signal (–36 dBFS at 46 MHz and 50 MHz)

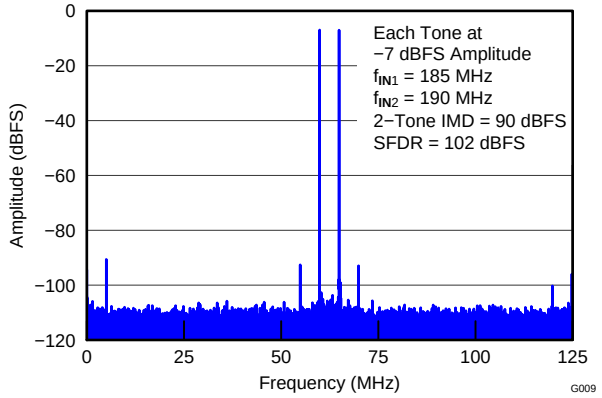


Figure 10. FFT for Two-Tone Input Signal (–7 dBFS at 185 MHz and 190 MHz)

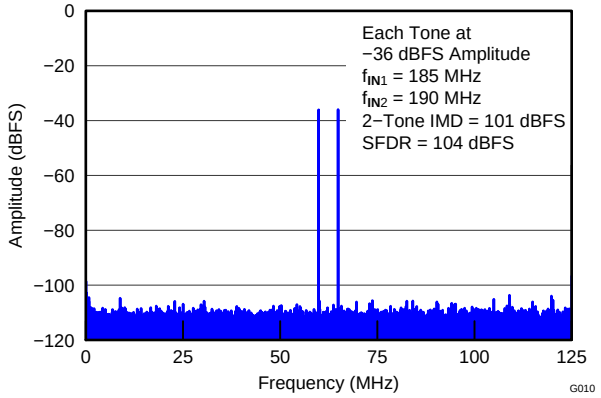


Figure 11. FFT for Two-Tone Input Signal (–36 dBFS at 185 MHz and 190 MHz)

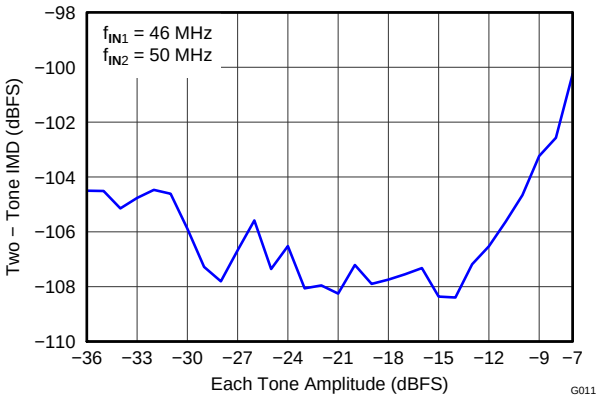


Figure 12. Intermodulation Distortion vs Input Amplitude (46 MHz and 50 MHz)

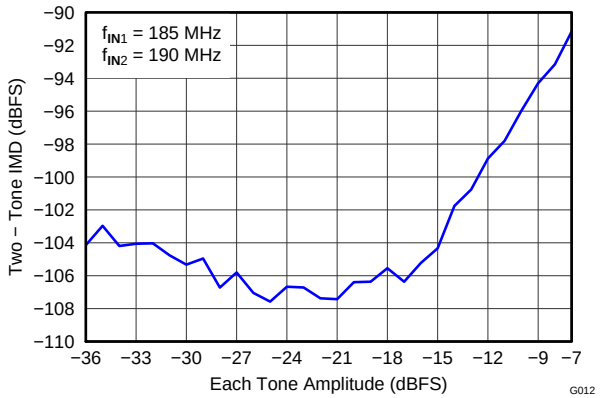


Figure 13. Intermodulation Distortion vs Input Amplitude (185 MHz and 190 MHz)

Typical Characteristics: ADS42JB69 (continued)

Typical values are at T_A = +25°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

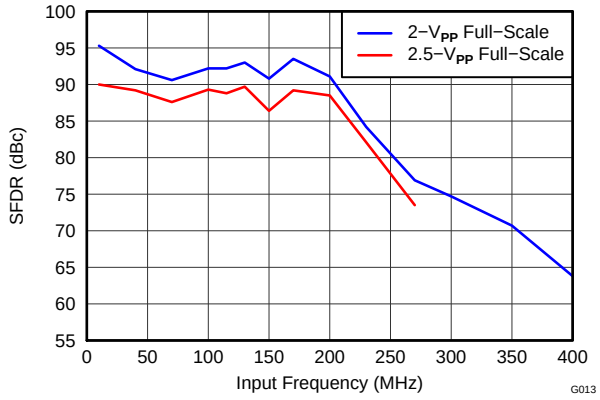


Figure 14. Spurious-Free Dynamic Range vs Input Frequency

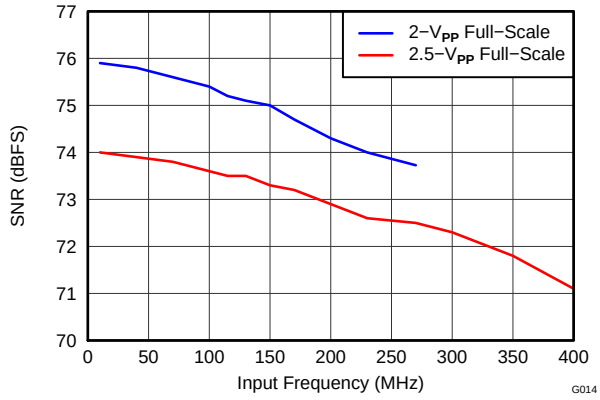


Figure 15. Signal-to-Noise Ratio vs Input Frequency

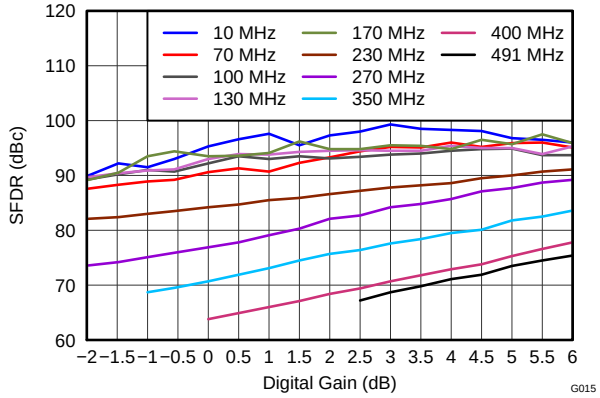


Figure 16. Spurious-Free Dynamic Range vs Digital Gain

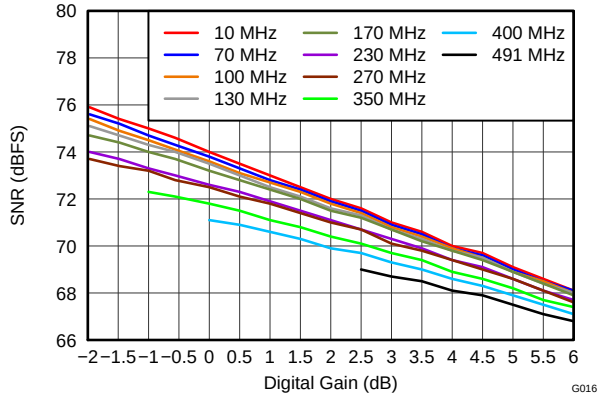


Figure 17. Signal-to-Noise Ratio vs Digital Gain

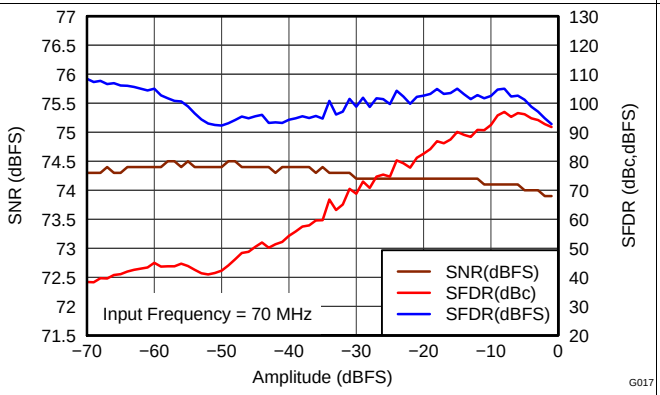


Figure 18. Performance vs Input Amplitude (70 MHz)

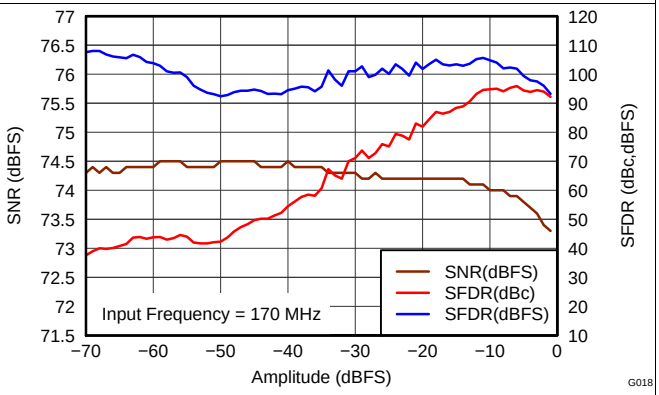


Figure 19. Performance vs Input Amplitude (170 MHz)

Typical Characteristics: ADS42JB69 (continued)

Typical values are at T_A = +25°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

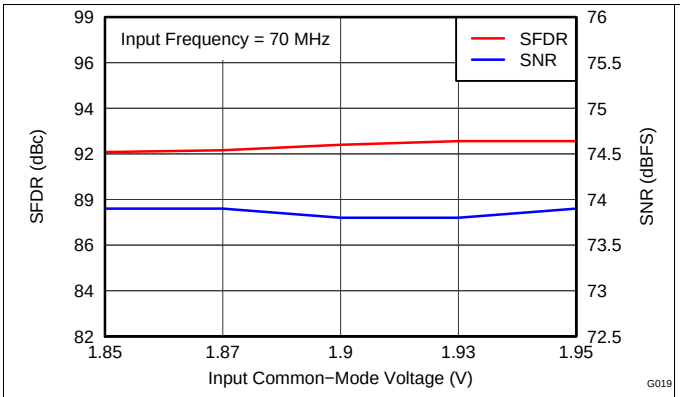


Figure 20. Performance vs Input Common-Mode Voltage (70 MHz)

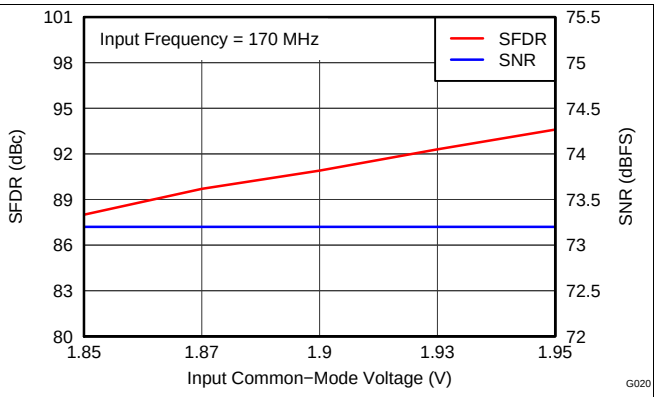


Figure 21. Performance vs Input Common-Mode Voltage (170 MHz)

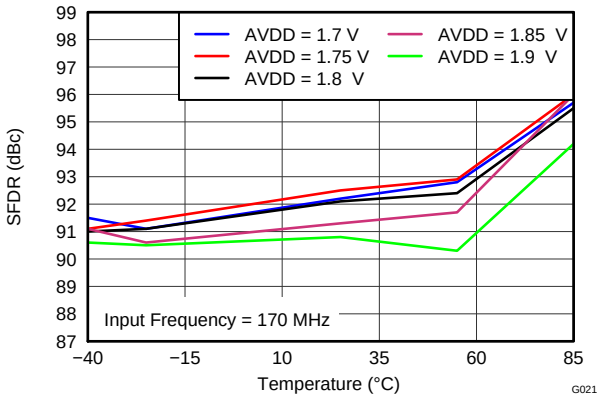


Figure 22. Spurious-Free Dynamic Range vs AVDD Supply and Temperature (170 MHz)

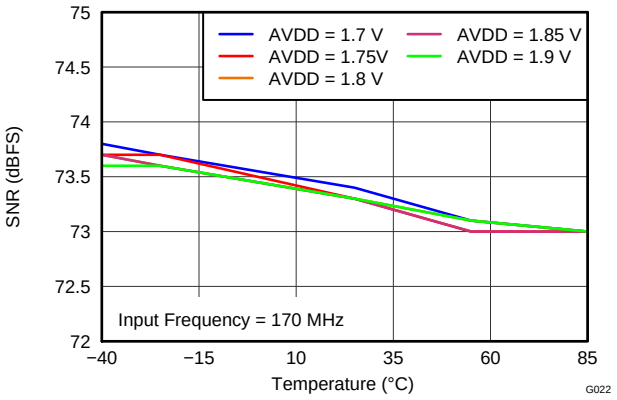


Figure 23. Signal-to-Noise Ratio vs AVDD Supply and Temperature (170 MHz)

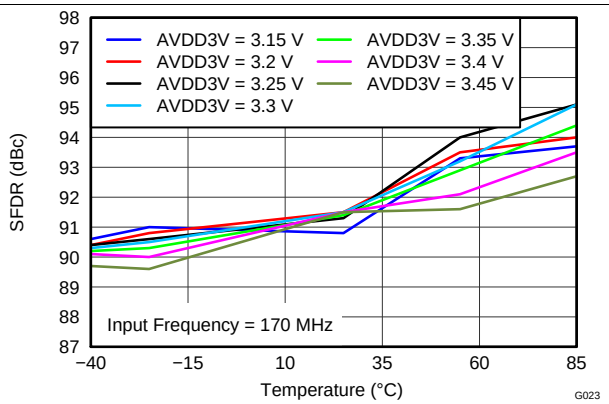


Figure 24. Spurious-free Dynamic Range vs AVDD_BUF Supply and Temperature (170 MHz)

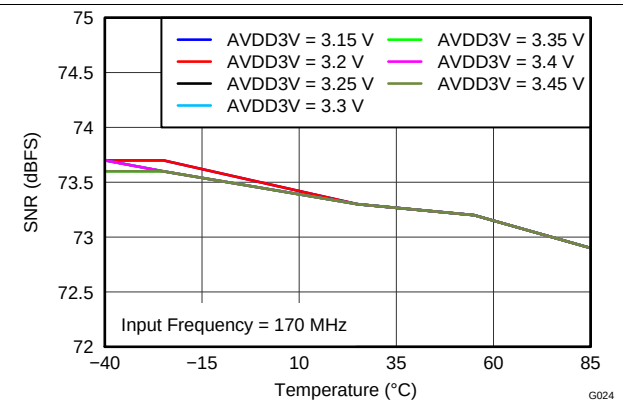


Figure 25. Signal-to-Noise Ratio vs AVDD_BUF Supply and Temperature (170 MHz)

Typical Characteristics: ADS42JB69 (continued)

Typical values are at T_A = +25°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

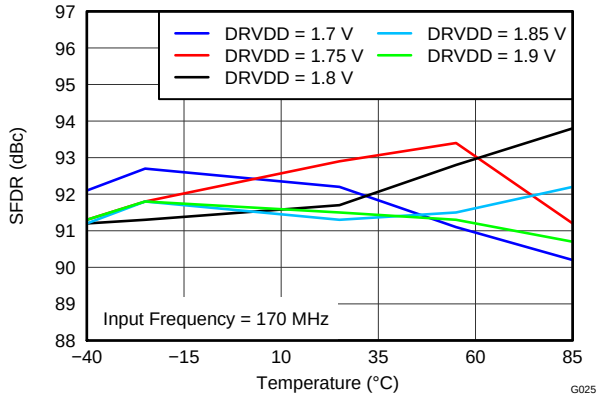


Figure 26. Spurious-Free Dynamic Range vs DRVDD Supply and Temperature (170 MHz)

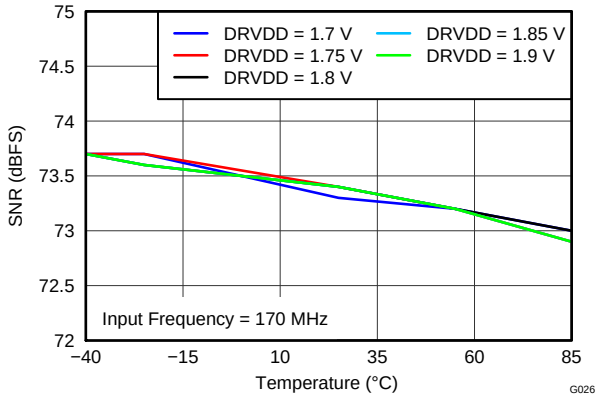


Figure 27. Signal-to-Noise Ratio vs DRVDD Supply and Temperature (170 MHz)

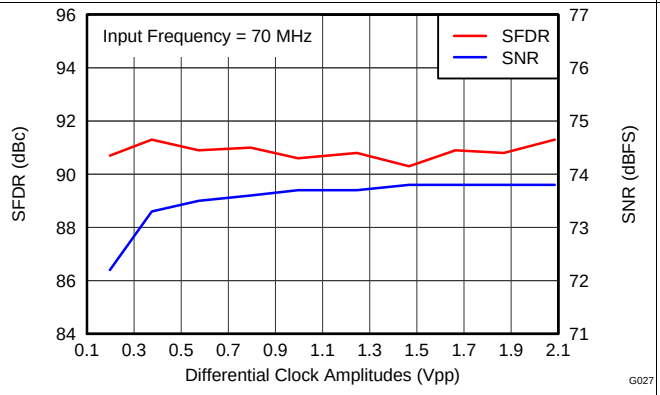


Figure 28. Performance vs Clock Amplitude (70 MHz)

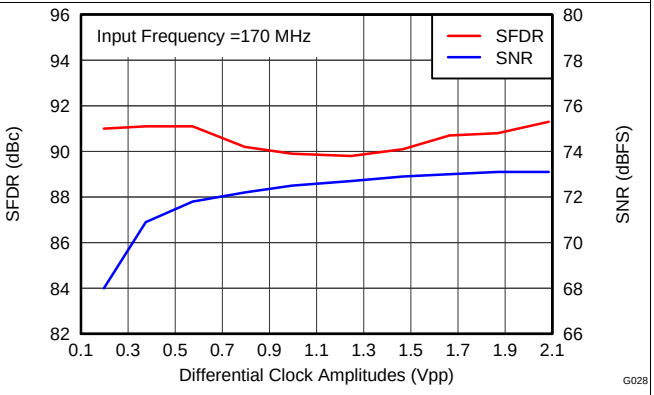


Figure 29. Performance vs Clock Amplitude (170 MHz)

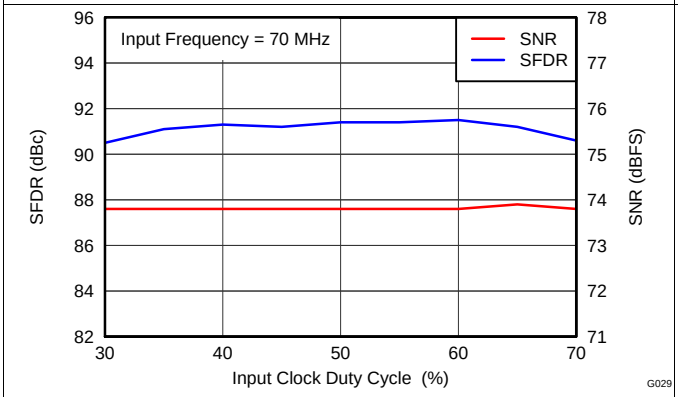


Figure 30. Performance vs Clock Duty Cycle (70 MHz)

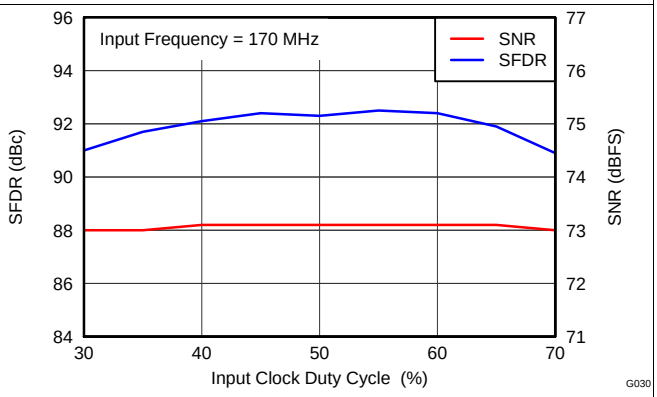


Figure 31. Performance vs Clock Duty Cycle (170 MHz)

7.11 Typical Characteristics: ADS42JB49

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

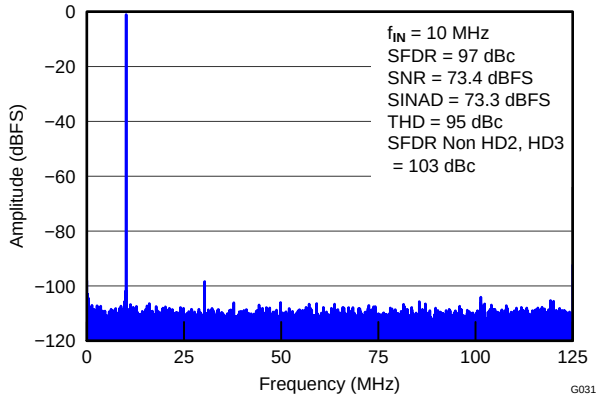


Figure 32. FFT for 10-MHz Input Signal

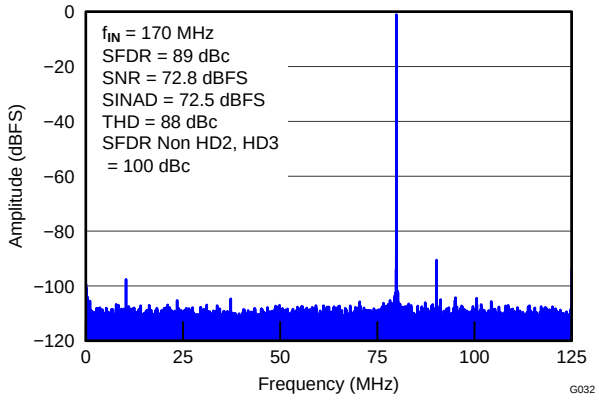


Figure 33. FFT for 170-MHz Input Signal

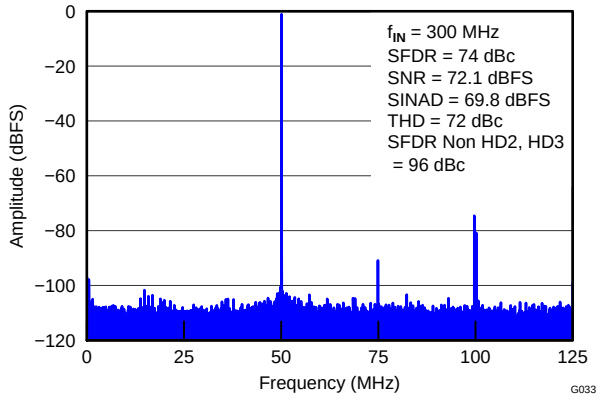


Figure 34. FFT for 300-MHz Input Signal

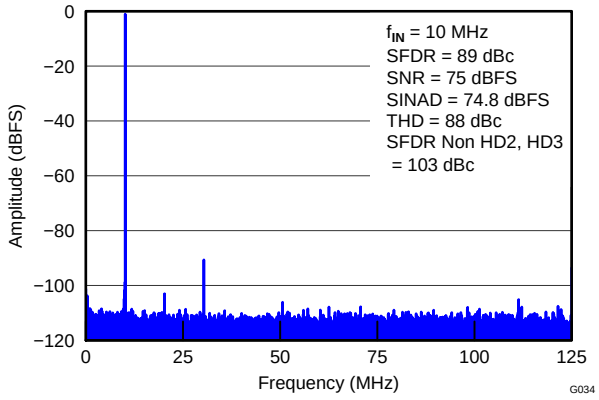


Figure 35. FFT for 10-MHz Input Signal (2.5-V_{PP} Full-Scale)

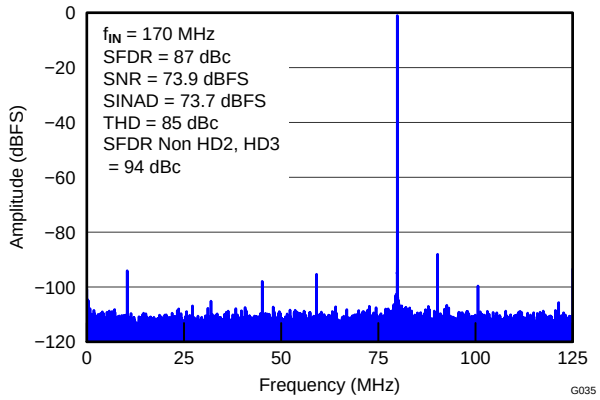


Figure 36. FFT for 170-MHz Input Signal (2.5-V_{PP} Full-Scale)

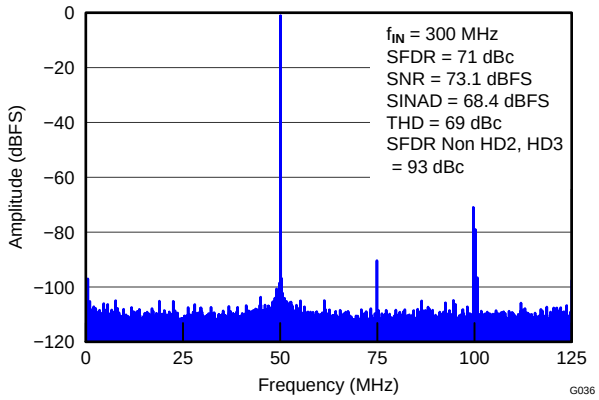


Figure 37. FFT for 300-MHz Input Signal (2.5-V_{PP} Full-Scale)

Typical Characteristics: ADS42JB49 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

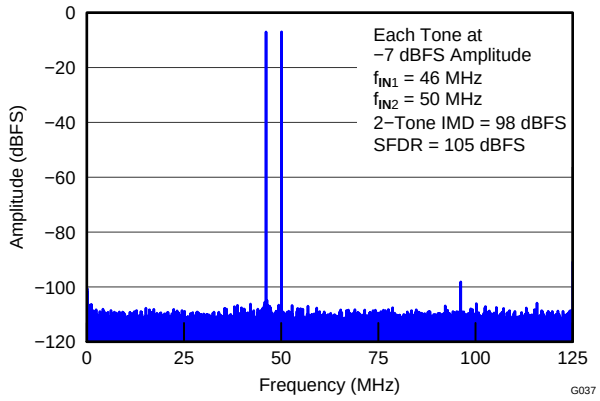


Figure 38. FFT for Two-Tone Input Signal (–7 dBFS at 46 MHz and 50 MHz)

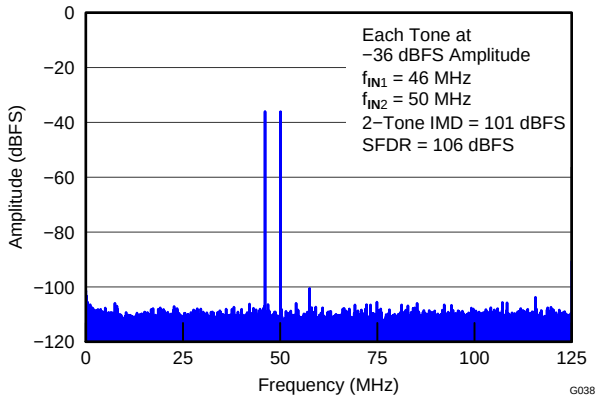


Figure 39. FFT for Two-Tone Input Signal (–36 dBFS at 46 MHz and 50 MHz)

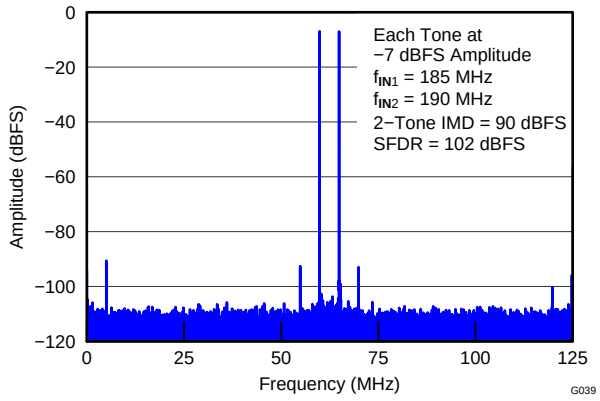


Figure 40. FFT for Two-Tone Input Signal (–7 dBFS at 185 MHz and 190 MHz)

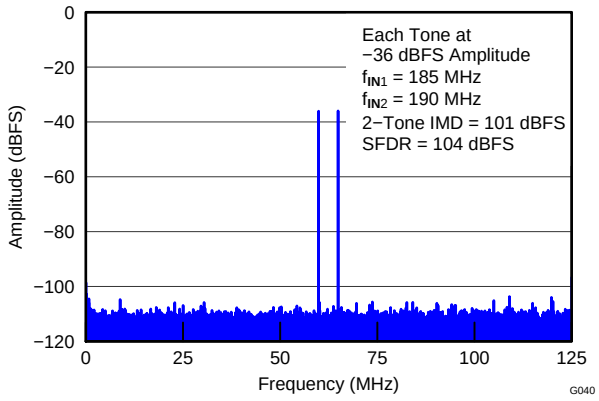


Figure 41. FFT for Two-Tone Input Signal (–36 dBFS at 185 MHz and 190 MHz)

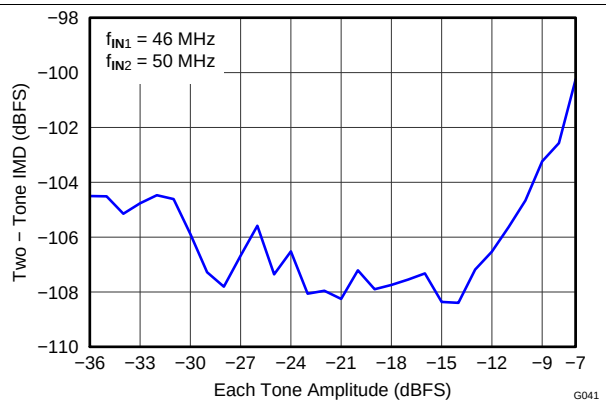


Figure 42. Intermodulation Distortion vs Input Amplitude (46 MHz and 50 MHz)

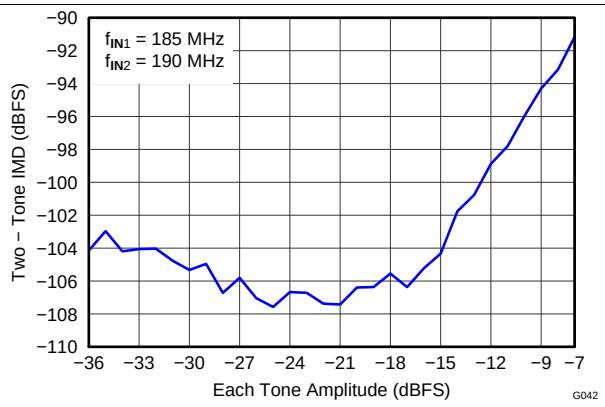


Figure 43. Intermodulation Distortion vs Input Amplitude (185 MHz and 190 MHz)

Typical Characteristics: ADS42JB49 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

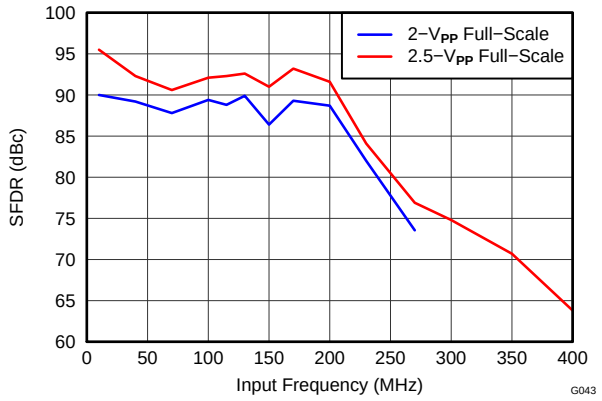


Figure 44. Spurious-Free Dynamic Range vs Input Frequency

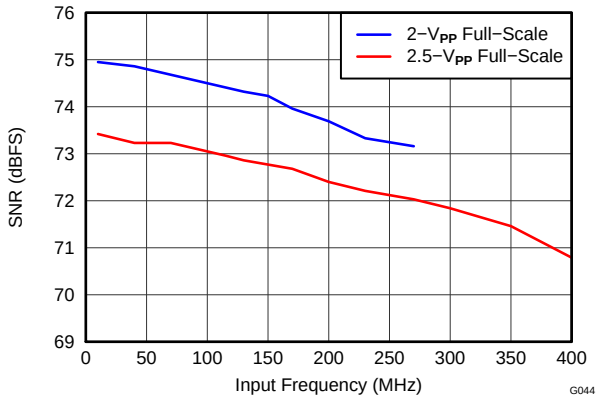


Figure 45. Signal-to-Noise Ratio vs Input Frequency

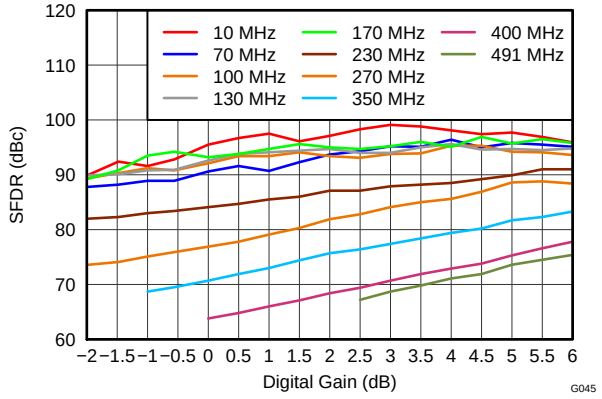


Figure 46. Spurious-Free Dynamic Range vs Digital Gain

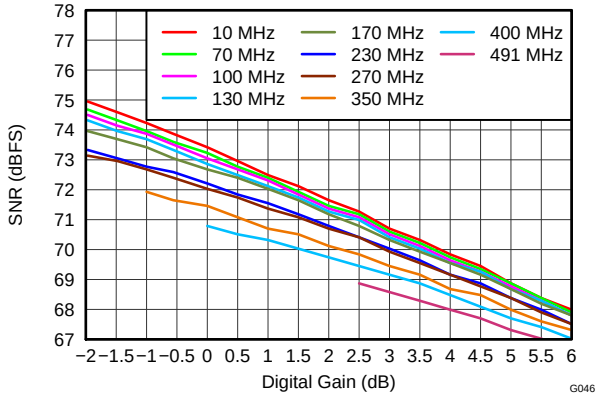


Figure 47. Signal-to-Noise Ratio vs Digital Gain

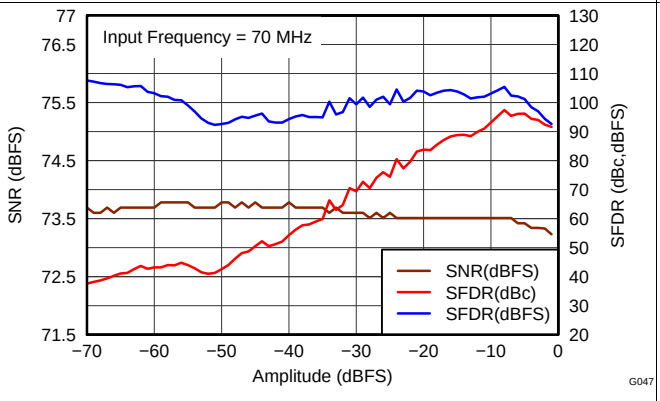


Figure 48. Performance vs Input Amplitude (70 MHz)

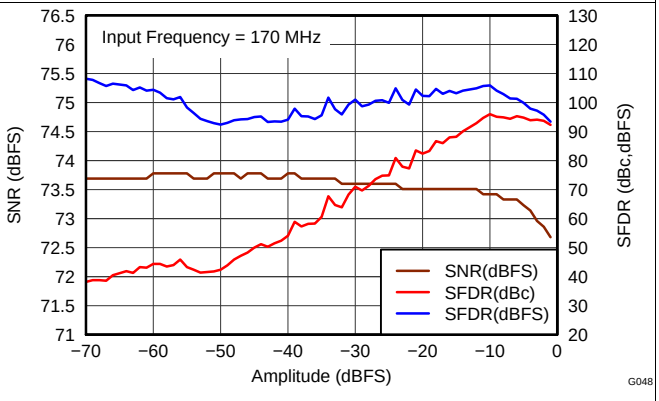


Figure 49. Performance vs Input Amplitude (170 MHz)

Typical Characteristics: ADS42JB49 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

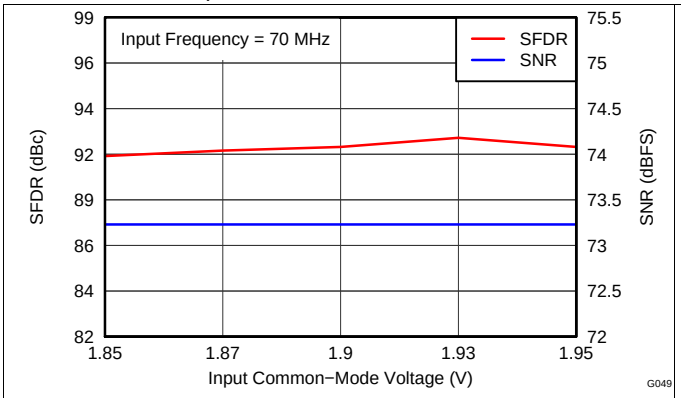


Figure 50. Performance vs Input Common-Mode Voltage (70 MHz)

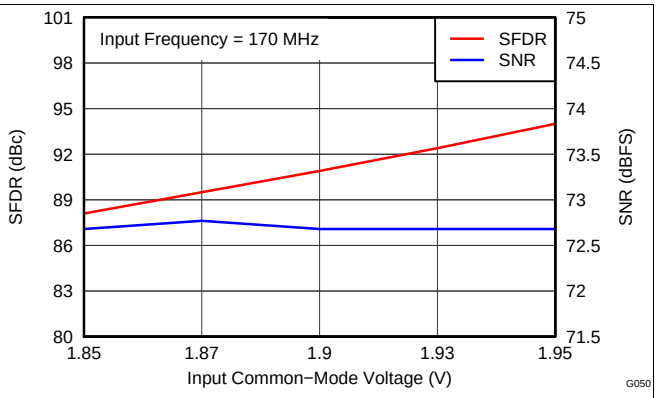


Figure 51. Performance vs Input Common-Mode Voltage (170 MHz)

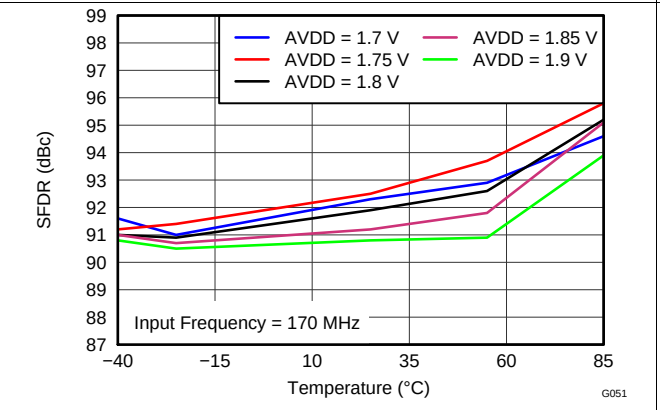


Figure 52. Spurious-Free Dynamic Range vs AVDD Supply and Temperature (170 MHz)

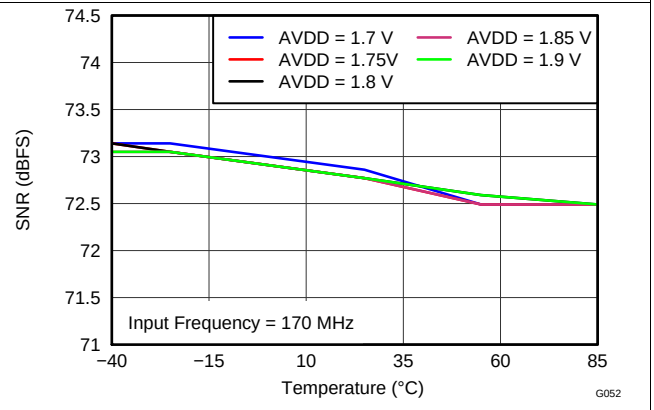


Figure 53. Signal-to-Noise Ratio vs AVDD Supply and Temperature (170 MHz)

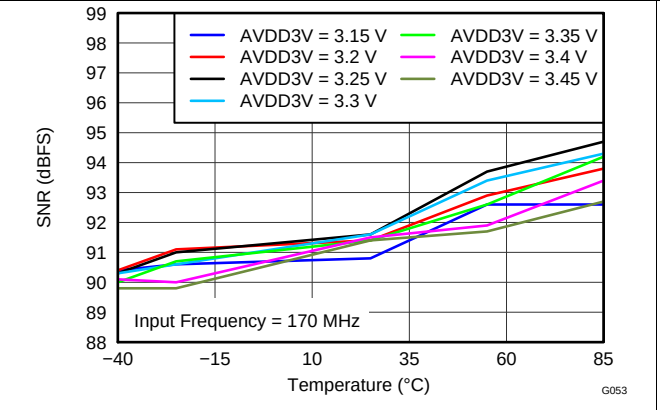


Figure 54. Spurious-Free Dynamic Range vs AVDD_BUF Supply and Temperature (170 MHz)

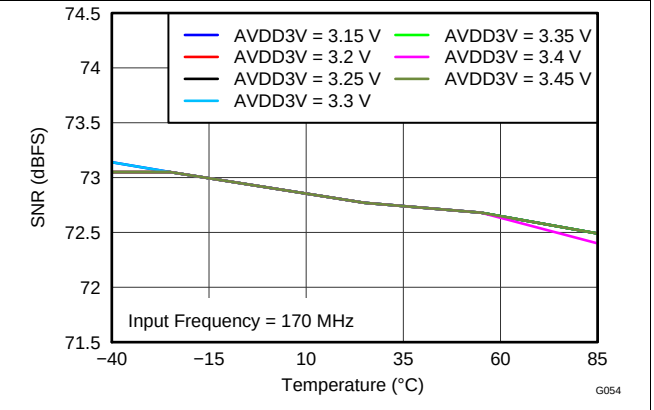


Figure 55. Signal-to-Noise Ratio vs AVDD_BUF Supply and Temperature (170 MHz)

Typical Characteristics: ADS42JB49 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 32k-point FFT, unless otherwise noted.

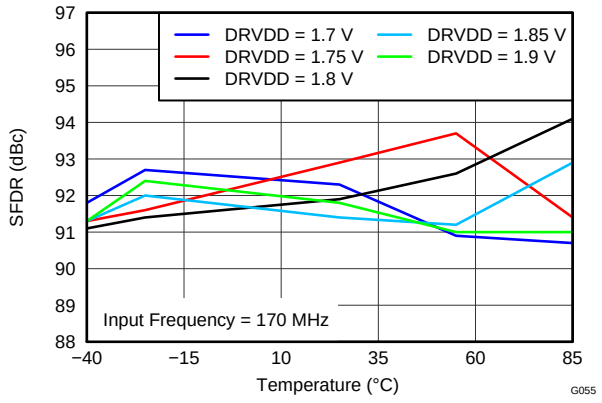


Figure 56. Spurious-Free Dynamic Range vs DRVDD Supply and Temperature (170 MHz)

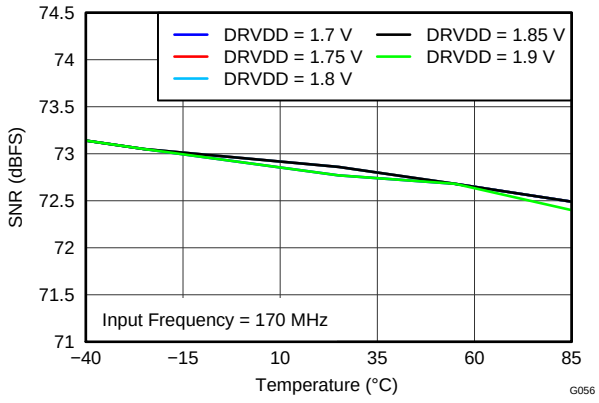


Figure 57. Signal-to-Noise Ratio vs DRVDD Supply and Temperature (170 MHz)

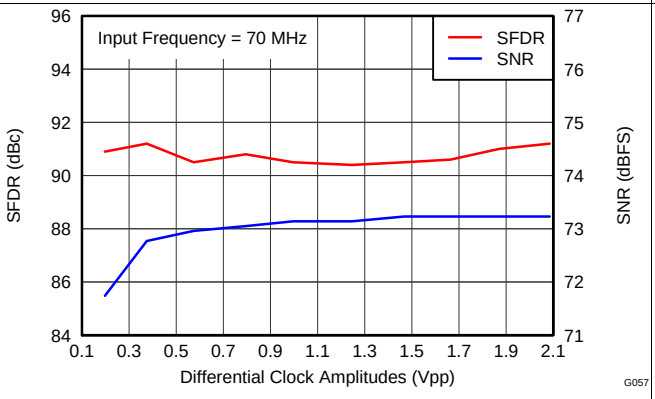


Figure 58. Performance vs Clock Amplitude (70 MHz)

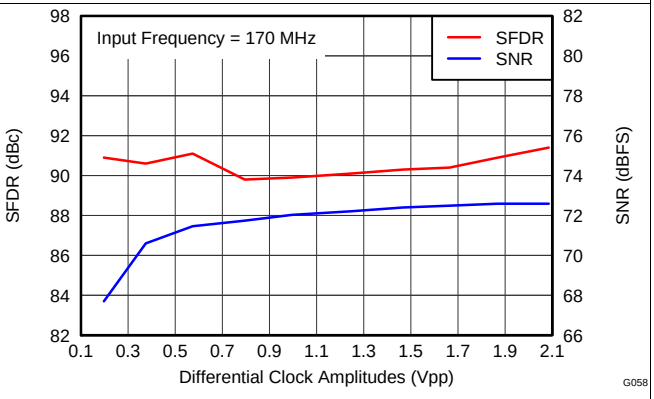


Figure 59. Performance vs Clock Amplitude (170 MHz)

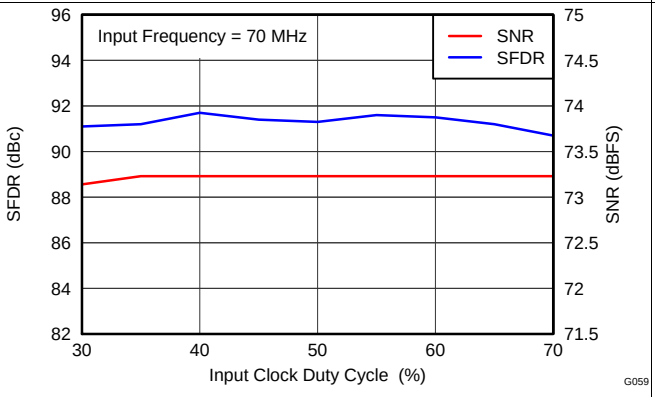


Figure 60. Performance vs Clock Duty Cycle (70 MHz)

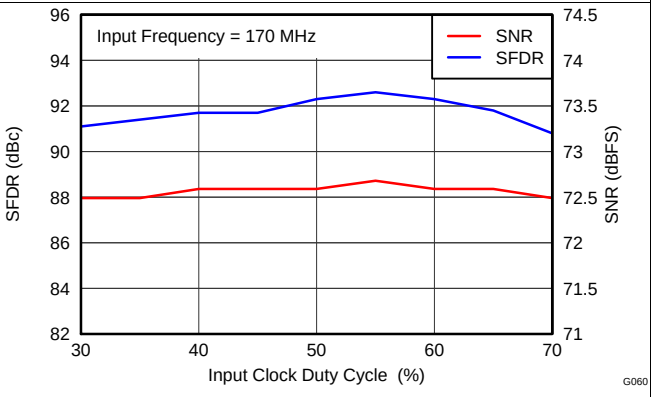


Figure 61. Performance vs Clock Duty Cycle (170 MHz)

7.12 Typical Characteristics: Common

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 64k-point FFT, unless otherwise noted.

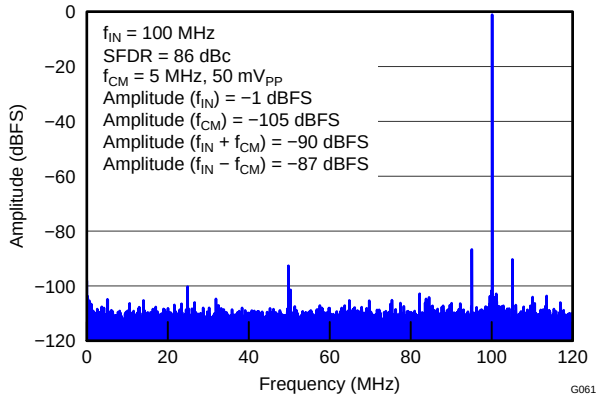


Figure 62. Common-Mode Rejection Ratio FFT

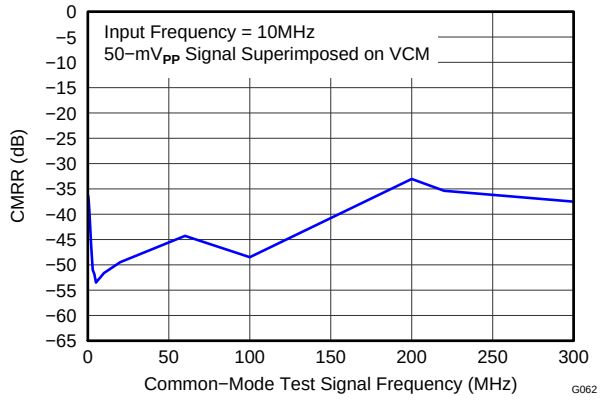


Figure 63. Common-Mode Rejection Ratio vs Test Signal Frequency

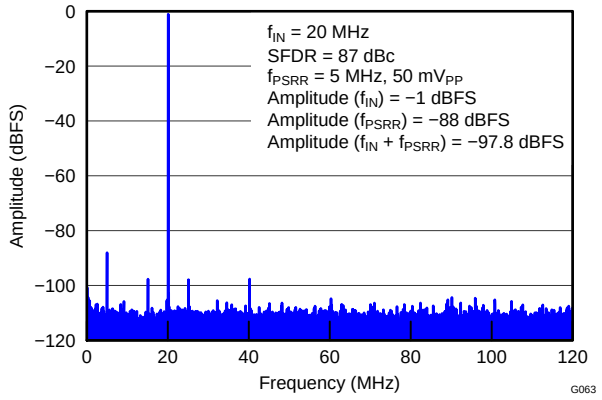


Figure 64. Power-Supply Rejection Ratio FFT for AVDD Supply

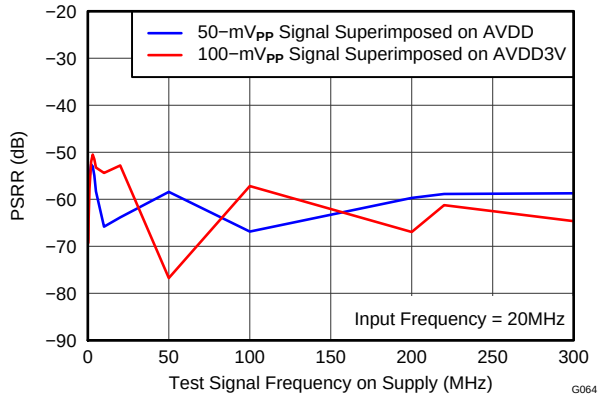


Figure 65. Power-Supply Rejection Ratio vs Test Signal Frequency

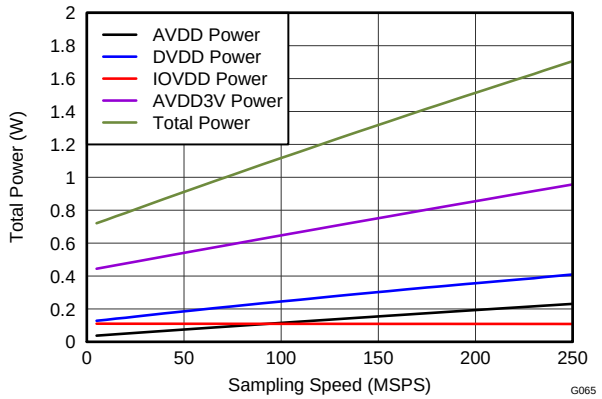


Figure 66. Total Power vs Sampling Frequency

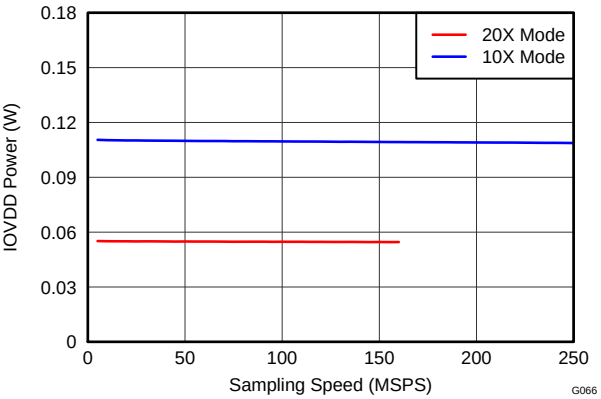


Figure 67. IOVDD Power vs Sampling Frequency

7.13 Typical Characteristics: Contour

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, IOVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, and 64k-point FFT, unless otherwise noted.

7.13.1 Spurious-Free Dynamic Range (SFDR): General

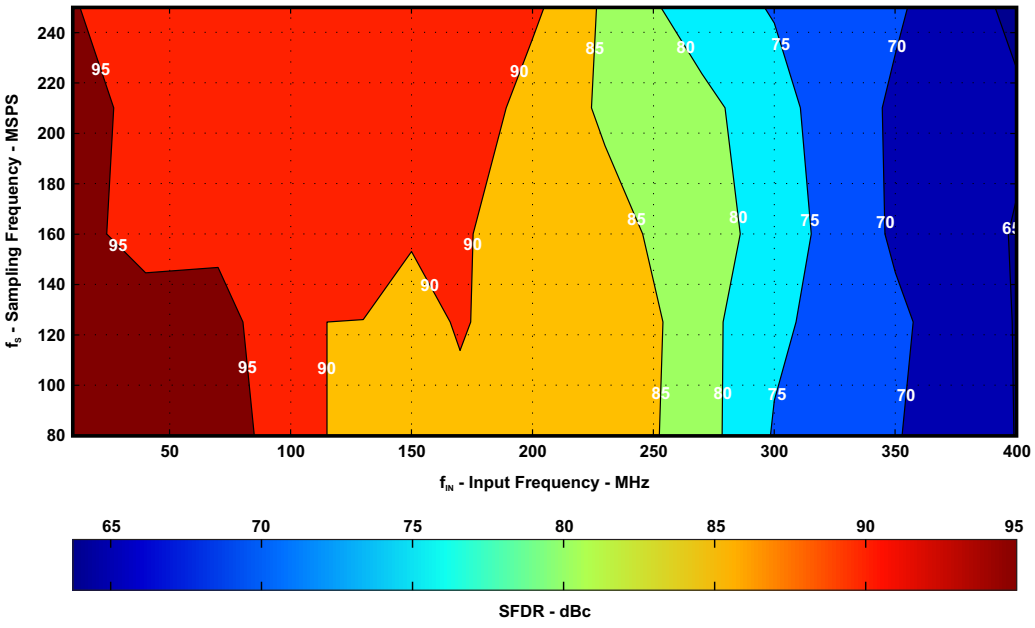


Figure 68. 0-dB Gain (SFDR)

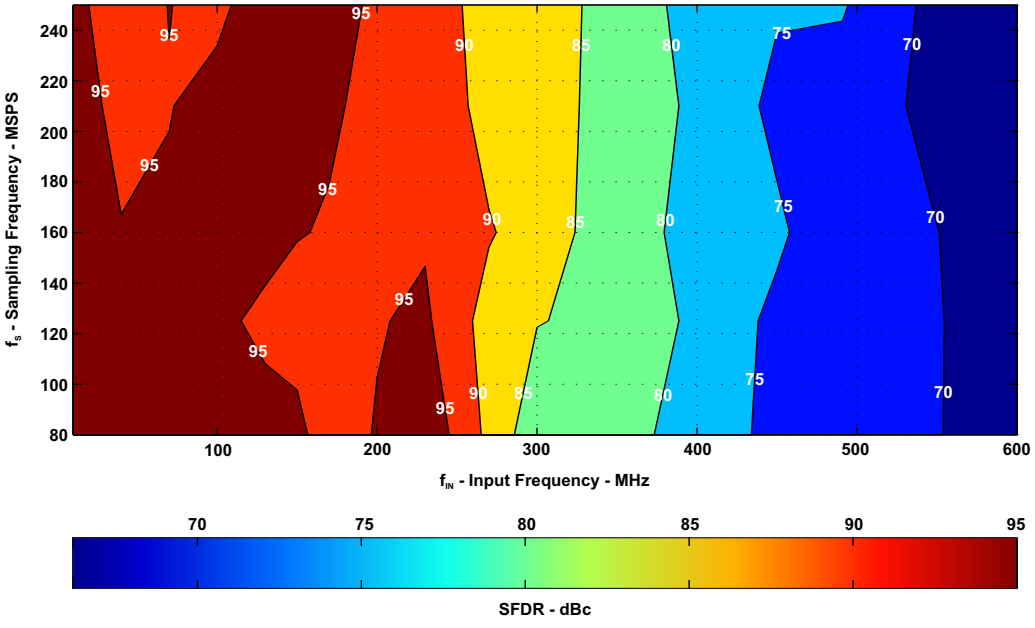


Figure 69. 6-dB Gain (SFDR)

7.13.2 Signal-to-Noise Ratio (SNR): ADS42JB69

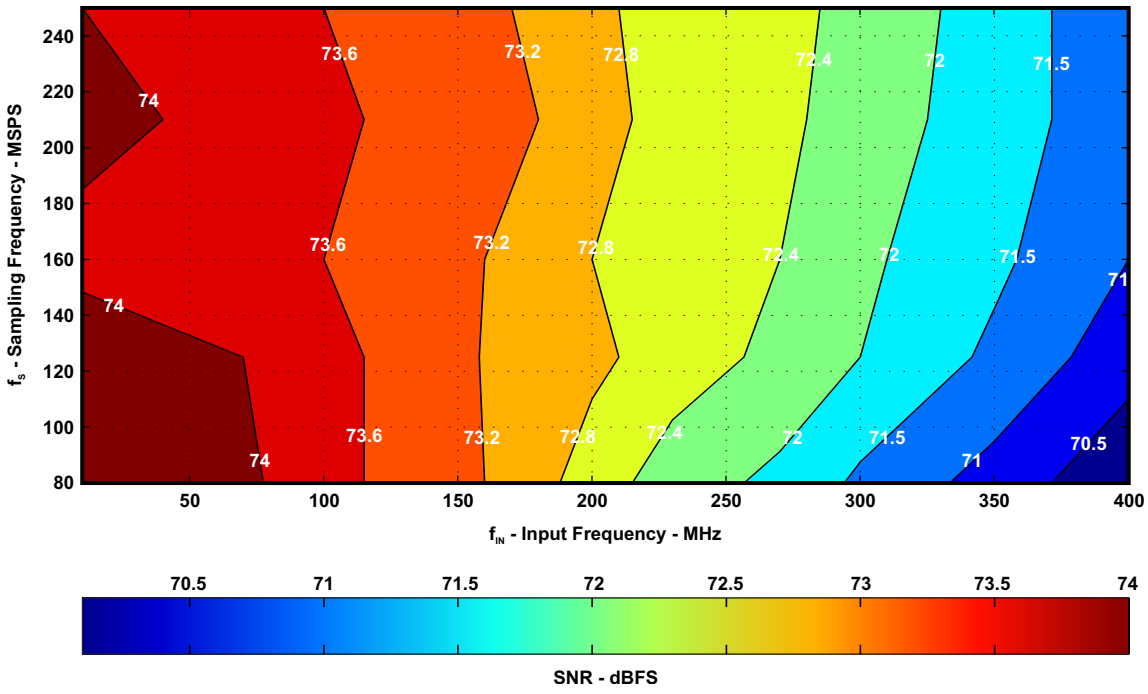


Figure 70. 0-dB Gain (SNR, ADS42JB69)

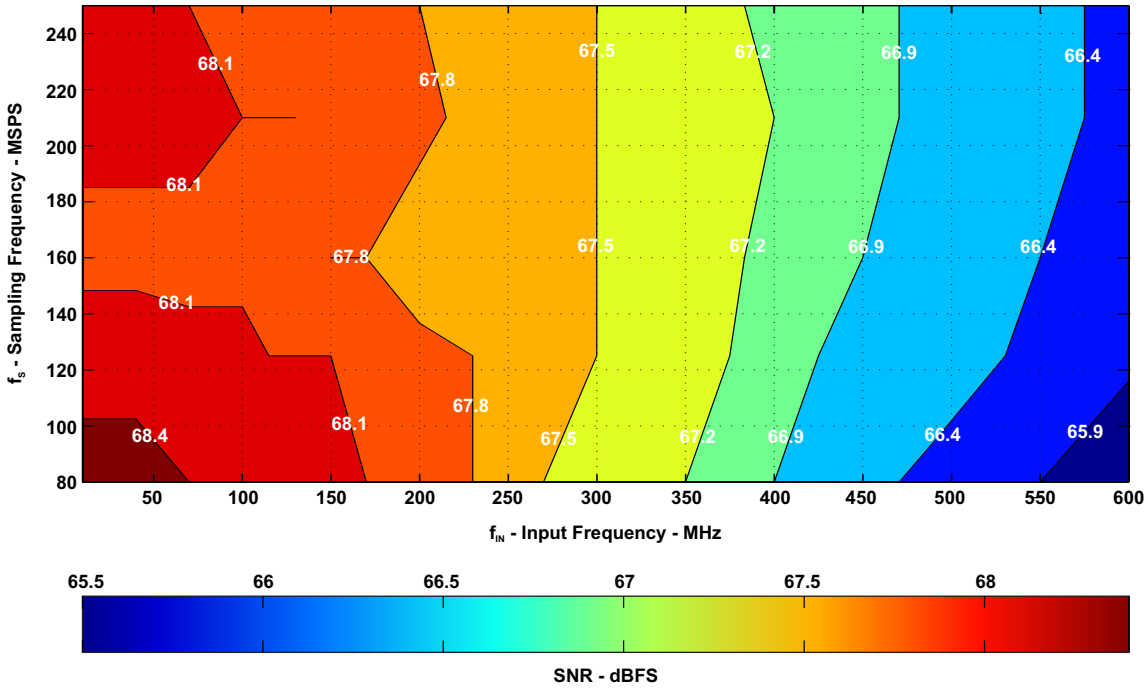


Figure 71. 6-dB Gain (SNR, ADS42JB69)

7.13.3 Signal-to-Noise Ratio (SNR): ADS42JB49

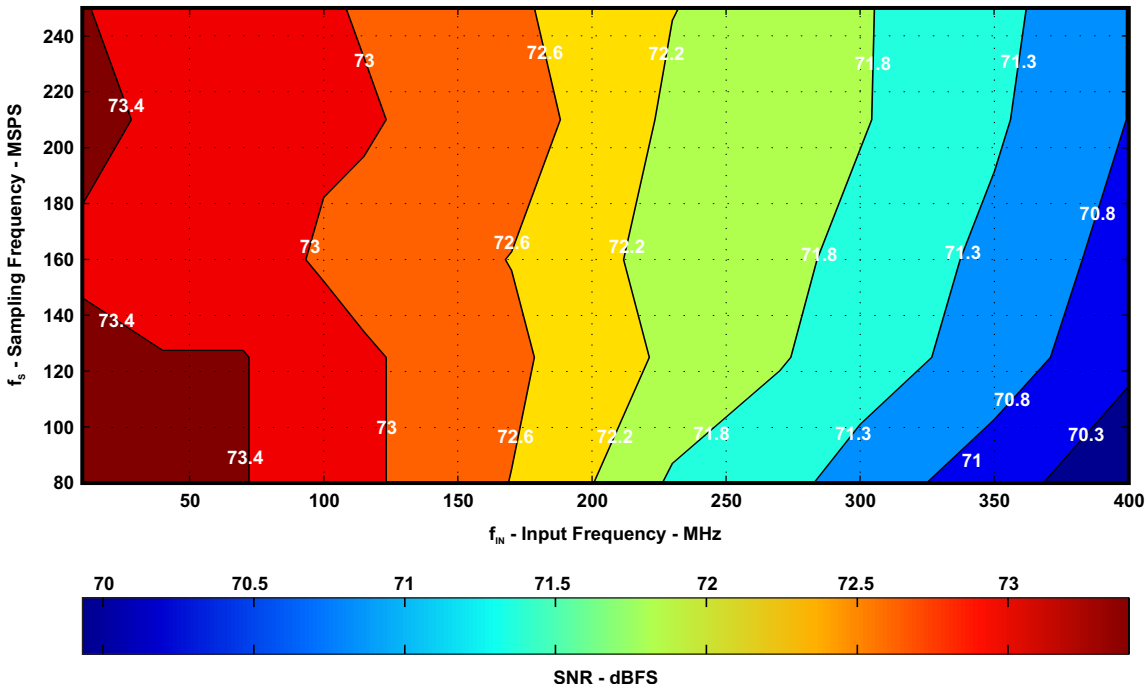


Figure 72. 0-dB Gain (SNR, ADS42JB49)

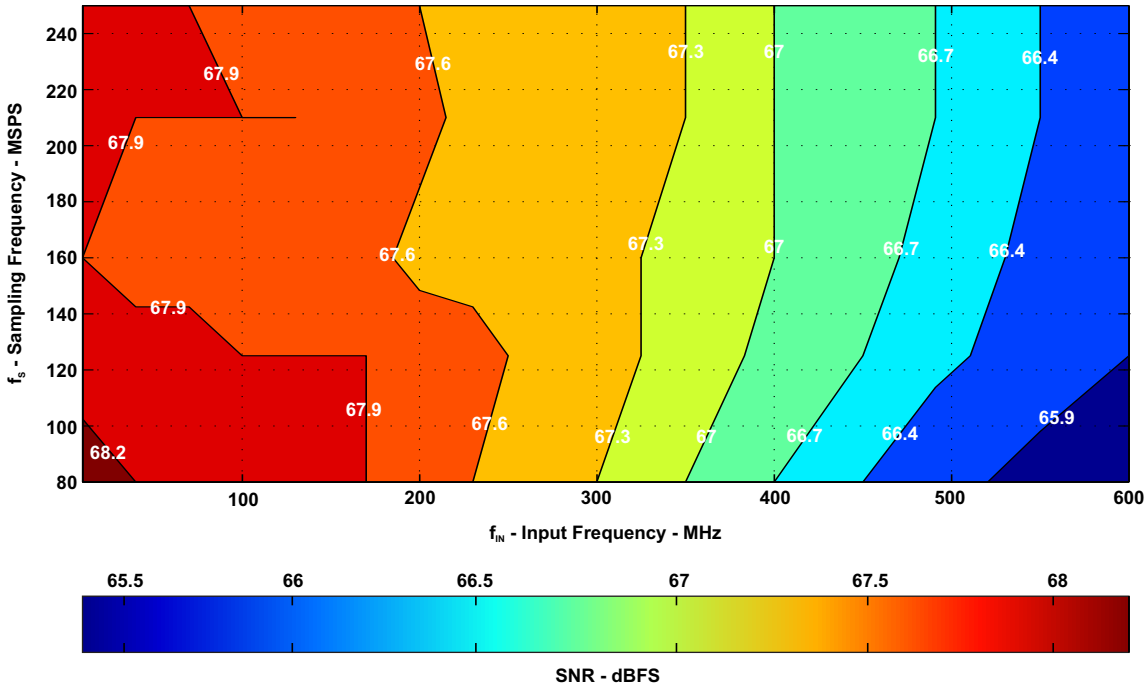
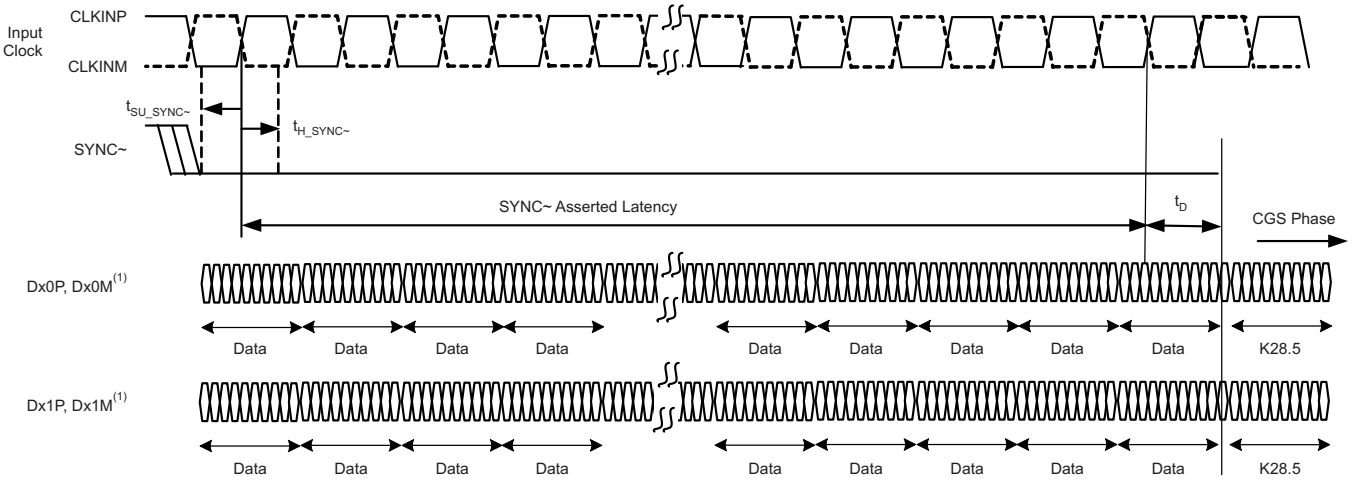


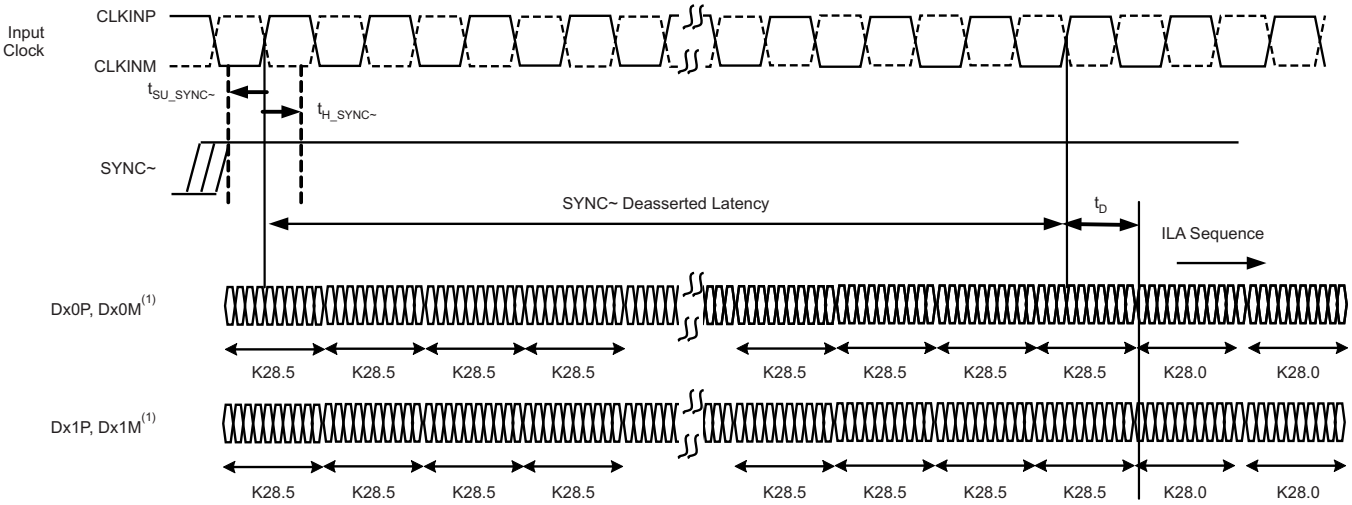
Figure 73. 6-dB Gain (SNR, ADS42JB49)

8 Parameter Measurement Information



(1) x = A for channel A and B for channel B.

Figure 74. SYNC~ Latency in CGS Phase (Two-Lane Mode)



(1) x = A for channel A and B for channel B.

Figure 75. SYNC~ Latency in ILAS Phase (Two-Lane Mode)

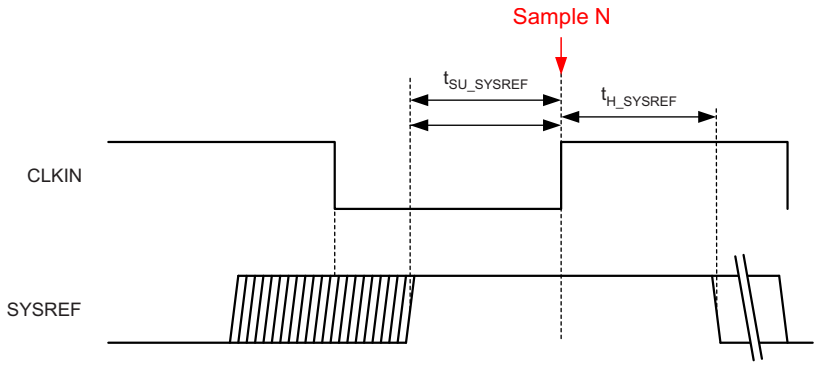


Figure 76. SYSREF Timing (Subclass 1)

Parameter Measurement Information (continued)

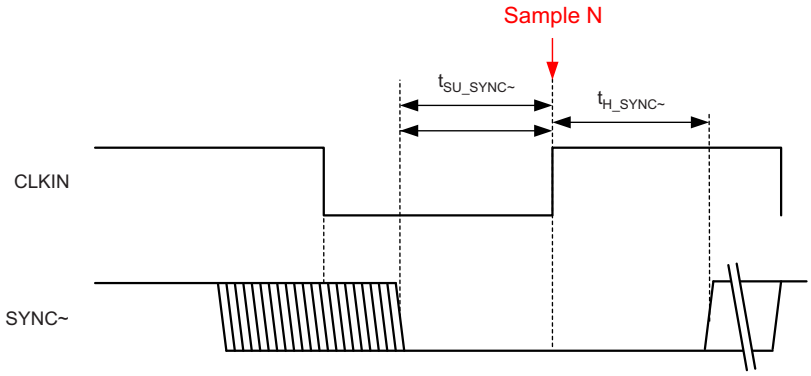


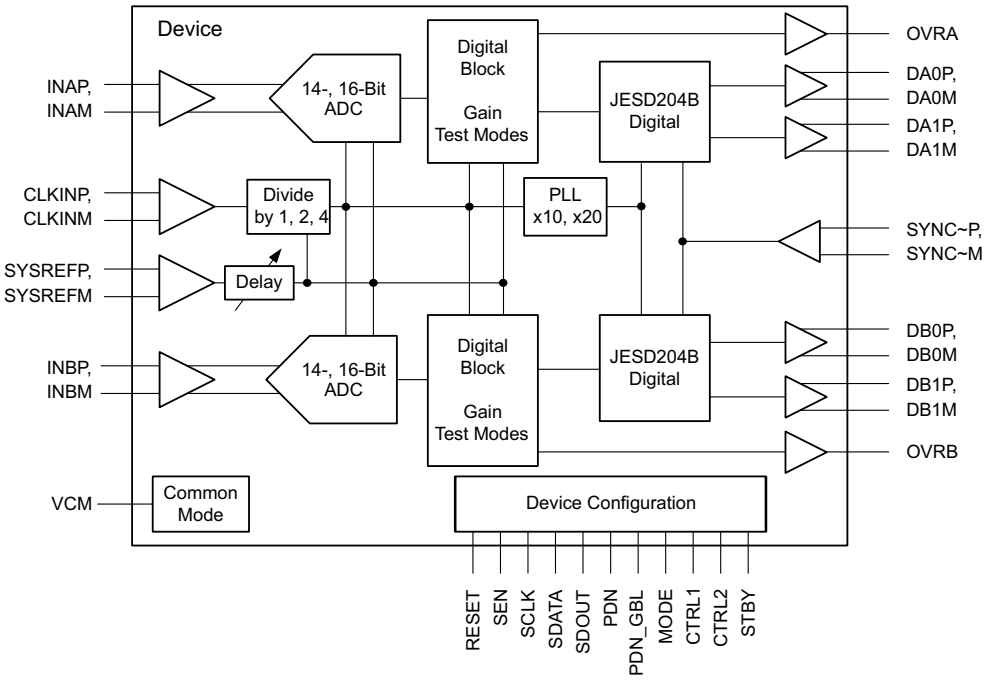
Figure 77. SYNC~ Timing (Subclass 2)

9 Detailed Description

9.1 Overview

The ADS42JB69 and ADS42JB49 is a family of high linearity, buffered analog input, dual-channel ADCs with maximum sampling rates up to 250 MSPS employing JESD204B interface. The conversion process is initiated by a rising edge of the external input clock and the analog input signal is sampled. The sampled signal is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. At every clock edge the sample propagates through the pipeline, resulting in a data latency of 23 clock cycles. The output is available in CML logic levels following JESD204B standard.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Digital Gain

The device includes gain settings that can be used to obtain improved SFDR performance (compared to no gain). Gain is programmable from –2 dB to 6 dB (in 0.5-dB steps). For each gain setting, the analog input full-scale range scales proportionally. Table 2 shows how full-scale input voltage changes when digital gain are programmed in 1-dB steps. Refer to Table 19 to set digital gain using a serial interface register.

SFDR improvement is achieved at the expense of SNR; for 1 dB increase in digital gain, SNR degrades approximately between 0.5 dB and 1 dB. Therefore, gain can be used as a trade-off between SFDR and SNR. Note that the default gain after reset is 0 dB with a 2.0-V_{PP} full-scale voltage.

Table 2. Full-Scale Range Across Gains

DIGITAL GAIN	FULL-SCALE INPUT VOLTAGE
–2 dB	2.5 V_{PP} (1)
–1 dB	2.2 V_{PP}
0 dB (default)	2.0 V_{PP}
1 dB	1.8 V_{PP}
2 dB	1.6 V_{PP}
3 dB	1.4 V_{PP}
4 dB	1.25 V_{PP}
5 dB	1.1 V_{PP}
6 dB	1.0 V_{PP}

(1) Shaded cells indicate performance settings used in the *Electrical Characteristics* and *Typical Characteristics*.

9.3.2 Input Clock Divider

The device is equipped with an internal divider on the clock input. This divider allows operation with a faster input clock, simplifying the system clock distribution design. The clock divider can be bypassed (divide-by-1) for operation with a 250-MHz clock. The divide-by-2 option supports a maximum 500-MHz input clock and the divide-by-4 option supports a maximum 1-GHz input clock frequency.

9.3.3 Overrange Indication

The device provides two different overrange indications. Normal OVR (default) is triggered if the final 16-bit data output exceeds the maximum code value. Fast OVR is triggered if the input voltage exceeds the programmable overrange threshold and is presented after only nine clock cycles, thus enabling a quicker reaction to an overrange event. By default, the normal overrange indication is output on the OVRA and OVRB pins. Using the register bit FAST OVR EN, the fast OVR indication can be presented on the overrange pins instead.

The input voltage level at which the overload is detected is referred to as the threshold and is programmable using the FAST OVR THRESHOLD bits. FAST OVR is triggered nine output clock cycles after the overload condition occurs. The threshold voltage amplitude at which fast OVR is triggered is: 1 × [the decimal value of the FAST OVR THRESH bits] / 127

When digital is programmed (for gain values > 0 dB), the threshold voltage amplitude is: $10^{-Gain\ /\ 20}$ × [the decimal value of the FAST OVR THRESH bits] / 127

9.3.4 Pin Controls

The device power-down functions can be controlled either through the parallel control pins (STBY, PDN_GBL, CTRL1, and CTRL2) or through an SPI register setting.

STBY places the device in a standby power-down mode. PDN_GBL places the device in global power-down mode.

Table 3. CTRL1, CTRL2 Pin Functions

CTRL1	CTRL2	DESCRIPTION
Low	Low	Normal operation
High	Low	Channel A powered down
Low	High	Channel B powered down
High	High	Global power-down

Table 4. PDN_GBL Pin Function

PDN_GBL	DESCRIPTION
Low	Normal operation
High	Global power-down. Wake-up from this mode is slow.

Table 5. STBY Pin Function

STBY	DESCRIPTION
Low	Normal operation
High	ADCs are powered down while the input clock buffer and output CML buffers are alive. Wake-up from this mode is fast.

9.4 Device Functional Modes

9.4.1 JESD204B Interface

The JESD interface of ADS42JB49 and ADS42JB69, as shown in Figure 78, supports device subclasses 0, 1, and 2 with a maximum output data rate (per lane) of 3.125 Gbps.

An external SYSREF (subclass 1) or SYNC~ (subclass 2) signal is used to align all internal clock phases and the local multiframe clock to a specific sampling clock edge. This alignment allows synchronization of multiple devices in a system and minimizes timing and alignment uncertainty.

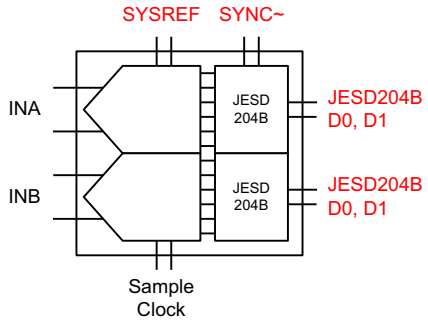


Figure 78. JESD204B Interface

Depending on the ADC sampling rate, the JESD204B output interface can be operated with either one or two lanes per ADC. The JESD204B interface can be configured using serial registers.

The JESD204B transmitter block (Figure 79) consists of the transport layer, the data scrambler, and the link layer. The transport layer maps the ADC output data into the selected JESD204B frame data format and manages if the ADC output data or test patterns are transmitted. The link layer performs the 8b and 10b data encoding as well as the synchronization and initial lane alignment using the SYNC~ input signal. Optionally, data from the transport layer can be scrambled.

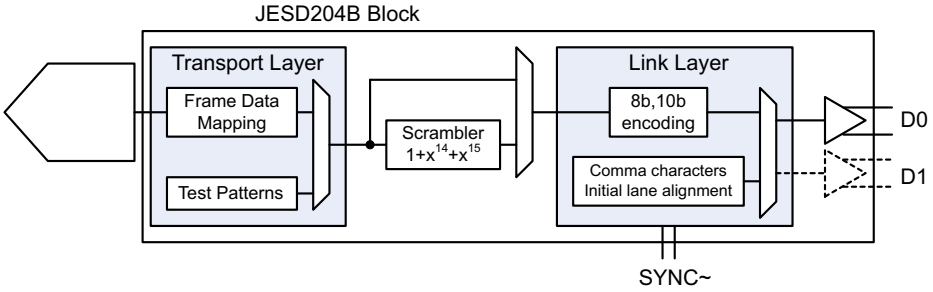


Figure 79. JESD204B Block

9.4.1.1 JESD204B Initial Lane Alignment (ILA)

When receiving device asserts the SYNC~ signal (i.e a logic low signal is applied on SYNC~P - SYNC~M), the device begins transmitting comma (K28.5) characters to establish code group synchronization (CGS).

Device Functional Modes (continued)

When synchronization is complete, the receiving device de-asserts the SYNC~ signal and the ADS42JB49 and ADS42JB69 begin the initial lane alignment (ILA) sequence with the next local multiframe clock boundary. The device transmits four multiframes, each containing K frames (where K is SPI programmable). Each multiframe contains the frame start and end symbols; the second multiframe also contains the JESD204 link configuration data.

9.4.1.2 JESD204B Test Patterns

There are three different test patterns available in the transport layer of the JESD204B interface. The device supports a clock output, an encoded, and a PRBS ($2^{15} – 1$) pattern. These patterns can be enabled by serial register write in address 26h, bits D[7:6].

9.4.1.3 JESD204B Frame Assembly

The JESD204B standard defines the following parameters:

- L is the number of lanes per Lane.
- M is the number of converters per device.
- F is the number of octets per frame clock period.
- S is the number of samples per frame.

Table 6 lists the available JESD204B formats and valid device ranges. Ranges are limited by the maximum ADC sample frequency and the SERDES line rate.

Table 6. JESD240B Ranges

L	M	F	S	MAX ADC SAMPLING RATE (MSPS)	MAX f_{SERDES} (Gbps)
4	2	1	1	250	2.5
2	2	2	1	156.25	3.125

The detailed frame assembly in 10x and 20x modes for dual-channel operation is shown in Table 7. Note that unused lanes in 10x mode become 3-stated.

Table 7. Frame Assembly for Dual-Channel Mode(1)

LANE	LMF = 421				LMF = 222					
DA0	A_0[15:8]	A_1[15:8]	A_2[15:8]		A_0[15:8]	A_0[7:0]	A_1[15:8]	A_1[7:0]	A_2[15:8]	A_2[7:0]
DA1	A_0[7:0]	A_1[7:0]	A_2[7:0]		—	—	—	—	—	—
DB0	B_0[15:8]	B_1[15:8]	B_2[15:8]		B_0[15:8]	B_0[7:0]	B_1[15:8]	B_1[7:0]	B_2[15:8]	B_2[7:0]
DB1	B_0[7:0]	B_1[7:0]	B_2[7:0]		—	—	—	—	—	—

(1) In ADS42JB49 two LSBs of 16-bit data are padded with 00.

9.4.1.4 JESD Link Configuration

During the lane alignment sequence, the ADS42JB69 and ADS42JB49 transmit JESD204B configuration parameters in the second multi-frame of the ILA sequence. Configuration bits are mapped in octets, as per the JESD204B standard described in Figure 80 and Table 8.

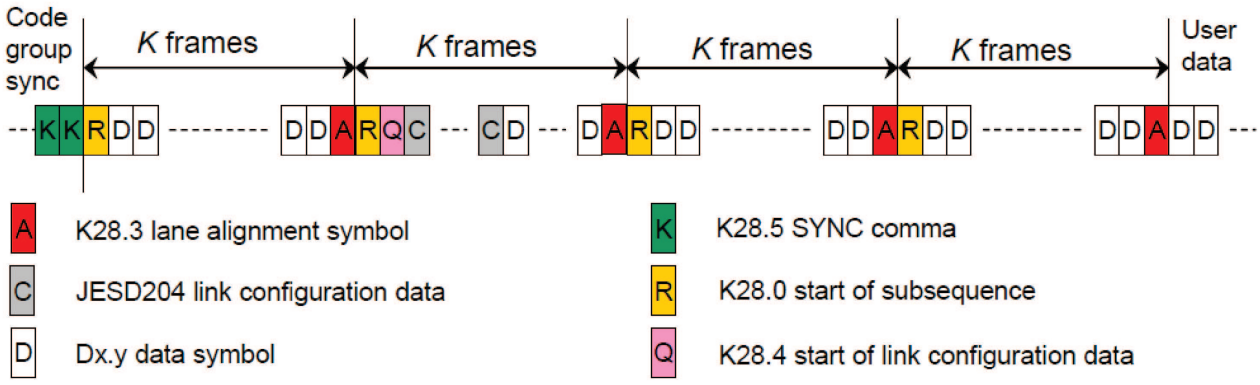


Figure 80. Initial Lane Alignment Sequence

Table 8. Mapping of Configuration Bits to Octets

OCTET NO.	MSB	D6	D5	D4	D3	D2	D1	LSB
0	DID[7:0]							
1	ADJCNT[3:0]				BID[3:0]			
2	X	ADJDIR[0]	PHADJ[0]	LID[4:0]				
3	SCR[0]			L[4:0]				
4	F[7:0]							
5				K[4:0]				
6	M[7:0]							
7	CS[1:0]		X	N[4:0]				
8	SUBCLASSV[2:0]			N'[4:0]				
9	JESDV[2:0]			S[4:0]				
10	HD[0]	X	X	CF[4:0]				
11	RES1[7:0]							
12	RES2[7:0]							
13	FCHK[7:0]							

9.4.1.4.1 Configuration for 2-Lane (20x) SERDES Mode

Table 9 lists the values of the JESD204B configuration bits applicable for the 2-lane SERDES Mode. The default value of these bits after reset is also specified in the table.

Table 9. Configuration for 2-Lane SERDES Mode

PARAMETER	DESCRIPTION	PARAMETER RANGE	FIELD	ENCODING	DEFAULT VALUE AFTER RESET
ADJCNT	Number of adjustment resolution steps to adjust DAC LMFC. Applies to subclass 2 operation only.	0-15	ADJCNT[3:0]	Binary value	0
ADJDIR	Direction to adjust DAC LMFC 0 : Advance 1 : Delay applies to subclass 2 operation only	0-1	ADJDIR[0]	Binary value	0
BID	Bank ID – extension to DID	0-15	BID[3:0]	Binary value	0
CF	No. of control words per frame clock period per link	0-32	CF[4:0]	Binary value	0
CS	No. of control bits per sample	0-3	CS[1:0]	Binary value	0
DID	Device (= link) identification no.	0-255	DID[7:0]	Binary value	0
F	No. of octets per frame	1-256	F[7:0]	Binary value minus 1	1
HD	High-density format	0-1	HD[0]	Binary value	0
JESDV	JESD204 version 000 : JESD204A 001 : JESD204B	0-7	JESDV[2:0]	Binary value	1
K	No. of frames per multi-frame	1-32	K[4:0]	Binary value minus 1	8
L	No. of lanes per converter device (link)	1-32	L[4:0]	Binary value minus 1	0
LID	Lane identification no. (within link)	0-31	LID[4:0]	Binary value	LID[0] = 0, LID[1] = 1
M	No. of converters per device	1-256	M[7:0]	Binary value minus 1	1
N	Converter resolution	1-32	N[4:0]	Binary value minus 1	15
N’	Total no. of bits per sample	1-32	N'[4:0]	Binary value minus 1	15
PHADJ	Phase adjustment request to DAC subclass 2 only.	0-1	PHADJ[0]	Binary value	0
S	No. of samples per converter per frame cycle	1-32	S[4:0]	Binary value minus 1	0
SCR	Scrambling enabled	0-1	SCR[0]	Binary value	0
SUBCLASSV	Device subclass version 000 : Subclass 0 001 : Subclass 1 010 : Subclass 2	0-7	SUBCLASSV[2:0]	Binary value	2
RES1	Device subclass version 000 : Subclass 0 001 : Subclass 1 010 : Subclass 2	0-255	RES1[7:0]	Binary value	0
RES2	Reserved field 2	0-255	RES2[7:0]	Binary value	0
CHKSUM	Checksum Σ (all above fields) mod 256	0-255	FCHK[7:0]	Binary value	44, 45

9.4.1.4.2 Configuration for 4-Lane (10x) SERDES Mode

Table 10 lists the values of the JESD204 configuration bits applicable for the 4-lane SERDES Mode. The default value of these bits after reset is also specified in the table.

Table 10. Configuration for 4-Lane SERDES Mode

PARAMETER	DESCRIPTION	PARAMETER RANGE	FIELD	ENCODING	DEFAULT VALUE AFTER RESET
ADJCNT	Number of adjustment resolution steps to adjust DAC LMFC. Applies to subclass 2 operation only.	0-15	ADJCNT[3:0]	Binary value	0
ADJDIR	Direction to adjust DAC LMFC 0 : Advance 1 : Delay applies to subclass 2 operation only	0-1	ADJDIR[0]	Binary value	0
BID	Bank ID; extension to DID	0-15	BID[3:0]	Binary value	0
CF	No. of control words per frame clock period per link	0-32	CF[4:0]	Binary value	0
CS	No. of control bits per sample	0-3	CS[1:0]	Binary value	0
DID	Device (= link) identification no.	0-255	DID[7:0]	Binary value	0
F	No. of octets per frame	1-256	F[7:0]	Binary value minus 1	0
HD	High-density format	0-1	HD[0]	Binary value	1
JESDV	JESD204 version 000 : JESD204A 001 : JESD204B	0-7	JESDV[2:0]	Binary value	1
K	No. of frames per multi-frame	1-32	K[4:0]	Binary value minus 1	16
L	No. of lanes per converter device (link)	1-32	L[4:0]	Binary value minus 1	3
LID	Lane identification no (within link)	0-31	LID[4:0]	Binary value	LID[0] = 0, LID[1] = 1, LID[2] = 2, LID[3] = 3
M	No. of converters per device	1-256	M[7:0]	Binary value minus 1	1
N	Converter resolution	1-32	N[4:0]	Binary value minus 1	15
N’	Total no. of bits per sample	1-32	N'[4:0]	Binary value minus 1	15
PHADJ	Phase adjustment request to DAC subclass 2 only.	0-1	PHADJ[0]	Binary value	0
S	No. of samples per converter per frame cycle	1-32	S[4:0]	Binary value minus 1	0
SCR	Scrambling enabled	0-1	SCR[0]	Binary value	0
SUBCLASSV	Device subclass version 000 : Subclass 0 001 : Subclass 1 010 : Subclass 2	0-7	SUBCLASSV[2:0]	Binary value	2
RES1	Device subclass version 000 : Subclass 0 001 : Subclass 1 010 : Subclass 2	0-255	RES1[7:0]	Binary value	0
RES2	Reserved field 2	0-255	RES2[7:0]	Binary value	0
CHKSUM	Checksum Σ (all above fields) mod 256	0-255	FCHK[7:0]	Binary value	54, 55, 56, 57

9.4.1.5 CML Outputs

The device JESD204B transmitter uses differential CML output drivers. The CML output current is programmable from 5 mA to 20 mA using register settings.

The output driver includes an internal 50-Ω termination to IOVDD supply. External 50-Ω termination resistors connected to receiver common-mode voltage should be placed close to receiver pins. AC coupling can be used to avoid the common-mode mismatch between transmitter and receiver, as shown in Figure 81.

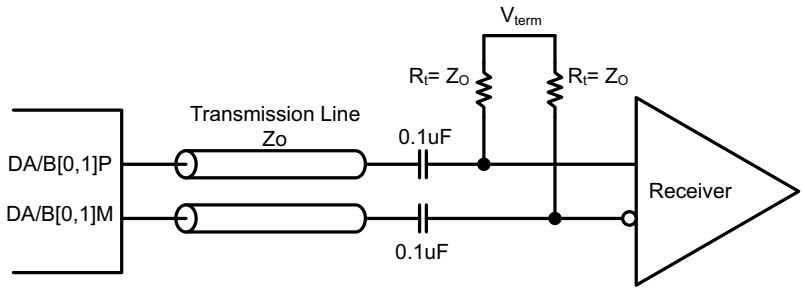


Figure 81. CML Output Connections

Figure 82 and Figure 83 show the data eye measurements of the device JESD204B transmitter against the JESD204B transmitter mask at 2.5 GBPS (10x mode) and 3.125 GBPS (20x mode), respectively.

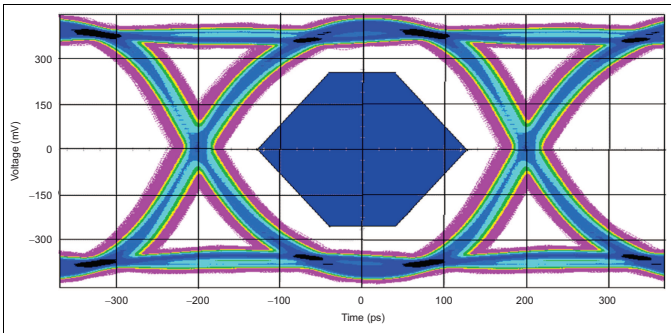


Figure 82. Eye Diagram: 2.5 Gbps

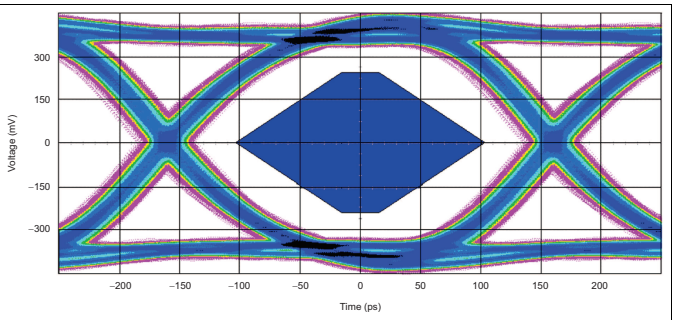


Figure 83. Eye Diagram: 3.125 Gbps

9.5 Programming

9.5.1 Device Configuration

The ADS42JB49 and ADS42JB69 can be configured using a serial programming interface, as described in the *Serial Interface* section. In addition, the device has four dedicated parallel pins (PDN_GBL, STBY, CTRL1, and CTRL2) for controlling the power-down modes.

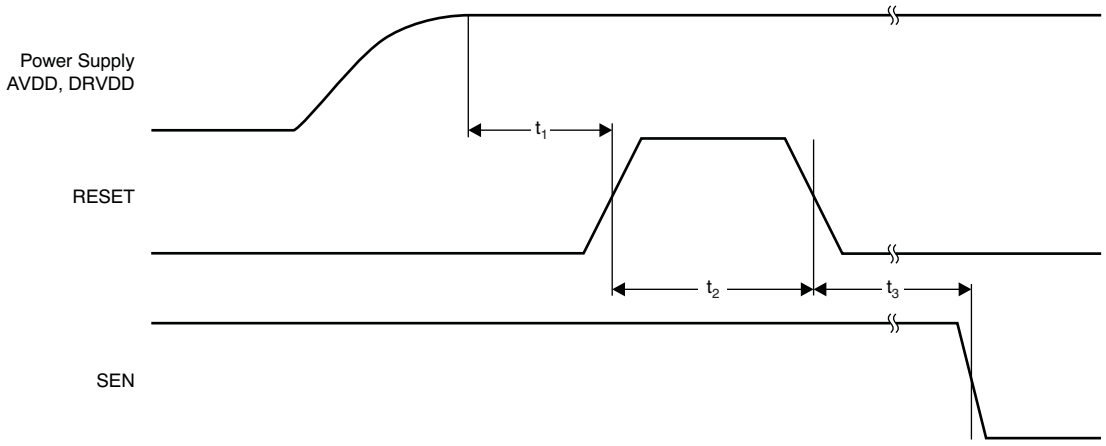
9.5.2 Details of Serial Interface

The ADC has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface data), and SDOUT (serial interface data output) pins. Serially shifting bits into the device is enabled when SEN is low. SDATA serial data are latched at every SCLK rising edge when SEN is active (low). The serial data are loaded into the register at every 16th SCLK rising edge when SEN is low. When the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse. The interface functions with SCLK frequencies from 20 MHz down to very low speeds (of a few hertz) and also with non-50% SCLK duty cycle.

9.5.2.1 Register Initialization

After power-up, the internal registers must be initialized to their default values through a **hardware reset** by applying a high pulse on the RESET pin (of widths greater than 10 ns), as shown in Figure 84. Later during operation, if required serial interface registers can be cleared by:

1. Either through a hardware reset or
2. By applying a software reset. When using the serial interface, set the RESET bit (D0 in register address 08h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.



NOTE: After power-up, the internal registers must be initialized to their default values through a hardware reset by applying a high pulse on the RESET pin.

Figure 84. Reset Timing Diagram

Table 11. Reset Timing (1)

		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from AVDD and DRVDD power-up to active RESET pulse	1			ms
t_2	Reset pulse width	Active RESET signal pulse width	10			ns
					1	µs
t_3	Register write delay	Delay from RESET disable to SEN active	100			ns

(1) Typical values at +25°C; minimum and maximum values across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, unless otherwise noted.

9.5.2.2 Serial Register Write

The internal device register can be programmed following these steps:

1. Drive the SEN pin low.
2. Set the R/W bit to '0' (bit A7 of the 8-bit address).
3. Set bit A6 in the address field to '0'.
4. Initiate a serial interface cycle specifying the address of the register (A5 to A0) whose content must be written (as shown in Figure 85 and Table 12).
5. Write the 8-bit data that is latched on the SCLK rising edge.

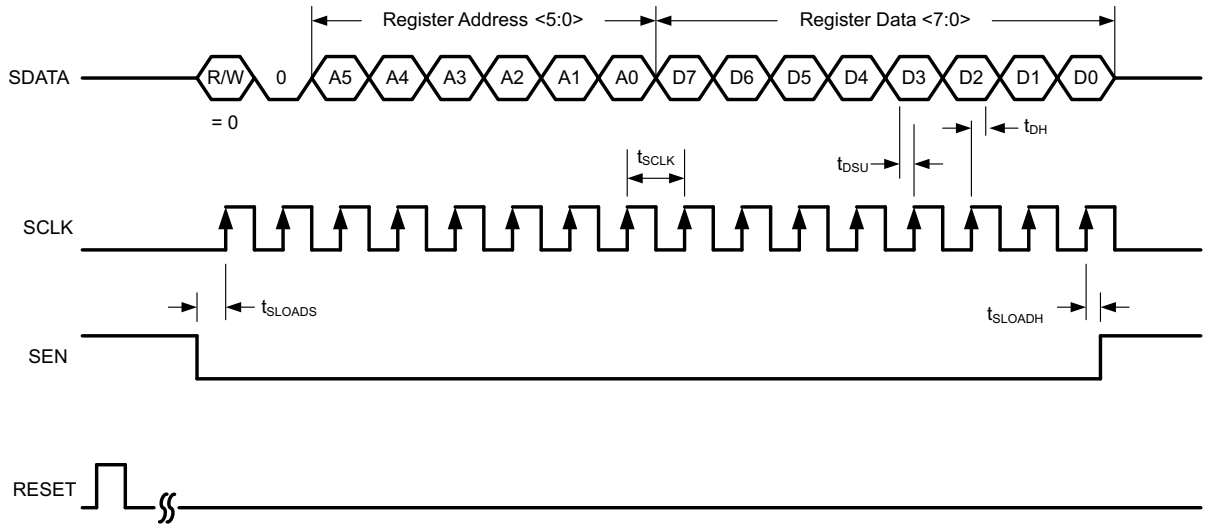


Figure 85. Serial Register Write Timing Diagram

Table 12. Serial Interface Timing(1)

		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to 1 / t_{SCLK})	> dc		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DSU}	SDIO setup time	25			ns
t_{DH}	SDIO hold time	25			ns

(1) Typical values are at +25°C, minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD3V = 3.3 V, and AVDD = DRVDD = IOVDD = 1.8 V, unless otherwise noted.

9.5.2.3 Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back. This readback mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

1. Set bit A7 (MSB) of 8 bit address to '1'.
2. Write the address of register on bits A5 through A0 whose contents must be read. See Figure 86
3. The device outputs the contents (D7 to D0) of the selected register on the SDOUT pin (pin 45).
4. The external controller can latch the contents at the SCLK rising edge.

When serial registers are enabled for writing (bit A7 of 8-bit address bus is 0), the SDOUT pin is in a high-impedance mode. If serial readout is not used, the SDOUT pin must float. Figure 86 shows a timing diagram of this readout mode. SDOUT comes out at the SCLK falling edge with an approximate delay (t_{SD_DELAY}) of 20 ns, as shown in Figure 87.

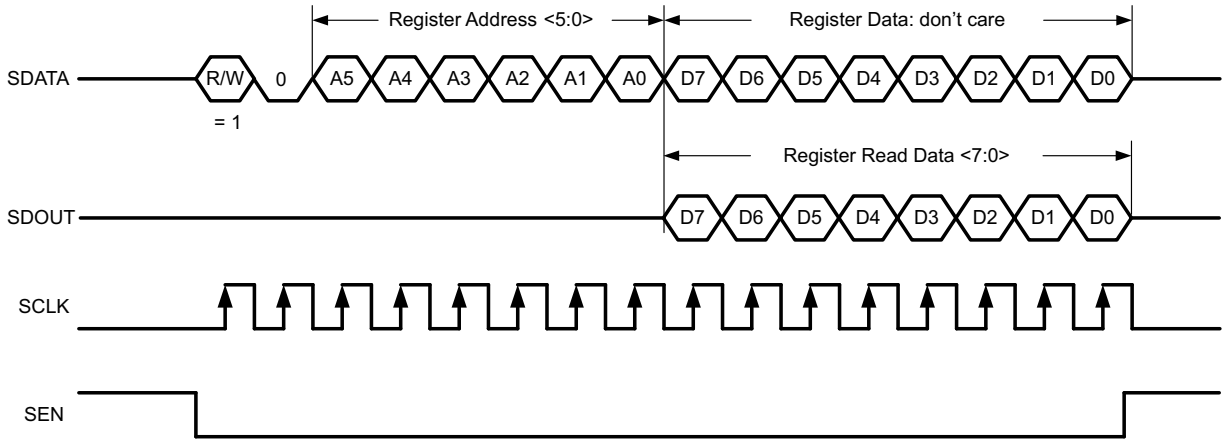


Figure 86. Serial Register Readout Timing Diagram

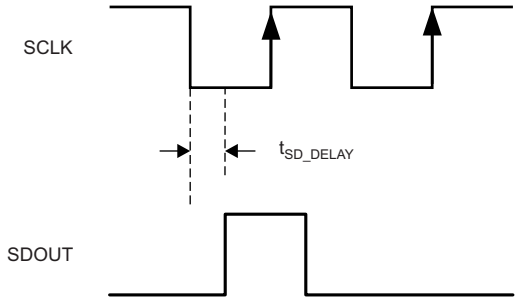


Figure 87. SDOUT Timing Diagram

9.6 Register Maps

Table 13 lists a summary of the serial interface registers.

Table 13. Summary of Serial Interface Registers

REGISTER ADDRESS	REGISTER DATA							
A[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
06	0	0	0	0	0	0	CLK DIV	
07	0	0	0	0	0	SYSREF DELAY		
08	PDN CHA	PDN CHB	STDBY	DATA FORMAT	Always write 1	0	0	RESET
0B	CHA GAIN					CHA GAIN EN	0	0
0C	CHBGAIN					CHB GAIN EN	0	0
0D	HIGH FREQ 1	0	0	HIGH FREQ 1	0	0	0	FAST OVR EN
0E	HIGH FREQ 2	0	0	HIGH FREQ 2	0	0	0	0
0F	CHA TEST PATTERNS				CHB TEST PATTERNS			
10	CUSTOM PATTERN 1[15:8]							
11	CUSTOM PATTERN 1[7:0]							
12	CUSTOM PATTERN 2[15:8]							
13	CUSTOM PATTERN 2[7:0]							
1F	Always write 0	FAST OVR THRESHOLD						
26	SERDES TEST PATTERN		IDLE SYNC	TESTMODE EN	FLIP ADC DATA	LAN ALIGN	FRAME ALIGN	TX LINK CONFIG DATA0
27	0	0	0	0	0	0	CTRLK	CTRLF
2B	SCRAMBLE EN	0	0	0	0	0	0	0
2C	0	0	0	0	0	0	0	OCTETS PER FRAME
2D	0	0	0	FRAMES PER MULTIFRAME				
30	SUBCLASS			0	0	0	0	0
36	SYNC REQ	LMFC RESET MASK	0	0	OUTPUT CURRENT SEL			
37	LINK LAYER TESTMODE			LINK LAYER RPAT	0	PULSE DET MODES		
38	FORCE LMFC COUNT	LMFC COUNT INIT					RELEASE ILANE SEQ	

Table 14. High-Frequency Modes Summary

REGISTER ADDRESS	VALUE	DESCRIPTION
Dh	90h	High-frequency modes should be enabled for input frequencies greater than 250 MHz.
Eh	90h	High-frequency modes should be enabled for input frequencies greater than 250 MHz.

9.6.1 Description of Serial Interface Registers

9.6.1.1 Register 6 (offset = 06h) [reset = 00h]

Figure 88. Register 6

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	CLK DIV	
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. Register 6 Field Descriptions

Bit	Field	Type	Reset	Description
D[7:2]	0	W	0h	Always write '0'
D[1:0]	CLK DIV	R/W	0h	Internal clock divider for input sample clock 00 : Divide-by-1 (clock divider bypassed) 01 : Divide-by-2 10 : Divide-by-1 11 : Divide-by-4

9.6.1.2 Register 7 (offset = 07h) [reset = 00h]

Figure 89. Register 7

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	SYSREF DELAY	
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. Register 7 Field Descriptions

Bit	Field	Type	Reset	Description
D[7:2]	0	W	0h	Always write '0'
D[1:0]	SYSREF DELAY	R/W	0h	Controls the delay of the SYSREF input with respect to the input clock. Typical values for the expected delay of different settings are: 000 : 0-ps delay 001 : 60-ps delay 010 : 120-ps delay 011 : 180-ps delay 100 : 240-ps delay 101 : 300-ps delay 110 : 360-ps delay 111 : 420-ps delay

9.6.1.3 Register 8 (offset = 08h) [reset = 00h]

Figure 90. Register 8

D7	D6	D5	D4	D3	D2	D1	D0
PDN CHA	PDN CHB	STDBY	DATA FORMAT	1	0	0	RESET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	W-1h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. Register 8 Field Descriptions

Bit	Field	Type	Reset	Description
D7	PDN CHA	R/W	0h	Power-down channel A 0 : Normal operation 1 : Channel A power-down
D6	PDN CHB	R/W	0h	Power-down channel B 0 : Normal operation 1 : Channel B power-down
D5	STBY	R/W	0h	Dual ADC is placed into standby mode 0 : Normal operation 1 : Both ADCs are powered down (input clock buffer and CML output buffers are alive)
D4	DATA FORMAT	R/W	0h	Digital output data format 0 : Twos complement 1 : Offset binary
D3	1	W	1h	Always write '1' Default value of this bit is '0'. This bit must always be set to '1'.
D[2:1]	0	W	0h	Always write '0'
D0	RESET	R/W	0h	Software reset applied This bit resets all internal registers to the default values and self-clears to ‘0’.

9.6.1.4 Register B (offset = 0Bh) [reset = 00h]

Figure 91. Register B

D7	D6	D5	D4	D3	D2	D1	D0
CHA GAIN					CHA GAIN EN	0	0
R/W-0h					R/W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. Register B Field Descriptions

Bit	Field	Type	Reset	Description
D[7:3]	CHA GAIN	R/W	0h	Digital gain for channel A (must set the CHA GAIN EN bit first, bit D2). Bit descriptions are listed in Table 19.
D2	CHA GAIN EN	R/W	0h	Digital gain enable bit for channel A 0 : Digital gain disabled 1 : Digital gain enabled
D[1:0]	0	W	0h	Always write '0'

Table 19. Digital Gain for Channel A

REGISTER VALUE	DIGITAL GAIN	FULL-SCALE INPUT VOLTAGE		REGISTER VALUE	DIGITAL GAIN	FULL-SCALE INPUT VOLTAGE
00000	0 dB	2.0 V_{PP}		01010	1.5 dB	1.7 V_{PP}
00001	Do not use	—		01011	2 dB	1.6 V_{PP}
00010	Do not use	—		01100	2.5 dB	1.5 V_{PP}
00011	–2.0 dB	2.5 V_{PP}		01101	3 dB	1.4 V_{PP}
00100	–1.5 dB	2.4 V_{PP}		01110	3.5 dB	1.3 V_{PP}
00101	–1.0 dB	2.2 V_{PP}		01111	4 dB	1.25 V_{PP}
00110	–0.5 dB	2.1 V_{PP}		10000	4.5 dB	1.2 V_{PP}
00111	0 dB	2.0 V_{PP}		10001	5 dB	1.1 V_{PP}
01000	0.5 dB	1.9 V_{PP}		10010	5.5 dB	1.05 V_{PP}
01001	1 dB	1.8 V_{PP}		10011	6 dB	1.0 V_{PP}

9.6.1.5 Register C (offset = 0Ch) [reset = 00h]

Figure 92. Register C

D7	D6	D5	D4	D3	D2	D1	D0
CHB GAIN					CHB GAIN EN	0	0
R/W-0h					R/W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 20. Register C Field Descriptions

Bit	Field	Type	Reset	Description
D[7:3]	CHB GAIN	R/W	0h	Digital gain for channel B (must set the CHA GAIN EN bit first, bit D2). Bit descriptions are listed in Table 21.
D2	CHB GAIN EN	R/W	0h	Digital gain enable bit for channel B 0 : Digital gain disabled 1 : Digital gain enabled
D[1:0]	0	W	0h	Always write '0'

Table 21. Digital Gain for Channel B

REGISTER VALUE	DIGITAL GAIN	FULL-SCALE INPUT VOLTAGE		REGISTER VALUE	DIGITAL GAIN	FULL-SCALE INPUT VOLTAGE
00000	0 dB	2.0 V_{PP}		01010	1.5 dB	1.7 V_{PP}
00001	Do not use	—		01011	2 dB	1.6 V_{PP}
00010	Do not use	—		01100	2.5 dB	1.5 V_{PP}
00011	–2.0 dB	2.5 V_{PP}		01101	3 dB	1.4 V_{PP}
00100	–1.5 dB	2.4 V_{PP}		01110	3.5 dB	1.3 V_{PP}
00101	–1.0 dB	2.2 V_{PP}		01111	4 dB	1.25 V_{PP}
00110	–0.5 dB	2.1 V_{PP}		10000	4.5 dB	1.2 V_{PP}
00111	0 dB	2.0 V_{PP}		10001	5 dB	1.1 V_{PP}
01000	0.5 dB	1.9 V_{PP}		10010	5.5 dB	1.05 V_{PP}
01001	1 dB	1.8 V_{PP}		10011	6 dB	1.0 V_{PP}

9.6.1.6 Register D (offset = 0Dh) [reset = 00h]

Figure 93. Register D

D7	D6	D5	D4	D3	D2	D1	D0
HIGH FREQ 1	0	0	HIGH FREQ 1	0	0	0	FAST OVR EN
R/W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 22. Register D Field Descriptions

Bit	Field	Type	Reset	Description
D7	HIGH FREQ 1	R/W	0h	High-frequency mode 1 00 : Default 11 : Use for input frequencies > 250 MHz along with HIGH FREQ 2
D[6:5]	0	W	0h	Always write '0'
D4	HIGH FREQ 1	R/W	0h	High-frequency mode 1 00 : Default 11 : Use for input frequencies > 250 MHz along with HIGH FREQ 2
D[3:1]	0	W	0h	Always write '0'
D0	FAST OVR EN	R/W	0h	Selects if normal or fast OVR signal is presented on OVRA, OVRB pins 0 : Normal OVR on OVRA, OVRB pins 1 : Fast OVR on OVRA, OVRB pins

9.6.1.7 Register E (offset = 0Eh) [reset = 00h]

Figure 94. Register E

D7	D6	D5	D4	D3	D2	D1	D0
HIGH FREQ 2	0	0	HIGH FREQ 2	0	0	0	0
R/W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 23. Register E Field Descriptions

Bit	Field	Type	Reset	Description
D7	HIGH FREQ 2	R/W	0h	High-frequency mode 2 00 : Default 11 : Use for input frequencies > 250 MHz along with HIGH FREQ 1
D[6:5]	0	W	0h	Always write '0'
D4	HIGH FREQ 2	R/W	0h	High-frequency mode 2 00 : Default 11 : Use for input frequencies > 250 MHz along with HIGH FREQ 1
D[3:0]	0	W	0h	Always write '0'

9.6.1.8 Register F (offset = 0Fh) [reset = 00h]

Figure 95. Register F

D7	D6	D5	D4	D3	D2	D1	D0
CHA TEST PATTERNS				CHB TEST PATTERNS			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. Register F Field Descriptions

Bit	Field	Type	Reset	Description
D[7:4]	CHA TEST PATTERNS	R/W	0h	Channel A test pattern programmability The 16-bit test pattern data are selected as an input to the JESD block (in the ADS42JB49, the last two LSBs of the 16-bit data are replaced by 00). 0000 : Normal operation 0001 : All '0's 0010 : All '1's 0011 : Toggle pattern: In the ADS42JB69, data are an alternating sequence of *1010101010101010* and *0101010101010101*. In the ADS42JB49, data alternate between *10101010101010* and *01010101010101*. 0100 : Digital ramp: In the ADS42JB69, data increment by 1 LSB every clock cycle from code 0 to 65535. In the ADS42JB49, data increment by 1 LSB every 4th clock cycle from code 0 to 16383. 0101 : Do not use 0110 : Single pattern: In the ADS42JB69, data are the same as programmed by the CUSTOM PATTERN 1[15:0] registers bits. In the ADS42JB49, data are the same as programmed by the CUSTOM PATTERN 1[15:2] register bits. 0111 : Double pattern: In the ADS42JB69, data alternate between CUSTOM PATTERN 1[15:0] and CUSTOM PATTERN 2[15:0]. In the ADS42JB49 data alternate between CUSTOM PATTERN 1[15:2] and CUSTOM PATTERN 2[15:2]. 1000 : Deskew pattern: In the ADS42JB69, data are AAAAh. In the ADS42JB49, data are 3AAAh. 1001 : Do not use 1010 : PRBS pattern: Data are a sequence of pseudo random numbers. 1011 : 8-point sine wave: In the ADS42JB69, data are a repetitive sequence of the following eight numbers, forming a sine-wave in twos complement format: 1, 9598, 32768, 55938, 65535, 55938, 32768, 9598. In the ADS42JB49, data are a repetitive sequence of the following eight numbers, forming a sine-wave in twos complement format: 0, 2399, 8192, 13984, 16383, 13984, 8192, 2399.

Table 24. Register F Field Descriptions (continued)

Bit	Field	Type	Reset	Description
D[3:0]	CHB TEST PATTERNS	R/W	0h	Channel B test pattern programmability 16-bit test pattern data are selected as an input to the JESD block (in the ADS42JB49, the last two LSBs of the 16-bit data are replaced by 00). 0000 : Normal operation 0001 : All '0's 0010 : All '1's 0011 : Toggle pattern: In the ADS42JB69, data are an alternating sequence of *1010101010101010* and *0101010101010101*. In the ADS42JB49, data alternate between *10101010101010* and *01010101010101*. 0100 : Digital ramp: In the ADS42JB69, data increment by 1 LSB every clock cycle from code 0 to 65535. In the ADS42JB49, data increment by 1 LSB every 4th clock cycle from code 0 to 16383. 0101 : Do not use 0110 : Single pattern: In the ADS42JB69, data are the same as programmed by the CUSTOM PATTERN 1[15:0] registers bits. In the ADS42JB49, data are the same as programmed by the CUSTOM PATTERN 1[15:2] register bits. 0111 : Double pattern: In the ADS42JB69, data alternate between CUSTOM PATTERN 1[15:0] and CUSTOM PATTERN 2[15:0]. In the ADS42JB49, data alternate between CUSTOM PATTERN 1[15:2] and CUSTOM PATTERN 2[15:2]. 1000 : Deskew pattern: In the ADS42JB69, data are AAAAh. In the ADS42JB49, data are 3AAAh. 1001 : Do not use 1010 : PRBS pattern: Data are a sequence of pseudo random numbers. 1011 : 8-point sine wave: In the ADS42JB69, data are a repetitive sequence of the following eight numbers, forming a sine-wave in twos complement format: 1, 9598, 32768, 55938, 65535, 55938, 32768, 9598. In the ADS42JB49, data are a repetitive sequence of the following eight numbers, forming a sine-wave in twos complement format: 0, 2399, 8192, 13984, 16383, 13984, 8192, 2399.

9.6.1.9 Register 10 (offset = 10h) [reset = 00h]

Figure 96. Register 10

D7	D6	D5	D4	D3	D2	D1	D0
CUSTOM PATTERN 1[15:8]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 25. Register 10 Field Descriptions

Bit	Field	Type	Reset	Description
D[7:0]	CUSTOM PATTERN 1[15:8]	R/W	0h	Sets CUSTOM PATTERN 1[15:8] using these bits for both channels

9.6.1.10 Register 11 (offset = 11h) [reset = 00h]

Figure 97. Register 11

D7	D6	D5	D4	D3	D2	D1	D0
CUSTOM PATTERN 1[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 26. Register 11 Field Descriptions

Bit	Field	Type	Reset	Description
D[7:0]	CUSTOM PATTERN 1[7:0]	R/W	0h	Sets CUSTOM PATTERN 1[7:0] using these bits for both channels

9.6.1.11 Register 12 (offset = 12h) [reset = 00h]

Figure 98. Register 12

D7	D6	D5	D4	D3	D2	D1	D0
CUSTOM PATTERN 2[15:8]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 27. Register 12 Field Descriptions

Bit	Field	Type	Reset	Description
D[7:0]	CUSTOM PATTERN 2[15:8]	R/W	0h	Sets CUSTOM PATTERN 2[15:8] using these bits for both channels

9.6.1.12 Register 13 (offset = 13h) [reset = 00h]

Figure 99. Register 13

D7	D6	D5	D4	D3	D2	D1	D0
CUSTOM PATTERN 2[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 28. Register 13 Field Descriptions

Bit	Field	Type	Reset	Description
D[7:0]	CUSTOM PATTERN 2[7:0]	R/W	0h	Sets CUSTOM PATTERN 2[7:0] using these bits for both channels

9.6.1.13 Register 1F (offset = 1Fh) [reset = FFh]

Figure 100. Register 1F

D7	D6	D5	D4	D3	D2	D1	D0
0	FAST OVR THRESHOLD						
W-1h	R/W-0h						

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 29. Register 1F Field Descriptions

Bit	Field	Type	Reset	Description
D7	0	W	W-1h	Always write '0' The default value of this bit is '1'. Always write this bit to '0' when fast OVR thresholds are programmed.
D[6:0]	FAST OVR THRESHOLD	R/W	0h	The device has a fast OVR mode that indicates an overload condition at the ADC input. The input voltage level at which the overload is detected is referred to as the threshold and is programmable using the FAST OVR THRESHOLD bits. FAST OVR is triggered nine output clock cycles after the overload condition occurs. The threshold at which fast OVR is triggered is (full-scale × [the decimal value of the FAST OVR THRESHOLD bits] / 127). See the *Overrange Indication* section for details.

9.6.1.14 Register 26 (offset = 26h) [reset = 00h]

Figure 101. Register 26

D7	D6	D5	D4	D3	D2	D1	D0
SERDES TEST PATTERN		IDLE SYNC	TESTMODE EN	FLIP ADC DATA	LANE ALIGN	FRANE ALIGN	TX LINK CONFIG DATA
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 30. Register 26 Field Descriptions

Bit	Field	Type	Reset	Description
D[7:6]	SERDES TEST PATTERN	R/W	0h	Sets test patterns in the transport layer of the JESD204B interface 00 : Normal operation 01 : Outputs clock pattern: Output is a *10101010* pattern 10 : Encoded pattern: Output is *1111111100000000* 11 : PRBS sequence: Output is $2^{15} – 1$
D5	IDLE SYNC	R/W	0h	Sets output pattern when SYNC~ is asserted 0 : Sync code is k28.5 (0xBCBC) 1 : Sync code is 0xBC50
D4	TESTMODE EN	R/W	0h	Generates a long transport layer test pattern mode according to the 5.1.63 clause of the JESD204B specification 0 : Test mode disabled 1 : Test mode enabled
D3	FLIP ADC DATA	R/W	0h	0 : Normal operation 1 : Output data order is reversed: MSB – LSB
D2	LANE ALIGN	R/W	0h	Inserts a lane alignment character (K28.3) for the receiver to align to the lane boundary per section 5.3.3.5 of the JESD204B specification. 0 : Lane alignment characters are not inserted. 1 : Inserts lane alignment characters
D1	FRAME ALIGN	R/W	0h	Inserts a frame alignment character (K28.7) for the receiver to align to the frame boundary per section 5.3.3.4 of the JESD204B specification. 0 : Frame alignment characters are not inserted. 1 : Inserts frame alignment characters
D0	TX LINK CONFIG DATA	R/W	0h	Disables sending initial link alignment (ILA) sequence when SYNC~ is de-asserted, '0' 0 : ILA enabled 1 : ILA disabled

9.6.1.15 Register 27 (offset = 27h) [reset = 00h]

Figure 102. Register 27

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	CTRL K	CTRL F
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 31. Register 27 Field Descriptions

Bit	Field	Type	Reset	Description
D[7:2]	0	W	0h	Always write '0'
D1	CTRL K	R/W	0h	Enables bit for number of frames per multiframe 0 : Default 1 : Frames per multiframe can be set in register 2Dh
D0	CTRL F	R/W	0h	Enables bit for number of octets per frame 0 : Default 1 : Octets per frame can be specified in register 2Ch

9.6.1.16 Register 2B (offset = 2Bh) [reset = 00h]

Figure 103. Register 2B

D7	D6	D5	D4	D3	D2	D1	D0
SCRAMBLE EN	0	0	0	0	0	0	0
R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 32. Register 2B Field Descriptions

Bit	Field	Type	Reset	Description
D7	SCRAMBLE EN	R/W	0h	Scramble enable bit in the JESD204B interface 0 : Scrambling disabled 1 : Scrambling enabled
D[6:0]	0	W	0h	Always write '0'

9.6.1.17 Register 2C (offset = 2Ch) [reset = 00h]

Figure 104. Register 2C

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	OCTETS PER FRAME
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 33. Register 2C Field Descriptions

Bit	Field	Type	Reset	Description
D[7:1]	0	W	0h	Always write '0'
D0	OCTETS PER FRAME	R/W	0h	Sets number of octets per frame (F) 0 : 10x mode using two lanes per ADC 1 : 20x mode using one lane per ADC

9.6.1.18 Register 2D (offset = 2Dh) [reset = 00h]

Figure 105. Register 2D

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	FRAMES PER MULTIFRAME				
W-0h	W-0h	W-0h	R/W-0h				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 34. Register 2D Field Descriptions

Bit	Field	Type	Reset	Description
D[7:5]	0	W	0h	Always write '0'
D[4:0]	FRAMES PER MULTIFRAME	R/W	0h	Sets number of frames per multiframe After reset, the default settings for frames per multiframe are: 10x : K = 16 20x : K = 8 For each mode, K must not be set to a lower value.

9.6.1.19 Register 30 (offset = 30h) [reset = 40h]

Figure 106. Register 30

D7	D6	D5	D4	D3	D2	D1	D0
SUBCLASS			0	0	0	0	0
R/W-0h			W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 35. Register 30 Field Descriptions

Bit	Field	Type	Reset	Description
D[7:5]	SUBCLASS	R/W	0h	Sets JESD204B subclass. Note that the default value of these bits after reset is 010, which makes subclass 2 the default class. 000 : Subclass 0. Backward compatibility with JESD204A. 001 : Subclass 1. Deterministic latency using the SYSREF signal. 010 : Subclass 2. Deterministic latency using SYNC~ detection (default subclass after reset).
D[4:0]	0	W	0h	Always write '0'

9.6.1.20 Register 36 (offset = 36h) [reset = 00h]

Figure 107. Register 36

D7	D6	D5	D4	D3	D2	D1	D0
SYNC REQ	LMFC RESET MASK	0	0	OUTPUT CURRENT SEL			
R/W-0h	R/W-0h	W-0h	W-0h	R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 36. Register 36 Field Descriptions

Bit	Field	Type	Reset	Description
D7	SYNC REQ	R/W	0h	Generates synchronization request 0 : Normal operation 1 : Generates sync request
D6	LMFC RESET MASK	R/W	0h	Mask LMFC reset coming to digital 0 : LMFC reset is not masked 1 : Ignores LMFC reset
D[5:4]	0	W	0h	Always write '0'
D[3:0]	OUTPUT CURRENT SEL	R/W	0h	Changes JESD output buffer current 0000 : 16 mA 0001 : 15 mA 0010 : 14 mA 0011 : 13 mA 0100 : 20 mA 0101 : 19 mA 0110 : 18 mA 0111 : 17 mA 1000 : 8 mA 1001 : 7 mA 1010 : 6 mA 1011 : 5 mA 1100 : 12 mA 1101 : 11 mA 1110 : 10 mA 1111 : 9 mA

9.6.1.21 Register 37 (offset = 37h) [reset = 00h]

Figure 108. Register 37

D7	D6	D5	D4	D3	D2	D1	D0
LINK LAYER TESTMODE			LINK LAYER RPAT	0	PULSE DET MODES		
R/W-0h			R/W-0h	W-0h	R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 37. Register 37 Field Descriptions

Bit	Field	Type	Reset	Description
D[7:5]	LINK LAYER TESTMODE	R/W	0h	Generates a pattern according to clause 5.3.3.8.2 of the JESD204B document 000 : Normal ADC data 001 : D21.5 (high-frequency jitter pattern) 010 : K28.5 (mixed-frequency jitter pattern) 011 : Repeats initial lane alignment (generates a K28.5 character and repeats lane alignment sequences continuously) 100 : 12-octet RPAT jitter pattern
D4	LINK LAYER RPAT	R/W	0h	Changes the running disparity in modified RPAT pattern test mode (only when link layer test mode = 100) 0 : Normal operation 1 : Changes disparity
D3	0	W	0h	Always write '0'
D[2:0]	PULSE DET MODES	R/W	0h	Selects different detection modes for SYSREF (subclass 1) and SYNC (subclass 2)

D2	D1	D0	FUNCTIONALITY
0	Don’t care	0	Allows all pulses to reset input clock dividers
1	Don’t care	0	Do not allow reset of analog clock dividers
Don’t care	0 to 1 transition	1	Allows one pulse immediately after the 0 to 1 transition to reset the divider

9.6.1.22 Register 38 (offset = 38h) [reset = 00h]

Figure 109. Register 38

D7	D6	D5	D4	D3	D2	D1	D0
FORCE LMFC COUNT	LMFC COUNT INIT					RELEASE ILANE SEQ	
R/W-0h	R/W-0h					R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 38. Register 38 Field Descriptions

Bit	Field	Type	Reset	Description
D7	FORCE LMFC COUNT	R/W	0h	Forces LMFC count 0 : Normal operation 1 : Enables using a different starting value for the LMFC counter
D[6:2]	LMFC COUNT INIT	R/W	0h	SYSREF receives the digital block and resets the LMFC count to '0'. K28.5 stops transmitting when the LMFC count reaches 31. The initial value that the LMFC count resets to can be set using LMFC COUNT INIT. In this manner, the Rx can be synchronized early because the Rx gets the LANE ALIGNMENT SEQUENCE early. The FORCE LMFC COUNT register bit must be enabled.
D[1:0]	RELEASE ILANE SEQ	R/W	0h	Delays the generation of the lane alignment sequence by 0, 1, 2, or 3 multiframes after the code group synchronization. 00 : 0 01 : 1 10 : 2 11 : 3

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

In a typical application (such as a dual-channel digitizer) the ADS42JBx9 is connected to a field-programmable gate array (FPGA) or application-specific integrated circuit (ASIC), as shown in Figure 110. A device clock and SYSREF signal must be provided to the ADC. TI recommends that the device clock and SYSREF are source synchronous (generated from a common source with matched trace lengths) if synchronizing multiple ADCs. An example of a device that can be used to generate a source-synchronous device clock and SYSREF is the LMK04828. The device clock frequency must be the same frequency as the desired sampling rate. The SYSREF period is required to be an integer multiple of the period of the multi-frame clock. Consequently, the frequency of SYSREF must be restricted to Equation 1

Device Clock Frequency / (n × K × F)

where:

- n = 1, 2, 3 and so forth,
- 1< K < 32 (set by SPI register address 2Dh), and
- F = 1, (two lanes per ADC mode), F = 2 (one lane per ADC mode). (1)

A large enough K is recommended (greater than 16) to absorb the lane skews and avoid data transmission errors across the JESD204B interface. The SYNC~ signal is used by the FPGA or ASIC to acknowledge the correction reception of comma characters from the ADC during the JESD204B link initialization process. During normal operation this signal must be logic 1 if there are no errors in the data transmission from the ADC to the FPGA or ASIC.

10.2 Typical Application

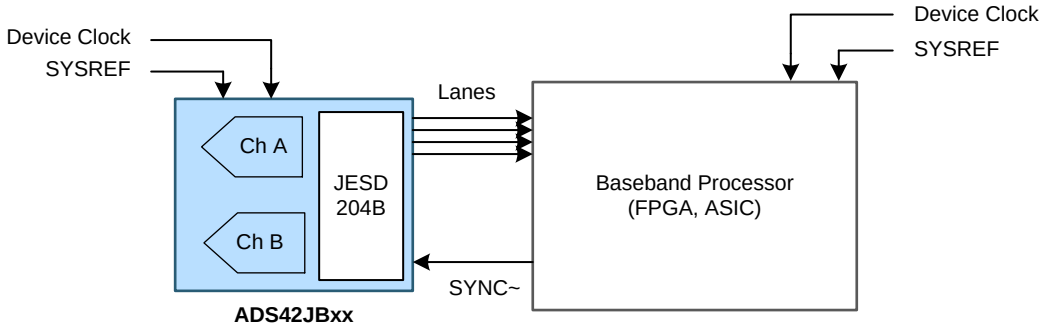


Figure 110. The ADS42JBx9 in a Dual-Channel Digitizer

10.2.1 Design Requirements

For this design example, use the parameters listed in Table 39 as the input parameters.

Table 39. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
f_{SAMPLE}	245.76 MSPS
Input frequency (IF)	10 MHz (Figure 122), 170 MHz (Figure 123)
Signal-to-noise ratio (SNR)	> 72 dBc
Spurious-free dynamic range (SFDR)	> 80 dBc
Second-order harmonic distortion (HD2)	> 90 dBc

10.2.2 Detailed Design Procedure

10.2.2.1 Analog Input

The analog input pins have analog buffers (running from the AVDD3V supply) that internally drive the differential sampling circuit. As a result of the analog buffer, the input pins present high input impedance to the external driving source (10-kΩ dc resistance and 4-pF input capacitance). The buffer helps isolate the external driving source from the switching currents of the sampling circuit. This buffering makes driving the buffered inputs easier than when compared to an ADC without the buffer.

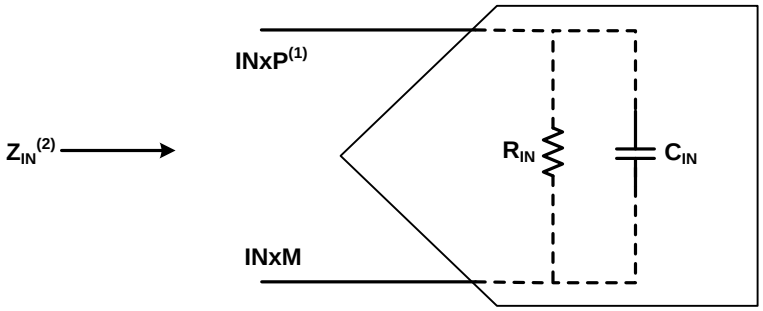
The input common-mode is set internally using a 5-kΩ resistor from each input pin to VCM so the input signal can be ac-coupled to the pins. Each input pin (INP, INM) must swing symmetrically between VCM + 0.5 V and VCM – 0.5 V, resulting in a 2-V $_{PP}$ differential input swing. When programmed for 2.5-V $_{PP}$ full-scale, each input pin must swing symmetrically between VCM + 0.625 V and VCM – 0.625 V.

The input sampling circuit has a high 3-dB bandwidth that extends up to 900 MHz (measured with a 50-Ω source driving a 50-Ω termination between INP and INM). The dynamic offset of the first-stage sub-ADC limits the maximum analog input frequency to approximately 250 MHz (with a 2.5-V_{PP} full-scale amplitude) and to approximately 400 MHz (with a 2-V_{PP} full-scale amplitude). This 3-dB bandwidth is different than the analog bandwidth of 900 MHz, which is only an indicator of signal amplitude versus frequency.

10.2.2.1.1 Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This technique improves the common-mode noise immunity and even-order harmonic rejection. A small resistor (5 Ω to 10 Ω) in series with each input pin is recommended to damp out ringing caused by package parasitics.

Figure 111, Figure 112, and Figure 113 illustrate the differential impedance ($Z_{IN} = R_{IN} \parallel C_{IN}$) at the ADC input pins. The presence of the analog input buffer results in an almost constant input capacitance up to 1 GHz.



(1) X = A or B.

(2) $Z_{IN} = R_{IN} \parallel (1 / j\omega C_{IN})$.

Figure 111. ADC Equivalent Input Impedance

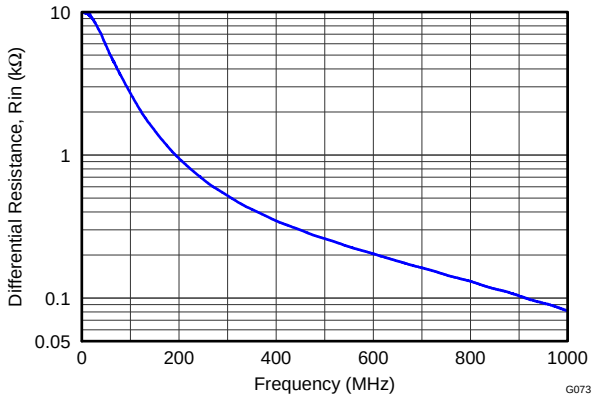


Figure 112. ADC Analog Input Resistance (R_{IN}) Across Frequency

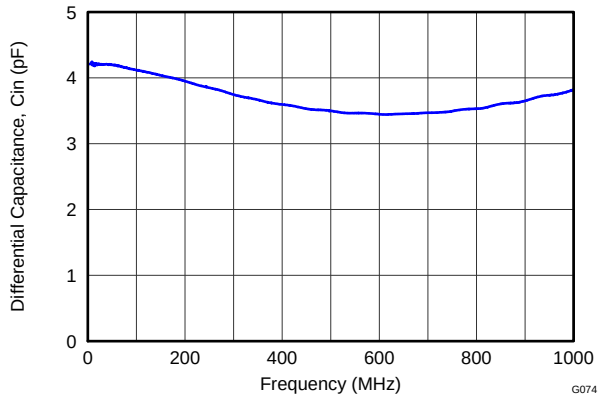


Figure 113. ADC Analog Input Capacitance (C_{IN}) Across Frequency

10.2.2.1.2 Driving Circuit

An example driving circuit configuration is shown in Figure 114. To optimize even-harmonic performance at high input frequencies (greater than the first Nyquist), the use of back-to-back transformers is recommended, as shown in Figure 114. Note that the drive circuit is terminated by 50 Ω near the ADC side. The ac-coupling capacitors allow the analog inputs to self-bias around the required common-mode voltage. An additional R-C-R (39 Ω - 6.8 pF - 39 Ω) circuit placed near device pins helps further improve HD3.

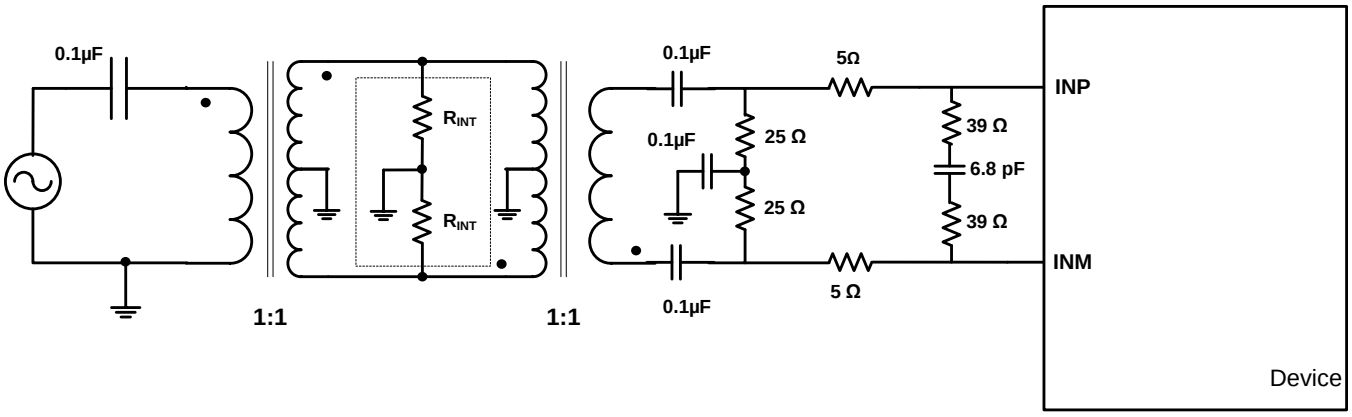


Figure 114. Drive Circuit for Input Frequencies up to 250 MHz

The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch and good performance is obtained for high-frequency input signals. An additional termination resistor pair may be required between the two transformers, as shown in Figure 114. The center point of this termination is connected to ground to improve the balance between the P (positive) and M (negative) sides. The values of the terminations between the transformers and on the secondary side must be chosen to obtain an effective 50 Ω (for a 50-Ω source impedance). For high input frequencies (> 250 MHz), the R-C-R circuit can be removed as indicated in Figure 115.

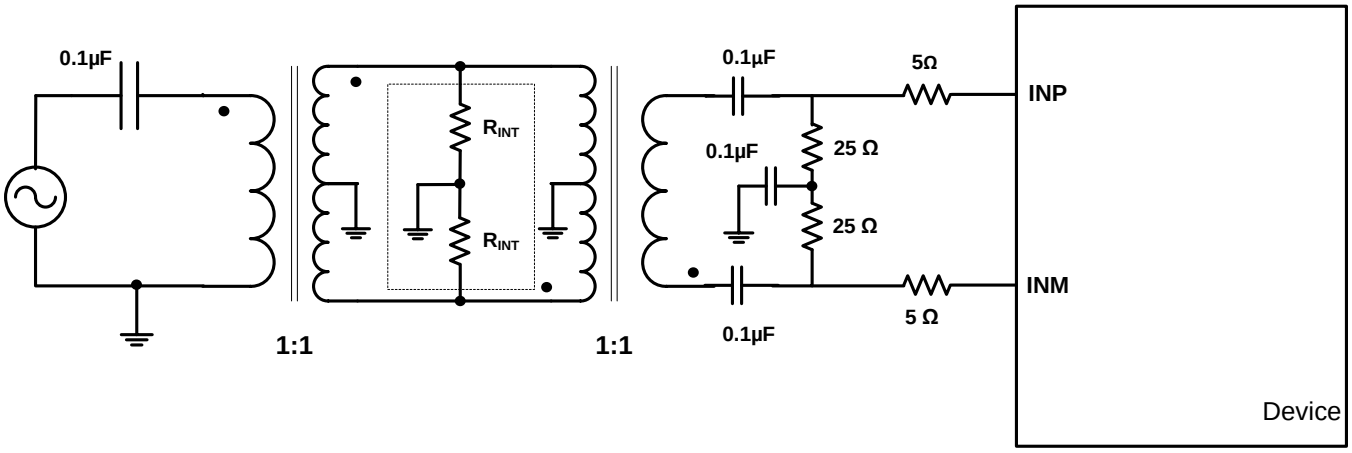


Figure 115. Drive Circuit for Input Frequencies > 250 MHz

10.2.2.2 Clock Input

The device clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to 1.4 V using internal 5-kΩ resistors. The self-bias clock inputs of the ADS42JB69 and ADS42JB49 can be driven by the transformer-coupled, sine-wave clock source or by the ac-coupled, LVPECL and LVDS clock sources, as shown in Figure 116, Figure 117, and Figure 118. Figure 119 details the internal clock buffer.

Note: R_T = termination resistor, if necessary.

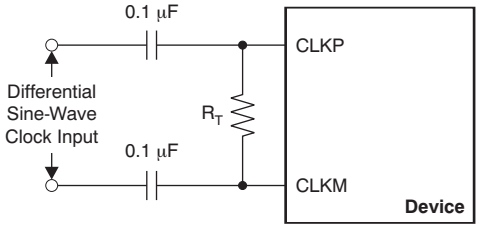


Figure 116. Differential Sine-Wave Clock Driving Circuit

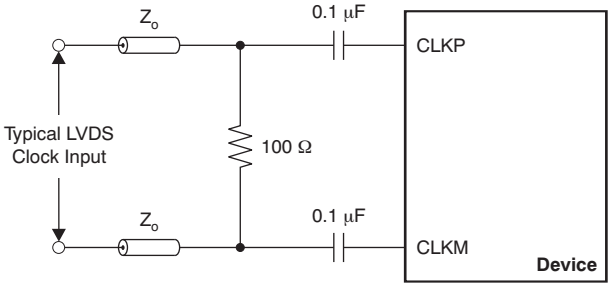


Figure 117. LVDS Clock Driving Circuit

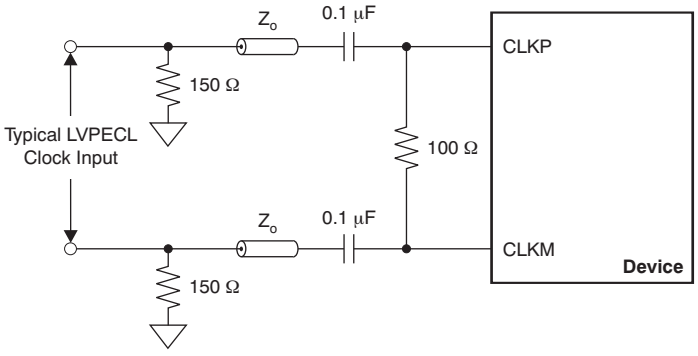
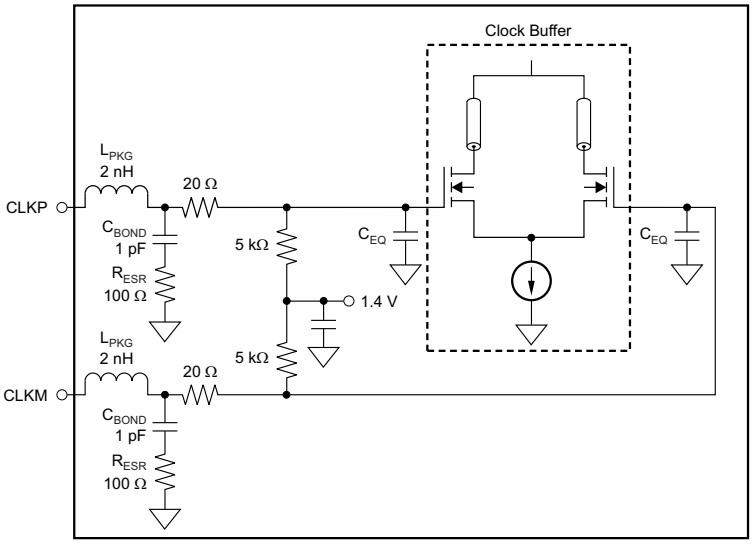


Figure 118. LVPECL Clock Driving Circuit



NOTE: C_{EQ} is 1 pF to 3 pF and is the equivalent input capacitance of the clock buffer.

Figure 119. Internal Clock Buffer

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1-µF capacitor, as shown in Figure 120. However, for best performance the clock inputs must be driven differentially, thereby reducing susceptibility to common-mode noise. For high input frequency sampling, TI recommends using a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input.

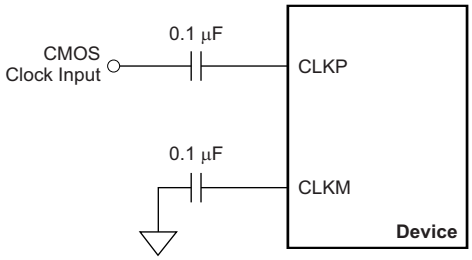


Figure 120. Single-Ended Clock Driving Circuit

10.2.2.2.1 SNR and Clock Jitter

The signal-to-noise ratio (SNR) of the ADC is limited by three different factors, as shown in Equation 2. Quantization noise is typically not noticeable in pipeline converters and is 96 dBFS for a 16-bit ADC. Thermal noise limits SNR at low input frequencies and clock jitter sets SNR for higher input frequencies.

$$SNR_{ADC}[dBc] = -20 \times \log \sqrt{\left(10 - \frac{SNR_{Quantization\_Noise}}{20}\right)^2 + \left(10 - \frac{SNR_{ThermalNoise}}{20}\right)^2 + \left(10 - \frac{SNR_{Jitter}}{20}\right)^2} \quad (2)$$

SNR limitation is a result of sample clock jitter and can be calculated by Equation 3:

$$SNR_{Jitter}\ [dBc] = -20 \times \log(2\pi \times f_{IN} \times t_{Jitter}) \quad (3)$$

The total clock jitter (T_{Jitter}) has three components: the internal aperture jitter (85 f_S for the device) is set by the noise of the clock input buffer, the external clock jitter, and the jitter from the analog input signal. T_{Jitter} can be calculated by Equation 4:

$$T_{Jitter} = \sqrt{(T_{Jitter,Ext.Clock\_Input})^2 + (T_{Aperture\_ADC})^2} \quad (4)$$

External clock jitter can be minimized by using high-quality clock sources and jitter cleaners as well as band-pass filters at the clock input while a faster clock slew rate improves ADC aperture jitter. The device has a 74.1-dBFS thermal noise and an 85-f_S internal aperture jitter. The SNR value depends on the amount of external jitter for different input frequencies, as shown in Figure 121.

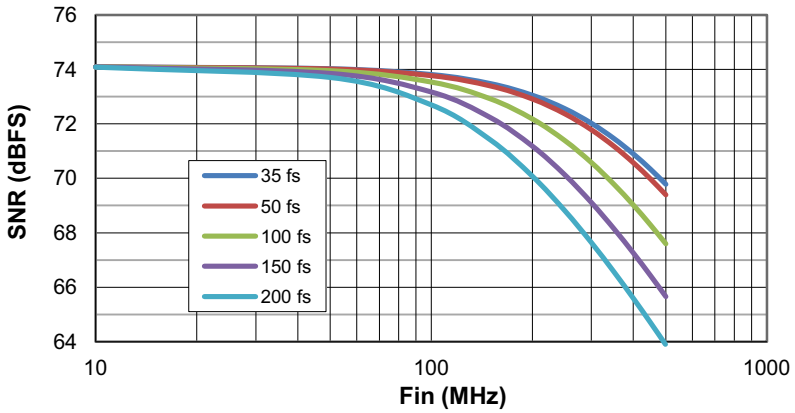


Figure 121. SNR versus Input Frequency and External Clock Jitter

10.2.3 Application Curves

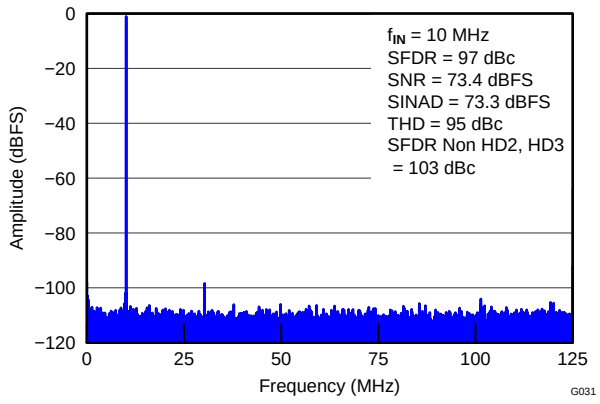


Figure 122. FFT for 10-MHz Input Signal

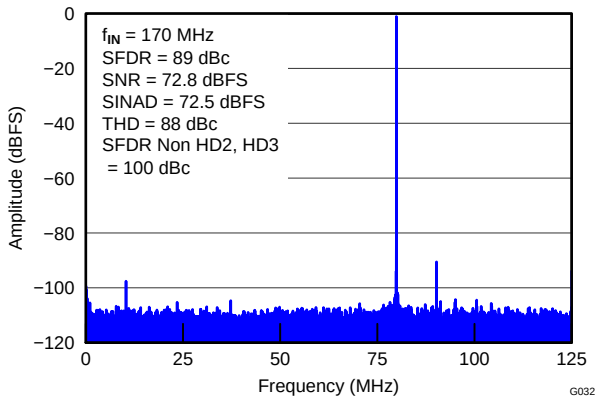


Figure 123. FFT for 170-MHz Input Signal

11 Power Supply Recommendations

Four different power supply rails are required for ADS42JBxx device family:

- A 3.3-V AVDD3V supply is used to supply power to the analog buffers.
- A 1.8-V AVDD supply is used to supply power to the analog core of the ADC.
- A 1.8-V DRVDD supply is used to supply power to the digital core of the ADC.
- A 1.8-V IOVDD supply is used to supply power to the output buffers.

TI recommends providing the 1.8-V digital and analog supplies from separate sources because of the switching activities on the digital rail. Both IOVDD and DRVDD can be supplied from a common source and a ferrite bead is recommended on each rail. An example power-supply scheme suitable for the ADS42JBx9 device family is shown in Figure 124. In this example supply scheme, AVDD is provided from a dc-dc converter and a low-dropout (LDO) regulator to increase the efficiency of the implementation. Where cost and area rather than power-supply efficiency are the main design goals, AVDD can be provided using only the LDO.

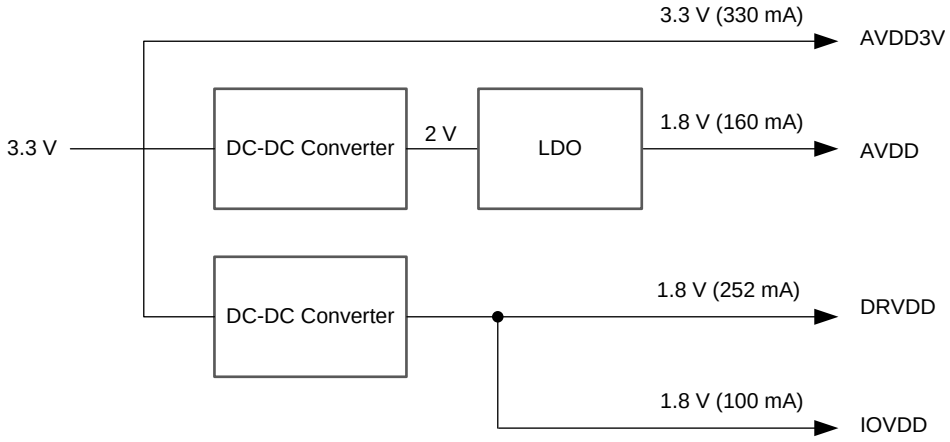


Figure 124. Example Power-Supply Scheme

12 Layout

12.1 Layout Guidelines

- The length of the positive and negative traces of a differential pair must be matched to within 2 mils of each other.
- Each differential pair length must be matched within 10 mils of each other.
- When the ADC is used on the same printed circuit board (PCB) with a digital intensive component (such as an FPGA or ASIC), separate digital and analog ground planes must be used. Do not overlap these separate ground planes to minimize undesired coupling.
- Connect decoupling capacitors directly to ground and place these capacitors close to the ADC power pins and the power-supply pins to filter high-frequency current transients directly to the ground plane, as shown in Figure 125.

Layout Guidelines (continued)

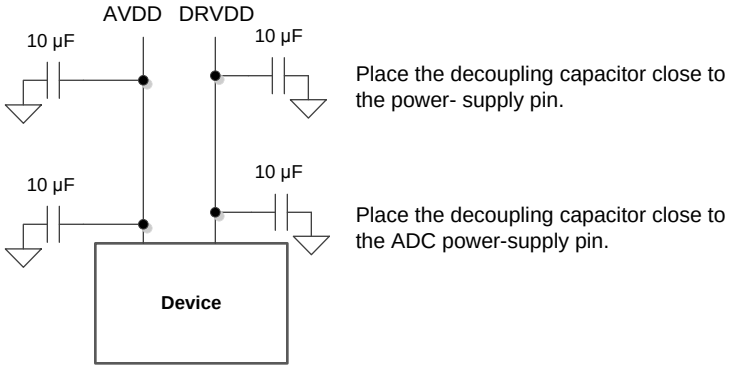


Figure 125. Recommended Placement of Power-Supply Decoupling Capacitors

- Ground and power planes must be wide enough to keep the impedance very low. In a multilayer PCB, one layer each must be dedicated to ground and power planes.
- All high-speed SERDES traces must be routed straight with minimum bends. Where a bend is necessary, avoid making very sharp right angle bends in the trace.
- FR4 material can be used for the PCB core dielectric, up to the maximum 3.125 Gbps bit rate supported by the ADS42JBx9 device family. Path loss can be compensated for by adjusting the drive strength from the device using SPI register 36h.

12.2 Layout Example

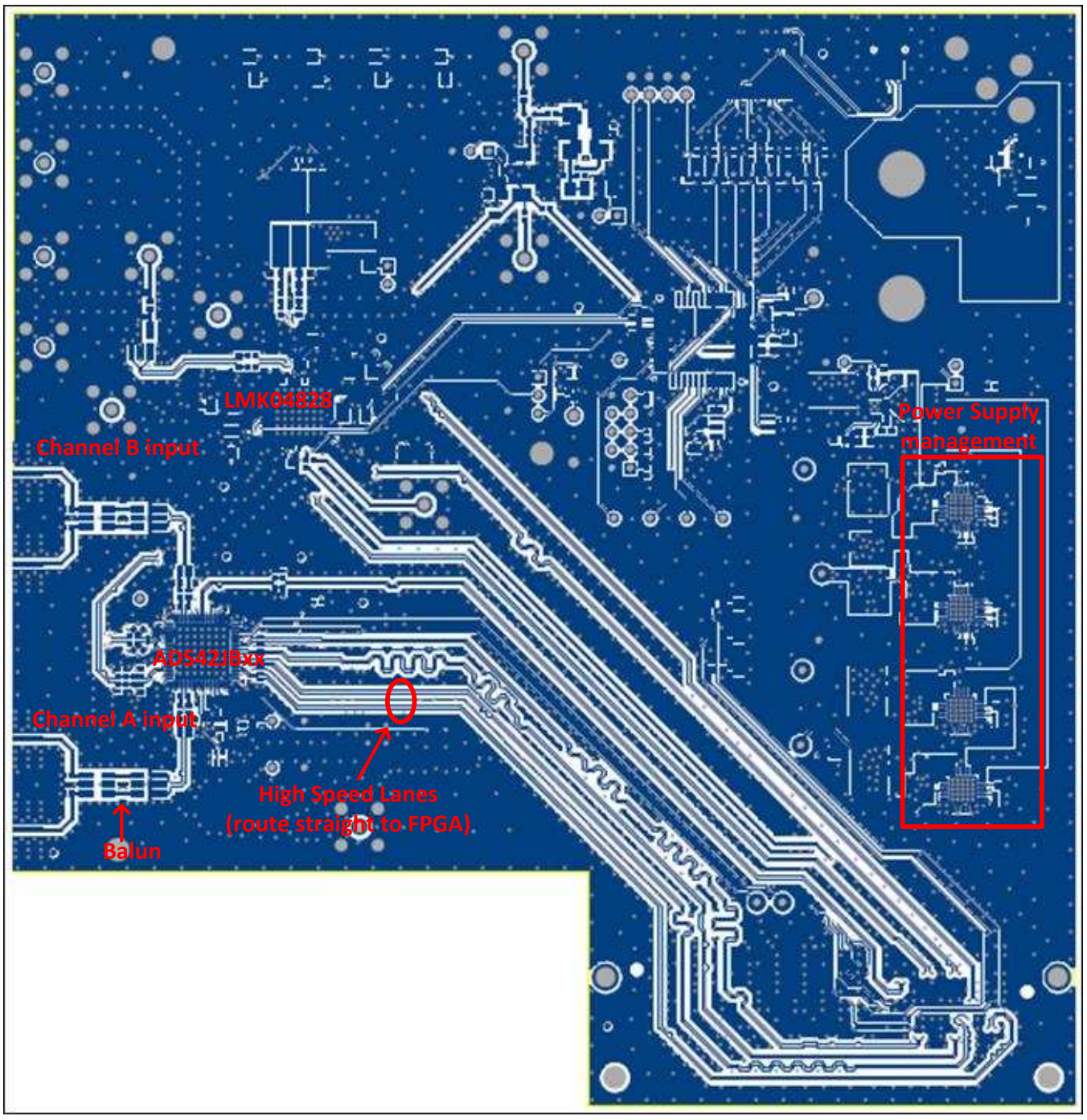


Figure 126. ADS42JBx9 EVM Top Layer

13 器件和文档支持

13.1 器件支持

13.1.1 器件命名规则

13.1.1.1 技术参数定义

交流电源抑制比 (AC PSRR)： AC PSRR 测量的是 ADC 对电源电压变化的抑制能力。 如果 ΔV_{SUP} 表示电源电压的变化，ΔV_{OUT} 表示 ADC 输出编码的相应变化（相对输入而言），则：

$$PSRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{SUP}} \text{ (Expressed in dBc)} \quad (5)$$

模拟带宽： 基频功率相对低频值下降 3dB 时的模拟输入频率。

孔径延迟： 从输入采样时钟的上升沿到实际发生采样之间的延迟时间。 该延迟在各通道中会有所不同。 最大差值被定义为孔径延迟差异（通道间）。

孔径不确定性（抖动）： 采样间的孔径延迟差异。

时钟脉冲宽度和占空比： 时钟信号的占空比为时钟信号保持逻辑高电平的时间（时钟脉冲宽度）与时钟信号周期的比值。 占空比通常以百分比的形式表示。 理想差分正弦波时钟的占空比为 50%。

共模抑制比 (CMRR)： CMRR 测量的是 ADC 对模拟输入共模变化的抑制能力。 如果 ΔV_{CM_IN} 表示输入引脚的共模电压变化，ΔV_{OUT} 表示 ADC 输出编码的相应变化（相对输入而言），则：

$$CMRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{CM}} \text{ (Expressed in dBc)} \quad (6)$$

串扰（仅限多通道 ADC）： 串扰测量的是目标通道与其相邻通道之间的内部信号耦合。 串扰分两种情况：一种是与紧邻通道（近端通道）之间的耦合，另一种是与跨封装通道（远端通道）之间的耦合。 通常采用对邻近通道施加满量程信号的方式来测量串扰。 串扰是指耦合信号功率（在目标通道的输出端测得）与邻近通道输入端所施加信号功率的比值。 串扰通常以 dBc 为单位进行表示。

直流电源抑制比 (DC PSRR)： DC PSSR 是偏移误差变化量与模拟电源电压变化量的比值。 DC PSRR 通常以 mV/V 为单位进行表示。

微分非线性 (DNL)： 理想 ADC 对模拟输入值进行编码转换时以 1 LSB 为步长。 DNL 是指任意单个步长与这一理想值之间的偏差（以 LSB 为计量单位）。

有效位数 (ENOB)： ENOB 测量的是转换器相对于理论限值（基于量化噪声）的性能。

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (7)$$

增益误差： 增益误差是指 ADC 实际输入满量程范围与其理想值的偏差。 增益误差以理想输入满量程范围的百分比形式表示。 增益误差包括两部分：基准不精确所导致的误差 (E_{GREF}) 和通道所导致的误差 (E_{GCHAN})。 这两种误差分别定义为 E_{GREF} 和 E_{GCHAN}。

对于一阶近似，总增益误差 $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$。

例如，如果 E_{TOTAL} = ±0.5%，则满量程输入范围为 (1 – 0.5 / 100) x FS_{ideal} 至 (1 + 0.5 / 100) × FS_{ideal}。

积分非线性 (INL)： INL 是 ADC 传递函数与其最小二乘法曲线拟合所确定的最佳拟合曲线的偏差（以 LSB 为计量单位）。

最大转换速率： 执行指定操作时所采用的最大采样率。 除非另外注明，否则所有参数测试均以该采样率执行。

最小转换速率： ADC 正常工作时的最小采样率。

偏移误差： 偏移误差是指 ADC 实际平均空闲通道输出编码与理想平均空闲通道输出编码之间的差值（以 LSB 数表示）。 该数量通常转换为毫伏。

信噪比和失真 (SINAD)： SINAD 是指基频功率 (P_S) 与所有其他频谱成分（包括噪声 (P_N) 和失真 (P_D)，但不包括直流）功率的比值。

器件支持 **(**接下页**)**

$$SNR = 10Log^{10}\frac{P_S}{P_N} \quad (8)$$

$$SINAD = 10Log^{10}\frac{P_S}{P_N + P_D} \quad (9)$$

当基频的绝对功率用作基准时，SINAD 以 dBc（相对于载波的分贝数）为单位；当基频功率被外推至转换器满量程范围时，SINAD 以 dBFS（相对于满量程的分贝数）为单位。

信噪比 (SNR)： SNR 是指基频功率 (P_S) 与噪底功率 (P_N) 的比值，不包括直流功率和前 9 个谐波的功率。

当基频的绝对功率用作基准时，SNR 以 dBc（相对于载波的分贝数）为单位；当基频功率被外推至转换器满量程范围时，SNR 以 dBFS（相对于满量程的分贝数）为单位。

无杂散动态范围 (SFDR)： 基频功率与最高的其他频谱成分（毛刺或谐波）功率的比值。 SFDR 通常以 dBc 为单位（相对于载波的分贝数）。

温度漂移： 温度漂移系数（相对于增益误差和偏移误差）指定参数从 T_{MIN} 到 T_{MAX} 每摄氏度的变化量。 温度漂移的计算方法是用参数在 T_{MIN} 至 T_{MAX} 范围内的最大变化量除以 $T_{MAX} – T_{MIN}$ 的值。

总谐波失真 (THD)： THD 是指基频功率 (P_S) 与前 9 个谐波功率 (P_D) 的比值。

$$THD = 10Log^{10}\frac{P_S}{P_N} \quad (10)$$

THD 通常以 dBc 为单位（相对于载波的分贝数）。

双频互调失真 (IMD3)： IMD3 是指基频功率（f_1 和 f_2 频率处）与最差频谱成分（$2f_1 – f_2$ 或 $2f_2 – f_1$ 频率处）功率的比值。 当基频的绝对功率用作基准时，IMD3 以 dBc（相对于载波的分贝数）为单位；当基频功率被外推至转换器满量程范围时，IMD3 以 dBFS（相对于满量程的分贝数）为单位。

电压过载恢复： 使过载的模拟输入端的误差恢复至 1% 以下所需的时钟数。 该技术参数的测试方法是分别施加具有 6dB 正过载和负过载的正弦波信号。 然后记录下过载后前几个采样（相对于期望值）的偏差。

13.2 文档支持

13.2.1 相关文档

《LMK04828 数据表》，SNAS605

13.3 相关链接

以下表格列出了快速访问链接。 范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **40.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
ADS42JB49	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ADS42JB69	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

13.4 商标

All trademarks are the property of their respective owners.

13.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

14 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS42JB49IRGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	Call TI | Nipdau	Level-3-260C-168 HR	-40 to 85	AZ42JB49
ADS42JB49IRGCR.A	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	AZ42JB49
ADS42JB49IRGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	Call TI | Nipdau	Level-3-260C-168 HR	-40 to 85	AZ42JB49
ADS42JB49IRGCT.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	AZ42JB49
ADS42JB69IRGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ42JB69
ADS42JB69IRGCR.A	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ42JB69
ADS42JB69IRGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU | NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ42JB69
ADS42JB69IRGCT.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ42JB69
ADS42JB69IRGCTG4.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

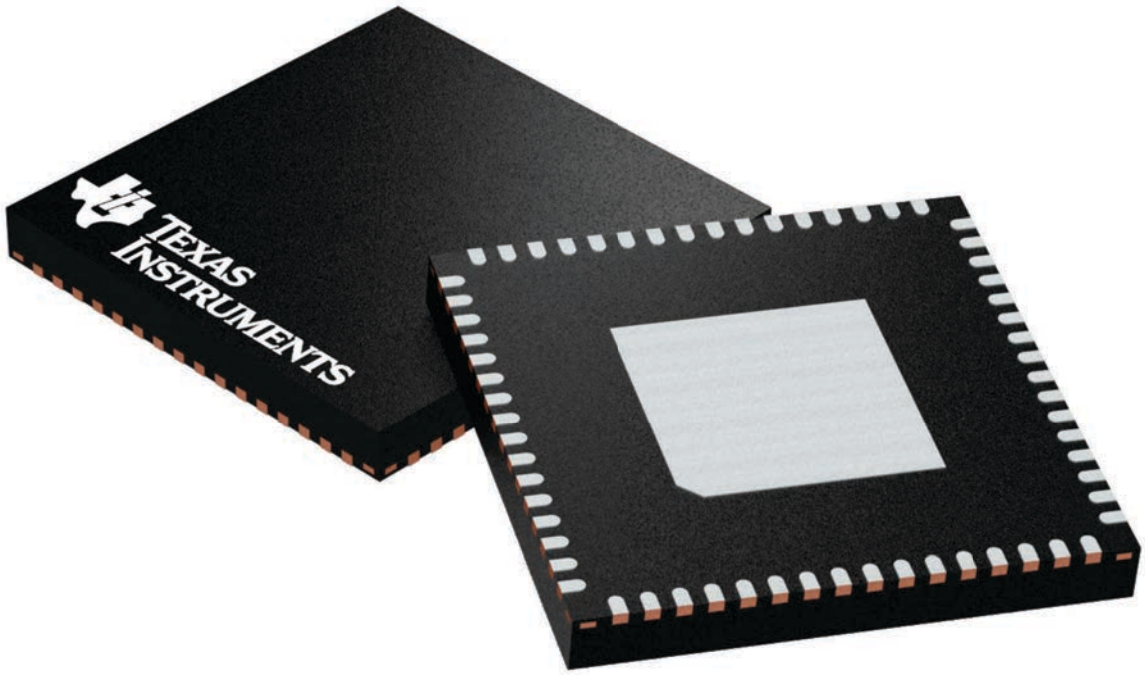
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

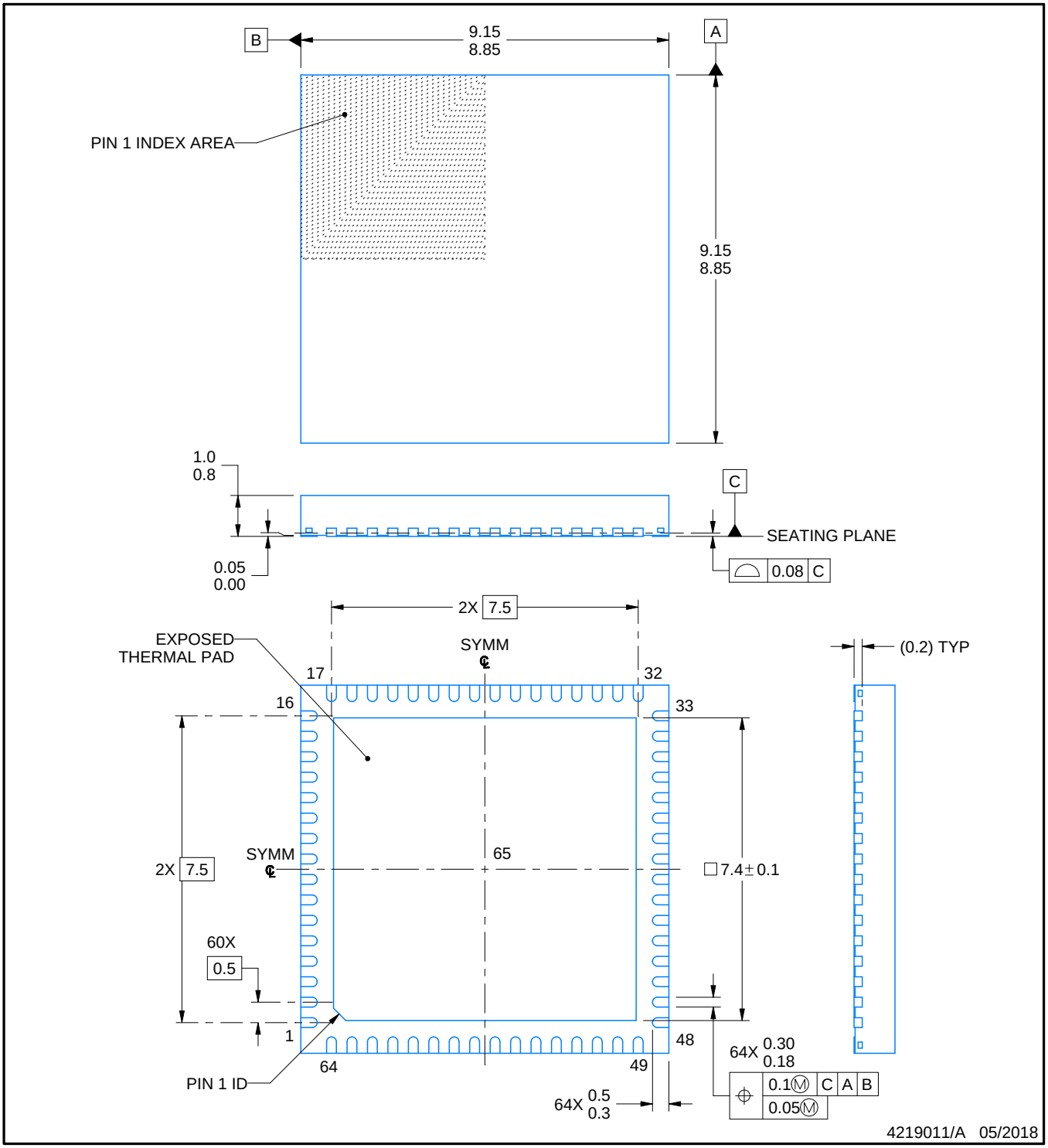
4224597/A

RGC0064H

PACKAGE OUTLINE

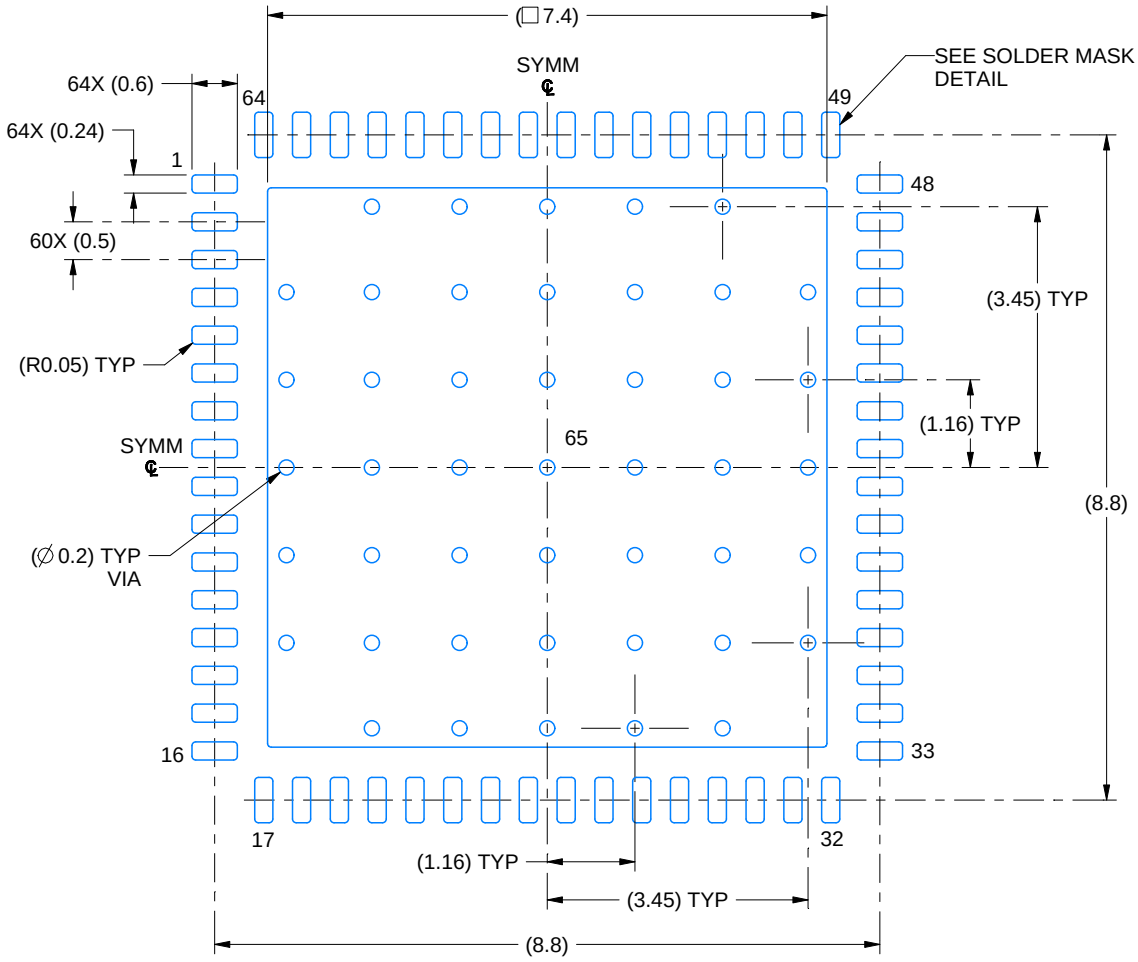
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

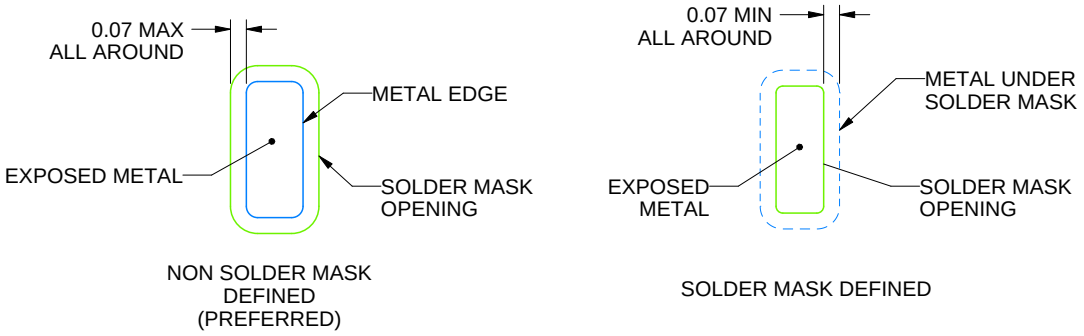


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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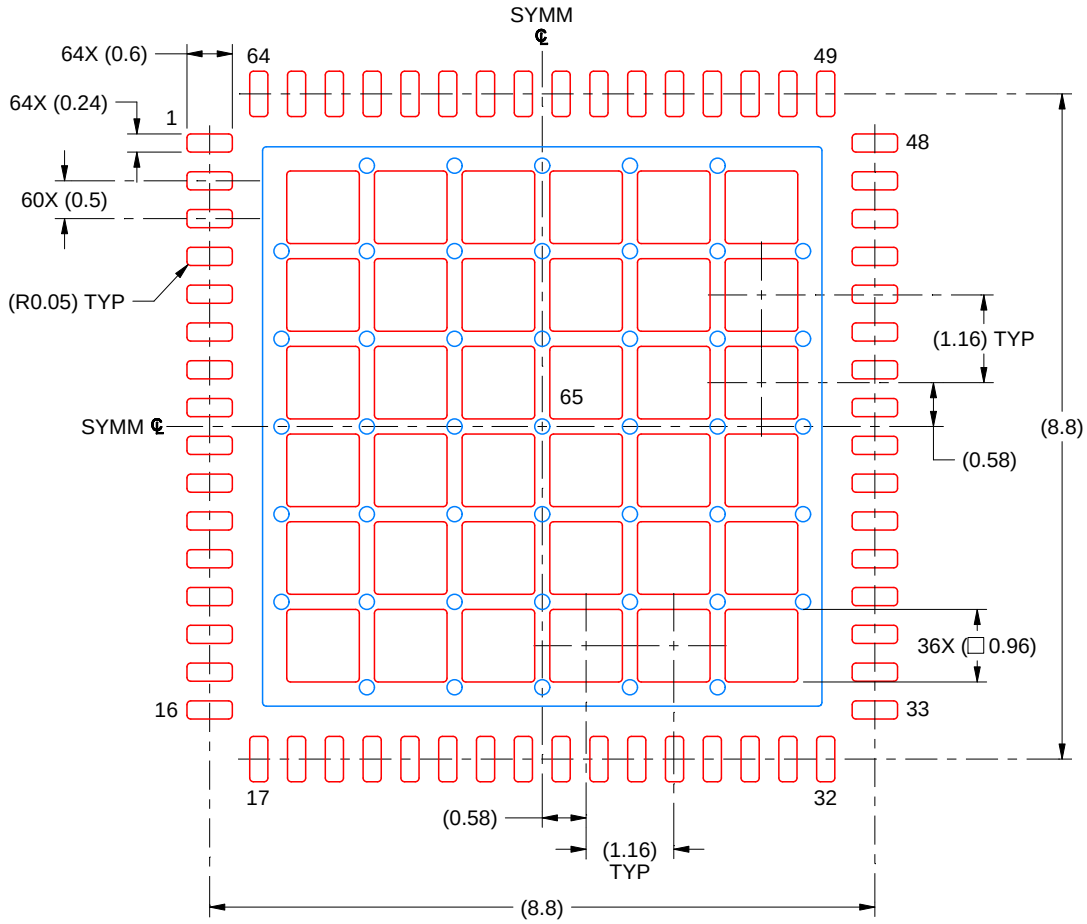
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
61% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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