# ADS4229 双通道、12 位、250MSPS 超低功耗 ADC

## 1 特性

- 最大采样率：250MSPS
- 使用单个 1.8V 电源时的超低功耗：
  - 250MSPS 时总体功耗为 545mW
- 高动态性能：
  - 170MHz 时为 80.8dBc 无杂散动态范围 (SFDR)
  - 170MHz 时信噪比 (SNR) 为 69.4dBFS
- 串扰：185MHz 时大于 90dB
- 针对
  SNR 和 SFDR 折衷的可编程增益高达 6dB
- DC 偏移校正
- 输出接口选项：
  - 1.8V 并行 CMOS 接口
  - 支持可编程摆幅的双数据速率 (DDR) 低压差分信令 (LVDS)：
    - 标准摆幅：350mV
    - 低摆幅：200mV
- 支持低输入时钟振幅
  低至 200$mV_{PP}$
- 封装：9mm x 9mm，64 引脚四方扁平无引线 (QFN) 封装

## 2 应用

- 无线通信基础设施
- 由软件定义的无线电
- 功率放大器线性化

## 3 说明

ADS4229 是 ADS42xx 双通道，12 位和 14 位模数转换器 (ADC) 超低功耗系列产品。 采用创新设计技术实现高动态性能，而同时功耗极低（采用一个 1.8 V 电源）。 该拓扑使 ADS4229 非常适合多载波、宽带宽通信应用。

ADS4229 具有可被用于在较低满量程输入范围内改进无杂散动态范围 (SFDR) 性能的增益选项。 这个器件还包括一个 dc 偏移校正环路，此环路可被用于消除 ADC 偏移。 双数据速率 (DDR) 低压差分信令 (LVDS) 和并行互补金属氧化物半导体 (CMOS) 数字输出接口采用一个紧凑型 QFN-64 PowerPAD™ 封装。

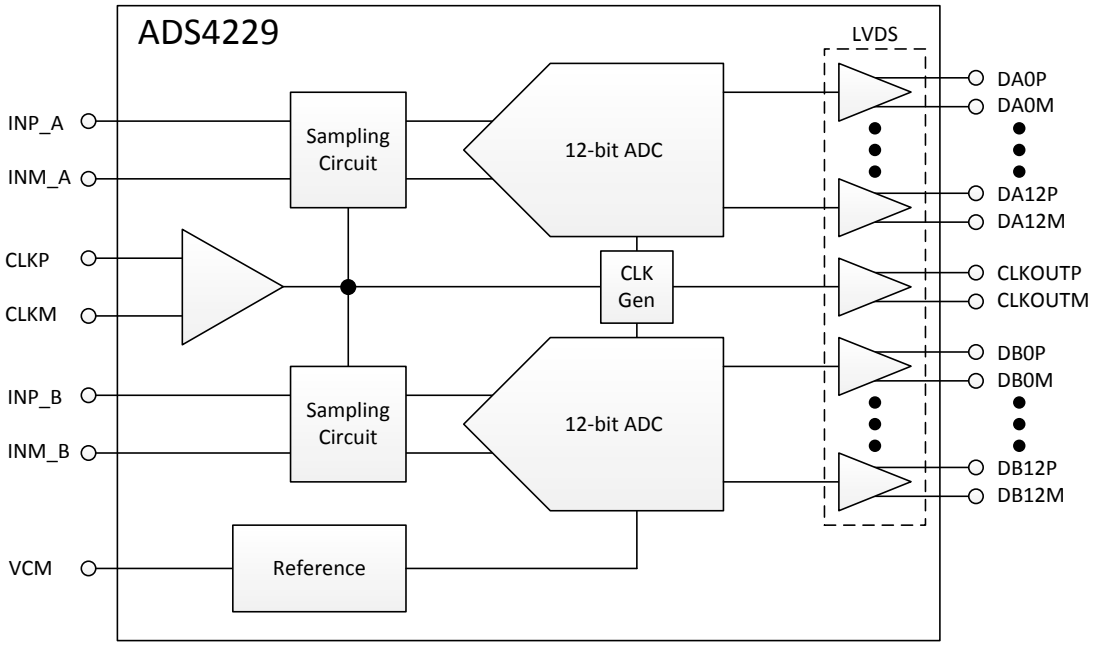
此器件包含内部基准，而删除了传统基准引脚和相关的去耦合电容器。 ADS4229 可在工业温度范围（-40°C 至 +85°C）内工作。

器件信息(1)

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| ADS4229 | VQFN (64) | 9.00mm x 9.00mm |

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

**ADS4229 框图**



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## 4 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision B (August 2012) to Revision C** **Page**

- 已添加 *引脚配置和功能*部分，*ESD 额定值*表，*特性描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1

**Changes from Revision A (October 2011) to Revision B** **Page**

- 已更改 *高动态性能的第一子着重号*特性着重号 ... 1
- Changed footnote 1 in CMOS Timings at Lower Sampling Frequencies ... 16
- Changed row D5 and consolidated the two DB rows in Table 10 ... 38
- Changed Register Address D5h ... 47
- Changed title of Register Address DBh, consolidated two DBh registers into one ... 47

**Changes from Original (June 2011) to Revision A** **Page**

- Changed ADS4229 *Input Common-Mode Voltage* parameter in Table 1 ... 5
- Changed *AC power-supply rejection ratio* parameter test condition in ADS4229 Electrical Characteristics table ... 12
- Updated Figure 3 ... 17
- Updated Figure 25 ... 23
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- Changed *Time Constant, $TC_{CLK}$ × 1/$f_S$ (ms)* column and footnote 1 in Table 3 ... 29
- Changed Revised *Channel Standby* section ... 29
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- Changed description of bits[7:2] in Register Address 40h ..... 42
- Updated Register Address D7h and Register Address D8h tables ..... 47
- Updated first paragraph of *Analog Input* section ..... 49
- Updated first paragraph of *Driving Circuit* subsection ..... 50

# 5 Device Comparison Table

| | 65 MSPS | 125 MSPS | 160 MSPS | 250 MSPS |
|---|---|---|---|---|
| ADS422x 12-bit family(1) | ADS4222 | ADS4225 | ADS4226 | ADS4229 |
| ADS424x 14-bit family(1) | ADS4242 | ADS4245 | ADS4246 | ADS4249 |

(1) See Table 1 for details on migrating from the ADS62P49 family.

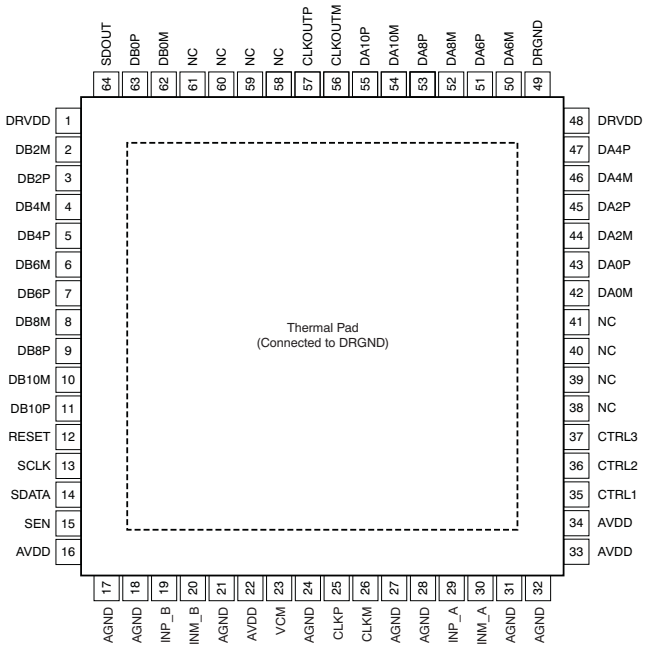
The ADS4229 is pin-compatible with the previous generation ADS62P49 data converter; this similar architecture enables easy migration. However, there are some important differences between the two device generations, summarized in Table 1.

**Table 1. Migrating from the ADS62P49**

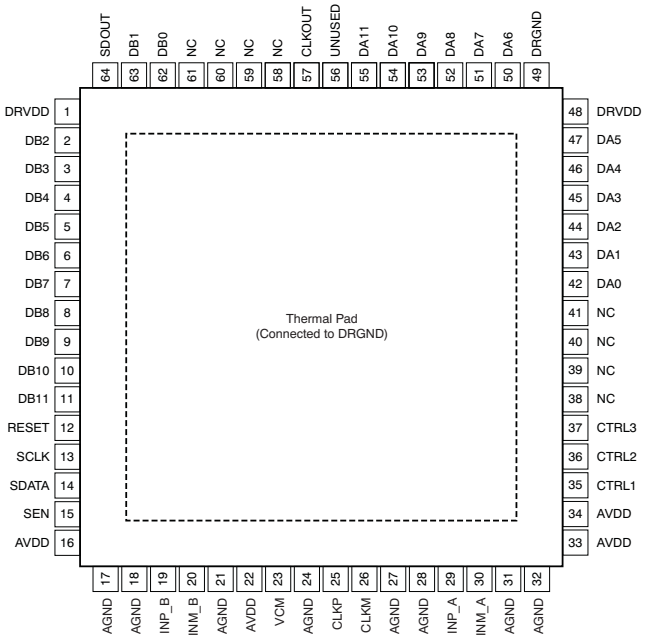
| ADS62P49 FAMILY | ADS4229 |
|---|---|
| **PINS** | |
| Pin 22 is NC (not connected) | Pin 22 is AVDD |
| Pins 38 and 58 are DRVDD | Pins 38 and 58 are NC (do not connect, must be floated) |
| Pins 39 and 59 are DRGND | Pins 39 and 59 are NC (do not connect, must be floated) |
| **SUPPLY** | |
| AVDD is 3.3 V | AVDD is 1.9 V |
| DRVDD is 1.8 V | No change |
| **INPUT COMMON-MODE VOLTAGE** | |
| VCM is 1.5 V | VCM is 0.95 V |
| **SERIAL INTERFACE** | |
| Protocol: 8-bit register address and 8-bit register data | No change in protocol<br>New serial register map |
| **EXTERNAL REFERENCE** | |
| Supported | Not supported |

# 6 Pin Configuration and Functions

**RGC Package (LVDS Mode)**
**64-Pin VQFN**
**Top View**




**RGC Package (CMOS Mode)**
**64-Pin VQFN**
**Top View**




(1) The PowerPAD is connected to DRGND.

NOTE: NC = do not connect; must float.

**Pin Functions (LVDS Mode)**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| AGND | 17 | I | Analog ground |
| | 18 | | |
| | 21 | | |
| | 24 | | |
| | 27 | | |
| | 28 | | |
| | 31 | | |
| | 32 | | |
| AVDD | 16 | I | Analog power supply |
| | 22 | | |
| | 23 | | |
| | 34 | | |
| CLKM | 26 | I | Differential clock negative input |
| CLKP | 25 | I | Differential clock positive input |
| CTRL1 | 35 | I | Digital control input pins. Together, they control the various power-down modes. |
| CTRL2 | 36 | I | Digital control input pins. Together, they control the various power-down modes. |
| CTRL3 | 37 | I | Digital control input pins. Together, they control the various power-down modes. |
| CLKOUTP | 57 | O | Differential output clock, true |

## Pin Functions (LVDS Mode) (continued)

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| CLKOUTM | 56 | O | Differential output clock, complement |
| DA0M | 42 | O | Channel A differential output data pair, D0 and D1 multiplexed |
| DA0P | 43 | | |
| DA2M | 44 | O | Channel A differential output data D2 and D3 multiplexed |
| DA2P | 45 | | |
| DA4M | 46 | O | Channel A differential output data D4 and D5 multiplexed |
| DA4P | 47 | | |
| DA6M | 50 | O | Channel A differential output data D6 and D7 multiplexed |
| DA6P | 51 | | |
| DA8M | 52 | O | Channel A differential output data D8 and D9 multiplexed |
| DA8P | 53 | | |
| DA10M | 54 | O | Channel A differential output data D10 and D11 multiplexed |
| DA10P | 55 | | |
| DB0M | 62 | O | Channel B differential output data pair, D0 and D1 multiplexed |
| DB0P | 63 | | |
| DB2M | 2 | O | Channel B differential output data D2 and D3 multiplexed |
| DB2P | 3 | | |
| DB4M | 4 | O | Channel B differential output data D4 and D5 multiplexed |
| DB4P | 5 | | |
| DB6M | 6 | O | Channel B differential output data D6 and D7 multiplexed |
| DB6P | 7 | | |
| DB8M | 8 | O | Channel B differential output data D8 and D9 multiplexed |
| DB8P | 9 | | |
| DB10M | 10 | O | Channel B differential output data D10 and D11 multiplexed |
| DB10P | 11 | | |
| DRGND | 49 | I | Output buffer ground |
| | PAD | | |
| DRVDD | 1 | I | Output buffer supply |
| | 48 | | |
| INP_A | 29 | I | Differential analog positive input, channel A |
| INM_A | 30 | I | Differential analog negative input, channel A |
| INP_B | 19 | I | Differential analog positive input, channel B |
| INM_B | 20 | I | Differential analog negative input, channel B |
| NC | 38 | — | Do not connect, must be floated |
| | 39 | | |
| | 40 | | |
| | 41 | | |
| | 58 | | |
| | 59 | | |
| | 60 | | |
| | 61 | | |
| RESET | 12 | I | Serial interface RESET input.<br>When using the serial interface mode, the internal registers must be initialized through a hardware RESET by applying a high pulse on this pin or by using the software reset option; refer to the *Serial Interface Configuration* section.<br>In parallel interface mode, the RESET pin must be permanently tied high. SCLK and SEN are used as parallel control pins in this mode. This pin has an internal 150-kΩ pull-down resistor. |

## Pin Functions (LVDS Mode) (continued)

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| SCLK | 13 | I | This pin functions as a serial interface clock input when RESET is low. It controls the low-speed mode selection when RESET is tied high; see Table 7 for detailed information. This pin has an internal 150-kΩ pull-down resistor. |
| SDATA | 14 | I | Serial interface data input; this pin has an internal 150-kΩ pull-down resistor. |
| SDOUT | 64 | O | This pin functions as a serial interface register readout when the READOUT bit is enabled. When READOUT = 0, this pin is put into a high-impedance state. |
| VCM | 23 | O | This pin outputs the common-mode voltage (0.95 V) that can be used externally to bias the analog input pins |

## Pin Functions (CMOS Mode)

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| AGND | 17 | I | Analog ground |
| | 18 | | |
| | 21 | | |
| | 24 | | |
| | 27 | | |
| | 28 | | |
| | 31 | | |
| | 32 | | |
| AVDD | 16 | I | Analog power supply |
| | 22 | | |
| | 33 | | |
| | 34 | | |
| CLKM | 26 | I | Differential clock negative input |
| CLKOUT | 57 | O | CMOS output clock |
| CLKP | 25 | I | Differential clock positive input |
| CTRL1 | 35 | I | Digital control input pins. Together, they control various power-down modes. |
| CTRL2 | 36 | I | Digital control input pins. Together, they control various power-down modes. |
| CTRL3 | 37 | I | Digital control input pins. Together, they control various power-down modes. |
| DA0 | 42 | O | Channel A ADC output data bits, CMOS levels |
| DA1 | 43 | | |
| DA2 | 44 | | |
| DA3 | 45 | | |
| DA4 | 46 | | |
| DA5 | 47 | | |
| DA6 | 50 | | |
| DA7 | 51 | | |
| DA8 | 52 | | |
| DA9 | 53 | | |
| DA10 | 54 | | |
| DA11 | 55 | | |

## Pin Functions (CMOS Mode) (continued)

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| DB0 | 62 | O | Channel B ADC output data bits, CMOS levels |
| DB1 | 63 | | |
| DB2 | 2 | | |
| DB3 | 3 | | |
| DB4 | 4 | | |
| DB5 | 5 | | |
| DB6 | 6 | | |
| DB7 | 7 | | |
| DB8 | 8 | | |
| DB9 | 9 | | |
| DB10 | 10 | | |
| DB11 | 11 | | |
| DRGND | 49 | I | Output buffer ground |
| | PAD | | |
| DRVDD | 1 | I | Output buffer supply |
| | 48 | | |
| NC | — | — | Do not connect, must be floated |
| RESET | 12 | I | Serial interface RESET input.<br>When using the serial interface mode, the internal registers must be initialized through a hardware RESET by applying a high pulse on this pin or by using the software reset option; refer to the *Serial Interface Configuration* section.<br>In parallel interface mode, the RESET pin must be permanently tied high. SDATA and SEN are used as parallel control pins in this mode. This pin has an internal 150-kΩ pull-down resistor. |
| INM_A | 30 | I | Differential analog negative input, channel A |
| INP_A | 29 | I | Differential analog positive input, channel A |
| INM_B | 20 | I | Differential analog negative input, channel B |
| INP_B | 19 | I | Differential analog positive input, channel B |
| SCLK | 13 | I | This pin functions as a serial interface clock input when RESET is low. It controls the low-speed mode when RESET is tied high; see Table 7 for detailed information. This pin has an internal 150-kΩ pull-down resistor. |
| SDATA | 14 | I | Serial interface data input; this pin has an internal 150-kΩ pull-down resistor. |
| SDOUT | 64 | O | This pin functions as a serial interface register readout when the READOUT bit is enabled. When READOUT = 0, this pin is put into a high-impedance state. |
| SEN | 15 | I | This pin functions as a serial interface enable input when RESET is low. It controls the output interface and data format selection when RESET is tied high; see Table 8 for detailed information. This pin has an internal 150-kΩ pull-up resistor to AVDD. |
| VCM | 23 | O | This pin outputs the common-mode voltage (0.95 V) that can be used externally to bias the analog input pins |
| UNUSED | 56 | — | This pin is not used in the CMOS interface |

# 7 Specifications

## 7.1 Absolute Maximum Ratings(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, AVDD | | –0.3 | 2.1 | V |
| Supply voltage, DRVDD | | –0.3 | 2.1 | V |
| Voltage between AGND and DRGND | | –0.3 | 0.3 | V |
| Voltage between AVDD to DRVDD (when AVDD leads DRVDD) | | –2.4 | 2.4 | V |
| Voltage between DRVDD to AVDD (when DRVDD leads AVDD) | | –2.4 | 2.4 | V |
| Voltage applied to input pins | INP_A, INM_A, INP_B, INM_B | –0.3 | Minimum (1.9, AVDD + 0.3) | V |
| | CLKP, CLKM(2) | –0.3 | AVDD + 0.3 | V |
| | RESET, SCLK, SDATA, SEN, CTRL1, CTRL2, CTRL3 | –0.3 | 3.9 | V |
| Operating free-air temperature, $T_A$ | | –40 | 85 | °C |
| Operating junction temperature, $T_J$ | | | 125 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) When AVDD is turned off, it is recommended to switch off the input clock (or ensure the voltage on CLKP, CLKM is less than |0.3 V|). This configuration prevents the ESD protection diodes at the clock input pins from turning on.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | 2000 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

Over operating free-air temperature range, unless otherwise noted.

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **SUPPLIES** | | | | | |
| Analog supply voltage, AVDD | | 1.7 | 1.8 | 1.9 | V |
| Digital supply voltage, DRVDD | | 1.7 | 1.8 | 1.9 | V |
| **ANALOG INPUTS** | | | | | |
| Differential input voltage range | | | 2 | | $V_{PP}$ |
| Input common-mode voltage | | | VCM ± 0.05 | | V |
| Maximum analog input frequency with 2-$V_{PP}$ input amplitude(1) | | | 400 | | MHz |
| Maximum analog input frequency with 1-$V_{PP}$ input amplitude(1) | | | 600 | | MHz |
| **CLOCK INPUT** | | | | | |
| **Input clock sample rate** | | | | | |
| Low-speed mode enabled(2) | | 1 | | 80 | MSPS |
| Low-speed mode disabled(2) (by default after reset) | | 80 | | 250 | MSPS |
| Input clock amplitude differential ($V_{CLKP} – V_{CLKM}$) | Sine wave, ac-coupled | 0.2 | 1.5 | | $V_{PP}$ |
| | LVPECL, ac-coupled | | 1.6 | | $V_{PP}$ |
| | LVDS, ac-coupled | | 0.7 | | $V_{PP}$ |
| | LVCMOS, single-ended, ac-coupled | | 1.5 | | V |
| **Input clock duty cycle** | | | | | |
| Low-speed mode disabled | | 35% | 50% | 65% | |
| Low-speed mode enabled | | 40% | 50% | 60% | |

(1) See *Theory of Operation*
(2) See *Serial Interface Configuration* for details on programming the low-speed mode.

## Recommended Operating Conditions (continued)

Over operating free-air temperature range, unless otherwise noted.

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| **DIGITAL OUTPUTS** | | | | |
| Maximum external load capacitance from each output pin to DRGND, $C_{LOAD}$ | | 5 | | pF |
| Differential load resistance between the LVDS output pairs (LVDS mode), $R_{LOAD}$ | | 100 | | Ω |
| Operating free-air temperature, $T_A$ | –40 | | +85 | °C |

## 7.4 Thermal Information

| THERMAL METRIC(1) | | ADS4229 RGC (VQFN) 64 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 23.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 10.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 4.3 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 4.4 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 0.6 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 7.5 Electrical Characteristics: ADS4229 (250 MSPS)

Typical values are at +25°C, AVDD = 1.8 V, DRVDD = 1.8 V, 50% clock duty cycle, –1 dBFS differential analog input, LVDS interface, and 0-dB gain, unless otherwise noted. Minimum and maximum values are across the full temperature range: $T_{MIN}$ = –40°C to $T_{MAX}$ = +85°C, AVDD = 1.8 V, and DRVDD = 1.8 V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Resolution | | | | | 12 | Bits |
| Signal-to-noise ratio | SNR | $f_{IN}$ = 20 MHz | | 70.5 | | dBFS |
| | | $f_{IN}$ = 70 MHz | | 70.3 | | dBFS |
| | | $f_{IN}$ = 100 MHz | | 70.1 | | dBFS |
| | | $f_{IN}$ = 170 MHz, 0-dB gain | | 69.8 | | dBFS |
| | | $f_{IN}$ = 170 MHz, 3-dB gain | 65.5 | 67.8 | | dBFS |
| | | $f_{IN}$ = 300 MHz | | 68.2 | | dBFS |
| Signal-to-noise and distortion ratio | SINAD | $f_{IN}$ = 20 MHz | | 70 | | dBFS |
| | | $f_{IN}$ = 70 MHz | | 69.7 | | dBFS |
| | | $f_{IN}$ = 100 MHz | | 69.8 | | dBFS |
| | | $f_{IN}$ = 170 MHz, 0-dB gain | | 68.1 | | dBFS |
| | | $f_{IN}$ = 170 MHz, 3-dB gain | 65 | 67.5 | | dBFS |
| | | $f_{IN}$ = 300 MHz | | 67.6 | | dBFS |
| Spurious-free dynamic range | SFDR | $f_{IN}$ = 20 MHz | | 80 | | dBc |
| | | $f_{IN}$ = 70 MHz | | 79 | | dBc |
| | | $f_{IN}$ = 100 MHz | | 82 | | dBc |
| | | $f_{IN}$ = 170 MHz, 0-dB gain | | 80 | | dBc |
| | | $f_{IN}$ = 170 MHz, 3-dB gain | 71 | 81 | | dBc |
| | | $f_{IN}$ = 300 MHz | | 77 | | dBc |
| Total harmonic distortion | THD | $f_{IN}$ = 20 MHz | | 78 | | dBc |
| | | $f_{IN}$ = 70 MHz | | 77 | | dBc |
| | | $f_{IN}$ = 100 MHz | | 79 | | dBc |
| | | $f_{IN}$ = 170 MHz, 0-dB gain | | 76 | | dBc |
| | | $f_{IN}$ = 170 MHz, 3-dB gain | 69.5 | 78 | | dBc |
| | | $f_{IN}$ = 300 MHz | | 75 | | dBc |

## Electrical Characteristics: ADS4229 (250 MSPS) (continued)

Typical values are at +25°C, AVDD = 1.8 V, DRVDD = 1.8 V, 50% clock duty cycle, –1 dBFS differential analog input, LVDS interface, and 0-dB gain, unless otherwise noted. Minimum and maximum values are across the full temperature range: $T_{MIN}$ = –40°C to $T_{MAX}$ = +85°C, AVDD = 1.8 V, and DRVDD = 1.8 V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Second-harmonic distortion | HD2 | $f_{IN}$ = 20 MHz | | 80 | | dBc |
| | | $f_{IN}$ = 70 MHz | | 79 | | dBc |
| | | $f_{IN}$ = 100 MHz | | 81 | | dBc |
| | | $f_{IN}$ = 170 MHz, 0-dB gain | | 80 | | dBc |
| | | $f_{IN}$ = 170 MHz, 3-dB gain | 71 | 81 | | dBc |
| | | $f_{IN}$ = 300 MHz | | 76 | | dBc |
| Third-harmonic distortion | HD3 | $f_{IN}$ = 20 MHz | | 85 | | dBc |
| | | $f_{IN}$ = 70 MHz | | 87 | | dBc |
| | | $f_{IN}$ = 100 MHz | | 96 | | dBc |
| | | $f_{IN}$ = 170 MHz, 0-dB gain | | 80 | | dBc |
| | | $f_{IN}$ = 170 MHz, 3-dB gain | 71 | 87 | | dBc |
| | | $f_{IN}$ = 300 MHz | | 84 | | dBc |
| Worst spur (other than second and third harmonics) | | $f_{IN}$ = 20 MHz | | 92 | | dBc |
| | | $f_{IN}$ = 70 MHz | | 95 | | dBc |
| | | $f_{IN}$ = 100 MHz | | 94 | | dBc |
| | | $f_{IN}$ = 170 MHz, 0-dB gain | | 93 | | dBc |
| | | $f_{IN}$ = 170 MHz, 3-dB gain | 77 | 92 | | dBc |
| | | $f_{IN}$ = 300 MHz | | 89 | | dBc |
| Two-tone intermodulation distortion | IMD | $f_1$ = 46 MHz, $f_2$ = 50 MHz, each tone at –7 dBFS | | 98 | | dBFS |
| | | $f_1$ = 185 MHz, $f_2$ = 190 MHz, each tone at –7 dBFS | | 84 | | dBFS |
| Crosstalk | | 20-MHz full-scale signal on channel under observation; 170-MHz full-scale signal on other channel | | 95 | | dB |
| Input overload recovery | | Recovery to within 1% (of full-scale) for 6 dB overload with sine-wave input | | 1 | | Clock cycle |
| AC power-supply rejection ratio | PSRR | For 50-$mV_{PP}$ signal on AVDD supply, up to 10 MHz | | 30 | | dB |
| Effective number of bits | ENOB | $f_{IN}$ = 170 MHz | | 11.15 | | LSBs |
| Differential nonlinearity | DNL | $f_{IN}$ = 170 MHz | –0.8 | ±0.5 | 1.5 | LSBs |
| Integrated nonlinearity | INL | $f_{IN}$ = 170 MHz | | ±1.8 | ±4 | LSBs |

## 7.6 Electrical Characteristics: General

Typical values are at +25°C, AVDD = 1.8 V, DRVDD = 1.8 V, 50% clock duty cycle, and –1 dBFS differential analog input, unless otherwise noted. Minimum and maximum values are across the full temperature range: $T_{MIN}$ = –40°C to $T_{MAX}$ = +85°C, AVDD = 1.8 V, and DRVDD = 1.8 V.

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **ANALOG INPUTS** | | | | | |
| Differential input voltage range | | | 2 | | $V_{PP}$ |
| Differential input resistance (at 200 MHz) | | | 0.75 | | kΩ |
| Differential input capacitance (at 200 MHz) | | | 3.7 | | pF |
| Analog input bandwidth<br>(with 50-Ω source impedance, and 50-Ω termination) | | | 550 | | MHz |
| Analog input common-mode current<br>(per input pin of each channel) | | | 1.5 | | µA/MSPS |
| Common-mode output voltage | VCM | | 0.95(1) | | V |
| VCM output current capability | | | 4 | | mA |
| **DC ACCURACY** | | | | | |
| Offset error | | –15 | 2.5 | 15 | mV |
| Temperature coefficient of offset error | | | 0.003 | | mV/°C |
| Gain error as a result of internal reference inaccuracy alone | $E_{GREF}$ | –2 | | 2 | %FS |
| Gain error of channel alone | $E_{GCHAN}$ | | ±0.1 | 1 | %FS |
| Temperature coefficient of $E_{GCHAN}$ | | | 0.002 | | Δ%/°C |
| **POWER SUPPLY** | | | | | |
| IAVDD<br>Analog supply current | | | 167 | 190 | mA |
| IDRVDD<br>Output buffer supply current<br>LVDS interface, 350-mV swing with 100-Ω external termination, $f_{IN}$ = 2.5 MHz | | | 136 | 160 | mA |
| IDRVDD<br>Output buffer supply current<br>CMOS interface, no load capacitance, $f_{IN}$ = 2.5 MHz(2) | | | 94 | | mA |
| Analog power | | | 301 | | mW |
| Digital power<br>LVDS interface, 350-mV swing with 100-Ω external termination, $f_{IN}$ = 2.5 MHz | | | 245 | | mW |
| Digital power<br>CMOS interface, 8-pF external load capacitance(2)<br>$f_{IN}$ = 2.5 MHz | | | 169 | | mW |
| Global power-down | | | | 25 | mW |

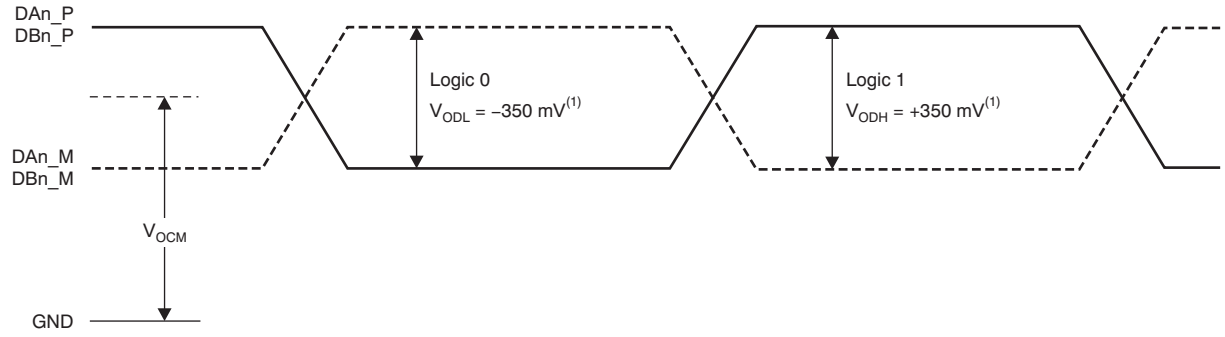
(1) VCM changes to 0.87 V when the HIGH PERF MODE[7:2] serial register bits are set.
(2) In CMOS mode, the DRVDD current scales with the sampling frequency, the load capacitance on output pins, input frequency, and the supply voltage (see *CMOS Interface Power Dissipation*).

## 7.7 Digital Characteristics

At AVDD = 1.8 V and DRVDD = 1.8 V, unless otherwise noted. DC specifications refer to the condition where the digital outputs do not switch, but are permanently at a valid logic level '0' or '1'.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DIGITAL INPUTS (RESET, SCLK, SDATA, SEN, CTRL1, CTRL2, CTRL3)(1)** | | | | | | |
| High-level input voltage | | All digital inputs support 1.8-V and 3.3-V CMOS logic levels | 1.3 | | | V |
| Low-level input voltage | | | | | 0.4 | V |
| High-level input current | SDATA, SCLK(2) | $V_{HIGH}$ = 1.8 V | | 10 | | µA |
| | SEN(3) | $V_{HIGH}$ = 1.8 V | | 0 | | µA |
| Low-level input current | SDATA, SCLK | $V_{LOW}$ = 0 V | | 0 | | µA |
| | SEN | $V_{LOW}$ = 0 V | | 10 | | µA |
| **DIGITAL OUTPUTS, CMOS INTERFACE (DA[13:0], DB[13:0], CLKOUT, SDOUT)** | | | | | | |
| High-level output voltage | | | DRVDD – 0.1 | DRVDD | | V |
| Low-level output voltage | | | | 0 | 0.1 | V |
| Output capacitance (internal to device) | | | | | | pF |
| **DIGITAL OUTPUTS, LVDS INTERFACE** | | | | | | |
| High-level output differential voltage | $V_{ODH}$ | With an external 100-Ω termination | 270 | 350 | 430 | mV |
| Low-level output differential voltage | $V_{ODL}$ | With an external 100-Ω termination | –430 | –350 | –270 | mV |
| Output common-mode voltage | $V_{OCM}$ | | 0.9 | 1.05 | 1.25 | V |

(1) SCLK, SDATA, and SEN function as digital input pins in serial configuration mode.
(2) SDATA, SCLK have internal 150-kΩ pull-down resistor.
(3) SEN has an internal 150-kΩ pull-up resistor to AVDD. Because the pull-up is weak, SEN can also be driven by 1.8 V or 3.3 V CMOS buffers.




(1) With external 100-Ω termination.

**Figure 1. LVDS Output Voltage Levels**

## 7.8 LVDS and CMOS Modes Timing Requirements(1)

Typical values are at +25°C, AVDD = 1.8 V, DRVDD = 1.8 V, sampling frequency = 250 MSPS, sine wave input clock, $C_{LOAD}$ = 5 pF, and $R_{LOAD}$ = 100 Ω, unless otherwise noted. Minimum and maximum values are across the full temperature range: $T_{MIN}$ = –40°C to $T_{MAX}$ = +85°C, AVDD = 1.8 V, and DRVDD = 1.7 V to 1.9 V.

| PARAMETER | | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_A$ | Aperture delay | | 0.5 | 0.8 | 1.1 | ns |
| | Aperture delay matching | Between the two channels of the same device | | ±70 | | ps |
| | Variation of aperture delay | Between two devices at the same temperature and DRVDD supply | | ±150 | | ps |
| $t_J$ | Aperture jitter | | | 140 | | $f_S$ rms |
| | Wakeup time | Time to valid data after coming out of STANDBY mode | | 50 | 100 | µs |
| | | Time to valid data after coming out of GLOBAL power-down mode | | 100 | 500 | µs |
| | ADC latency(2) | Default latency after reset | | 16 | | Clock cycles |
| | | Digital functions enabled (EN DIGITAL = 1) | | 24 | | Clock cycles |
| **DDR LVDS MODE(3)** | | | | | | |
| $t_{SU}$ | Data setup time | Data valid(4) to zero-crossing of CLKOUTP | 0.6 | 0.88 | | ns |
| $t_H$ | Data hold time | Zero-crossing of CLKOUTP to data becoming invalid(4) | 0.33 | 0.55 | | ns |
| $t_{PDI}$ | Clock propagation delay | Input clock rising edge cross-over to output clock rising edge cross-over | 5 | 6 | 7.5 | ns |
| | LVDS bit clock duty cycle | Duty cycle of differential clock, (CLKOUTP-CLKOUTM) | | 48% | | |
| $t_{RISE}$, $t_{FALL}$ | Data rise time, Data fall time | Rise time measured from –100 mV to +100 mV<br>Fall time measured from +100 mV to –100 mV<br>*1 MSPS ≤ Sampling frequency ≤ 250 MSPS* | | 0.13 | | ns |
| $t_{CLKRISE}$, $t_{CLKFALL}$ | Output clock rise time, Output clock fall time | Rise time measured from –100 mV to +100 mV<br>Fall time measured from +100 mV to –100 mV<br>*1 MSPS ≤ Sampling frequency ≤ 250 MSPS* | | 0.13 | | ns |
| **PARALLEL CMOS MODE** | | | | | | |
| $t_{PDI}$ | Clock propagation delay | Input clock rising edge cross-over to output clock rising edge cross-over | 4.5 | 6.2 | 8.5 | ns |
| | Output clock duty cycle | Duty cycle of output clock, CLKOUT<br>*1 MSPS ≤ Sampling frequency ≤ 200 MSPS* | | 50% | | |
| $t_{RISE}$, $t_{FALL}$ | Data rise time, Data fall time | Rise time measured from 20% to 80% of DRVDD<br>Fall time measured from 80% to 20% of DRVDD<br>*1 MSPS ≤ Sampling frequency ≤ 200 MSPS* | | 0.7 | | ns |
| $t_{CLKRISE}$, $t_{CLKFALL}$ | Output clock rise time<br>Output clock fall time | Rise time measured from 20% to 80% of DRVDD<br>Fall time measured from 80% to 20% of DRVDD<br>*1 MSPS ≤ Sampling frequency ≤ 200 MSPS* | | 0.7 | | ns |

(1) Timing parameters are ensured by design and characterization and not tested in production.
(2) At higher frequencies, $t_{PDI}$ is greater than one clock period and overall latency = ADC latency + 1.
(3) Measurements are done with a transmission line of 100-Ω characteristic impedance between the device and the load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(4) Data valid refers to a logic high of +100 mV and a logic low of –100 mV.

## 7.9 LVDS Timings at Lower Sampling Frequencies

Typical values are at +25°C, AVDD = 1.8 V, DRVDD = 1.8 V, sampling frequency = 250 MSPS, sine wave input clock, $C_{LOAD}$ = 5 pF, and $R_{LOAD}$ = 100 Ω, unless otherwise noted. Minimum and maximum values are across the full temperature range: $T_{MIN}$ = –40°C to $T_{MAX}$ = +85°C, AVDD = 1.8 V, and DRVDD = 1.7 V to 1.9 V.

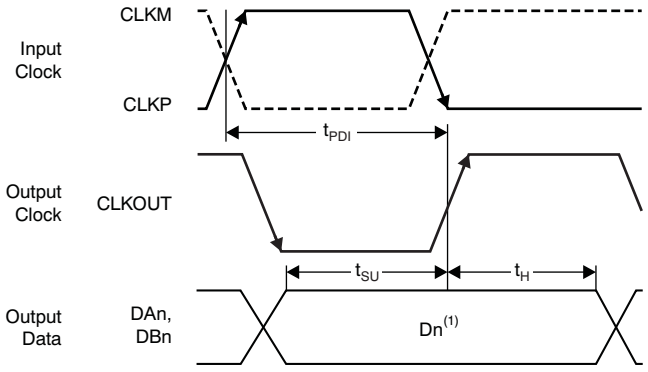
| SAMPLING FREQUENCY (MSPS) | SETUP TIME (ns) | | | HOLD TIME (ns) | | | $t_{PDI}$, CLOCK PROPAGATION DELAY (ns) | | |
|---|---|---|---|---|---|---|---|---|---|
| | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX |
| 65 | 5.9 | 6.6 | | 0.35 | 0.6 | | 5 | 6 | 7.5 |
| 80 | 4.5 | 5.2 | | 0.35 | 0.6 | | 5 | 6 | 7.5 |
| 125 | 2.3 | 2.9 | | 0.35 | 0.6 | | 5 | 6 | 7.5 |
| 160 | 1.5 | 2 | | 0.33 | 0.55 | | 5 | 6 | 7.5 |
| 185 | 1.3 | 1.6 | | 0.33 | 0.55 | | 5 | 6 | 7.5 |
| 200 | 1.1 | 1.4 | | 0.33 | 0.55 | | 5 | 6 | 7.5 |
| 230 | 0.76 | 1.06 | | 0.33 | 0.55 | | 5 | 6 | 7.5 |

## 7.10 CMOS Timings at Lower Sampling Frequencies

Typical values are at +25°C, AVDD = 1.8 V, DRVDD = 1.8 V, sampling frequency = 250 MSPS, sine wave input clock, $C_{LOAD}$ = 5 pF, and $R_{LOAD}$ = 100 Ω, unless otherwise noted. Minimum and maximum values are across the full temperature range: $T_{MIN}$ = –40°C to $T_{MAX}$ = +85°C, AVDD = 1.8 V, and DRVDD = 1.7 V to 1.9 V.

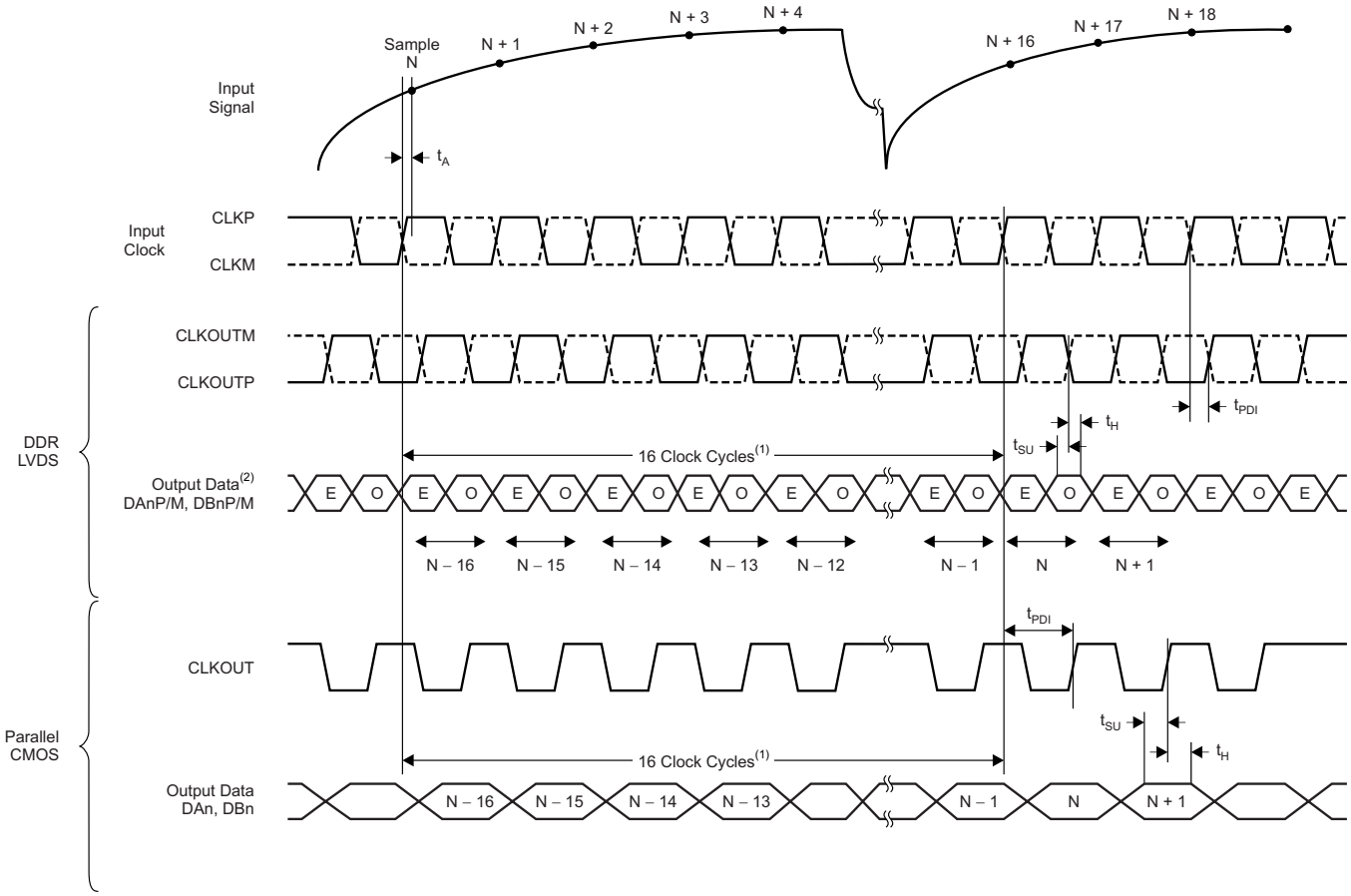
| SAMPLING FREQUENCY (MSPS) | TIMINGS SPECIFIED WITH RESPECT TO CLKOUT | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | SETUP TIME(1) (ns) | | | HOLD TIME(1) (ns) | | | $t_{PDI}$, CLOCK PROPAGATION DELAY (ns) | | |
| | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX |
| 65 | 6.1 | 6.7 | | 6.7 | 7.5 | | 4.5 | 6.2 | 8.5 |
| 80 | 4.7 | 5.2 | | 5.3 | 6 | | 4.5 | 6.2 | 8.5 |
| 125 | 2.7 | 3.1 | | 3.1 | 3.6 | | 4.5 | 6.2 | 8.5 |
| 160 | 1.6 | 2.1 | | 2.3 | 2.8 | | 4.5 | 6.2 | 8.5 |
| 185 | 1.1 | 1.6 | | 1.9 | 2.4 | | 4.5 | 6.2 | 8.5 |
| 200 | 1 | 1.4 | | 1.7 | 2.2 | | 4.5 | 6.2 | 8.5 |

(1) In CMOS mode, setup time is measured from the beginning of data valid to 50% of the CLKOUT rising edge, whereas hold time is measured from 50% of the CLKOUT rising edge to data becoming invalid. Data valid refers to a logic high of 1.26 V and a logic low of 0.54 V.




(1) Dn = bits D0, D1, D2, and so forth, of channels A and B.

**Figure 2. CMOS Interface Timing Diagram**




(1) ADC latency after reset. At higher sampling frequencies, $t_{PDI}$ is greater than one clock cycle, which then makes the overall latency = ADC latency + 1.

(2) E = even bits (D0, D2, D4, and so forth); O = odd bits (D1, D3, D5, and so forth).

**Figure 3. Latency Timing Diagram**

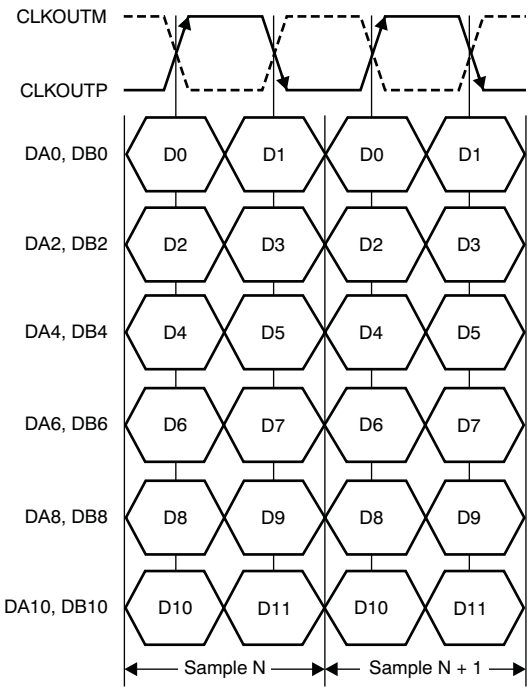



**Figure 4. LVDS Interface Timing Diagram**

## 7.11 Serial Interface Timing Characteristics

See (1).

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{SCLK}$ | SCLK frequency (equal to $1/t_{SCLK}$) | > DC | | 20 | MHz |
| $t_{SLOADS}$ | SEN to SCLK setup time | 25 | | | ns |
| $t_{SLOADH}$ | SCLK to SEN hold time | 25 | | | ns |
| $t_{DSU}$ | SDATA setup time | 25 | | | ns |
| $t_{DH}$ | SDATA hold time | 25 | | | ns |

(1) Typical values at +25°C; minimum and maximum values across the full temperature range: $T_{MIN}$ = –40°C to $T_{MAX}$ = +85°C, AVDD = 1.8 V, and DRVDD = 1.8 V, unless otherwise noted.

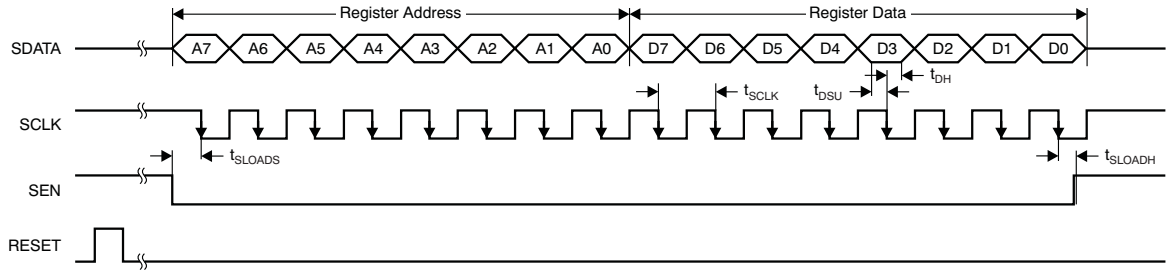


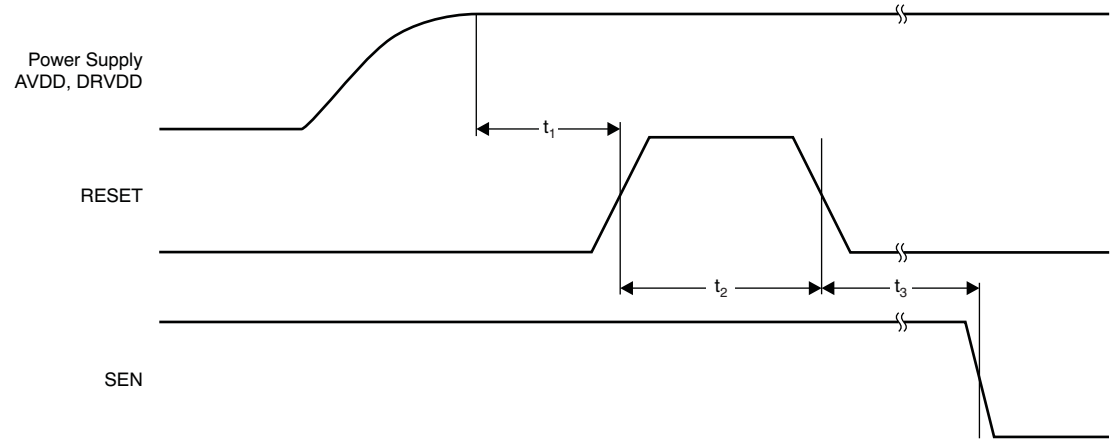

**Figure 5. Serial Interface Timing Diagram**

## 7.12 Reset Timing (Only when Serial Interface is Used)

See (1).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_1$ | Power-on delay | Delay from AVDD and DRVDD power-up to active RESET pulse | 1 | | | ms |
| $t_2$ | Reset pulse width | Active RESET signal pulse width | 10 | | | ns |
| | | | | | 1 | µs |
| $t_3$ | Register write delay | Delay from RESET disable to SEN active | 100 | | | ns |

(1) Typical values at +25°C; minimum and maximum values across the full temperature range: $T_{MIN}$ = –40°C to $T_{MAX}$ = +85°C, unless otherwise noted.




NOTE: A high pulse on the RESET pin is required in the serial interface mode when initialized through a hardware reset. For parallel interface operation, RESET must be permanently tied high.

**Figure 6. Reset Timing Diagram**

## 7.13 Typical Characteristics

### 7.13.1 Typical Characteristics: ADS4229

At $T_A$ = +25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5 $V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, High-Performance Mode enabled, 0-dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

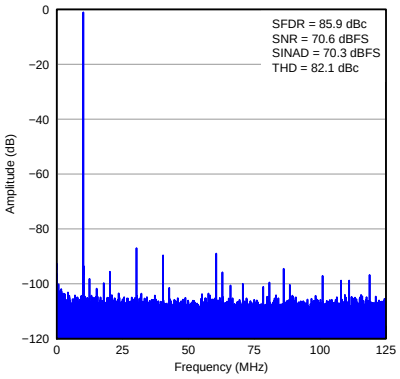



**Figure 7. Input Signal (10 MHz)**

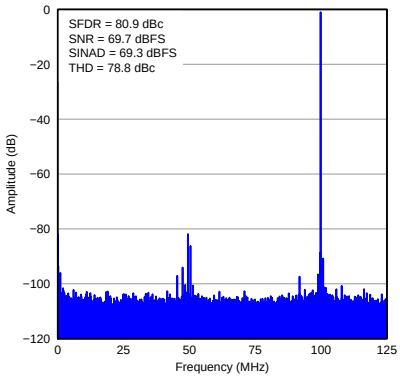



**Figure 8. Input Signal (150 MHz)**

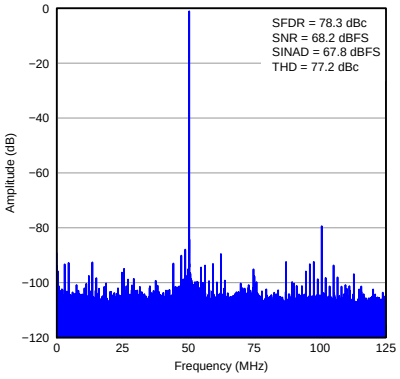



**Figure 9. Input Signal (300 MHz)**

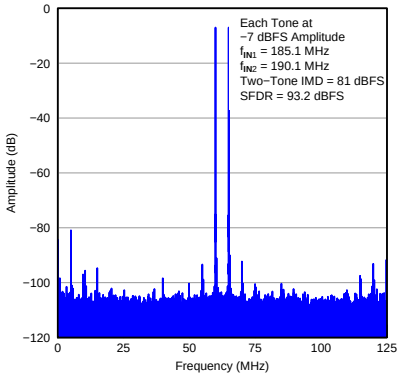



**Figure 10. Two-Tone Input Signal**

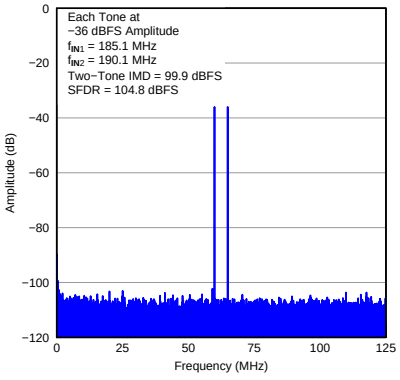



**Figure 11. Two-Tone Input Signal**

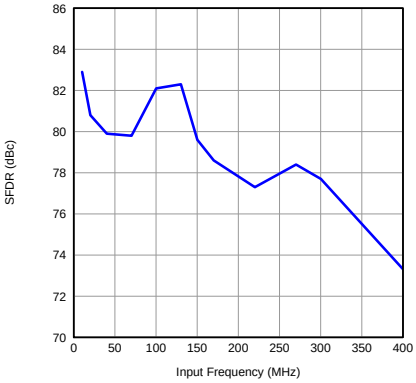



**Figure 12. SFDR vs Input Frequency**

## Typical Characteristics: ADS4229 (continued)

At $T_A$ = +25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5 $V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, High-Performance Mode enabled, 0-dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

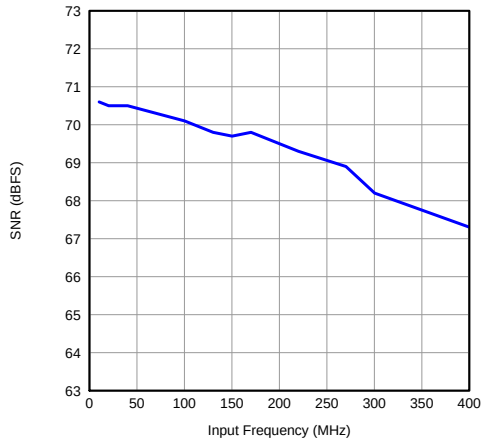



**Figure 13. SNR vs Input Frequency**

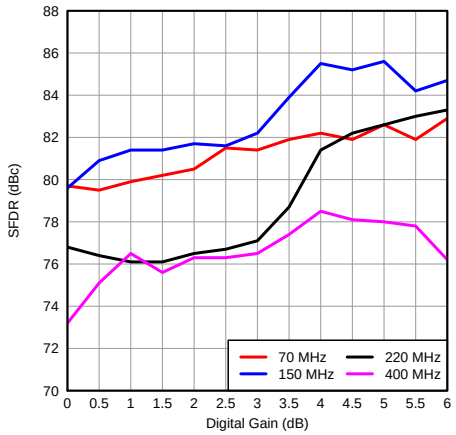



**Figure 14. SFDR vs Gain and Input Frequency**

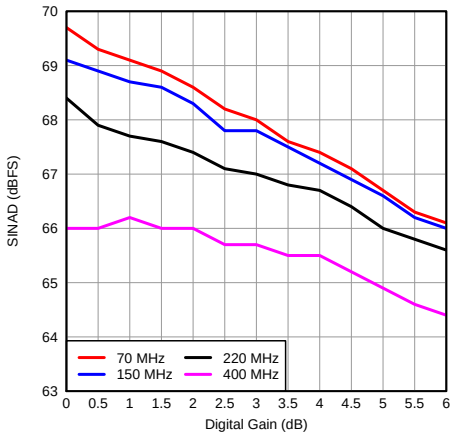



**Figure 15. SINAD vs Gain and Input Frequency**

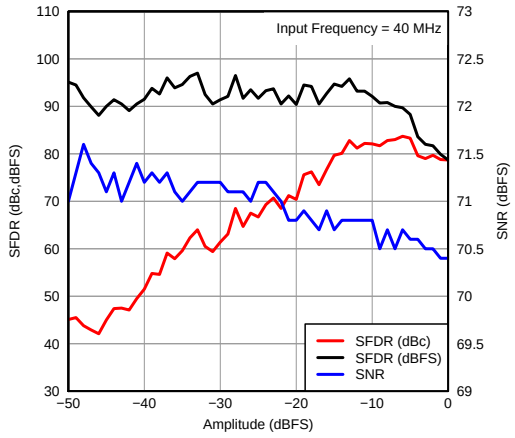



**Figure 16. Performance vs Input Amplitude**

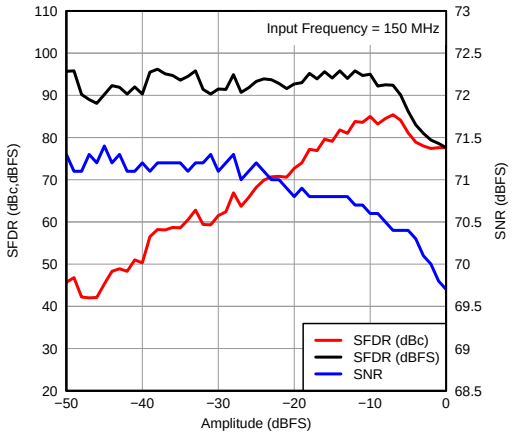



**Figure 17. Performance vs Input Amplitude**

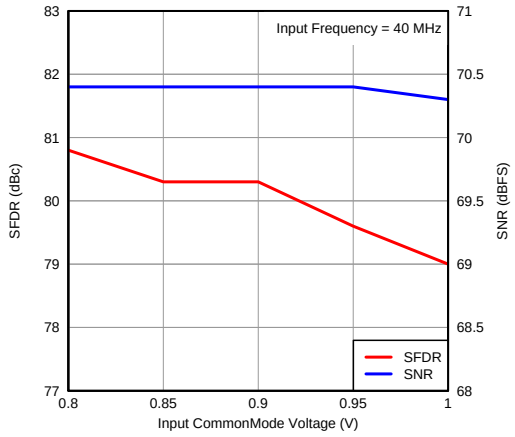



**Figure 18. Performance vs Input Common-Mode Voltage**

## Typical Characteristics: ADS4229 (continued)

At $T_A$ = +25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5 $V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, High-Performance Mode enabled, 0-dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

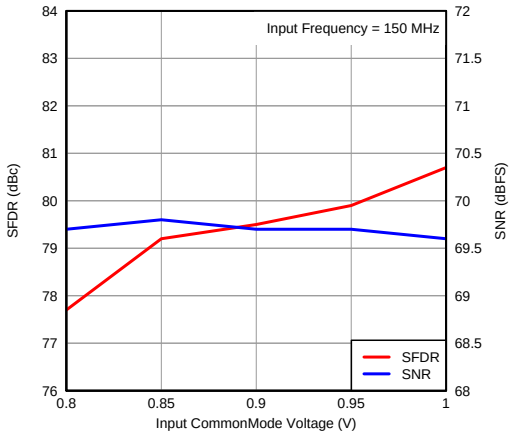



**Figure 19. Performance vs Input Common-Mode Voltage**

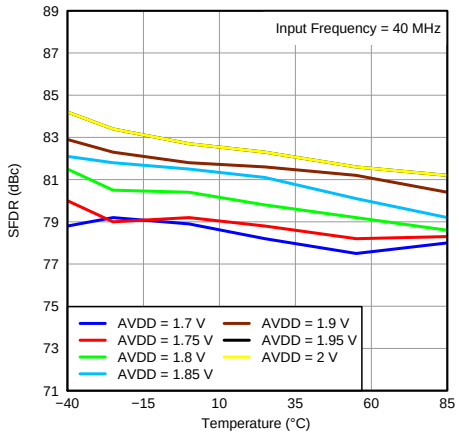



**Figure 20. SFDR vs Temperature and AVDD Supply**

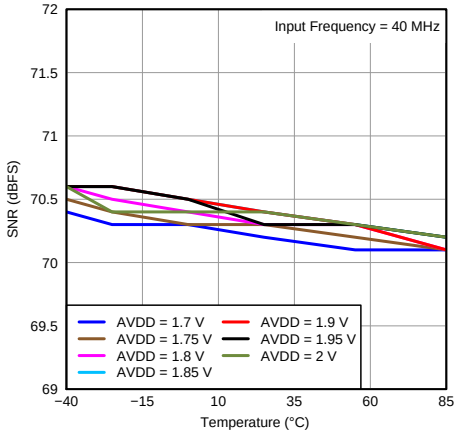



**Figure 21. SNR vs Temperature and AVDD Supply**

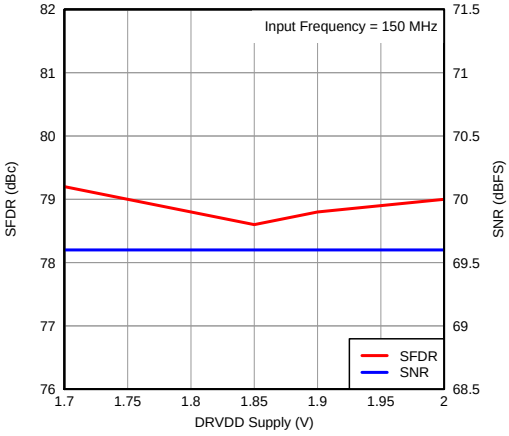



**Figure 22. Performance vs DRVDD Supply Voltage**

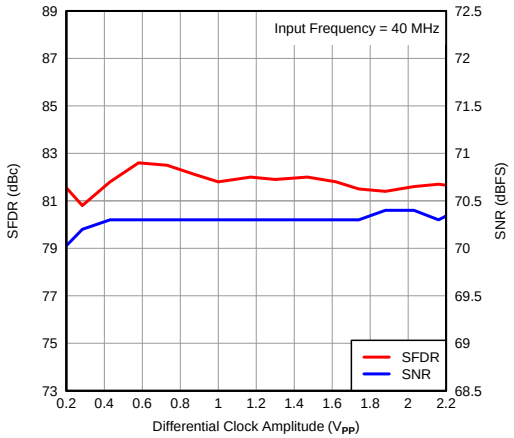



**Figure 23. Performance vs Input Clock Amplitude**

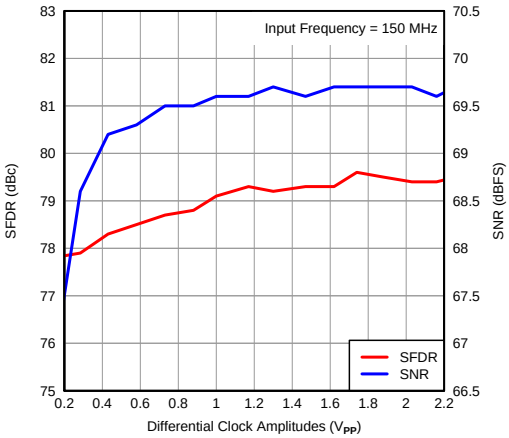



**Figure 24. Performance vs Input Clock Amplitude**

## Typical Characteristics: ADS4229 (continued)

At $T_A$ = +25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5 $V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, High-Performance Mode enabled, 0-dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

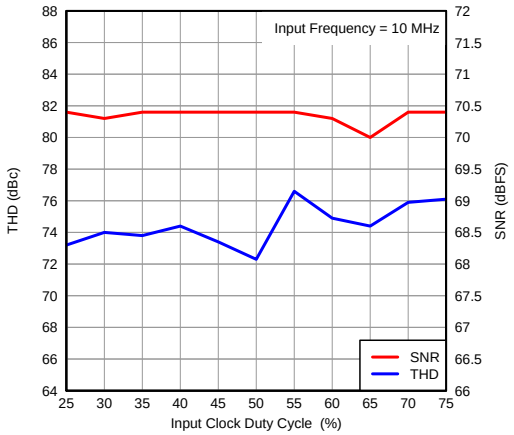



**Figure 25. Performance vs Input Clock Duty Cycle**

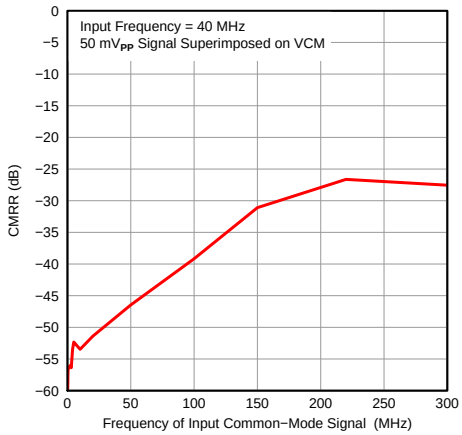



**Figure 26. CMRR vs Test Signal Frequency**

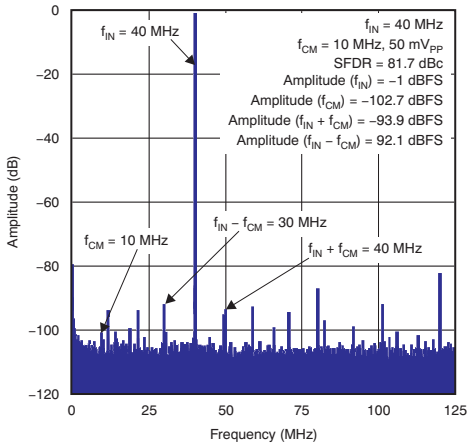



**Figure 27. CMRR Plot**

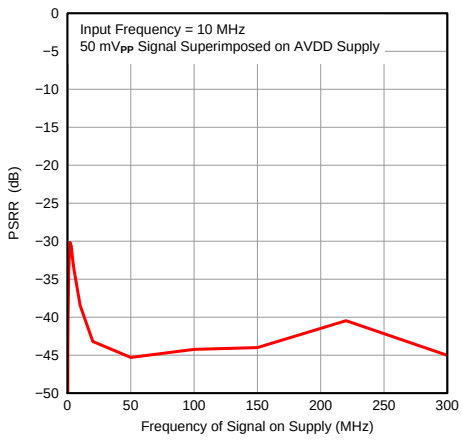



**Figure 28. PSRR vs Test Signal Frequency**

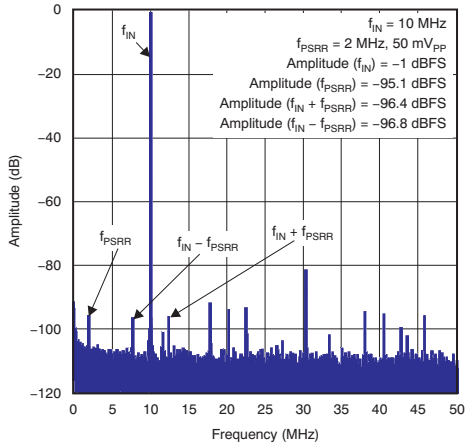



**Figure 29. PSRR Plot**

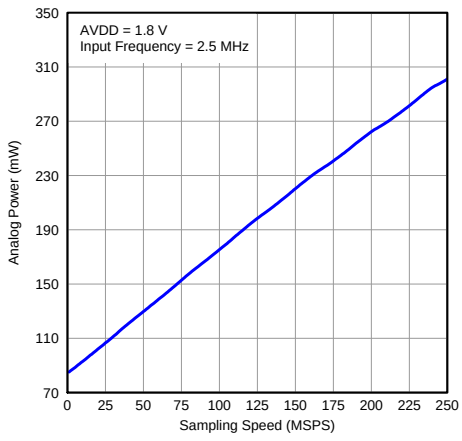



**Figure 30. Analog Power vs Sampling Frequency**

## Typical Characteristics: ADS4229 (continued)

At $T_A$ = +25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5 $V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, High-Performance Mode enabled, 0-dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

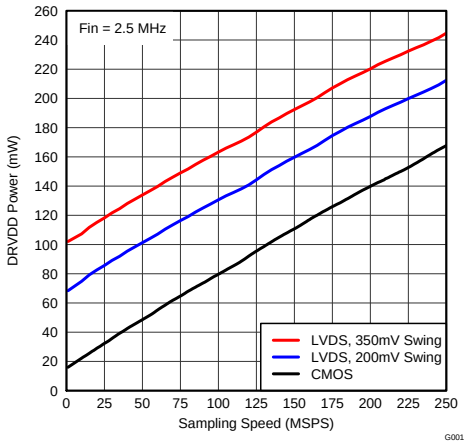



**Figure 31. Digital Power LVDS CMOS**

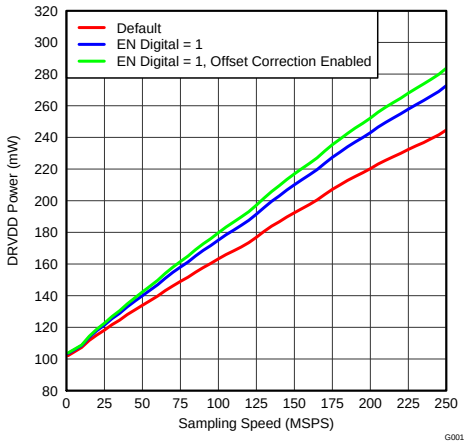



**Figure 32. Digital Power in Various Modes**

### 7.13.2 Typical Characteristics: Contour

All graphs are at +25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 $V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, High-Performance Mode enabled, 0-dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

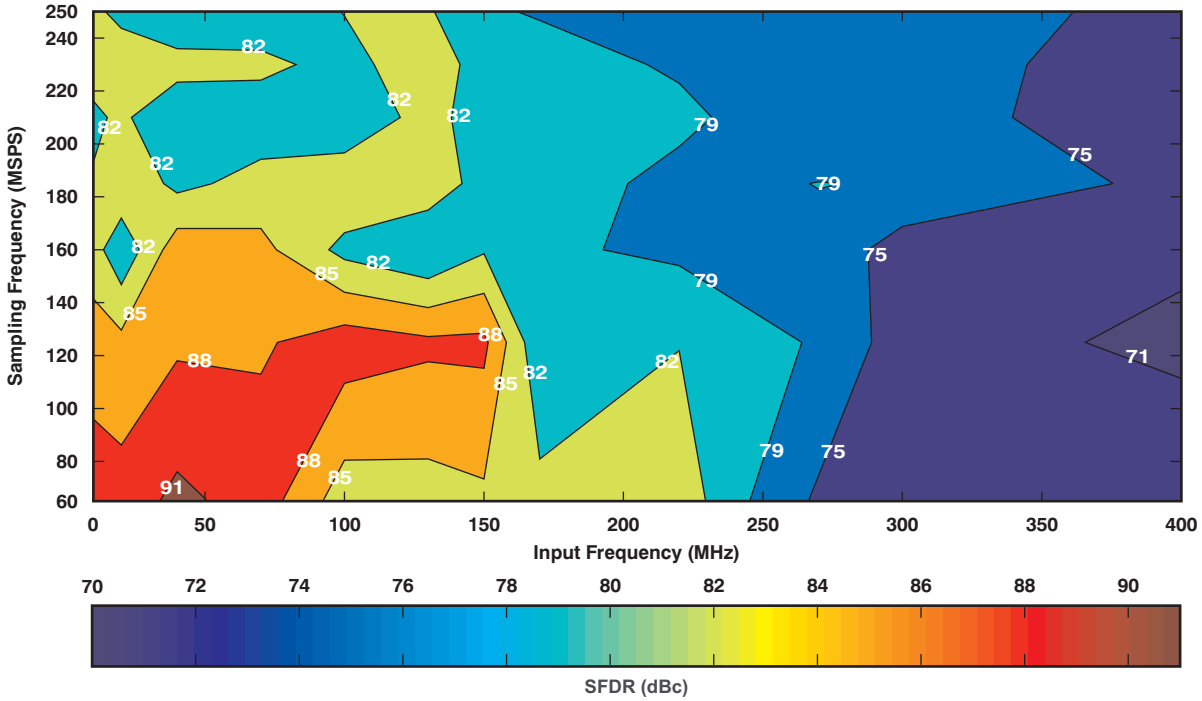



**Figure 33. Spurious-Free Dynamic Range (0-dB Gain)**

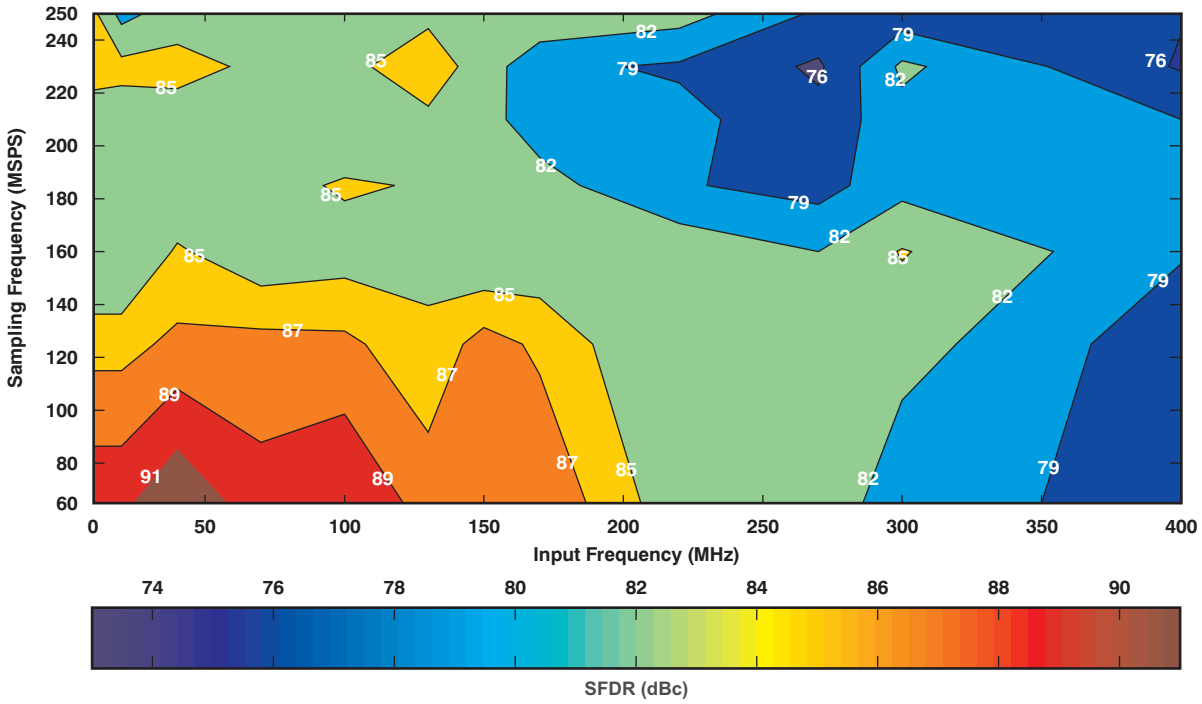



**Figure 34. Spurious-Free Dynamic Range (6-dB Gain)**

## Typical Characteristics: Contour (continued)

All graphs are at +25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 $V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, High-Performance Mode enabled, 0-dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

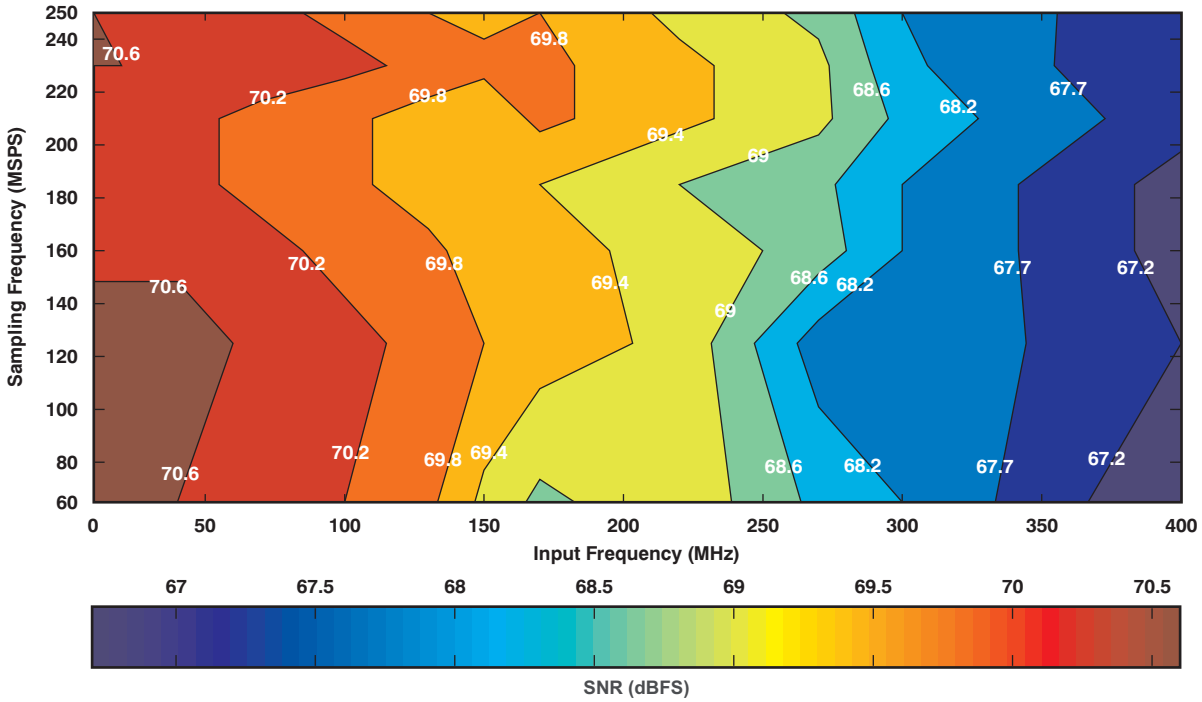



**Figure 35. Signal-to-Noise Ratio (0-dB Gain)**

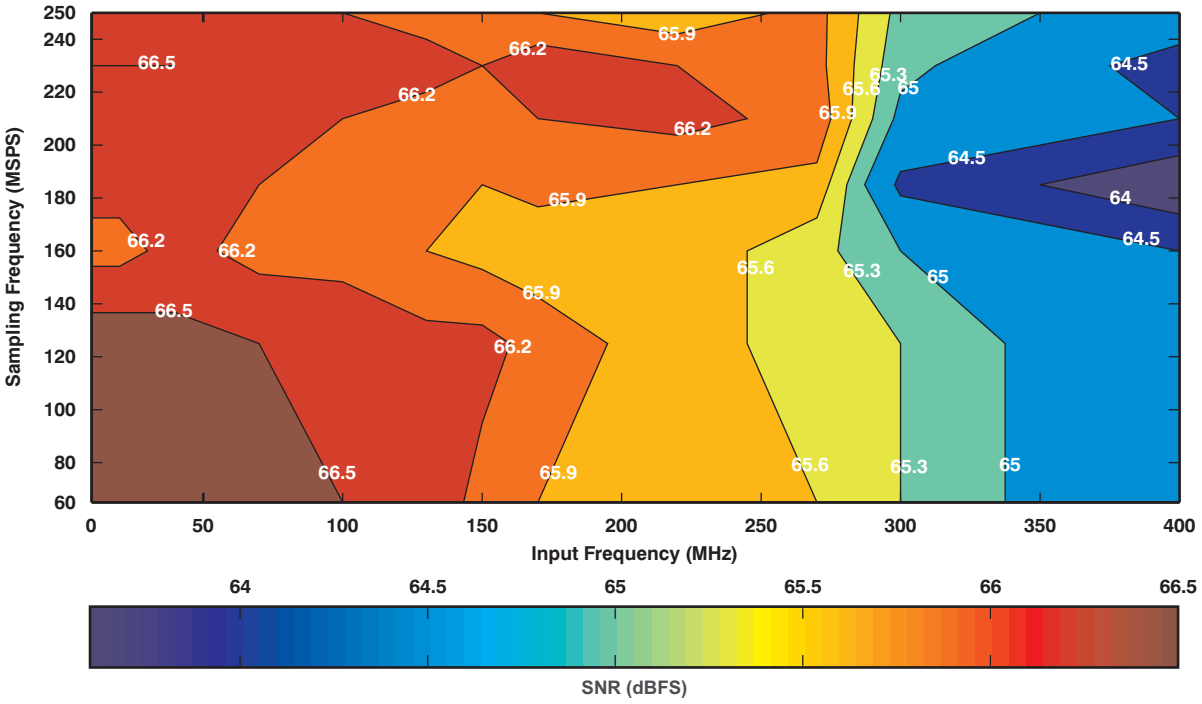


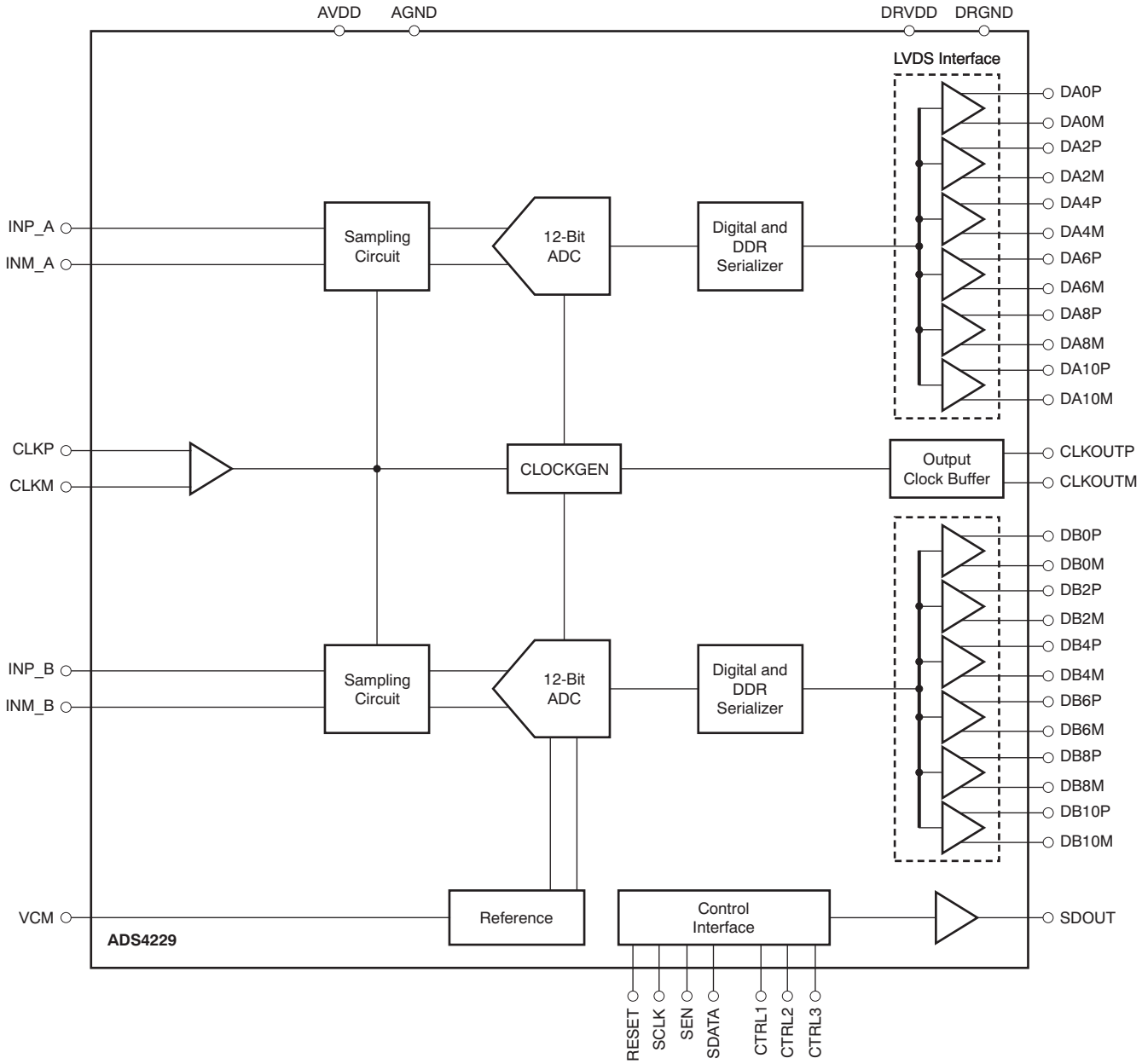

**Figure 36. Signal-to-Noise Ratio (6-dB Gain)**

# 8 Detailed Description

## 8.1 Overview

The ADS4229 belongs to TI's ultra low-power family of dual-channel, 12-bit analog-to-digital converters (ADCs). High performance is maintained while reducing power for power sensitive applications. In addition to its low power and high performance, the ADS4229 has a number of digital features and operating modes to enable design flexibility.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Digital Functions

The device has several useful digital functions (such as test patterns, gain, and offset correction). These functions require extra clock cycles for operation and increase the overall latency and power of the device. These digital functions are disabled by default after reset and the raw ADC output is routed to the output data pins with a latency of 16 clock cycles. Figure 37 shows more details of the processing after the ADC. In order to use any of the digital functions, the EN DIGITAL bit must be set to '1'. After this, the respective register bits must be programmed as described in the following sections and in the *Serial Register Map* section.

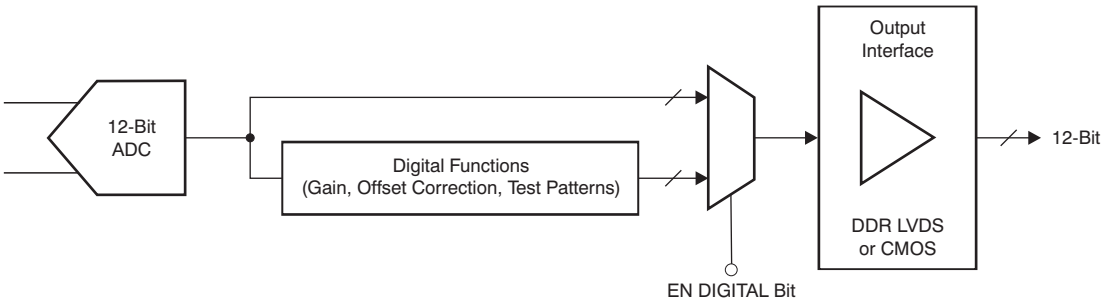



**Figure 37. Digital Processing Block**

### 8.3.2 Gain for SFDR/SNR Trade-off

The ADS4229 includes gain settings that can be used to get improved SFDR performance (compared to no gain). The gain is programmable from 0 dB to 6 dB (in 0.5-dB steps). For each gain setting, the analog input full-scale range scales proportionally, as shown in Table 2.

The SFDR improvement is achieved at the expense of SNR; for each gain setting, the SNR degrades approximately between 0.5 dB and 1 dB. The SNR degradation is reduced at high input frequencies. As a result, the gain is very useful at high input frequencies because the SFDR improvement is significant with marginal degradation in SNR. Therefore, the gain can be used as a trade-off between SFDR and SNR. Note that the default gain after reset is 0 dB.

**Table 2. Full-Scale Range Across Gains**

| GAIN (dB) | TYPE | FULL-SCALE ($V_{PP}$) |
|---|---|---|
| 0 | Default after reset | 2 |
| 1 | Fine, programmable | 1.78 |
| 2 | Fine, programmable | 1.59 |
| 3 | Fine, programmable | 1.42 |
| 4 | Fine, programmable | 1.26 |
| 5 | Fine, programmable | 1.12 |
| 6 | Fine, programmable | 1 |

### 8.3.3 Offset Correction

The ADS4229 has an internal offset corretion algorithm that estimates and corrects dc offset up to ±10 mV. The correction can be enabled using the ENABLE OFFSET CORR serial register bit. Once enabled, the algorithm estimates the channel offset and applies the correction every clock cycle. The time constant of the correction loop is a function of the sampling clock frequency. The time constant can be controlled using the OFFSET CORR TIME CONSTANT register bits, as described in Table 3.

After the offset is estimated, the correction can be frozen by setting FREEZE OFFSET CORR = 0. Once frozen, the last estimated value is used for the offset correction of every clock cycle. Note that offset correction is disabled by default after reset.

**Table 3. Time Constant of Offset Correction Algorithm**

| OFFSET CORR TIME CONSTANT | TIME CONSTANT, $TC_{CLK}$ (Number of Clock Cycles) | TIME CONSTANT, $TC_{CLK} \times 1/f_S$ (ms)(1) |
|---|---|---|
| 0000 | 1 M | 4 |
| 0001 | 2 M | 8 |
| 0010 | 4 M | 16 |
| 0011 | 8 M | 32 |
| 0100 | 16 M | 64 |
| 0101 | 32 M | 128 |
| 0110 | 64 M | 256 |
| 0111 | 128 M | 512 |
| 1000 | 256 M | 1024 |
| 1001 | 512 M | 2048 |
| 1010 | 1 G | 4096 |
| 1011 | 2 G | 8192 |
| 1100 | Reserved | — |
| 1101 | Reserved | — |
| 1110 | Reserved | — |
| 1111 | Reserved | — |

(1) Sampling frequency, $f_S$ = 250 MSPS.

### 8.3.4 Power-Down

The ADS4229 has two power-down modes: global power-down and channel standby. These modes can be set using either the serial register bits or using the control pins CTRL1 to CTRL3 (as shown in Table 4).

**Table 4. Power-Down Settings**

| CTRL1 | CTRL2 | CTRL3 | DESCRIPTION |
|---|---|---|---|
| Low | Low | Low | Default |
| Low | Low | High | Not available |
| Low | High | Low | Not available |
| Low | High | High | Not available |
| High | Low | Low | Global power-down |
| High | Low | High | Channel A powered down, channel B is active |
| High | High | Low | Not available |
| High | High | High | MUX mode of operation, channel A and B data is multiplexed and output on DB[10:0] pins |

#### *8.3.4.1 Global Power-Down*

In this mode, the entire chip (including ADCs, internal reference, and output buffers) are powered down, resulting in reduced total power dissipation of approximately 20 mW when the CTRL pins are used and 3mW when the PDN GLOBAL serial register bit is used. The output buffers are in high-impedance state. The wake-up time from global power-down to data becoming valid in normal mode is typically 100 µs.

#### *8.3.4.2 Channel Standby*

In this mode, each ADC channel can be powered down. The internal references are active, resulting in a quick wake-up time of 50 µs. The total power dissipation in standby is approximately 250 mW at 250 MSPS.

#### *8.3.4.3 Input Clock Stop*

In addition to the previous modes, the converter enters a low-power mode when the input clock frequency falls below 1 MSPS. The power dissipation is approximately 160 mW.

### 8.3.5 Output Data Format

Two output data formats are supported: twos complement and offset binary. The format can be selected using the DATA FORMAT serial interface register bit or by controlling the DFS pin in parallel configuration mode.

In the event of an input voltage overdrive, the digital outputs go to the appropriate full-scale level. For a positive overdrive, the output code is FFFh for the ADS4229 in offset binary output format; the output code is 7FFh for the ADS4229 in twos complement output format. For a negative input overdrive, the output code is 0000h in offset binary output format and 800h for the ADS4229 in twos complement output format.

## 8.4 Device Functional Modes

### 8.4.1 Output Interface Modes

The ADS4229 provides 12-bit digital data for each channel and an output clock synchronized with the data.

#### *8.4.1.1 Output Interface*

Two output interface options are available: double data rate (DDR) LVDS and parallel CMOS. They can be selected using the serial interface register bit or by setting the proper voltage on the SEN pin in parallel configuration mode.

#### *8.4.1.2 DDR LVDS Outputs*

In this mode, the data bits and clock are output using low-voltage differential signal (LVDS) levels. Two data bits are multiplexed and output on each LVDS differential pair, as shown in Figure 38.

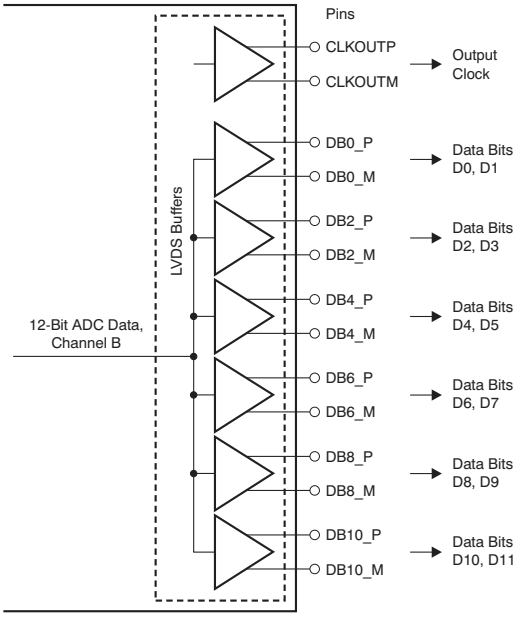



**Figure 38. LVDS Interface**

Even data bits (D0, D2, D4, and so forth) are output at the CLKOUTP rising edge and the odd data bits (D1, D3, D5, and so forth) are output at the CLKOUTP falling edge. Both the CLKOUTP rising and falling edges must be used to capture all the data bits, as shown in Figure 39.

## Device Functional Modes (continued)

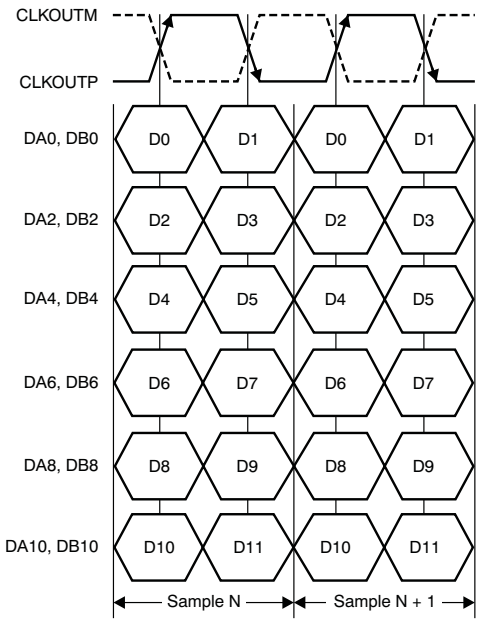
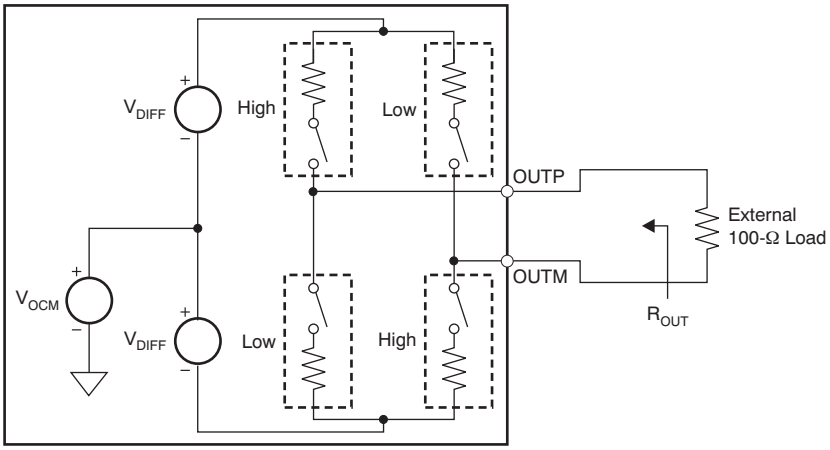



**Figure 39. DDR LVDS Interface Timing**

### *8.4.1.3 LVDS Buffer*

The equivalent circuit of each LVDS output buffer is shown in Figure 40. After reset, the buffer presents an output impedance of 100Ω to match with the external 100-Ω termination.




NOTE: Default swing across 100-Ω load is ±350 mV. Use the LVDS SWING bits to change the swing.

**Figure 40. LVDS Buffer Equivalent Circuit**

The $V_{DIFF}$ voltage is nominally 350 mV, resulting in an output swing of ±350 mV with 100-Ω external termination. The $V_{DIFF}$ voltage is programmable using the LVDS SWING register bits from ±125 mV to ±570 mV.

Additionally, a mode exists to double the strength of the LVDS buffer to support 50-Ω differential termination, as shown in Figure 41. This mode can be used when the output LVDS signal is routed to two separate receiver chips, each using a 100-Ω termination. The mode can be enabled using the LVDS DATA STRENGTH and LVDS CLKOUT STRENGTH register bits for data and output clock buffers, respectively.

The buffer output impedance behaves in the same way as a source-side series termination. By absorbing reflections from the receiver end, it helps to improve signal integrity.

## Device Functional Modes (continued)

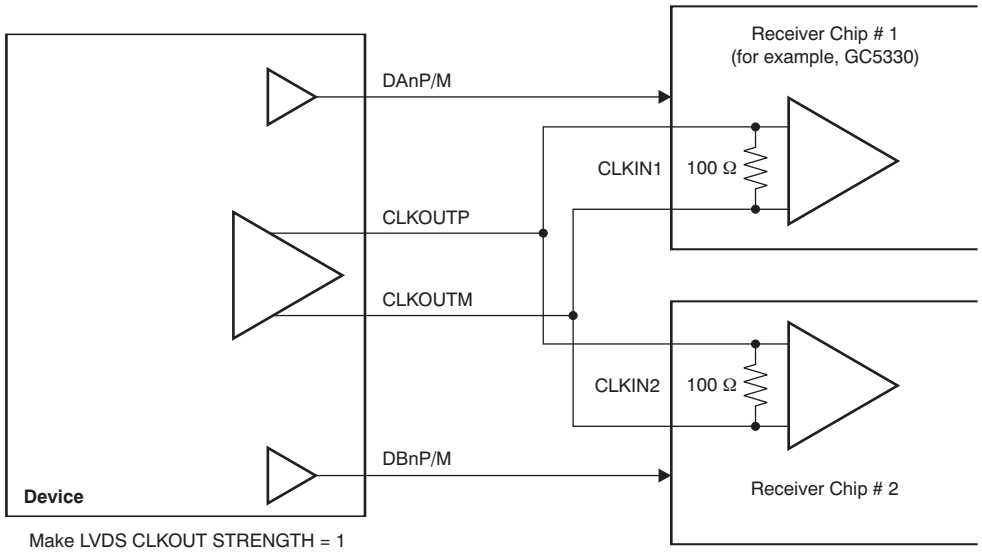



**Figure 41. LVDS Buffer Differential Termination**

## Device Functional Modes (continued)

### 8.4.1.4 Parallel CMOS Interface

In the CMOS mode, each data bit is output on separate pins as CMOS voltage level, every clock cycle, as Figure 42 shows. The rising edge of the output clock CLKOUT can be used to latch data in the receiver. It is recommended to minimize the load capacitance of the data and clock output pins by using short traces to the receiver. Furthermore, match the output data and clock traces to minimize the skew between them.

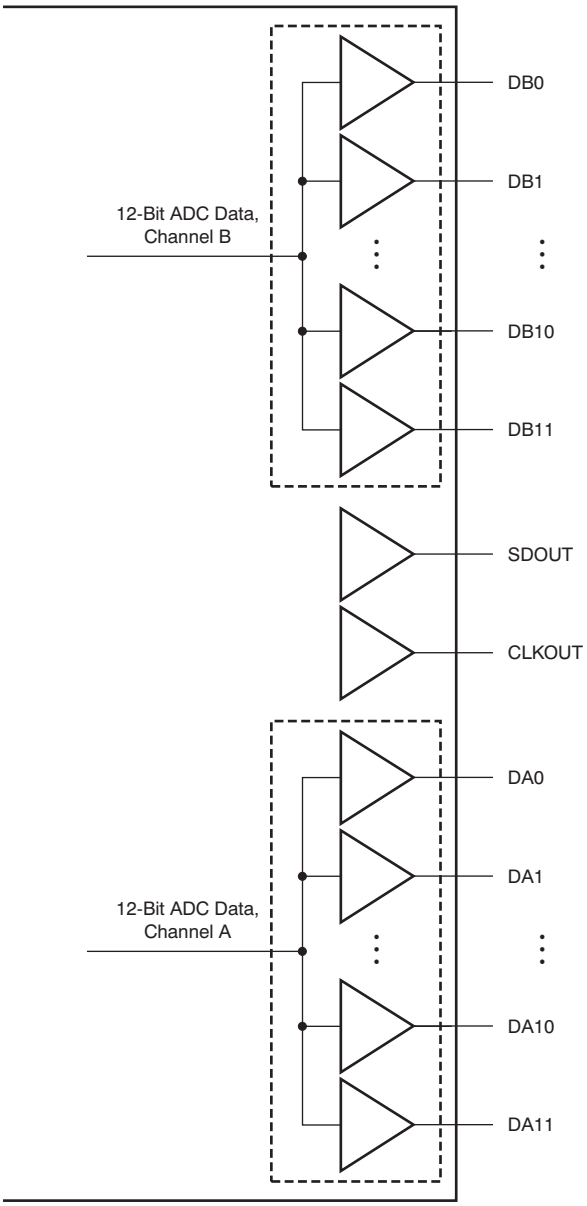



**Figure 42. CMOS Outputs**

### 8.4.1.5 CMOS Interface Power Dissipation

With CMOS outputs, the DRVDD current scales with the sampling frequency and the load capacitance on every output pin. The maximum DRVDD current occurs when each output bit toggles between 0 and 1 every clock cycle. In actual applications, this condition is unlikely to occur. The actual DRVDD current would be determined by the average number of output bits switching, which is a function of the sampling frequency and the nature of the analog input signal. This relationship is shown by the formula:

## Device Functional Modes (continued)

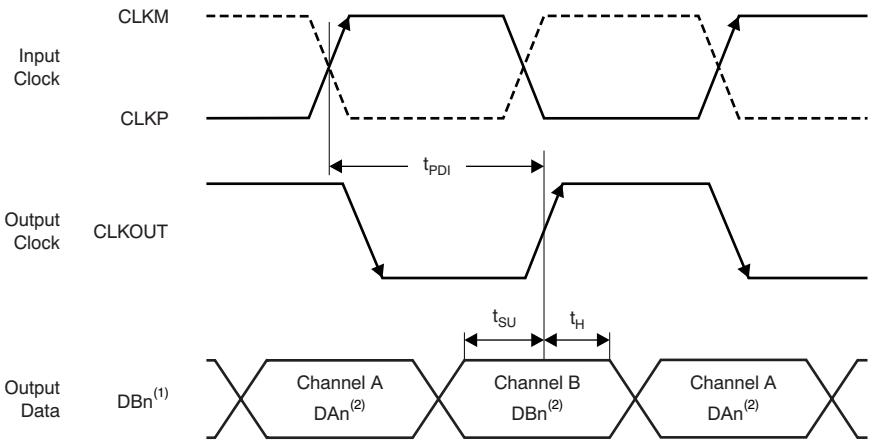
Digital current as a result of CMOS output switching = $C_L \times DRVDD \times (N \times F_{AVG})$

where

- $C_L$ = load capacitance,
- $N \times F_{AVG}$ = average number of output bits switching. (1)

### 8.4.1.6 Multiplexed Mode of Operation

In this mode, the digital outputs of both channels are multiplexed and output on a single bus (DB[11:0] pins), as shown in Figure 43. The channel A output pins (DA[11:0]) are in 3-state. Because the output data rate on the DB bus is effectively doubled, this mode is recommended only for low sampling frequencies (less than 80 MSPS). This mode can be enabled using the POWER-DOWN MODE register bits or using the CTRL[3:1] parallel pins.




(1) In multiplexed mode, both channels outputs come on the channel B output pins.

(2) Dn = bits D0, D1, D2, and so forth.

**Figure 43. Multiplexed Mode Timing Diagram**

## 8.5 Programming

Table 5 shows all the high-performance modes for the ADS4229 device.

**Table 5. High-Performance Modes(1)(2)**

| PARAMETER | DESCRIPTION |
|---|---|
| High-performance mode | Set the HIGH PERF MODE[2:1] register bit to obtain best performance across sample clock and input signal frequencies.<br>Register address = 03h, data = 03h |
| High-frequency mode | Set the HIGH FREQ MODE CH A and HIGH FREQ MODE CH B register bits for high input signal frequencies greater than 200 MHz.<br>Register address = 4Ah, data = 01h<br>Register address = 58h, data = 01h |
| High-speed mode | Set the HIGH PERF MODE[2:7] bits to obtain best performance across input signal frequencies for sampling rates greater than 160 MSPS.<br>Note that this mode changes VCM to 0.87 V from its default value of 0.95 V.<br>Register address = 2h, data = 40h<br>Register address = D5h, data = 18h<br>Register address = D7h, data = 0Ch<br>Register address = DBh, data = 20h |

(1) It is recommended to use these modes to obtain best performance.
(2) See the *Serial Interface Configuration* section for details on register programming.

### 8.5.1 Device Configuration

The ADS4229 can be configured independently using either parallel interface control or serial interface programming.

### 8.5.2 Parallel Configuration Only

To put the device into parallel configuration mode, keep RESET tied high (AVDD). Then, use the SEN, SCLK, CTRL1, CTRL2, and CTRL3 pins to directly control certain modes of the ADC. The device can be easily configured by connecting the parallel pins to the correct voltage levels (as described in Table 6 to Table 9). There is no need to apply a reset and SDATA can be connected to ground.

In this mode, SEN and SCLK function as parallel interface control pins. Some frequently-used functions can be controlled using these pins. Table 6 describes the modes controlled by the parallel pins.

**Table 6. Parallel Pin Definition**

| PIN | CONTROL MODE |
|---|---|
| SCLK | Low-speed mode selection |
| SEN | Output data format and output interface selection |
| CTRL1 | Together, these pins control the power-down modes |
| CTRL2 | |
| CTRL3 | |

### 8.5.3 Serial Interface Configuration Only

To enable this mode, the serial registers must first be reset to the default values and the RESET pin must be kept low. SEN, SDATA, and SCLK function as serial interface pins in this mode and can be used to access the internal registers of the ADC. The registers can be reset either by applying a pulse on the RESET pin or by setting the RESET bit high. The *Serial Register Map* section describes the register programming and the register reset process in more detail.

### 8.5.4 Using Both Serial Interface and Parallel Controls

For increased flexibility, a combination of serial interface registers and parallel pin controls (CTRL1 to CTRL3) can also be used to configure the device. To enable this option, keep RESET low. The parallel interface control pins CTRL1 to CTRL3 are available. After power-up, the device is automatically configured according to the voltage settings on these pins (see Table 9). SEN, SDATA, and SCLK function as serial interface digital pins and are used to access the internal registers of the ADC. The registers must first be reset to the default values either by applying a pulse on the RESET pin or by setting the RESET bit to '1'. After reset, the RESET pin must be kept low. The *Serial Register Map* section describes register programming and the register reset process in more detail.

### 8.5.5 Parallel Configuration Details

The functions controlled by each parallel pin are described in Table 7, Table 8, and Table 9. A simple way of configuring the parallel pins is shown in Figure 44.

**Table 7. SCLK Control Pin**

| VOLTAGE APPLIED ON SCLK | DESCRIPTION |
|---|---|
| Low | Low-speed mode is disabled |
| High | Low-speed mode is enabled |

**Table 8. SEN Control Pin**

| VOLTAGE APPLIED ON SEN | DESCRIPTION |
|---|---|
| 0<br>(+50mV/0mV) | Twos complement and parallel CMOS output |
| (3/8) AVDD<br>(±50mV) | Offset binary and parallel CMOS output |

**Table 8. SEN Control Pin (continued)**

| VOLTAGE APPLIED ON SEN | DESCRIPTION |
|---|---|
| (5/8) 2AVDD (±50mV) | Offset binary and DDR LVDS output |
| AVDD (0mV/–50mV) | Twos complement and DDR LVDS output |

**Table 9. CTRL1, CTRL2, and CTRL3 Pins**

| CTRL1 | CTRL2 | CTRL3 | DESCRIPTION |
|---|---|---|---|
| Low | Low | Low | Normal operation |
| Low | Low | High | Not available |
| Low | High | Low | Not available |
| Low | High | High | Not available |
| High | Low | Low | Global power-down |
| High | Low | High | Channel A standby, channel B is active |
| High | High | Low | Not available |
| High | High | High | MUX mode of operation, channel A and B data are multiplexed and output on the DB[11:0] pins. |

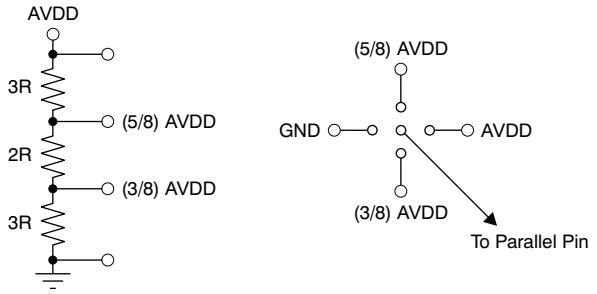



**Figure 44. Simple Scheme to Configure the Parallel Pins**

### 8.5.6 Serial Interface Details

The ADC has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), and SDATA (serial interface data) pins. Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA are latched at every SCLK falling edge when SEN is active (low). The serial data are loaded into the register at every 16th SCLK falling edge when SEN is low. When the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse. The first eight bits form the register address and the remaining eight bits are the register data. The interface can work with SCLK frequencies from 20 MHz down to very low speeds (of a few hertz) and also with non-50% SCLK duty cycle.

#### *8.5.6.1 Register Initialization*

After power-up, the internal registers must be initialized to the default values. Initialization can be accomplished in one of two ways:

1. Through a hardware reset by applying a high pulse on the RESET pin (of width greater than 10 ns), as shown in Figure 5 and *Serial Interface Timing Characteristics*; or
2. By applying a software reset. When using the serial interface, set the RESET bit high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low. See *Reset Timing (Only when Serial Interface is Used)* and Figure 6 for reset timing.

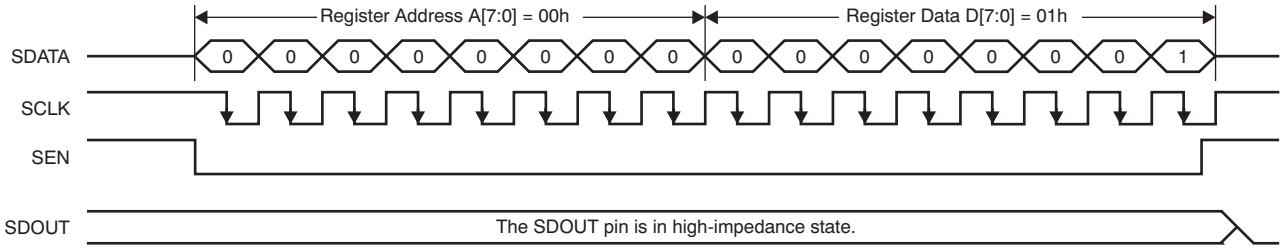
#### *8.5.6.2 Serial Register Readout*

The device includes a mode where the contents of the internal registers can be read back. This readback mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC. To use readback mode, follow this procedure:

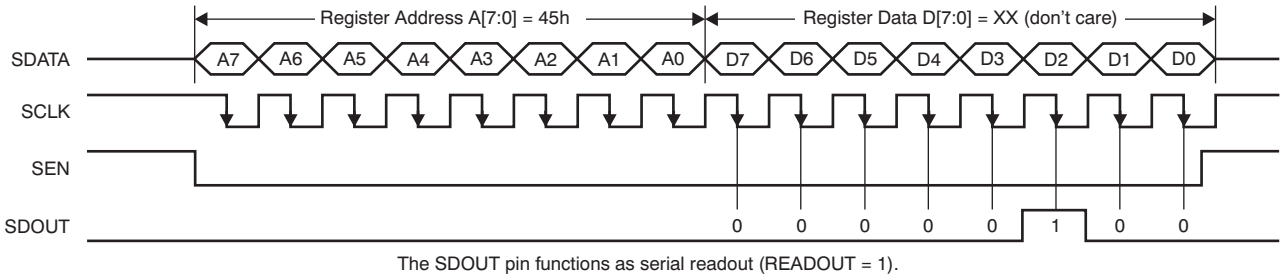
1. Set the READOUT register bit to '1'. This setting disables any further writes to the registers.
2. Initiate a serial interface cycle specifying the address of the register (A7 to A0) whose content has to be read.
3. The device outputs the contents (D7 to D0) of the selected register on the SDOUT pin (pin 64).
4. The external controller can latch the contents at the SCLK falling edge.
5. To enable register writes, reset the READOUT register bit to '0'.

The serial register readout works with both CMOS and LVDS interfaces on pin 64. See Figure 45 for serial readout timing diagram.

When READOUT is disabled, the SDOUT pin is in high-impedance state.




**a) Enable serial readout (READOUT = 1)**




**b) Read contents of Register 45h. This register has been initialized with 04h (device is put into global power-down mode.)**

**Figure 45. Serial Readout Timing Diagram**

## 8.6 Register Maps

### 8.6.1 Serial Register Map

Table 10 summarizes the functions supported by the serial interface.

**Table 10. Serial Interface Register Map(1)**

| REGISTER ADDRESS | REGISTER DATA | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| A[7:0] (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00 | 0 | 0 | 0 | 0 | 0 | 0 | RESET | READOUT |
| 01 | LVDS SWING | | | | | | 0 | 0 |
| 03 | 0 | 0 | 0 | 0 | 0 | 0 | HIGH PERF MODE 2 | HIGH PERF MODE 1 |
| 25 | CH A GAIN | | | | 0 | CH A TEST PATTERNS | | |
| 29 | 0 | 0 | 0 | DATA FORMAT | | 0 | 0 | 0 |
| 2B | CH B GAIN | | | | 0 | CH B TEST PATTERNS | | |
| 3D | 0 | 0 | ENABLE OFFSET CORR | 0 | 0 | 0 | 0 | 0 |
| 3F | 0 | 0 | CUSTOM PATTERN D[11:6] | | | | | |
| 40 | CUSTOM PATTERN D[5:0] | | | | | | 0 | 0 |
| 41 | LVDS CMOS | | CMOS CLKOUT STRENGTH | | 0 | 0 | DIS OBUF | |
| 42 | CLKOUT FALL POSN | | CLKOUT RISE POSN | | EN DIGITAL | 0 | 0 | 0 |
| 45 | STBY | LVDS CLKOUT STRENGTH | LVDS DATA STRENGTH | 0 | 0 | PDN GLOBAL | 0 | 0 |
| 4A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | HIGH FREQ MODE CH B |
| 58 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | HIGH FREQ MODE CH A |
| BF | CH A OFFSET PEDESTAL | | | | 0 | 0 | 0 | 0 |
| C1 | CH B OFFSET PEDESTAL | | | | 0 | 0 | 0 | 0 |
| CF | FREEZE OFFSET CORR | 0 | OFFSET CORR TIME CONSTANT | | | | 0 | 0 |
| EF | 0 | 0 | 0 | EN LOW SPEED MODE | 0 | 0 | 0 | 0 |
| F1 | 0 | 0 | 0 | 0 | 0 | 0 | EN LVDS SWING | |
| F2 | 0 | 0 | 0 | 0 | LOW SPEED MODE CH A | 0 | 0 | 0 |
| 2 | 0 | HIGH PERF MODE3 | 0 | 0 | 0 | 0 | 0 | 0 |
| D5 | 0 | 0 | 0 | HIGH PERF MODE4 | HIGH PERF MODE5 | 0 | 0 | 0 |
| D7 | 0 | 0 | 0 | 0 | HIGH PERF MODE6 | HIGH PERF MODE7 | 0 | 0 |
| DB | 0 | 0 | HIGH PERF MODE8 | 0 | 0 | 0 | 0 | LOW SPEED MODE CH B |

(1) Multiple functions in a register can be programmed in a single write operation. All registers default to '0' after reset.

### 8.6.2 Description of Serial Registers

#### *8.6.2.1 Register Address 00h (Default = 00h)*

**Figure 46. Register Address 00h (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | RESET | READOUT |

**Bits[7:2] Always write '0'**

**Bit 1 RESET: Software reset applied**

This bit resets all internal registers to the default values and self-clears to 0 (default = 1).

**Bit 0 READOUT: Serial readout**

This bit sets the serial readout of the registers.
0 = Serial readout of registers disabled; the SDOUT pin is placed in a high-impedance state.
1 = Serial readout enabled; the SDOUT pin functions as a serial data readout with CMOS logic levels running from the DRVDD supply. See the *Serial Register Readout* section.

#### *8.6.2.2 Register Address 01h (Default = 00h)*

**Figure 47. Register Address 01h (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LVDS SWING | | | | | | 0 | 0 |

**Bits[7:2] LVDS SWING: LVDS swing programmability**

These bits program the LVDS swing. Set the EN LVDS SWING bit to '1' before programming swing.
000000 = Default LVDS swing; ±350 mV with external 100-Ω termination
011011 = LVDS swing increases to ±410 mV
110010 = LVDS swing increases to ±465 mV
010100 = LVDS swing increases to ±570 mV
111110 = LVDS swing increases to ±200 mV
001111 = LVDS swing increases to ±125 mV

**Bits[1:0] Always write '0'**

#### *8.6.2.3 Register Address 03h (Default = 00h)*

**Figure 48. Register Address 03h (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | HIGH PERF MODE 2 | HIGH PERF MODE 1 |

**Bits[7:2] Always write '0'**

**Bits[1:0] HIGH PERF MODE[2:1]: High-performance mode**

00 = Default performance
01 = Do not use
10 = Do not use
11 = Obtain best performance across sample clock and input signal frequencies

### 8.6.2.4 Register Address 25h (Default = 00h)

**Figure 49. Register Address 25h (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CH A GAIN | | | | 0 | CH A TEST PATTERNS | | |

**Bits[7:4] CH A GAIN: Channel A gain programmability**

These bits set the gain programmability in 0.5-dB steps for channel A.

0000 = 0-dB gain (default after reset)
0001 = 0.5-dB gain
0010 = 1-dB gain
0011 = 1.5-dB gain
0100 = 2-dB gain
0101 = 2.5-dB gain
0110 = 3-dB gain
0111 = 3.5-dB gain
1000 = 4-dB gain
1001 = 4.5-dB gain
1010 = 5-dB gain
1011 = 5.5-dB gain
1100 = 6-dB gain

**Bit 3 Always write '0'**

**Bits[2:0] CH A TEST PATTERNS: Channel A data capture**

These bits verify data capture for channel A.
000 = Normal operation
001 = Outputs all 0s
010 = Outputs all 1s
011 = Outputs toggle pattern.
For the ADS4229, the output data D[11:0] are an alternating sequence of *101010101010* and *010101010101*.
100 = Outputs digital ramp.
101 = Outputs custom pattern; use registers 3Fh and 40h to set the custom pattern
110 = Unused
111 = Unused

### 8.6.2.5 Register Address 29h (Default = 00h)

**Figure 50. Register Address 29h (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | DATA FORMAT | | 0 | 0 | 0 |

**Bits[7:5] Always write '0'**

**Bits[4:3] DATA FORMAT: Data format selection**

00 = Twos complement
01 = Twos complement
10 = Twos complement
11 = Offset binary

**Bits[2:0] Always write '0'**

### 8.6.2.6 Register Address 2Bh (Default = 00h)

**Figure 51. Register Address 2Bh (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CH B GAIN | | | | 0 | CH B TEST PATTERNS | | |

**Bits[7:4] CH B GAIN: Channel B gain programmability**

These bits set the gain programmability in 0.5-dB steps for channel B.

0000 = 0-dB gain (default after reset)
0001 = 0.5-dB gain
0010 = 1-dB gain
0011 = 1.5-dB gain
0100 = 2-dB gain
0101 = 2.5-dB gain
0110 = 3-dB gain
0111 = 3.5-dB gain
1000 = 4-dB gain
1001 = 4.5-dB gain
1010 = 5-dB gain
1011 = 5.5-dB gain
1100 = 6-dB gain

**Bit 3 Always write '0'**

**Bits[2:0] CH B TEST PATTERNS: Channel B data capture**

These bits verify data capture for channel B.
000 = Normal operation
001 = Outputs all 0s
010 = Outputs all 1s
011 = Outputs toggle pattern.
For the ADS4229, the output data D[11:0] are an alternating sequence of *101010101010* and *010101010101*.
100 = Outputs digital ramp.
101 = Outputs custom pattern; use registers 3Fh and 40h to set the custom pattern
110 = Unused
111 = Unused

### 8.6.2.7 Register Address 3Dh (Default = 00h)

**Figure 52. Register Address 3Dh (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | ENABLE OFFSET CORR | 0 | 0 | 0 | 0 | 0 |

**Bits[7:6] Always write '0'**

**Bit 5 ENABLE OFFSET CORR: Offset correction setting**

This bit enables the offset correction.
0 = Offset correction disabled
1 = Offset correction enabled

**Bits[4:0] Always write '0'**

#### 8.6.2.8 Register Address 3Fh (Default = 00h)

**Figure 53. Register Address 3Fh (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | CUSTOM PATTERN D11 | CUSTOM PATTERN D10 | CUSTOM PATTERN D9 | CUSTOM PATTERN D8 | CUSTOM PATTERN D7 | CUSTOM PATTERN D6 |

**Bits[7:6] Always write '0'**

**Bits[5:0] CUSTOM PATTERN D[11:6]**

These are the six upper bits of the custom pattern available at the output instead of ADC data. The ADS4229 custom pattern is 12-bit.

#### 8.6.2.9 Register Address 40h (Default = 00h)

**Figure 54. Register Address 40h (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CUSTOM PATTERN D5 | CUSTOM PATTERN D4 | CUSTOM PATTERN D3 | CUSTOM PATTERN D2 | CUSTOM PATTERN D1 | CUSTOM PATTERN D0 | 0 | 0 |

**Bits[7:2] CUSTOM PATTERN D[5:0]**

These are the six lower bits of the custom pattern available at the output instead of ADC data. The ADS4229 custom pattern is 12-bit; use the CUSTOM PATTERN D[11:0] register bits.

**Bits[1:0] Always write '0'**

#### 8.6.2.10 Register Address 41h (Default = 00h)

**Figure 55. Register Address 41h (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LVDS CMOS | | CMOS CLKOUT STRENGTH | | 0 | 0 | DIS OBUF | |

**Bits[7:6] LVDS CMOS: Interface selection**

These bits select the interface.
00 = DDR LVDS interface
01 = DDR LVDS interface
10 = DDR LVDS interface
11 = Parallel CMOS interface

**Bits[5:4] CMOS CLKOUT STRENGTH**

These bits control the strength of the CMOS output clock.
00 = Maximum strength (recommended)
01 = Medium strength
10 = Low strength
11 = Very low strength

**Bits[3:2] Always write '0'**

**Bits[1:0] DIS OBUF**

These bits power down data and clock output buffers for both the CMOS and LVDS output interface. When powered down, the output buffers are in 3-state.
00 = Default
01 = Power-down data output buffers for channel B
10 = Power-down data output buffers for channel A
11 = Power-down data output buffers for both channels as well as the clock output buffer

### 8.6.2.11 Register Address 42h (Default = 00h)

**Figure 56. Register Address 42h (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CLKOUT FALL POSN | | CLKOUT RISE POSN | | EN DIGITAL | 0 | 0 | 0 |

**Bits[7:6] CLKOUT FALL POSN**

In LVDS mode:
00 = Default
01 = The falling edge of the output clock advances by 450 ps
10 = The falling edge of the output clock advances by 150 ps
11 = The falling edge of the output clock is delayed by 550 ps
In CMOS mode:
00 = Default
01 = The falling edge of the output clock is delayed by 150 ps
10 = Do not use
11 = The falling edge of the output clock advances by 100 ps

**Bits[5:6] CLKOUT RISE POSN**

In LVDS mode:
00 = Default
01 = The rising edge of the output clock advances by 450 ps
10 = The rising edge of the output clock advances by 150 ps
11 = The rising edge of the output clock is delayed by 250 ps
In CMOS mode:
00 = Default
01 = The rising edge of the output clock is delayed by 150 ps
10 = Do not use
11 = The rising edge of the output clock advances by 100 ps

**Bit 3 EN DIGITAL: Digital function enable**

0 = All digital functions disabled
1 = All digital functions (such as test patterns, gain, and offset correction) enabled

**Bits[2:0] Always write '0'**

### 8.6.2.12 Register Address 45h (Default = 00h)

**Figure 57. Register Address 45h (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| STBY | LVDS CLKOUT STRENGTH | LVDS DATA STRENGTH | 0 | 0 | PDN GLOBAL | 0 | 0 |

**Bit 7 STBY: Standby setting**

0 = Normal operation
1 = Both channels are put in standby; wakeup time from this mode is fast (typically 50 µs).

**Bit 6 LVDS CLKOUT STRENGTH: LVDS output clock buffer strength setting**

0 = LVDS output clock buffer at default strength to be used with 100-Ω external termination
1 = LVDS output clock buffer has double strength to be used with 50-Ω external termination

**Bit 5 LVDS DATA STRENGTH**

0 = All LVDS data buffers at default strength to be used with 100-Ω external termination
1 = All LVDS data buffers have double strength to be used with 50-Ω external termination

**Bits[4:3] Always write '0'**

**Bit 2 PDN GLOBAL**

0 = Normal operation
1 = Total power down; all ADC channels, internal references, and output buffers are powered down. Wakeup time from this mode is slow (typically 100 µs).

**Bits[1:0] Always write '0'**

### 8.6.2.13 Register Address 4Ah (Default = 00h)

**Figure 58. Register Address 4Ah (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | HIGH FREQ MODE CH B |

**Bits[7:1] Always write '0'**

**Bit 0 HIGH FREQ MODE CH B: High-frequency mode for channel B**

0 = Default
1 = Use this mode for high input frequencies greater than 200 MHz

### 8.6.2.14 Register Address 58h (Default = 00h)

**Figure 59. Register Address 58h (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | HIGH FREQ MODE CH A |

**Bits[7:1] Always write '0'**

**Bit 0 HIGH FREQ MODE CH A: High-frequency mode for channel A**

0 = Default
1 = Use this mode for high input frequencies greater than 200 MHz

### 8.6.2.15 Register Address BFh (Default = 00h)

**Figure 60. Register Address BFh (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CH A OFFSET PEDESTAL | | | | 0 | 0 | 0 | 0 |

**Bits[7:4] CH A OFFSET PEDESTAL: Channel A offset pedestal selection**

When the offset correction is enabled, the final converged value after the offset is corrected is the ADC midcode value. A pedestal can be added to the final converged value by programming these bits. See the *Offset Correction* section. Channels can be independently programmed for different offset pedestals by choosing the relevant register address.
For the ADS4229, the pedestal ranges from –8 to +7, so the output code can vary from midcode-8 to midcode+7 by adding pedestal D7-D4.

**Program bits D[7:4]**

0111 = Midcode+7
0110 = Midcode+6
0101 = Midcode+5
…
0000 = Midcode
1111 = Midcode-1
1110 = Midcode-2
1101 = Midcode-3
…
1000 = Midcode-8

**Bits[3:0] Always write '0'**

### 8.6.2.16 Register Address C1h (Default = 00h)

**Figure 61. Register Address C1h (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CH B OFFSET PEDESTAL | | | | 0 | 0 | 0 | 0 |

**Bits[7:4] CH B OFFSET PEDESTAL: Channel B offset pedestal selection**

When offset correction is enabled, the final converged value after the offset is corrected is the ADC midcode value. A pedestal can be added to the final converged value by programming these bits; see the *Offset Correction* section. Channels can be independently programmed for different offset pedestals by choosing the relevant register address.
For the ADS4229, the pedestal ranges from –8 to +7, so the output code can vary from midcode-8 to midcode+7 by adding pedestal D[7:4].

**Program Bits D[7:4]**

0111 = Midcode+7
0110 = Midcode+6
0101 = Midcode+5
…
0000 = Midcode
1111 = Midcode-1
1110 = Midcode-2
1101 = Midcode-3
…
1000 = Midcode-8

**Bits[3:0] Always write '0'**

### 8.6.2.17 Register Address CFh (Default = 00h)

**Figure 62. Register Address CFh (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FREEZE OFFSET CORR | 0 | OFFSET CORR TIME CONSTANT | | | | 0 | 0 |

**Bit 7 FREEZE OFFSET CORR: Freeze offset correction setting**

This bit sets the freeze offset correction estimation.
0 = Estimation of offset correction is not frozen (the EN OFFSET CORR bit must be set)
1 = Estimation of offset correction is frozen (the EN OFFSET CORR bit must be set); when frozen, the last estimated value is used for offset correction of every clock cycle. See the *Offset Correction* section.

**Bit 6 Always write '0'**

**Bits[5:2] OFFSET CORR TIME CONSTANT**

The offset correction loop time constant in number of clock cycles. Refer to the *Offset Correction* section.

**Bits[1:0] Always write '0'**

### 8.6.2.18 Register Address EFh (Default = 00h)

**Figure 63. Register Address EFh (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | EN LOW SPEED MODE | 0 | 0 | 0 | 0 |

**Bits[7:5] Always write '0'**

**Bit 4 EN LOW SPEED MODE: Enable control of low-speed mode through serial register bits**

This bit enables the control of the low-speed mode using the LOW SPEED MODE CH B and LOW SPEED MODE CH A register bits.
0 = Low-speed mode is disabled
1 = Low-speed mode is controlled by serial register bits

**Bits[3:0] Always write '0'**

### 8.6.2.19 Register Address F1h (Default = 00h)

**Figure 64. Register Address F1h (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | EN LVDS SWING | |

**Bits[7:2] Always write '0'**

**Bits[1:0] EN LVDS SWING: LVDS swing enable**

These bits enable LVDS swing control using the LVDS SWING register bits.
00 = LVDS swing control using the LVDS SWING register bits is disabled
01 = Do not use
10 = Do not use
11 = LVDS swing control using the LVDS SWING register bits is enabled

### 8.6.2.20 Register Address F2h (Default = 00h)

**Figure 65. Register Address F2h (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | LOW SPEED MODE CH A | 0 | 0 | 0 |

**Bits[7:4] Always write '0'**

**Bit 3 LOW SPEED MODE CH A: Channel A low-speed mode enable**

This bit enables the low-speed mode for channel A. Set the EN LOW SPEED MODE bit to '1' before using this bit.
0 = Low-speed mode is disabled for channel A
1 = Low-speed mode is enabled for channel A

**Bits[2:0] Always write '0'**

### 8.6.2.21 Register Address 2h (Default = 00h)

**Figure 66. Register Address 2h (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | HIGH PERF MODE3 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 7 Always write '0'**

**Bit 6 HIGH PERF MODE3**

HIGH PERF MODE3 to HIGH PERF MODE8 must be set to '1' to ensure best performance at high sampling speed (greater than 160 MSPS)

**Bits[5:0] Always write '0'**

### *8.6.2.22 Register Address D5h (Default = 00h)*

**Figure 67. Register Address D5h (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | HIGH PERF MODE4 | HIGH PERF MODE5 | 0 | 0 | 0 |

**Bits[7:5] Always write '0'**

**Bit 4 HIGH PERF MODE4**

HIGH PERF MODE3 to HIGH PERF MODE8 must be set to '1' to ensure best performance at high sampling speed (greater than 160 MSPS)

**Bit 3 HIGH PERF MODE5**

HIGH PERF MODE3 to HIGH PERF MODE8 must be set to '1' to ensure best performance at high sampling speed (greater than 160 MSPS)

**Bits[2:0] Always write '0'**

### *8.6.2.23 Register Address D7h (Default = 00h)*

**Figure 68. Register Address D7h (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | HIGH PERF MODE6 | HIGH PERF MODE7 | 0 | 0 |

**Bits[7:4] Always write '0'**

**Bit 3 HIGH PERF MODE6**

HIGH PERF MODE3 to HIGH PERF MODE8 must be set to '1' to ensure best performance at high sampling speed (greater than 160 MSPS)

**Bit 2 HIGH PERF MODE7**

HIGH PERF MODE3 to HIGH PERF MODE8 must be set to '1' to ensure best performance at high sampling speed (greater than 160 MSPS)

**Bits[1:0] Always write '0'**

### *8.6.2.24 Register Address DBh (Default = 00h)*

**Figure 69. Register Address DBh (Default = 00h)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | HIGH PERF MODE80 | 0 | 0 | 0 | 0 | LOW SPEED MODE CH B |

**Bits[7:6] Always write '0'**

**Bit 5 HIGH PERF MODE8**

HIGH PERF MODE3 to HIGH PERF MODE8 must be set to '1' to ensure best performance at high sampling speed (greater than 160 MSPS)

**Bits[4:1] Always write '0'**

**Bit 0 LOW SPEED MODE CH B: Channel B low-speed mode enable**

This bit enables the low-speed mode for channel B. Set the EN LOW SPEED MODE bit to '1' before using this bit.
0 = Low-speed mode is disabled for channel B
1 = Low-speed mode is enabled for channel B

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The ADS4229 dual-channel 12-bit ADC is designed for use in communications receivers designed to receive modern communication signals such as LTE, WIMAX, W-CDMA, and high-order QAM signals. A typical diversity receiver example is shown in Figure 70, where the antennas are placed at some distance to optimize performance in the presence of multipath fading. The path includes a low noise amplifier (LNA), RF mixer, and a digital variable gain amplifier (DVGA). Filtering is used throughout the path to remove blocking signals and mixing products and to prevent aliasing during sampling.

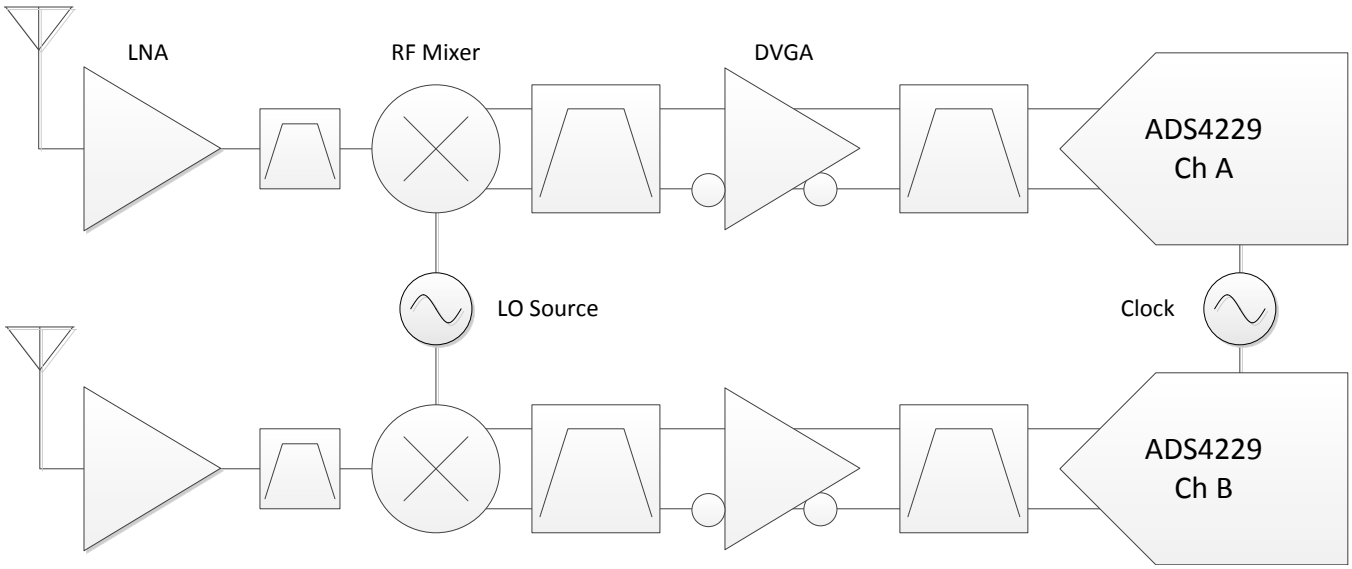



**Figure 70. Diversity Communications Receiver**

### 9.1.1 Theory of Operation

At every rising edge of the input clock, the analog input signal of each channel is simultaneously sampled. The sampled signal in each channel is converted by a pipeline of low-resolution stages. In each stage, the sampled/held signal is converted by a high-speed, low-resolution, flash sub-ADC. The difference between the stage input and the quantized equivalent is gained and propagates to the next stage. At every clock, each succeeding stage resolves the sampled input with greater accuracy. The digital outputs from all stages are combined in a digital correction logic block and digitally processed to create the final code after a data latency of 16 clock cycles. The digital output is available as either DDR LVDS or parallel CMOS and coded in either straight offset binary or binary twos complement format. The dynamic offset of the first stage sub-ADC limits the maximum analog input frequency to approximately 400 MHz (with 2-$V_{PP}$ amplitude) or approximately 600 MHz (with 1-$V_{PP}$ amplitude).

## Application Information (continued)

### 9.1.2 Analog Input

The analog input consists of a switched-capacitor-based, differential sample-and-hold (S/H) architecture. This differential topology results in very good ac performance even for high input frequencies at high sampling rates. The INP and INM pins must be externally biased around a common-mode voltage of 0.95 V, available on the VCM pin. For a full-scale differential input, each input pin (INP and INM) must swing symmetrically between VCM + 0.5 V and VCM – 0.5 V, resulting in a 2-$V_{PP}$ differential input swing. The input sampling circuit has a high 3-dB bandwidth that extends up to 550 MHz (measured from the input pins to the sampled voltage). Figure 71 shows an equivalent circuit for the analog input.

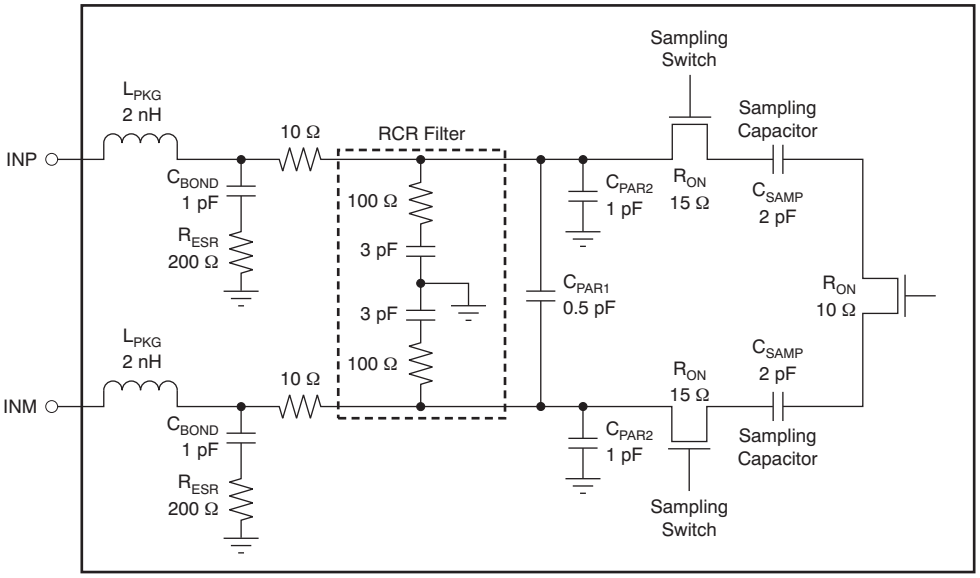



**Figure 71. Analog Input Equivalent Circuit**

#### *9.1.2.1 Drive Circuit Requirements*

For optimum performance, the analog inputs must be driven differentially. This operation improves the common-mode noise immunity and even-order harmonic rejection. A 5-Ω to 15-Ω resistor in series with each input pin is recommended to damp out ringing caused by package parasitics.

SFDR performance can be limited as a result of several reasons, including the effects of sampling glitches; nonlinearity of the sampling circuit; and nonlinearity of the quantizer that follows the sampling circuit. Depending on the input frequency, sample rate, and input amplitude, one of these factors generally plays a dominant part in limiting performance. At very high input frequencies (greater than approximately 300 MHz), SFDR is determined largely by the device sampling circuit nonlinearity. At low input amplitudes, the quantizer nonlinearity usually limits performance.

Glitches are caused by the opening and closing of the sampling switches. The driving circuit should present a low source impedance to absorb these glitches. Otherwise, glitches could limit performance, primarily at low input frequencies (up to approximately 200 MHz). It is also necessary to present low impedance (less than 50 Ω) for the common-mode switching currents. This configuration can be achieved by using two resistors from each input terminated to the common-mode voltage (VCM pin).

The device includes an internal R-C filter from each input to ground. The purpose of this filter is to absorb the sampling glitches inside the device itself. The cutoff frequency of the R-C filter involves a trade-off. A lower cutoff frequency (larger C) absorbs glitches better, but it reduces the input bandwidth. On the other hand, with a higher cutoff frequency (smaller C), bandwidth support is maximized. However, the sampling glitches must then be supplied by the external drive circuit. This tradeoff has limitations as a result of the presence of the package bond-wire inductance.

## Application Information (continued)

In the ADS4229, the R-C component values have been optimized while supporting high input bandwidth (up to 550 MHz). However, in applications with input frequencies up to 200 MHz to 300 MHz, the filtering of the glitches can be improved further using an external R-C-R filter; see Figure 74 and Figure 75.

In addition, the drive circuit may have to be designed to provide a low insertion loss over the desired frequency range and matched impedance to the source. Furthermore, the ADC input impedance must be considered. Figure 72 and Figure 73 show the impedance ($Z_{IN} = R_{IN} \parallel C_{IN}$) looking into the ADC input pins.

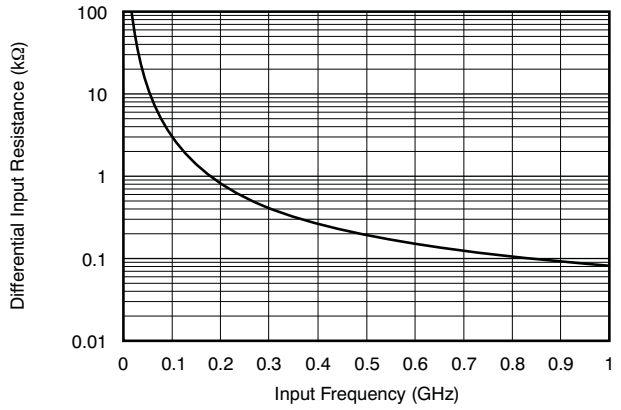



**Figure 72. ADC Analog Input Resistance ($R_{IN}$) Across Frequency**

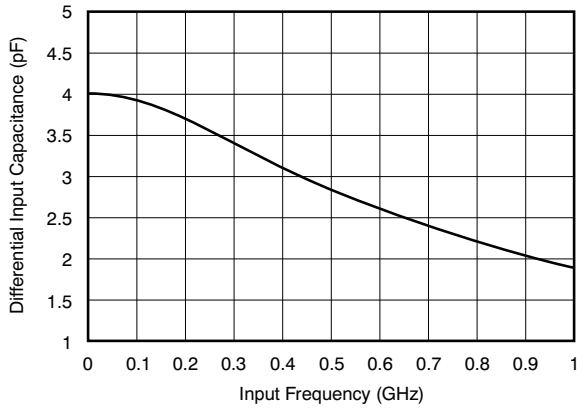



**Figure 73. ADC Analog Input Capacitance ($C_{IN}$) Across Frequency**

### 9.1.2.2 Driving Circuit

Figure 74, Figure 75, and Figure 76 show examples of driving circuit configurations optimized for low bandwidth (to support low input frequencies), high bandwidth (to support higher input frequencies), and very high bandwidth, respectively. Note that each of the drive circuits has been terminated by 50 Ω near the ADC side. The transformers (such as ADTL1-1WT or WBC1-1) can be used up to 270 MHz IF. For very high IF (> 270 MHz), transformer ADTL2-18 can be used. The termination is accomplished by a 25-Ω resistor from each input to the 0.95-V common-mode (VCM) from the device. This architecture allows the analog inputs to be biased around the required common-mode voltage.

The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch; good performance is obtained for high-frequency input signals. An optional termination resistor pair may be required between the two transformers, as shown in Figure 74, Figure 75, and Figure 76. The center point of this termination is connected to ground to improve the balance between the P and M sides. The values of the terminations between the transformers and on the secondary side must be chosen to obtain an effective 50 Ω (in the case of 50-Ω source impedance).

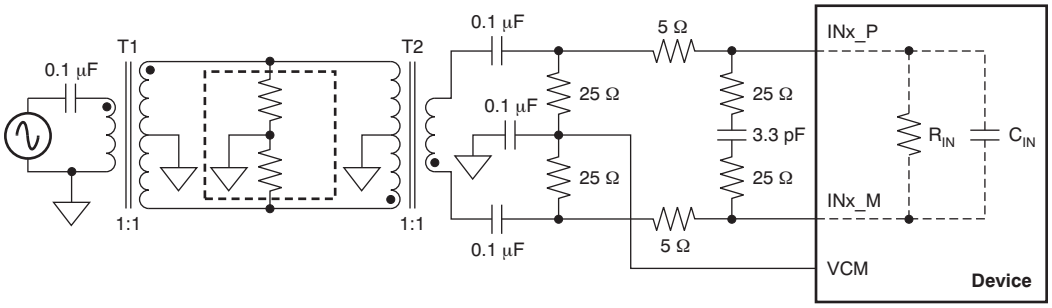



**Figure 74. Drive Circuit With Low Bandwidth (for Low Input Frequencies Less Than 150 MHz)**

## Application Information (continued)

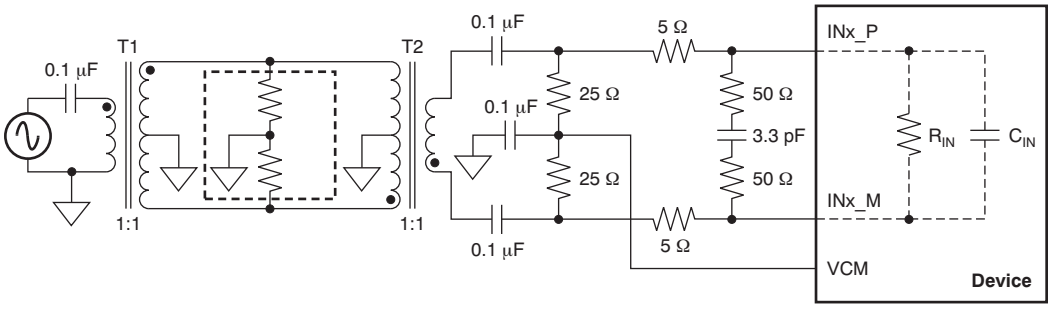



**Figure 75. Drive Circuit With High Bandwidth (for High Input Frequencies Greater Than 150 MHz and Less Than 270 MHz)**

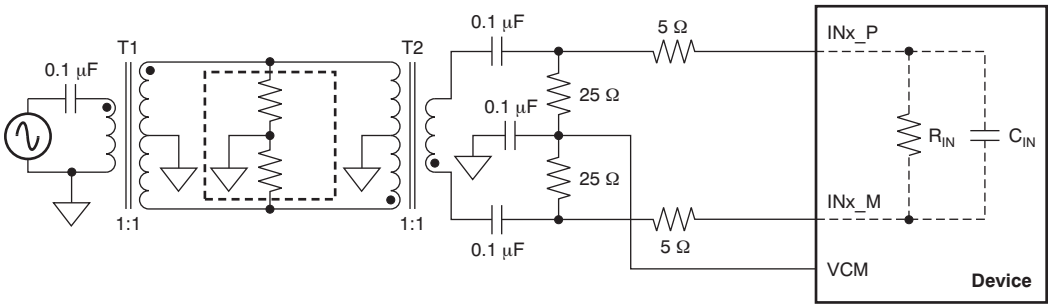



**Figure 76. Drive Circuit With Very High Bandwidth (Greater Than 270 MHz)**

All of these examples show 1:1 transformers being used with a 50-Ω source. As explained in the *Drive Circuit Requirements* section, this configuration helps to present a low source impedance to absorb the sampling glitches. With a 1:4 transformer, the source impedance is 200 Ω. The higher source impedance is unable to absorb the sampling glitches effectively and can lead to degradation in performance (compared to using 1:1 transformers).

In almost all cases, either a band-pass or low-pass filter is required to obtain the desired dynamic performance, as shown in Figure 77. Such filters present low source impedance at the high frequencies corresponding to the sampling glitch and help avoid performance losses associated with the high source impedance.

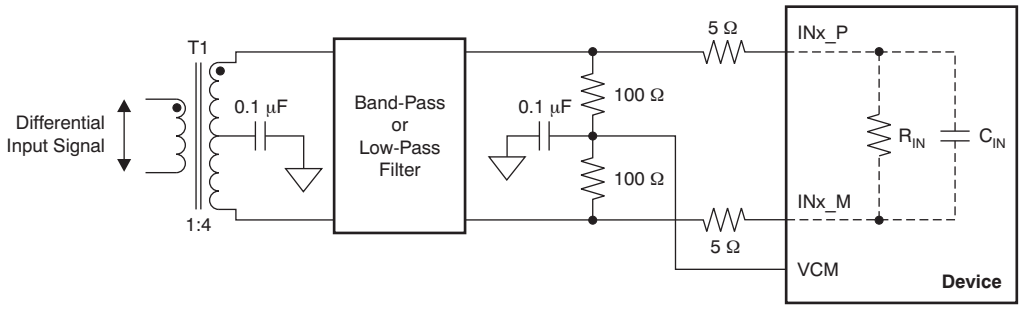
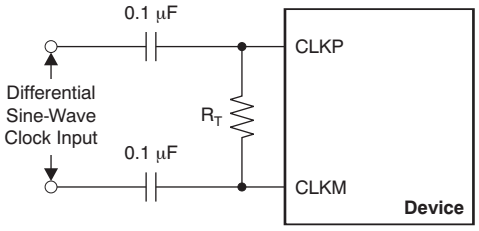



**Figure 77. Drive Circuit With a 1:4 Transformer**

## Application Information (continued)

### 9.1.3 Clock Input

The ADS4229 clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to VCM using internal 5-kΩ resistors. This setting allows the use of transformer-coupled drive circuits for sine-wave clock or ac-coupling for LVPECL and LVDS clock sources are shown in Figure 78, Figure 79, and Figure 80. The internal clock buffer is shown in Figure 81.




(1) $R_T$ = termination resister, if necessary.

**Figure 78. Differential Sine-Wave Clock Driving Circuit**

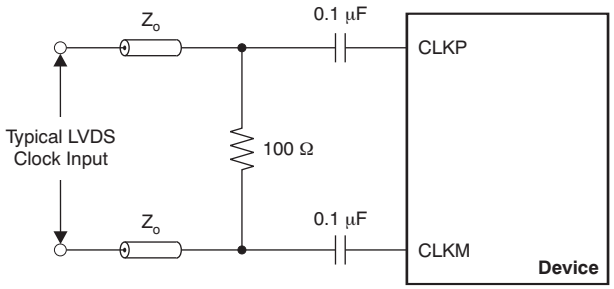



**Figure 79. LVDS Clock Driving Circuit**

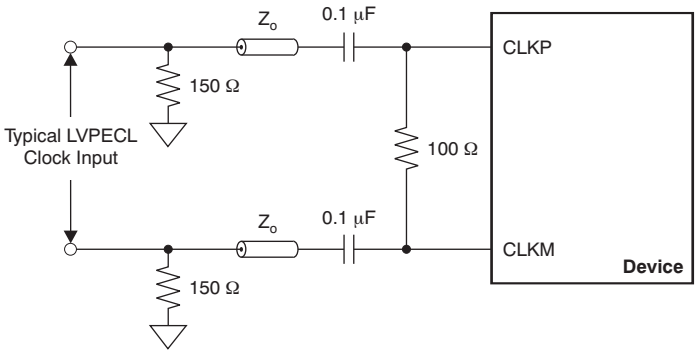
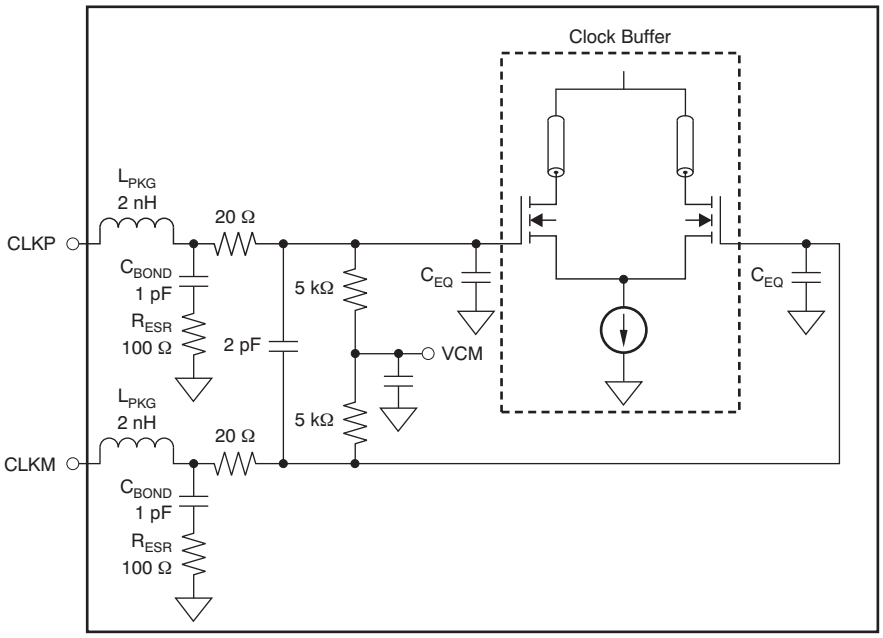



**Figure 80. LVPECL Clock Driving Circuit**

## Application Information (continued)




NOTE: $C_{EQ}$ is 1 pF to 3 pF and is the equivalent input capacitance of the clock buffer.

**Figure 81. Internal Clock Buffer**

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1-µF capacitor, as shown in Figure 82. For best performance, the clock inputs must be driven differentially, thereby reducing susceptibility to common-mode noise. For high input frequency sampling, it is recommended to use a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input.

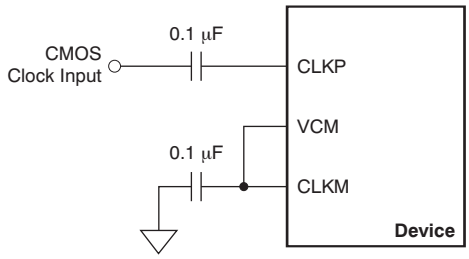



**Figure 82. Single-Ended Clock Driving Circuit**

## 9.2 Typical Application

An example schematic for a typical application of the ADS4229 is shown in Figure 83.

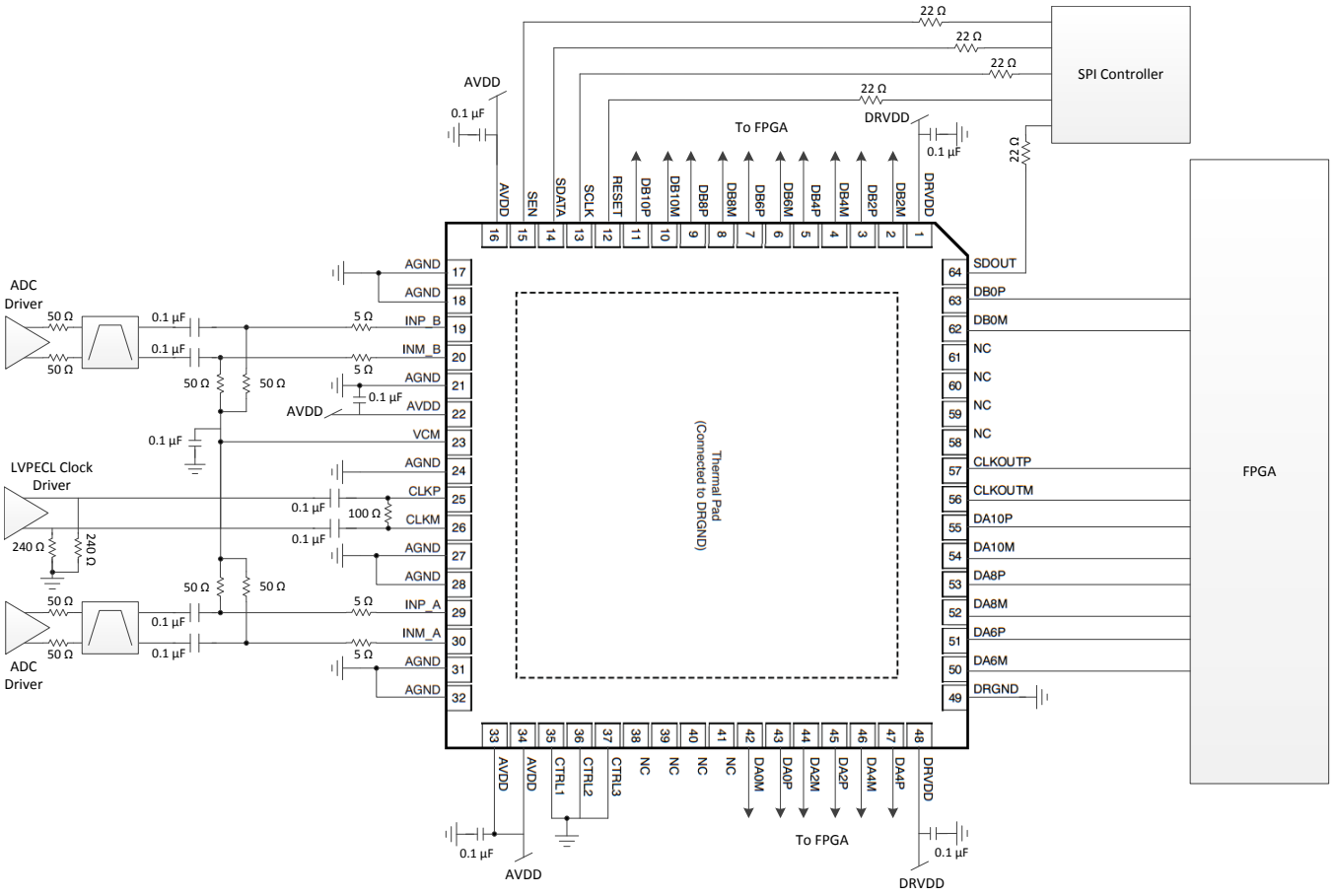



**Figure 83. Example Schematic for ADS4229**

### 9.2.1 Design Requirements

Example design requirements are listed in Table 11 for the ADC portion of the signal chain. These do not necessary reflect the requirements of an actual system, but rather demonstrate why the ADS4229 may be chosen for a system based on a set of requirements.

**Table 11. Example Design Requirements for ADS4229**

| DESIGN PARAMETER | EXAMPLE DESIGN REQUIREMENT | ADS4229 CAPABILITY |
|---|---|---|
| Sampling rate | ≥ 245.76 Msps to allow 80 MHz of unaliased bandwidth | Max sampling rate: 250 Msps |
| Input frequency | > 250 MHz to accommodate full 2nd nyquist zone operation | Large signal –3 dB bandwidth: 400 MHz |
| SNR | > 65 dBFS at –1 dFBS, 170 MHz | 69.8 dBFS at –1 dBFS, 170 MHz |
| SFDR | > 75 dBc at –1 dFBS, 170 MHz | 80 dBc at –1 dBFS, 170 MHz |
| Input full scale voltage | 2 Vpp | 2 Vpp |
| Channel-to-channel isolation | < 80 dB | 95 dB |
| Overload recovery time | < 3 clock cycles | 1 clock cycle |
| Digital interface | Parallel LVDS | Parallel LVDS |
| Power consumption | < 300 mW per channel | 273 mW per channel |

### 9.2.2 Detailed Design Procedure

#### *9.2.2.1 Analog Input*

The analog inputs of the ADS4229 are typically driven by a fully differential amplifier. The amplifier must have sufficient bandwidth for the frequencies of interest. The noise and distortion performance of the amplifier will affect the combined performance of the ADC and amplifier. The amplifier is often AC coupled to the ADC to allow both the amplifier and ADC to operate at the optimal common mode voltages. It is possible to DC couple the amplifier to the ADC if required. An alternate approach is to drive the ADC using transformers. DC coupling cannot be used with the transformer approach.

#### *9.2.2.2 Common Mode Voltage Output (VCM)*

The common mode voltage output is shared between both ADC channels. To maintain optimal isolation, an LC filter may need to be placed on the VCM node between the channels (not shown in schematic). At a minimum, a bypass capacitor should be placed on the node that has sufficiently low impedance at the desired operating frequencies. Note the VCM pin maximum output current in the electrical tables when using VCM in alternate ways.

#### *9.2.2.3 Clock Driver*

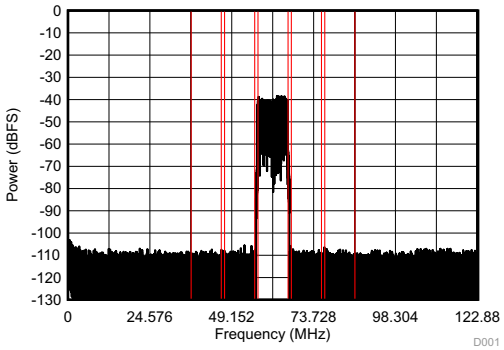
The ADS4229 supports both LVDS and CMOS interfaces. The LVDS interface should be used for best performance when operating at maximum sampling rate. The LVDS outputs can be connected directly to the FPGA without any additional components. When using CMOS outputs resistors should be placed in series with the outputs to reduce the output current spikes to limit the performance degradation. The resistors should be large enough to limit current spikes but not so large as to significantly distort the digital output waveform. An external CMOS buffer should be used when driving distances greater than a few inches to reduce ground bounce within the ADC.

#### *9.2.2.4 Digital Interface*

The ADS4229 supports both LVDS and CMOS interfaces. The LVDS interface should be used for best performance when operating at maximum sampling rate. The LVDS outputs can be connected directly to the FPGA without any additional components. When using CMOS outputs resistors should be placed in series with the outputs to reduce the output current spikes to limit the performance degradation. The resistors should be large enough to limit current spikes but not so large as to significantly distort the digital output waveform. An external CMOS buffer should be used when driving distances greater than a few inches to reduce ground bounce within the ADC.

### 9.2.3 Application Curve

Figure 83 shows the results of a 10-MHz LTE signal centered at 184.32 MHz captured by the ADS4229.




Ref. Power = –11.98 dFBS Lower Adj. = 69.92 dBc Lower Alt. = 70.28 dBc
Upper Adj. = 69.92 dBc Upper Alt. = 70.17 dBc

**Figure 84. 10-MHz LTE Signal Captured by ADS4229**

# 10 Power Supply Recommendations

The ADS4229 has two power supplies, one analog (AVDD) and one digital (DRVDD) supply. Both supplies have a nominal voltage of 1.8 V. The AVDD supply is noise sensitive and the digital supply is not.

## 10.1 Sharing DRVDD and AVDD Supplies

For best performance the AVDD supply should be driven by a low noise linear regulator (LDO) and separated from the DRVDD supply. It is possible to have AVDD and DRVDD share a single supply but they should be isolated by a ferrite bead and bypass capacitors, in a PI-filter configuration, at a minimum. The digital noise will be concentrated at the sampling frequency and harmonics of the sampling frequency and could contain noise related to the sampled signal. While developing schematics, it is a good idea to leave extra placeholders for additional supply filtering.

## 10.2 Using DC/DC Power Supplies

For best performance the AVDD supply should be driven by a low noise linear regulator (LDO) and separated from the DRVDD supply. It is possible to have AVDD and DRVDD share a single supply but they should be isolated by a ferrite bead and bypass capacitors, in a PI-filter configuration, at a minimum. The digital noise will be concentrated at the sampling frequency and harmonics of the sampling frequency and could contain noise related to the sampled signal. While developing schematics, it is a good idea to leave extra placeholders for additional supply filtering.

## 10.3 Power Supply Bypassing

Because the ADS4229 already includes internal decoupling, minimal external decoupling can be used without loss in performance. Note that decoupling capacitors can help filter external power-supply noise; thus, the optimum number of capacitors depends on the actual application. A 0.1-uF capacitor is recommended near each supply pin. The decoupling capacitors should be placed very close to the converter supply pins.

# 11 Layout

## 11.1 Layout Guidelines

### 11.1.1 Grounding

A single ground plane is sufficient to give good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. See the *ADS4226 Evaluation Module* (SLAU333) for details on layout and grounding.

### 11.1.2 Exposed Pad

In addition to providing a path for heat dissipation, the PowerPAD is also electrically connected internally to the digital ground. Therefore, it is necessary to solder the exposed pad to the ground plane for best thermal and electrical performance. For detailed information, see application notes *QFN Layout Guidelines* (SLOA122) and *QFN/SON PCB Attachment* (SLUA271).

### 11.1.3 Routing Analog Inputs

It is advisable to route differential analog input pairs (INP_x and INM_x) close to each other. To minimize the possibility of coupling from a channel analog input to the sampling clock, the analog input pairs of both channels should be routed perpendicular to the sampling clock; see the *ADS4226 Evaluation Module* (SLAU333) for reference routing. Figure 85 shows a snapshot of the PCB layout from the ADS42xxEVM.

### 11.1.4 Routing Digital Outputs

The digital outputs should be routed away from the analog inputs and any noise sensitive circuits. Avoid routing the digital outputs in parallel to any analog trace. The digital outputs should be routed over a solid ground plane all the way to the FPGA. Keep the digital traces as short as possible to reduce EMI emissions. The traces should be matched length to maintain timing, however mismatches in the trace lengths can be taken into account by including the delay differences in the FPGA timing constraints.

## 11.2 Layout Example

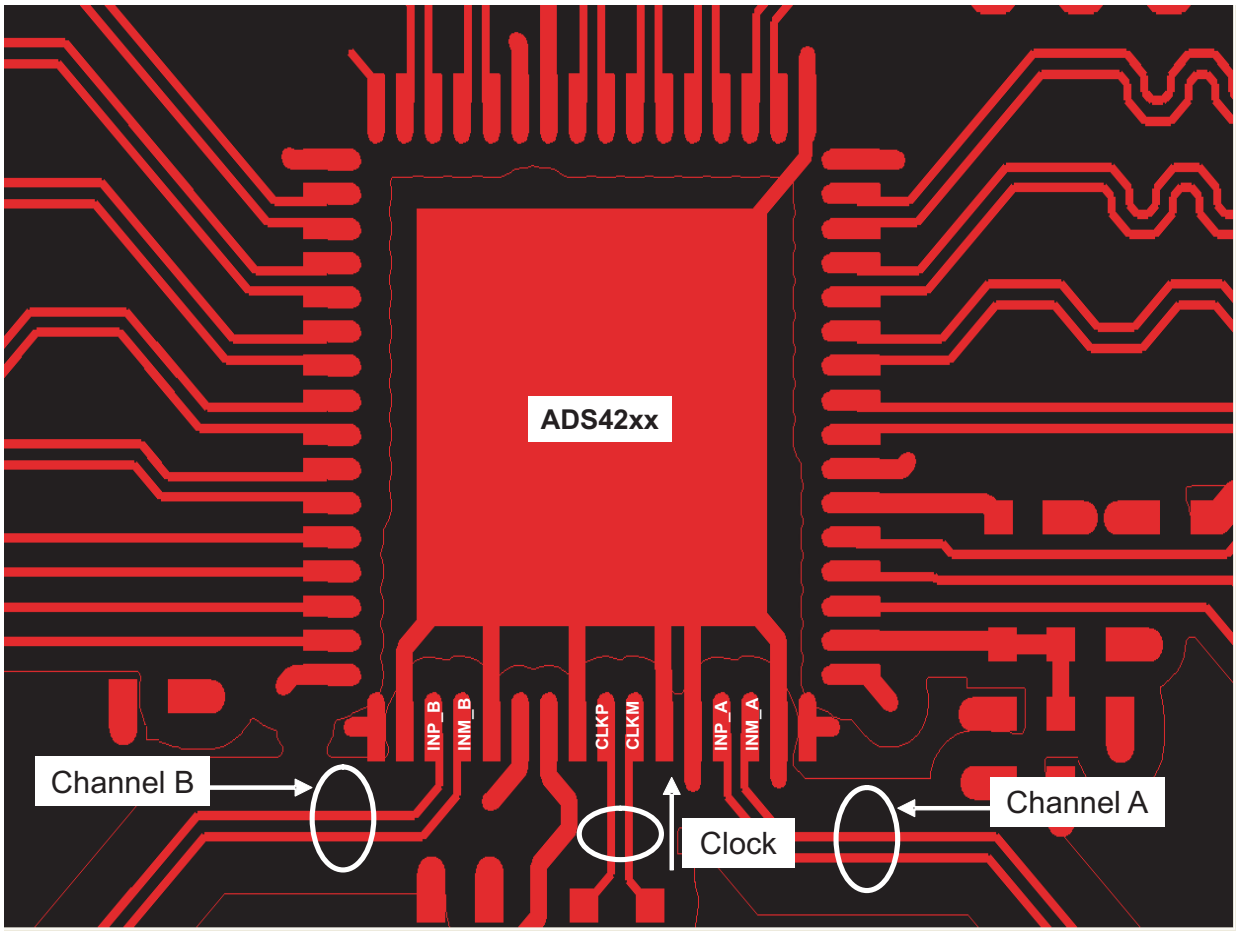



**Figure 85. ADS42xxEVM PCB Layout**

# 12 器件和文档支持

## 12.1 器件支持

### 12.1.1 开发支持

#### *12.1.1.1 技术参数定义*

**模拟带宽 –** 基频功率相对低频值下降 3dB 时的模拟输入频率。

**孔径延迟 –** 从输入采样时钟的上升沿到实际发生采样之间的延迟时间。 该延迟在各通道中会有所不同。 最大差值被定义为孔径延迟差异（通道间）。

**孔径不确定性（抖动） –** 采样间的孔径延迟差异。

**时钟脉冲宽度/占空比 –** 时钟信号的占空比为时钟信号保持逻辑高电平的时间（时钟脉冲宽度）与时钟信号周期的比值。 占空比通常以百分比的形式表示。 理想差分正弦波时钟的占空比为 50%。

**最大转换速率 –** 执行指定操作时所采用的最大采样率。 除非另外注明，否则所有参数测试均以该采样率执行。

**最小转换速率 –** ADC 正常工作时的最小采样率。

**微分非线性 (DNL) –** 理想 ADC 对模拟输入值进行编码转换时以 1 LSB 为步长。 DNL 是指任意单个步长与这一理想值之间的偏差（以 LSB 为计量单位）。

**积分非线性 (INL) –** INL 是 ADC 传递函数与其最小二乘法曲线拟合所确定的最佳拟合曲线的偏差（以 LSB 为计量单位）。

**增益误差 –** 增益误差是指 ADC 实际输入满量程范围与其理想值的偏差。 增益误差以理想输入满量程范围的百分比形式表示。 增益误差包括两部分：基准不精确所导致的误差 ($E_{GREF}$) 和通道所导致的误差 ($E_{GCHAN}$)。 这两种误差分别定义为 $E_{GREF}$ 和 $E_{GCHAN}$。

对于一阶近似，总增益误差 $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$。

例如，如果 $E_{TOTAL} = \pm 0.5\%$，则满量程输入范围为 $(1 – 0.5 / 100) \times FS_{ideal}$ 至 $(1 + 0.5 / 100) \times FS_{ideal}$。

**偏移误差 –** 偏移误差是指 ADC 实际平均空闲通道输出编码与理想平均空闲通道输出编码之间的差值（以 LSB 数表示）。 该数量通常转换为毫伏。

**温度漂移 –** 温度漂移系数（相对于增益误差和偏移误差）指定参数从 $T_{MIN}$ 到 $T_{MAX}$ 每摄氏度的变化量。 温度漂移的计算方法是用参数在 $T_{MIN}$ 至 $T_{MAX}$ 范围内的最大变化量除以 $T_{MAX} – T_{MIN}$ 的值。

**信噪比 –** SNR 是指基频功率 ($P_S$) 与噪底功率 ($P_N$) 的比值，不包括直流功率和前 9 个谐波的功率。

$$SNR = 10Log^{10} \frac{P_S}{P_N} \quad (2)$$

当基频的绝对功率用作基准时，SNR 以 dBc（相对于载波的分贝数）为单位；当基频功率被外推至转换器满量程范围时，SNR 以 dBFS（相对于满量程的分贝数）为单位。

**信噪比和失真 (SINAD) –** SINAD 是指基频功率 ($P_S$) 与所有其他频谱成分（包括噪声 ($P_N$) 和失真 ($P_D$)，但不包括直流）功率的比值。

$$SINAD = 10Log^{10} \frac{P_S}{P_N + P_D} \quad (3)$$

当基频的绝对功率用作基准时，SINAD 以 dBc（相对于载波的分贝数）为单位；当基频功率被外推至转换器满量程范围时，SINAD 以 dBFS（相对于满量程的分贝数）为单位。

**有效位数 (ENOB) –** ENOB 测量的是转换器相对于理论限值（基于量化噪声）的性能。

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (4)$$

**总谐波失真 (THD) –** THD 是指基频功率 ($P_S$) 与前 9 个谐波功率 ($P_D$) 的比值。

器件支持 (接下页)

$$THD = 10Log^{10} \frac{P_S}{P_N} \quad (5)$$

THD 通常以 dBc 为单位（相对于载波的分贝数）。

**无杂散动态范围 (SFDR) –** 基频功率与最高的其他频谱成分（毛刺或谐波）功率的比值。 SFDR 通常以 dBc 为单位（相对于载波的分贝数）。

**双频互调失真 –** IMD3 是指基频功率（$f_1$ 和 $f_2$ 频率处）与最差频谱成分（$2f_1 – f_2$ 或 $2f_2 – f_1$ 频率处）功率的比值。当基频的绝对功率用作基准时，IMD3 以 dBc（相对于载波的分贝数）为单位；当基频功率被外推至转换器满量程范围时，IMD3 以 dBFS（相对于满量程的分贝数）为单位。

**直流电源抑制比 (DC PSRR) –** DC PSSR 是偏移误差变化量与模拟电源电压变化量的比值。 DC PSRR 通常以 mV/V 为单位进行表示。

**交流电源抑制比 (AC PSRR) –** AC PSRR 测量的是 ADC 对电源电压变化的抑制能力。 如果 $\Delta V_{SUP}$ 表示电源电压的变化，$\Delta V_{OUT}$ 表示 ADC 输出编码的相应变化（相对输入而言），则：

$$PSRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{SUP}} \text{ (Expressed in dBc)} \quad (6)$$

**电压过载恢复 –** 使过载的模拟输入端的误差恢复至 1% 以下所需的时钟数。 该技术参数的测试方法是分别施加具有 6dB 正过载和负过载的正弦波信号。 然后记录下过载后前几个采样（相对于期望值）的偏差。

**共模抑制比 (CMRR) –** CMRR 测量的是 ADC 对模拟输入共模变化的抑制能力。 如果 $\Delta V_{CM\_IN}$ 表示输入引脚的共模电压变化，$\Delta V_{OUT}$ 表示 ADC 输出编码的相应变化（相对输入而言），则：

$$CMRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{CM}} \text{ (Expressed in dBc)} \quad (7)$$

**串扰（仅限多通道 ADC）–** 串扰测量的是目标通道与其相邻通道之间的内部信号耦合。 串扰分两种情况：一种是与紧邻通道（近端通道）之间的耦合，另一种是与跨封装通道（远端通道）之间的耦合。 通常采用对邻近通道施加满量程信号的方式来测量串扰。 串扰是指耦合信号功率（在目标通道的输出端测得）与邻近通道输入端所施加信号功率的比值。 串扰通常以 dBc 为单位进行表示。

## 12.2 文档支持

### 12.2.1 相关文档

相关文档如下：

- *《QFN 布局指南》*（文献编号：SLOA122）
- *《QFN/SON PCB 连接》*（文献编号：SLUA271）
- *《ADS4226 评估模块》*（文献编号：SLAU333）

## 12.3 社区资源

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## 12.4 商标

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### 12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 12.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

## 13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| ADS4229IRGCR | Active | Production | VQFN (RGC) \| 64 | 2000 \| LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ4229 |
| ADS4229IRGCR.A | Active | Production | VQFN (RGC) \| 64 | 2000 \| LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ4229 |
| ADS4229IRGCT | Active | Production | VQFN (RGC) \| 64 | 250 \| SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ4229 |
| ADS4229IRGCT.A | Active | Production | VQFN (RGC) \| 64 | 250 \| SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ4229 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

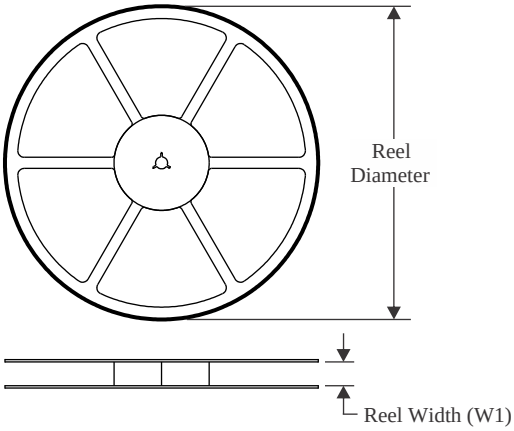
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

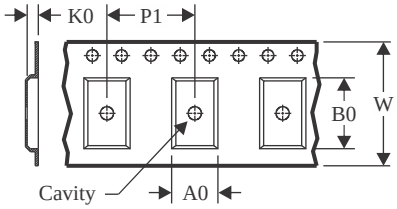
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

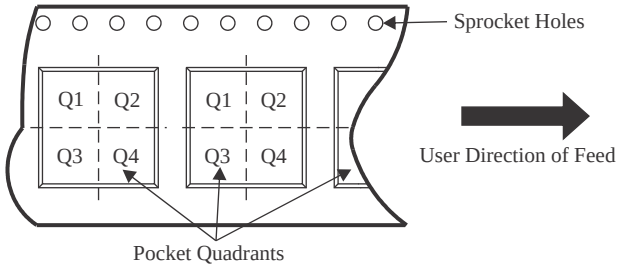



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

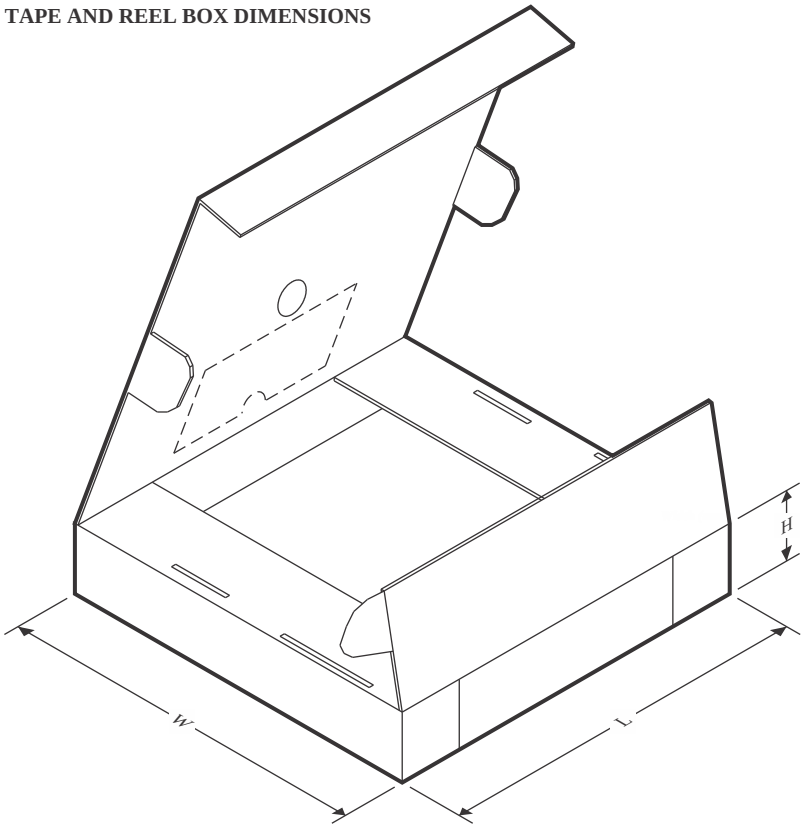
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS4229IRGCR | VQFN | RGC | 64 | 2000 | 330.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ADS4229IRGCR | VQFN | RGC | 64 | 2000 | 350.0 | 350.0 | 43.0 |

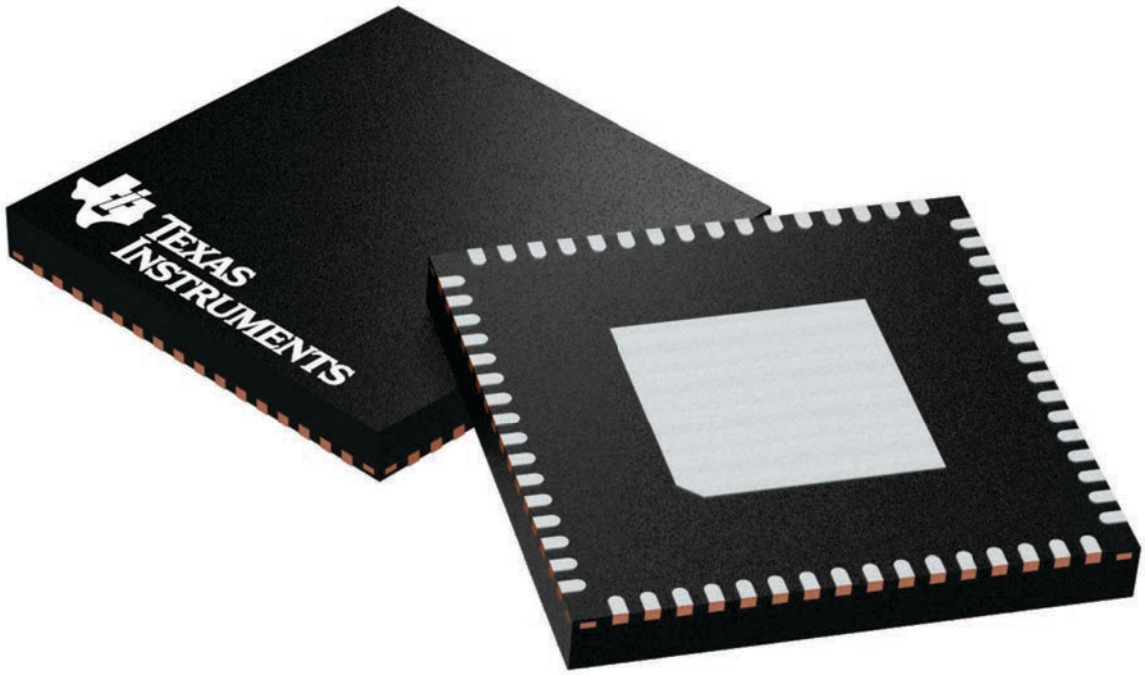
# GENERIC PACKAGE VIEW

## RGC 64

## VQFN - 1 mm max height

**9 x 9, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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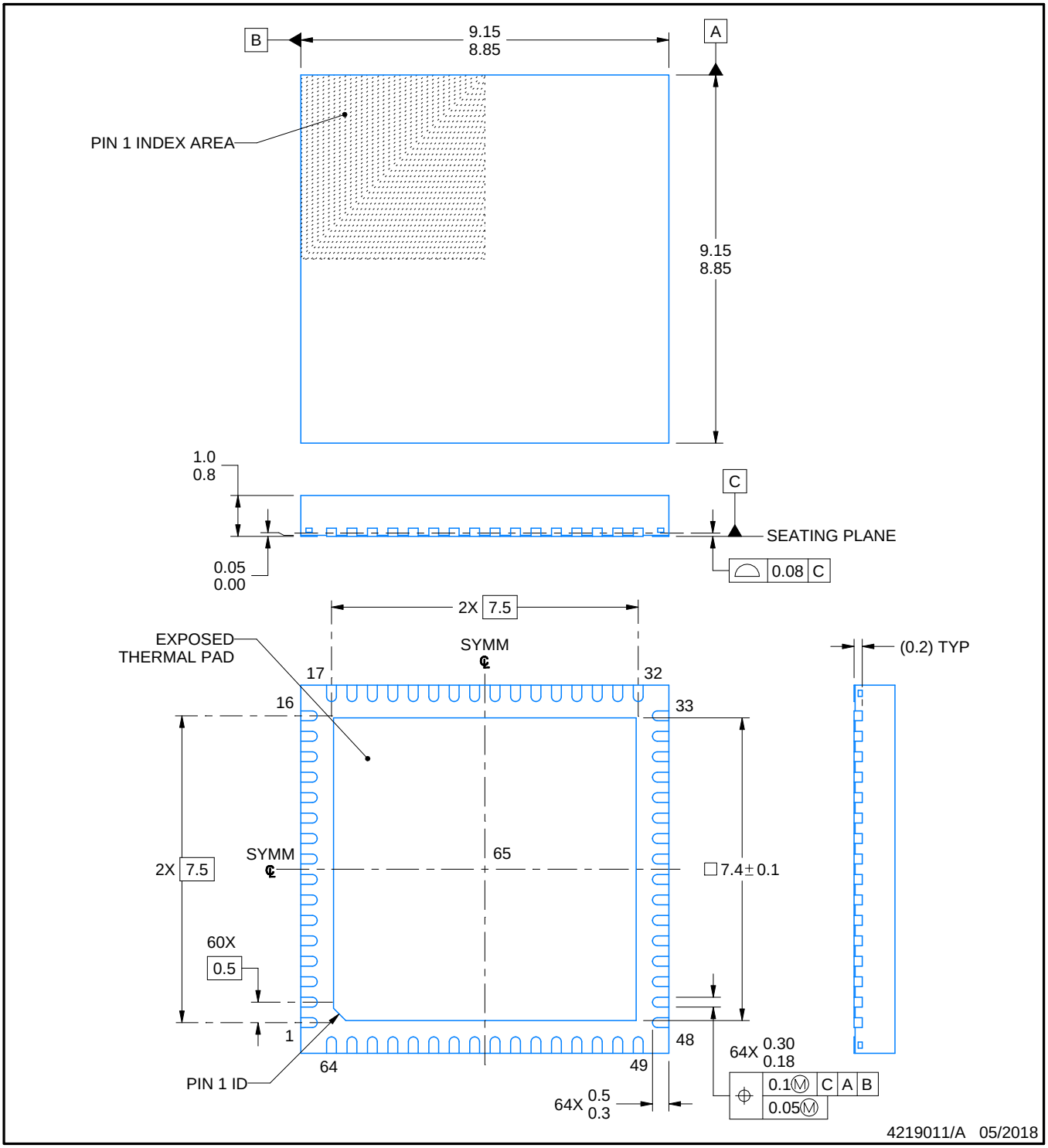
# RGC0064H

# PACKAGE OUTLINE

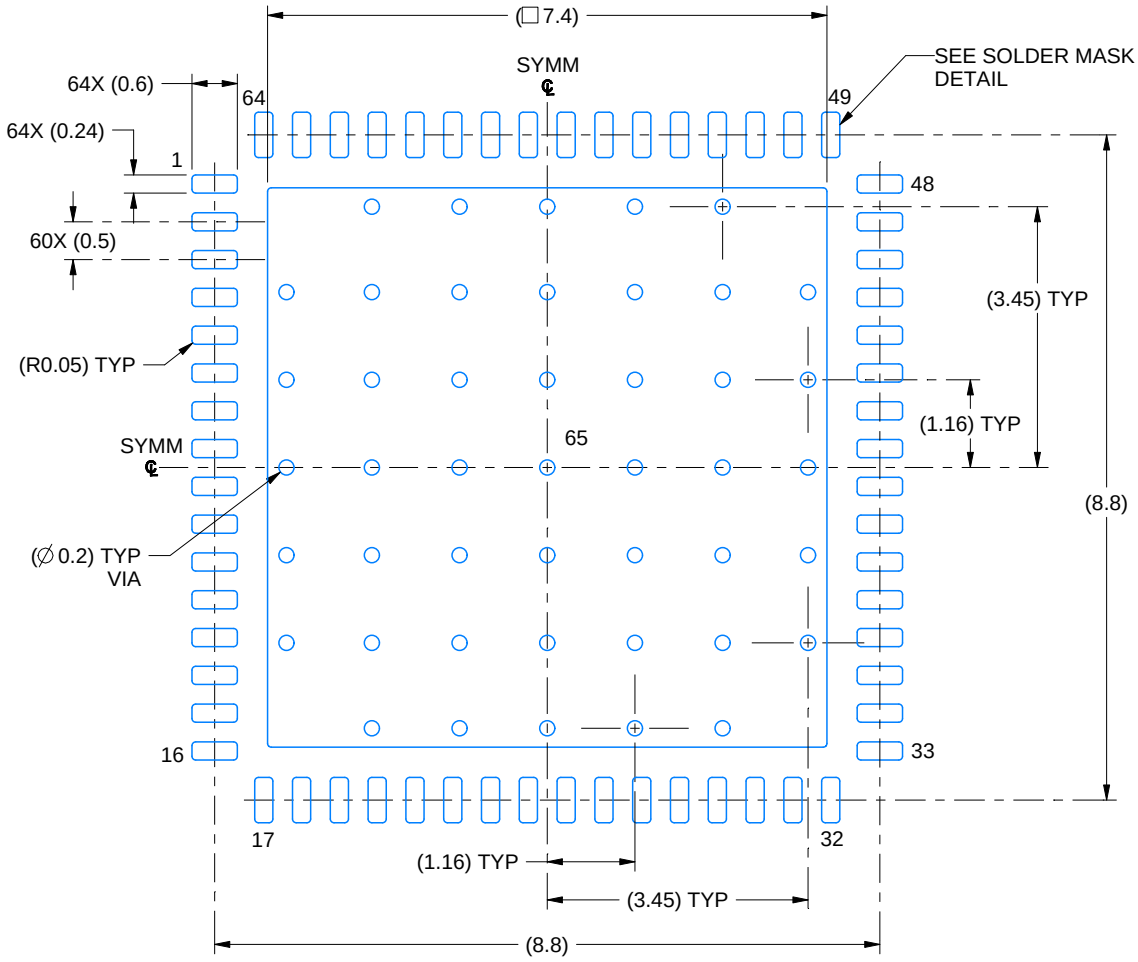
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

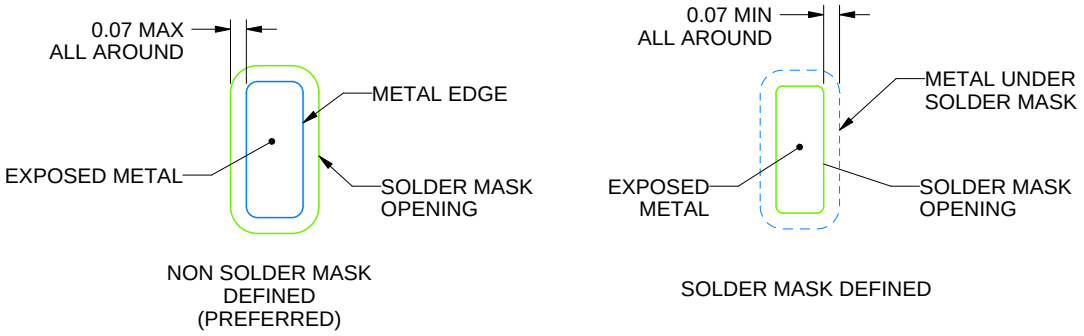



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X




SOLDER MASK DETAILS

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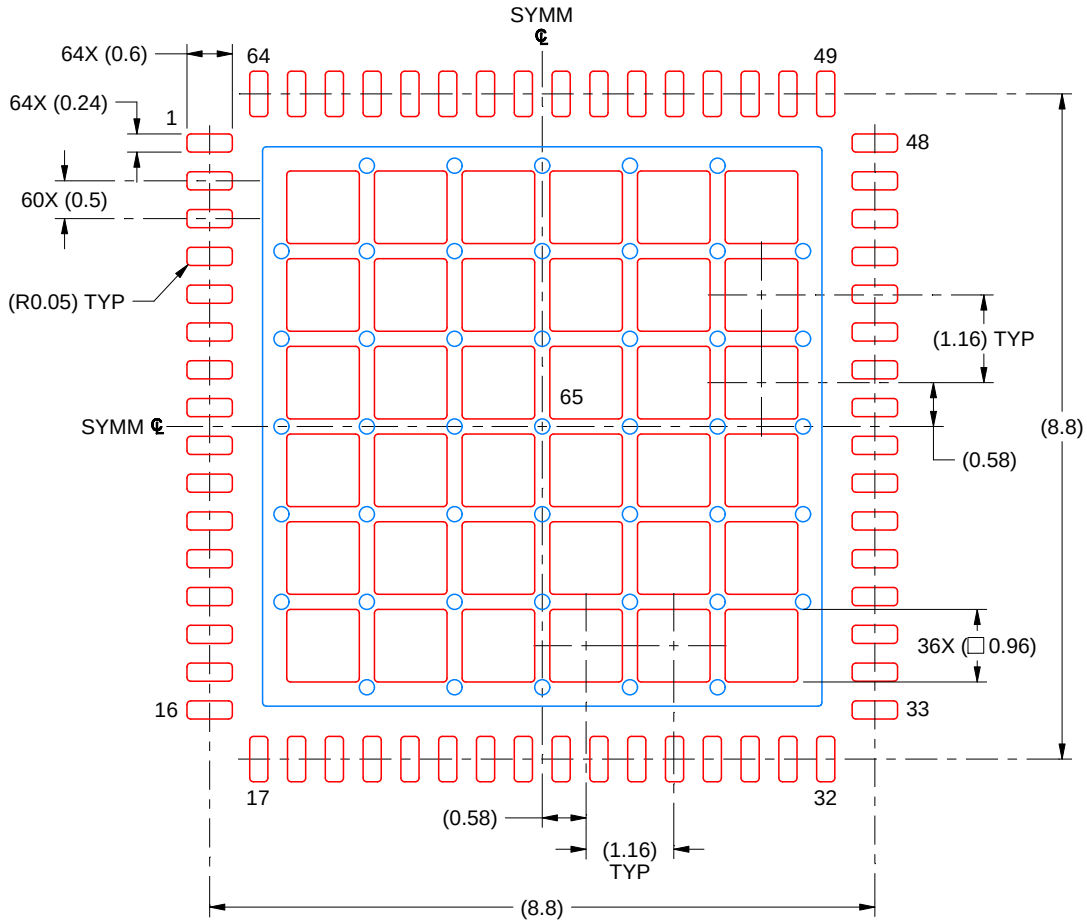
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
61% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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