ADS131E0x 4 通道、6 通道 和 8 通道、24 位同步采样 Δ-Σ ADC

1 特性

- 八路差分模数转换器 (ADC) 输入
- 优异的性能：
  - 动态范围：1kSPS 时为 118dB
  - 串扰：-110dB
  - 总谐波失真 (THD)：50Hz 和 60Hz 时为 -90dB
- 模拟电源范围选项：
  - 3V 至 5V（单极）
  - ±2.5V（双极，允许直流耦合）
- 数字：1.8V 至 3.6V
- 低功耗：每通道 2mW
- 数据速率：1，2，4，8，16，32，和 64kSPS
- 可编程增益：1、2、4、8 和 12
- 故障检测和器件测试功能
- SPI™数据接口和四个通用输入输出接口 (GPIO)
- 封装：薄型四方扁平封装 (TQFQ)-64 (PAG)
- 工作温度范围：
  -40°C 至 +105°C

2 应用

- 电源保护：断路器和继电器保护
- 电能计量：单相、多相和电能质量
- 电池测试系统
- 测试和测量
- 同步采样数据采集系统

3 说明

ADS131E0x 是一系列多通道同步采样、24 位 Δ-Σ 模数转换器 (ADC)，内置可编程增益放大器(PGA)、内部基准和板载振荡器。凭借 ADC 的宽动态范围、可扩展数据传输速率以及内部故障检测监测计，ADS131E0x 受到工业电源监测和保护 以及测试和测量应用的青睐。真正的高阻抗输入支持 ADS131E0x 直接与电阻分压器网络或电压互感器相连以测量线路电压或与电流互感器或罗戈夫斯基线圈相连来测量电流。借助于高集成度和出色的性能，ADS131E0x 系列产品可在大大降低尺寸、功耗和总体成本的前提下创建可升级的工业用电源系统。

ADS131E0x 在每通道上有一个灵活输入多路复用器，此多路复用器被独立连接至内部生成信号以实现测试、温度、和故障检测。故障检测可在器件内部执行，此器件使用集成的带有受数模转换器 (DAC) 控制的触发电平的比较器。ADS131E0x 运行的数据速率可高达 64kSPS。

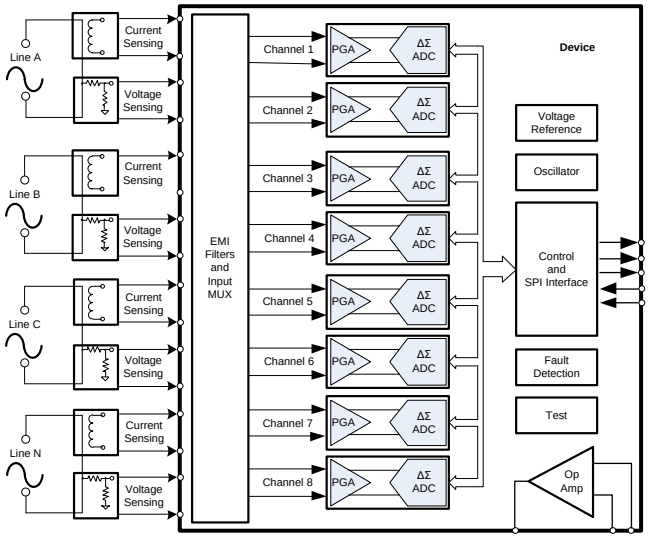
这些完整的模拟前端 (AFE) 解决方案封装在 TQFP-64 封装内并且额定工业用温度范围为 -40°C 至 +105°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ADS131E0x	TQFP (64)	10.00mm x 10.00mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

ADS131E08 简化电路原理图



目录

1 特性 ... 1
2 应用 ... 1
3 说明 ... 1
4 修订历史记录 ... 2
5 **Device Comparison** ... 4
6 **Pin Configuration and Functions** ... 4
7 **Specifications** ... 7
7.1 Absolute Maximum Ratings ... 7
7.2 ESD Ratings ... 7
7.3 Recommended Operating Conditions ... 7
7.4 Thermal Information ... 8
7.5 Electrical Characteristics ... 9
7.6 Timing Requirements ... 12
7.7 Switching Characteristics ... 12
7.8 Typical Characteristics ... 13
8 **Parameter Measurement Information** ... 16
8.1 Noise Measurements ... 16
9 **Detailed Description** ... 17
9.1 Overview ... 17
9.2 Functional Block Diagram ... 18
9.3 Feature Description ... 19
9.4 Device Functional Modes ... 28
9.5 Programming ... 33
9.6 Register Map ... 39
10 **Application and Implementation** ... 49
10.1 Application Information ... 49
10.2 Typical Application ... 58
11 **Power Supply Recommendations** ... 61
11.1 Power-Up Timing ... 61
11.2 Recommended External Capacitor Values ... 62
11.3 Device Connections for Unipolar Power Supplies ... 62
11.4 Device Connections for Bipolar Power Supplies ... 63
12 **Layout** ... 64
12.1 Layout Guidelines ... 64
12.2 Layout Example ... 64
13 器件和文档支持 ... 66
13.1 器件支持 ... 66
13.2 相关链接 ... 66
13.3 接收文档更新通知 ... 66
13.4 社区资源 ... 66
13.5 商标 ... 66
13.6 静电放电警告 ... 66
13.7 Glossary ... 66
14 机械、封装和可订购信息 ... 66

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (December 2013) to Revision C **Page**

- 已添加 *ESD 额定值表*，*特性 描述* 部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1
- Changed formatting of *Thermal Information* table note ... 8

Changes from Revision A (April 2013) to Revision B **Page**

- 已删除 器件图 ... 1
- 已更改 通篇文档中的 ADS131E0x 系列器件 说明 至仅为 24 位 ... 1
- Added *AVSS to DGND* row to Absolute Maximum Ratings table ... 7
- Changed minimum specification to External Reference, *VREFP* parameter in Electrical Characteristics table ... 7
- Changed conditions in Figure 10 ... 13
- Changed conditions in Figure 11 ... 13
- Changed *START Opcode* to *START* in Figure 39 ... 28
- Changed *Reset ($\overline{RESET}$)* section for clarity ... 29
- Changed *Power-Up Sequencing* section ... 61

Changes from Original (June 2012) to Revision A **Page**

- Deleted *AGND to DGND* row from Absolute Maximum Ratings table ... 7
- Changed value of *Digital input to DVDD* row in Absolute Maximum Ratings table ... 7
- Added minimum and maximum specifications to External Reference, *Reference input voltage* parameter in Electrical Characteristics table ... 7

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- Added minimum and maximum specifications to External Reference, *VREFP* parameter in Electrical Characteristics table 7
- Changed Channel Performance (AC Performance), *Accuracy* parameter in Electrical Characteristics table 9
- Changed Internal Reference, V_O parameter in Electrical Characteristics table 9
- Changed Internal Reference, *Temperature drift* parameter in Electrical Characteristics table 9
- Added Figure 15 14

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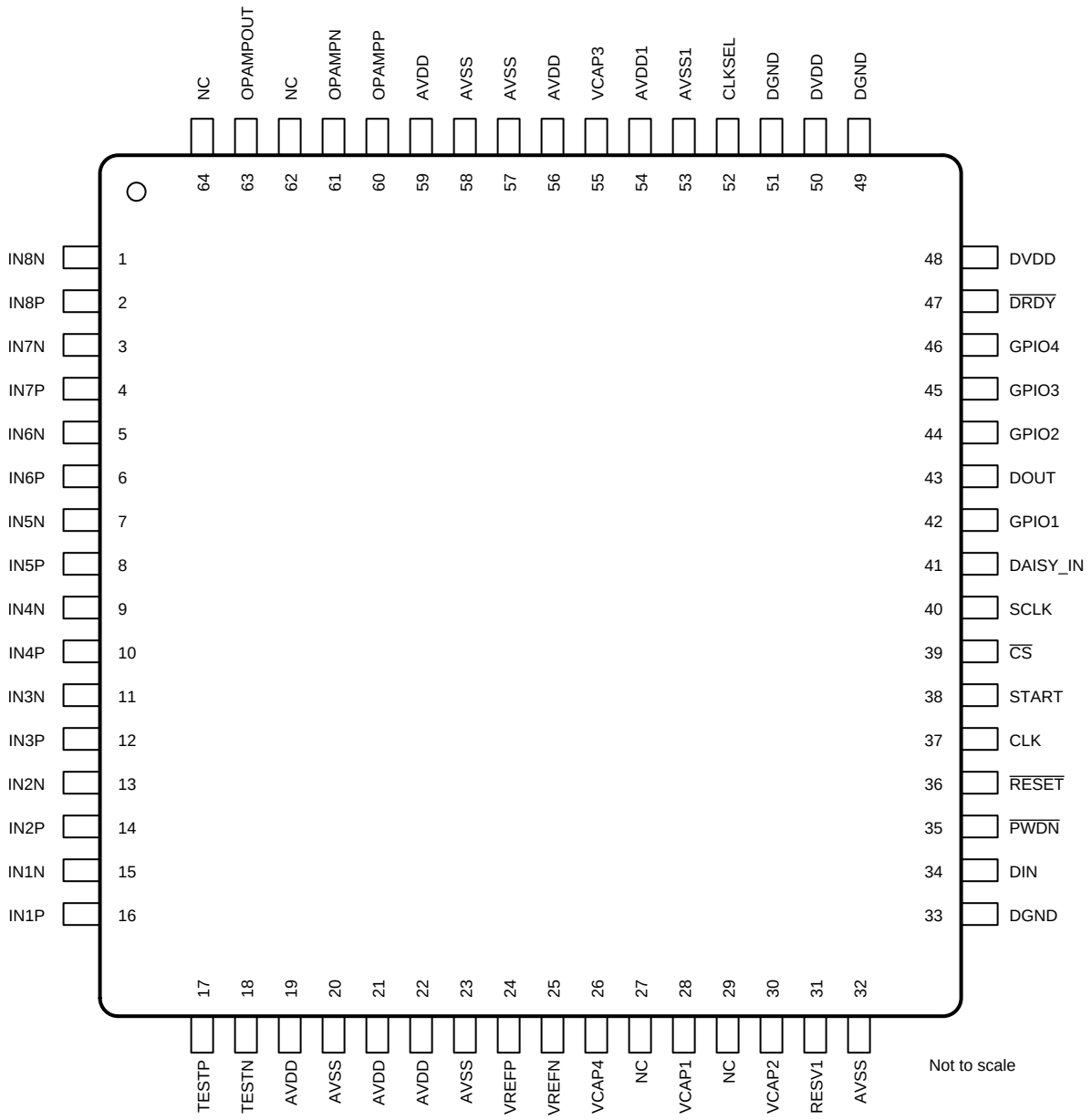
5 Device Comparison

PRODUCT	NO. OF INPUTS	REFERENCE OPTIONS	RESOLUTION (Bits)	POWER-UP TIME (ms)
ADS130E08	8	Internal, external	16	128
ADS131E04	4	Internal, external	24	128
ADS131E06	6	Internal, external	24	128
ADS131E08	8	Internal, external	24	128
ADS131E08S	8	Internal only	24	3

6 Pin Configuration and Functions

PAG Package
64-Pin TQFP
Top View



Not to scale

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Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AVDD	19, 21, 22, 56, 59	Supply	Analog supply. Connect a 1-µF (or larger) capacitor to AVSS for each AVDD pin.
AVDD1	54	Supply	Charge pump analog supply. Connect a 1-µF (or larger) capacitor to AVSS1.
AVSS	20, 23, 32, 57, 58	Supply	Analog ground
AVSS1	53	Supply	Charge pump analog ground
$\overline{CS}$	39	Digital input	Chip select; active low
CLK	37	Digital input	Master clock input. Connect to DGND if unused.
CLKSEL	52	Digital input	Master clock select
DAISY_IN	41	Digital input	Daisy-chain input. Connect to DGND if unused.
DGND	33, 49, 51	Supply	Digital ground
DIN	34	Digital input	Serial data input
DOUT	43	Digital output	Serial data output
$\overline{DRDY}$	47	Digital output	Data ready; active low. Connect to DGND with a 10-kΩ resistor if unused.
DVDD	48, 50	Supply	Digital core power supply. Connect a 1-µF (or larger) capacitor to DGND for each DVDD pin.
GPIO1	42	Digital input/output	General-purpose input/output pin 1. Connect to DGND with a 10-kΩ resistor if unused.
GPIO2	44	Digital input/output	General-purpose input/output pin 2. Connect to DGND with a 10-kΩ resistor if unused.
GPIO3	45	Digital input/output	General-purpose input/output pin 3. Connect to DGND with a 10-kΩ resistor if unused.
GPIO4	46	Digital input/output	General-purpose input/output pin 4. Connect to DGND with a 10-kΩ resistor if unused.
IN1N(1)	15	Analog input	Negative analog input 1
IN1P(1)	16	Analog input	Positive analog input 1
IN2N(1)	13	Analog input	Negative analog input 2
IN2P(1)	14	Analog input	Positive analog input 2
IN3N(1)	11	Analog input	Negative analog input 3
IN3P(1)	12	Analog input	Positive analog input 3
IN4N(1)	9	Analog input	Negative analog input 4
IN4P(1)	10	Analog input	Positive analog input 4
IN5N(1)	7	Analog input	Negative analog input 5 (ADS131E06 and ADS131E08 only)
IN5P(1)	8	Analog input	Positive analog input 5 (ADS131E06 and ADS131E08 only)
IN6N(1)	5	Analog input	Negative analog input 6 (ADS131E06 and ADS131E08 only)
IN6P(1)	6	Analog input	Positive analog input 6 (ADS131E06 and ADS131E08 only)
IN7N(1)	3	Analog input	Negative analog input 7 (ADS131E08 only)
IN7P(1)	4	Analog input	Positive analog input 7 (ADS131E08 only)
IN8N(1)	1	Analog input	Negative analog input 8 (ADS131E08 only)
IN8P(1)	2	Analog input	Positive analog input 8 (ADS131E08 only)
NC	27, 29, 62, 64	—	No connection, leave floating. Can be connected to AVDD or AVSS with a 10-kΩ or higher resistor.
OPAMPN	61	Analog input	Op amp inverting input; leave floating if unused and power-down the op amp.
OPAMPP	60	Analog input	Op amp noninverting input; leave floating if unused and power-down the op amp.
OPAMPOUT	63	Analog output	Op amp output; leave floating if unused and power-down the op amp.
$\overline{PWDN}$	35	Digital input	Power-down; active low

(1) Connect any unused or powered-down analog input pins to AVDD.

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{RESET}}$	36	Digital input	System reset; active low
RESV1	31	Digital input	Reserved for future use. Connect directly to DGND.
SCLK	40	Digital input	Serial clock input
START	38	Digital input	Start conversion
TESTN	18	Analog input/output	Test signal, negative pin. See the *Unused Inputs and Outputs* section for unused pins.
TESTP	17	Analog input/output	Test signal, positive pin. See the *Unused Inputs and Outputs* section for unused pins.
VCAP1	28	Analog output	Analog bypass capacitor. Connect a 22-µF capacitor to AVSS.
VCAP2	30	Analog output	Analog bypass capacitor. Connect a 1-µF capacitor to AVSS.
VCAP3	55	Analog output	Analog bypass capacitor. Connect a parallel combination of 1-µF and 0.1-µF capacitors to AVSS.
VCAP4	26	Analog output	Analog bypass capacitor. Connect a 1-µF capacitor to AVSS.
VREFN	25	Analog input	Negative reference voltage. Connect to AVSS
VREFP	24	Analog input/output	Positive reference voltage. Connect a minimum 10-µF capacitor to VREFN.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power-supply voltage	AVDD to AVSS	–0.3	5.5	V
	AVSS to DGND	–3	0.2	
	DVDD to DGND	–0.3	3.9	
Analog input voltage	Analog input to AVSS	AVSS – 0.3	AVDD + 0.3	V
Digital input voltage	Digital input to DVDD	DGND – 0.3	DVDD + 0.3	V
Input current	Momentary	–100	100	mA
	Continuous, all other pins except power-supply pins	–10	10	
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–60	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
AVDD	Analog power supply	AVDD to AVSS	2.7	5.0	5.25	V
DVDD	Digital power supply	DVDD to DGND	1.7	1.8	3.6	V
	Analog to digital supply	AVDD to DVDD	–2.1		3.6	V
ANALOG INPUTS						
V_{IN}	Differential input voltage	$V_{IN} = V_{(INxP)} – V_{(INxN)}$	$–V_{REF}$ / Gain		V_{REF} / Gain	V
V_{CM}	Common-mode input voltage	$V_{CM} = (V_{(INxP)} – V_{(INxN)}) / 2$	See the *Input Common-Mode Range* section			V
VOLTAGE REFERENCE INPUTS						
V_{REF}	Reference input voltage	AVDD = 3 V, $V_{REF} = (V_{VREFP} – V_{VREFN})$	2	2.5	AVDD	V
		AVDD = 5 V, $V_{REF} = (V_{VREFP} – V_{VREFN})$	2	4	AVDD	V
VREFN	Negative reference input			AVSS		V
VREFP	Positive input		AVDD – 3	AVSS + 2.5	AVDD	V
EXTERNAL CLOCK SOURCE						
f_{CLK}	Master clock rate	CLKSEL pin = 0, (AVDD – AVSS) = 3 V	1.7	2.048	2.25	MHz
		CLKSEL pin = 0, (AVDD – AVSS) = 5 V	1.0	2.048	2.25	
DIGITAL INPUTS						
	Input voltage		DGND – 0.1		DVDD + 0.1	V
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–40		105	°C

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7.4 Thermal Information

THERMAL METRIC(1)		ADS131E0x PAG (TQFP) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	NA	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

Minimum and maximum specifications apply from –40°C to +105°C. Typical specifications are at 25°C. All specifications are at DVDD = 1.8 V, AVDD = 3 V, AVSS = 0 V, V_{REF} = 2.4 V, external f_{CLK} = 2.048 MHz, data rate = 8 kSPS, and gain = 1, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG INPUTS							
C_i	Input capacitance				20		pF
I_{IB}	Input bias current	PGA output in normal range			5		nA
	DC input impedance				200		MΩ
PGA PERFORMANCE							
	Gain settings				1, 2, 4, 8, 12		
BW	Bandwidth				See Table 3		
ADC PERFORMANCE							
DR	Data rate	f_{CLK} = 2.048 MHz		1		64	kSPS
	Resolution	DR = 1 kSPS, 2 kSPS, 4 kSPS, 8 kSPS, and 16 kSPS		24			Bits
		DR = 32 kSPS and 64 kSPS		16			Bits
CHANNEL PERFORMANCE (DC PERFORMANCE)							
INL	Integral nonlinearity	Full-scale, best fit			10		ppm
	Dynamic range	G = 1		105			dB
		Gain settings other than 1		See the *Noise Measurements* section			
E_O	Offset error				350		µV
	Offset error drift				0.65		µV/°C
E_G	Gain error	Excluding voltage reference error			0.1%		
	Gain drift	Excluding voltage reference drift			3		ppm/°C
	Gain match between channels				0.2		% of FS
CHANNEL PERFORMANCE (AC PERFORMANCE)							
CMRR	Common-mode rejection ratio	f_{CM} = 50 Hz and 60 Hz(1)			–110		dB
PSRR	Power-supply rejection ratio	f_{PS} = 50 Hz and 60 Hz			–80		dB
	Crosstalk	f_{IN} = 50 Hz and 60 Hz			–110		dB
	Accuracy	3000:1 dynamic range with a 1-second measurement (V_{RMS} / I_{RMS})	AVDD = 3 V, V_{REF} = 2.4 V		0.04%		
			AVDD = 5 V, V_{REF} = 4 V		0.025%		
SNR	Signal-to-noise ratio	f_{IN} = 50 Hz and 60 Hz, gain = 1			107		dB
THD	Total harmonic distortion	10 Hz, –0.5 dBFs			–93		dB
INTERNAL REFERENCE							
V_{REF}	Output voltage	T_A = 25°C, V_{REF} = 2.4 V		2.394	2.4	2.406	V
		T_A = 25°C, V_{REF} = 4 V			4		V
	V_{REF} accuracy				±0.2%		
	Temperature drift	T_A = –40°C to +105°C			20		ppm/°C
	Start-up time	Settled to 0.2%			150		ms
EXTERNAL REFERENCE							
	Input impedance				6		kΩ
INTERNAL OSCILLATOR							
	Accuracy				±2%		
		T_A = 25°C				±0.5%	
		T_A = –40°C to 105°C				2.5%	
	Internal oscillator clock frequency	Nominal frequency			2.048		MHz
	Internal oscillator start-up time				20		µs
	Internal oscillator power consumption				120		µW
FAULT DETECT AND ALARM							
	Comparator threshold accuracy				±30		mV

(1) CMRR is measured with a common-mode signal of (AVSS + 0.3 V) to (AVDD – 0.3 V). The values indicated are the minimum of the eight channels.

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Electrical Characteristics (continued)

Minimum and maximum specifications apply from –40°C to +105°C. Typical specifications are at 25°C. All specifications are at DVDD = 1.8 V, AVDD = 3 V, AVSS = 0 V, V_{REF} = 2.4 V, external f_{CLK} = 2.048 MHz, data rate = 8 kSPS, and gain = 1, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATIONAL AMPLIFIER							
	Integrated noise		0.1 Hz to 250 Hz		9		μV_{RMS}
	Noise density		2 kHz		120		nV/√Hz
GBP	Gain bandwidth product		50 kΩ || 10-pF load		100		kHz
SR	Slew rate		50 kΩ || 10-pF load		0.25		V/µs
	Load current				50		µA
THD	Total harmonic distortion		f_{IN} = 100 Hz		70		dB
	Common-mode input range			AVSS + 0.7		AVDD – 0.3	V
	Quiescent power consumption				20		µA
SYSTEM MONITORS							
	Supply reading error	Analog			2%		
		Digital			2%		
	Device wake up		From power-up to $\overline{DRDY}$ low		150		ms
			STANDBY mode		31.25		µs
	Temperature sensor reading	Voltage	T_A = 25°C		145		mV
		Coefficient			490		µV/°C
SELF-TEST SIGNAL							
	Signal frequency		See the *Register Map* section for settings		$f_{CLK} / 2^{21}$		Hz
					$f_{CLK} / 2^{20}$		
	Signal voltage		See the *Register Map* section for settings		±1		mV
					±2		
DIGITAL INPUT AND OUTPUT (DVDD = 1.8 V to 3.6 V)							
V_{IH}	Logic level, input voltage	High		0.8 DVDD		DVDD+0.1	V
V_{IL}		Low		–0.1		0.2 DVDD	V
V_{OH}	Logic level, output voltage	High	I_{OH} = –500 µA	0.9 DVDD			V
V_{OL}		Low	I_{OL} = +500 µA			0.1 DVDD	V
I_{IN}	Input current		0 V < $V_{DigitalInput}$ < DVDD	–10		10	µA

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Electrical Characteristics (continued)

Minimum and maximum specifications apply from –40°C to +105°C. Typical specifications are at 25°C. All specifications are at DVDD = 1.8 V, AVDD = 3 V, AVSS = 0 V, V_{REF} = 2.4 V, external f_{CLK} = 2.048 MHz, data rate = 8 kSPS, and gain = 1, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT (OPERATIONAL AMPLIFIER TURNED OFF)							
I_{AVDD}	Normal mode		AVDD – AVSS = 3 V		5.1		mA
			AVDD – AVSS = 5 V		5.8		mA
I_{DVDD}			DVDD = 3.3 V		1		mA
			DVDD = 1.8 V		0.4		mA
POWER DISSIPATION (ANALOG SUPPLY = 3 V)							
Quiescent power dissipation		ADS131E04	Normal mode		9.3	10.2	mW
			Power-down mode		10		µW
			Standby mode		2		mW
		ADS131E06	Normal mode		12.7	13.5	mW
			Power-down mode		10		µW
			Standby mode		2		mW
		ADS131E08	Normal mode		16	17.6	mW
			Power-down mode		10		µW
			Standby mode		2		mW
POWER DISSIPATION (ANALOG SUPPLY = 5 V)							
Quiescent power dissipation		ADS131E04	Normal mode		18		mW
			Power-down mode		20		µW
			Standby mode		4.2		mW
		ADS131E06	Normal mode		24.3		mW
			Power-down mode		20		µW
			Standby mode		4.2		mW
		ADS131E08	Normal mode		29.7		mW
			Power-down mode		20		µW
			Standby mode		4.2		mW

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7.6 Timing Requirements

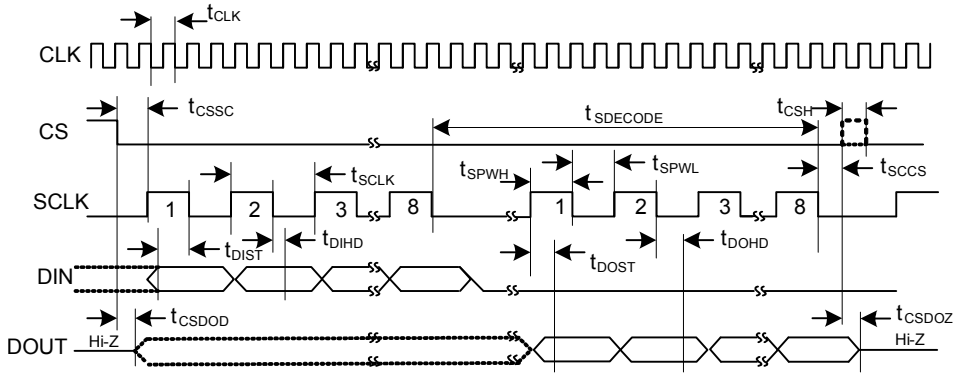
over operating ambient temperature range and DVDD = 1.7 V to 3.6 V (unless otherwise noted)

		2.7 V ≤ DVDD ≤ 3.6 V		1.7 V ≤ DVDD ≤ 2.0 V		UNIT
		MIN	MAX	MIN	MAX	
t_{CLK}	Master clock period	444	588	444	588	ns
t_{CSSC}	Delay time, first SCLK rising edge after $\overline{CS}$ falling edge	6		17		ns
t_{SCLK}	SCLK period	50		66.6		ns
$t_{SPWH, L}$	Pulse duration, SCLK high or low	15		25		ns
t_{DIST}	Setup time, DIN valid before SCLK falling edge	10		10		ns
t_{DIHD}	Hold time, DIN valid after SCLK falling edge	10		11		ns
t_{CSH}	Pulse duration, $\overline{CS}$ high	2		2		t_{CLK}
t_{SCCS}	Delay time, $\overline{CS}$ rising edge after final SCLK falling edge	4		4		t_{CLK}
$t_{SDECODE}$	Command decode time	4		4		t_{CLK}
$t_{DISCK2ST}$	Setup time, DAISY_IN valid before SCLK falling edge	10		10		ns
$t_{DISCK2HT}$	Hold time, DAISY_IN valid after SCLK falling edge	10		10		ns

7.7 Switching Characteristics

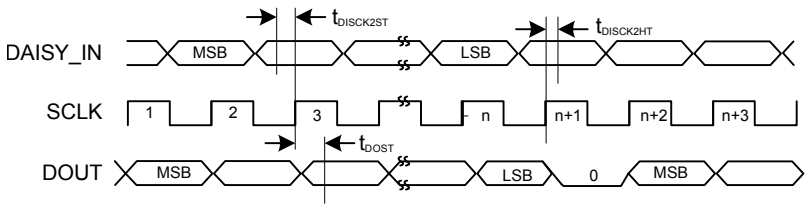
over operating ambient temperature range, DVDD = 1.7 V to 3.6 V, and load on DOUT = 20 pF || 100 kΩ (unless otherwise noted)

PARAMETER		2.7 V ≤ DVDD ≤ 3.6 V		1.7 V ≤ DVDD ≤ 2.0 V		UNIT
		MIN	MAX	MIN	MAX	
t_{CSDOD}	Propagation delay time, $\overline{CS}$ falling edge to DOUT driven	10		20		ns
t_{DOST}	Propagation delay time, SCLK rising edge to valid new DOUT		17		32	ns
t_{DOHD}	Hold time, SCLK falling edge to invalid DOUT	10		10		ns
t_{CSDOZ}	Propagation delay time, $\overline{CS}$ rising edge to DOUT high impedance		10		20	ns



NOTE: SPI settings are CPOL = 0 and CPHA = 1.

Figure 1. Serial Interface Timing



(1) n = Number of channels × resolution + 24 bits. Number of channels is 8; resolution is 24-bit.

Figure 2. Daisy-Chain Interface Timing

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7.8 Typical Characteristics

all plots are at T_A = 25°C, AVDD = 3 V, AVSS = 0 V, DVDD = 1.8 V, internal VREFP = 2.4 V, VREFN = AVSS, external clock = 2.048 MHz, data rate = 8 kSPS, and gain = 1, unless otherwise noted.

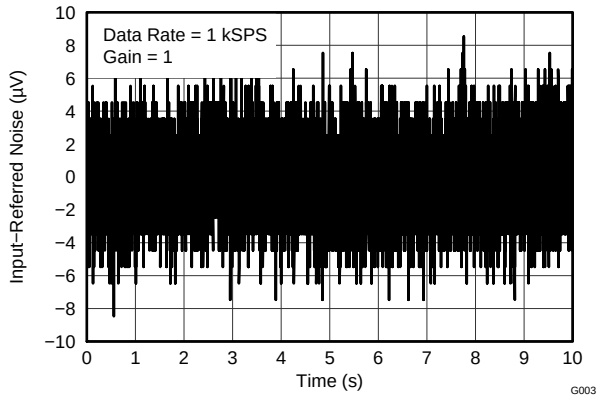

Figure 3. Input-Referred Noise

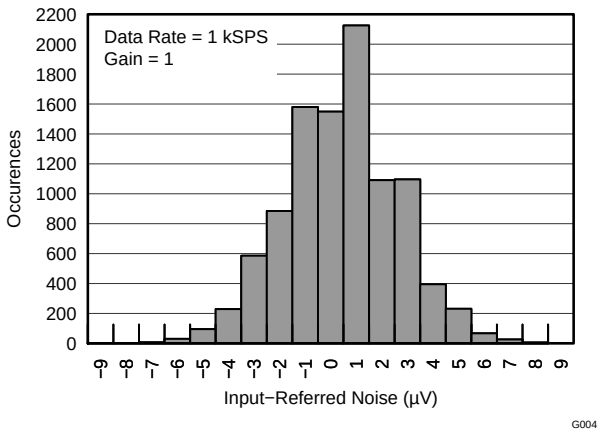

Figure 4. Noise Histogram

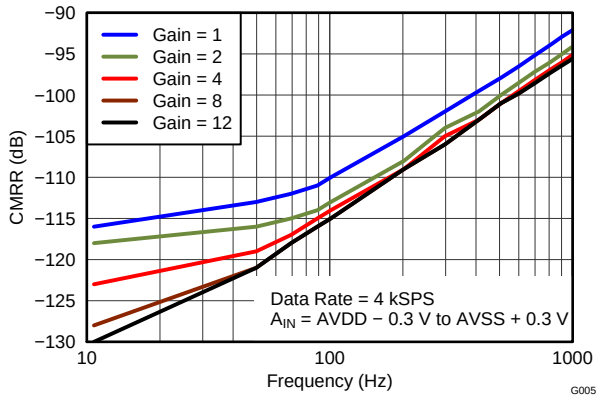

Figure 5. CMRR vs Frequency

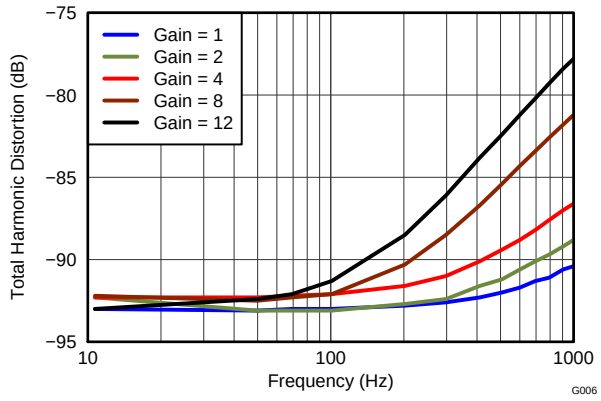

Figure 6. THD vs Frequency

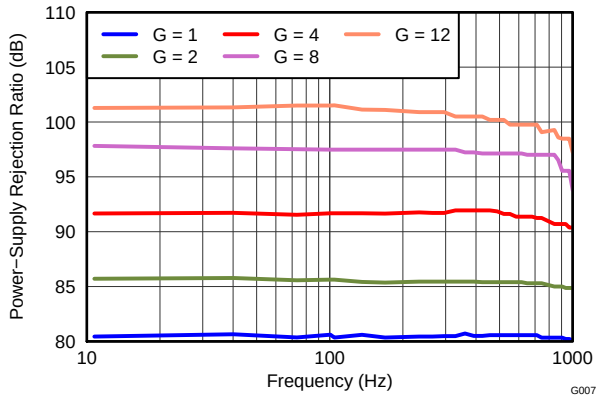

Figure 7. PSRR vs Frequency

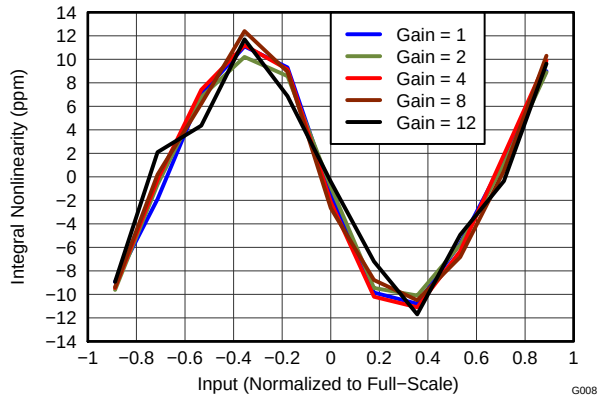

Figure 8. INL vs PGA Gain

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Typical Characteristics (continued)

all plots are at T_A = 25°C, AVDD = 3 V, AVSS = 0 V, DVDD = 1.8 V, internal VREFP = 2.4 V, VREFN = AVSS, external clock = 2.048 MHz, data rate = 8 kSPS, and gain = 1, unless otherwise noted.

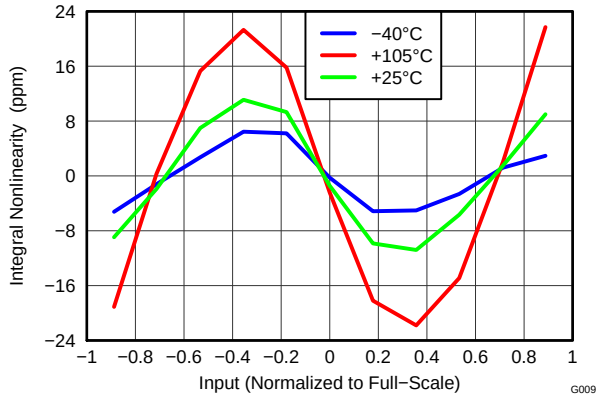

Figure 9. INL vs Temperature

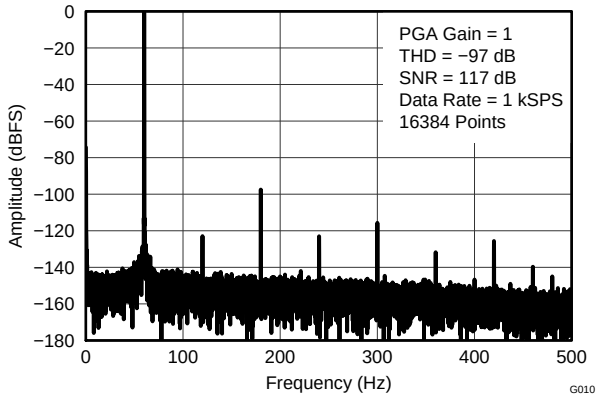

Figure 10. THD FFT Plot

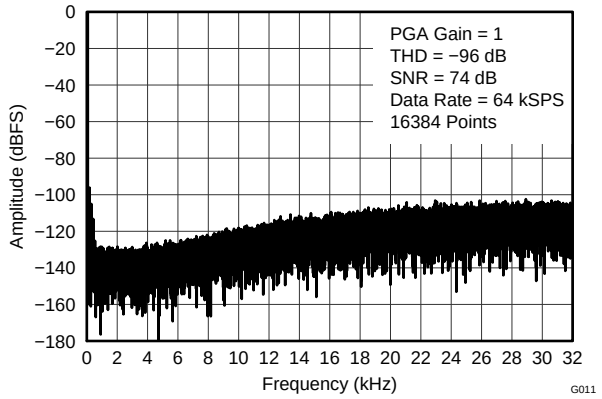

Figure 11. FFT Plot

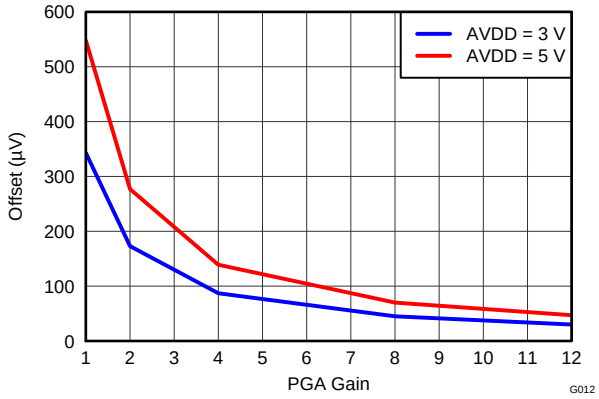

Figure 12. Offset vs PGA Gain (Absolute Value)

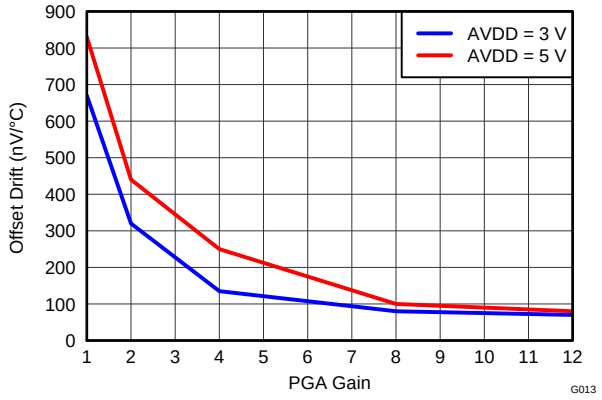

Figure 13. Offset Drift vs PGA Gain

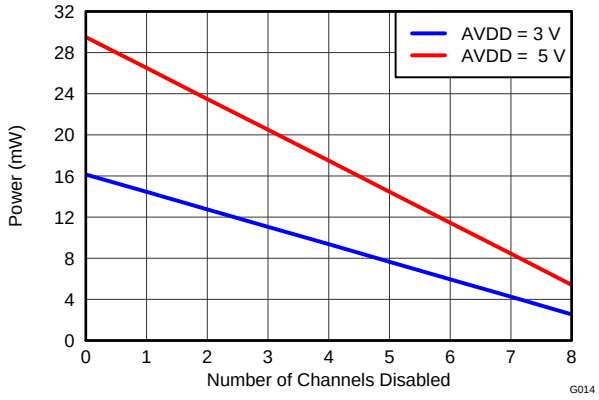

Figure 14. ADS131E08 Channel Power

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Typical Characteristics (continued)

all plots are at T_A = 25°C, AVDD = 3 V, AVSS = 0 V, DVDD = 1.8 V, internal VREFP = 2.4 V, VREFN = AVSS, external clock = 2.048 MHz, data rate = 8 kSPS, and gain = 1, unless otherwise noted.

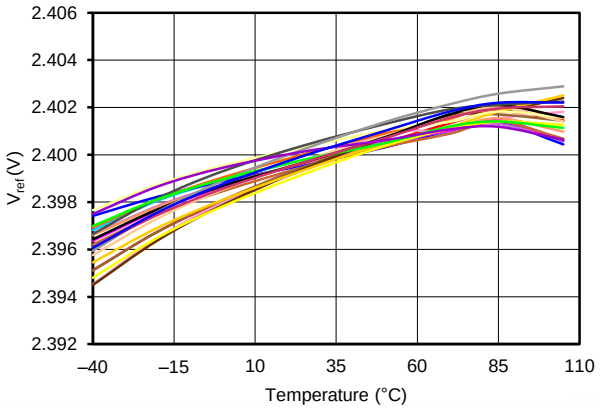

Figure 15. Internal V_{REF} vs Temperature

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8 Parameter Measurement Information

8.1 Noise Measurements

Adjust the data rate and PGA gain to optimize the ADS131E0x noise performance. When averaging is increased by reducing the data rate, noise drops correspondingly. Increasing the PGA gain reduces the input-referred noise, which is particularly useful when measuring low-level signals. Table 1 summarizes the ADS131E0x noise performance with a 3-V analog power supply. Table 2 summarizes the ADS131E0x noise performance with a 5-V analog power supply. Data are representative of typical noise performance at T_A = 25°C. Data shown are the result of averaging the readings from multiple devices and are measured with the inputs shorted together. A minimum of 1000 consecutive readings are used to calculate the RMS noise for each reading. For the two highest data rates, noise is limited by the ADC quantization noise and does not have a Gaussian distribution. Table 1 and Table 2 show measurements taken with an internal reference. Data are representative of the ADS131E0x noise performance shown in both effective number of bits (ENOB) and dynamic range when using a low-noise external reference (such as the REF5025). ENOB data in Table 1 and Table 2 are calculated using Equation 1 and dynamic range data in Table 1 and Table 2 are calculated using Equation 2.

$$\text{ENOB} = \log_2 \left| \frac{\text{VREF}}{\sqrt{2} \times V_{\text{RMS_Noise}} \times \text{Gain}} \right| \quad (1)$$

$$\text{Dynamic Range} = 20 \times \log_{10} \left| \frac{\text{VREF}}{\sqrt{2} \times V_{\text{RMS_Noise}} \times \text{Gain}} \right| \quad (2)$$

Table 1. Input-Referred Noise, 3-V Analog Supply, and 2.4-V Reference

DR BITS (CONFIG1 Register)	OUTPUT DATA RATE (kSPS)	–3-dB BANDWIDTH (Hz)	PGA GAIN									
			x1		x2		x4		x8		x12	
			DYNAMIC RANGE (dB)	ENOB	DYNAMIC RANGE (dB)	ENOB	DYNAMIC RANGE (dB)	ENOB	DYNAMIC RANGE (dB)	ENOB	DYNAMIC RANGE (dB)	ENOB
000	64	16768	74.1	12.31	74.1	12.30	74.0	12.29	74.0	12.29	73.9	12.27
001	32	8384	89.6	14.89	89.6	14.88	89.4	14.85	88.6	14.71	87.6	14.55
010	16	4192	102.8	17.07	102.3	16.99	100.6	16.72	97.1	16.12	94.2	15.65
011	8	2096	108.2	18.0	107.4	17.9	105.2	17.5	101.6	16.9	98.9	16.5
100	4	1048	111.4	18.6	109.4	18.4	107.4	18.1	103.5	17.4	100.5	17.0
101	2	524	114.6	19.1	113.7	19.0	111.4	18.6	107.7	18.0	104.9	17.5
110	1	262	117.7	19.6	116.8	19.5	114.5	19.1	110.7	18.5	108.0	18.0

Table 2. Input-Referred Noise, 5-V Analog Supply, And 4-V Reference

DR BITS (CONFIG1 Register)	OUTPUT DATA RATE (kSPS)	–3-dB BANDWIDTH (Hz)	PGA GAIN									
			x1		x2		x4		x8		x12	
			DYNAMIC RANGE (dB)	ENOB	DYNAMIC RANGE (dB)	ENOB	DYNAMIC RANGE (dB)	ENOB	DYNAMIC RANGE (dB)	ENOB	DYNAMIC RANGE (dB)	ENOB
000	64	16768	74.7	12.41	74.7	12.41	74.7	12.41	74.7	12.41	74.6	12.39
001	32	8384	90.3	15.01	90.3	15.00	90.2	14.99	89.9	14.93	89.4	14.85
010	16	4192	104.3	17.33	104	17.28	103.1	17.12	100.5	16.70	98.1	16.3
011	8	2096	112.3	18.7	111.6	18.6	109.7	18.3	106.3	17.7	103.8	17.3
100	4	1048	116	19.3	115.2	19.2	113.1	18.8	109.5	18.3	106.9	17.8
101	2	524	119.1	19.8	118.2	19.7	116.2	19.4	112.6	18.8	109.9	18.3
110	1	262	122.1	20.4	121.3	20.2	119.1	19.9	115.6	19.3	112.9	18.8

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9 Detailed Description

9.1 Overview

The ADS131E0x series are low-power, multichannel, simultaneously-sampling, 24-bit, delta-sigma (ΔΣ), analog-to-digital converter (ADC) with an integrated programmable gain amplifier (PGA). The analog device performance across a scalable data rate makes the device well-suited for smart-grid and other industrial power monitor, control, and protection applications.

The ADS131E0x devices have a programmable multiplexer that allows for various internal monitoring signal measurements including temperature, supply, and input-short for device noise testing. The PGA gain can be chosen from one of five settings: 1, 2, 4, 8, or 12. The ADCs in the device offer data rates of 1 kSPS, 2 kSPS, 4 kSPS, 8 kSPS, 16 kSPS, 32 kSPS, and 64 kSPS. The devices communicate using a serial peripheral interface (SPI)-compatible interface. The devices provide four general-purpose I/O (GPIO) pins for general use. Use multiple devices to easily add channels to the system and synchronize them with the START pins.

Program the internal reference to either 2.4 V or 4 V. The internal oscillator generates a 2.048-MHz clock. Use the integrated comparators, with programmable trigger-points, for input overrange or underrange detection. A detailed diagram of the ADS131E0x is provided in .

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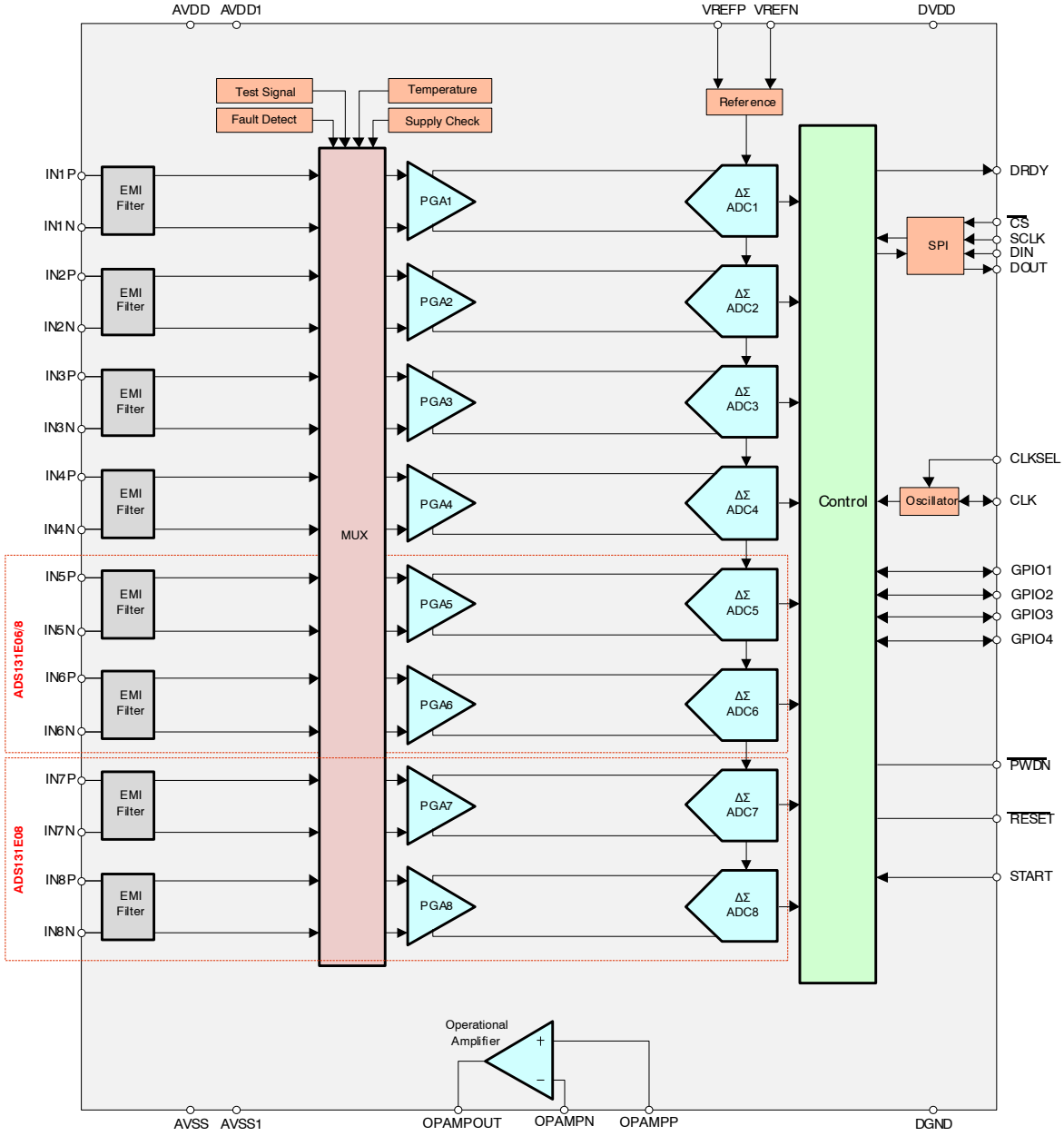
9.2 Functional Block Diagram



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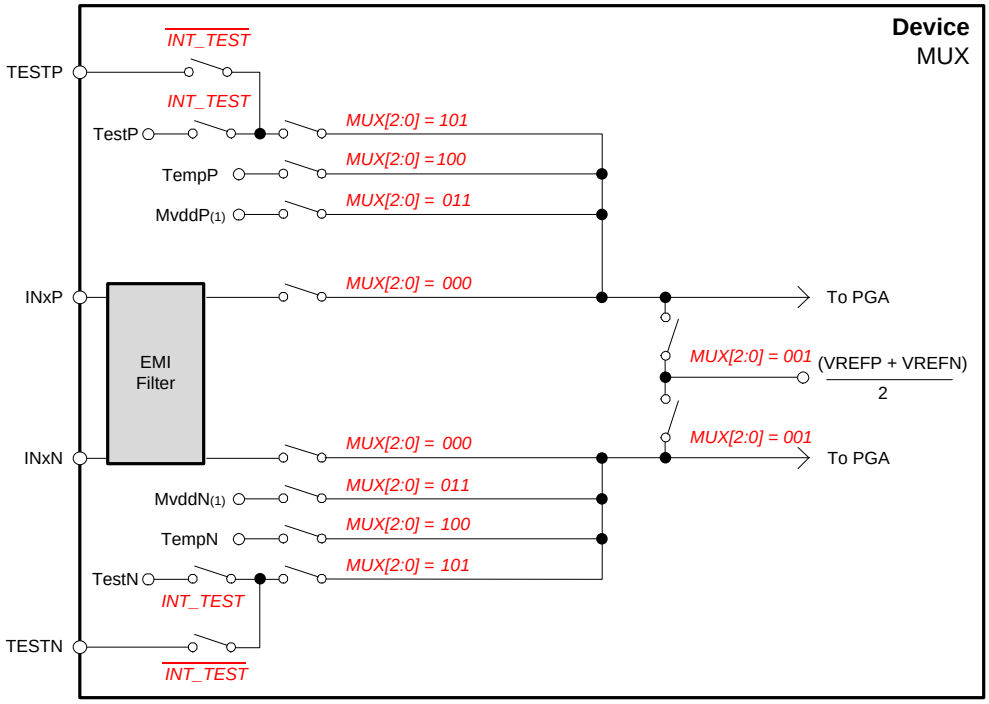
9.3 Feature Description

9.3.1 Electromagnetic Interference (EMI) Filter

An RC filter at the input functions as an EMI filter on all channels. The –3-dB filter bandwidth is approximately 3 MHz.

9.3.2 Input Multiplexer

The ADS131E0x input multiplexers are very flexible and provide many configurable signal-switching options. Figure 16 shows a diagram of the multiplexer on a single channel of the device. INxP and INxN are separate for each of the four, six or eight blocks (depending on device). This flexibility allows for significant device and sub-system diagnostics, calibration, and configuration. Switch settings for each channel are selected by writing the appropriate values to the CHnSET registers (see the *CHnSET* registers in the *Register Map* section for details). The output of each multiplexer is connected to the individual channel PGA.



(1) MVDD monitor voltage supply depends on channel number; see the *Power-Supply Measurements (MVDDP, MVDDN)* section.

Figure 16. Input Multiplexer Block for One Channel

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Feature Description (continued)

9.3.2.1 Device Noise Measurements

Setting CHnSET[2:0] = 001 sets the common-mode voltage of [(V_{VREFP} + V_{VREFN}) / 2] to both channel inputs. Use this setting to test inherent device noise in the user system.

9.3.2.2 Test Signals (TestP and TestN)

Setting CHnSET[2:0] = 101 provides internally-generated test signals for use in sub-system verification at power-up. The test signals are controlled through register settings (see the *CONFIG2: Configuration Register 2* section for details). TEST_AMP controls the signal amplitude and TEST_FREQ controls the switching frequency of the test signal. The test signals are multiplexed and transmitted out of the device at the TESTP and TESTN pins. The INT_TEST register bit (in the *CONFIG2: Configuration Register 2* section) deactivates the internal test signals so that the test signal can be driven externally. This feature allows the test or calibration of multiple devices with the same signal.

9.3.2.3 Temperature Sensor (TempP, TempN)

Setting CHnSET[2:0] = 100 sets the channel input to the temperature sensor. This sensor uses two internal diodes with one diode having a current density 16 times that of the other, as shown in Figure 17. The difference in diode current densities yields a difference in voltage that is proportional to absolute temperature.

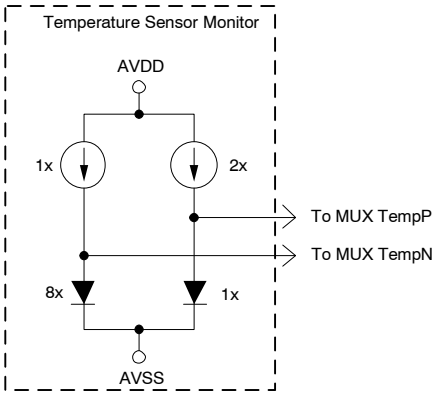

Figure 17. Temperature Sensor Implementation

The internal device temperature tracks the PCB temperature closely because of the low thermal resistance of the package to the PCB. Self-heating of the ADS131E0x causes a higher reading than the temperature of the surrounding PCB. Setting the channel gain to 1 is recommended when the temperature measurement is taken.

The scale factor of Equation 3 converts the temperature reading to °C. Before using this equation, the temperature reading code must first be scaled to μV.

$$\text{Temperature (°C)} = \left(\frac{\text{Temperature Reading (μV)} - 145{,}300\ \mu\text{V}}{490\ \mu\text{V/°C}} \right) + 25°\text{C} \quad (3)$$

9.3.2.4 Power-Supply Measurements (MVDDP, MVDDN)

Setting CHnSET[2:0] = 011 sets the channel inputs to different device supply voltages. For channels 1, 2, 5, 6, 7, and 8 (MVDDP – MVDDN) is [0.5 × (AVDD – AVSS)]; for channels 3 and 4 (MVDDP – MVDDN) is DVDD / 4. Set the gain to 1 to avoid saturating the PGA when measuring power supplies.

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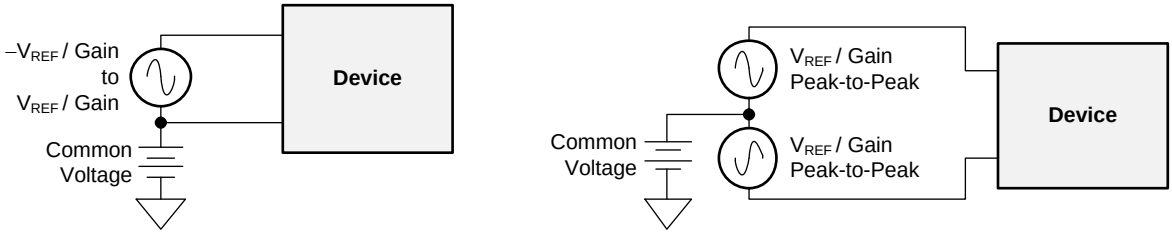
Feature Description (continued)

9.3.3 Analog Input

The analog inputs to the device connect directly to an integrated low-noise, low-drift, high input impedance, programmable gain amplifier. The amplifier is located following the individual channel multiplexer.

The ADS131E0x analog inputs are fully differential. The differential input voltage ($V_{INxP} – V_{INxN}$) can span from $–V_{REF}$ / gain to V_{REF} / gain. See the *Data Format* section for an explanation of the correlation between the analog input and digital codes. There are two general methods of driving the ADS131E0x analog inputs: pseudo-differential or fully-differential, as shown in Figure 18, Figure 19, and Figure 20.



a) Psuedo-Differential Input

b) Differential Input

Figure 18. Methods of Driving the ADS131E0x: Pseudo-Differential or Fully Differential

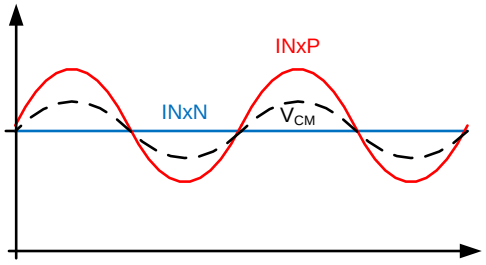


Figure 19. Pseudo-Differential Input Mode

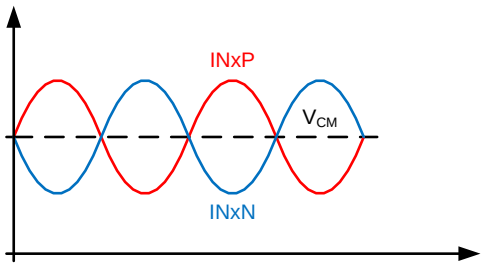


Figure 20. Fully-Differential Input Mode

Hold the INxN pin at a common voltage, preferably at mid supply, to configure the fully differential input for a pseudo-differential signal. Swing the INxP pin around the common voltage $–V_{REF}$ / gain to V_{REF} / gain and remain within the absolute maximum specifications. Verify that the differential signal at the minimum and maximum points meets the common-mode input specification discussed in the *Input Common-Mode Range* section.

Configure the signals at INxP and INxN to be 180° out-of-phase centered around a common-mode voltage, V_{CM}, to use a fully-differential input method. Both the INxP and INxN inputs swing from the V_{CM} + ½ V_{REF} / gain to the V_{CM} – ½ V_{REF} / gain. The differential voltage at the maximum and minimum points is equal to $–V_{REF}$ / gain to V_{REF} / gain. Use the ADS131E0x in a differential configuration to maximize the dynamic range of the data converter. For optimal performance, the common-mode voltage is recommended to be set at the midpoint of the analog supplies [(AVDD + AVSS) / 2].

If any of the analog input channels are not used, then power-down these pins using register bits to conserve power. See the *SPI Command Definitions* section for more information on how to power-down individual channels. Tie any unused or powered down analog input pins directly to AVDD.

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9.3.4 PGA Settings and Input Range

Each channel has its own configurable programmable gain amplifier (PGA) following its multiplexer. The PGA is designed using two operational amplifiers in a differential configuration, as shown in Figure 21. Set the gain to one of five settings (1, 2, 4, 8, and 12) using the CHnSET registers for each individual channel (see the *CHnSET* registers in the *Register Map* section for details). The ADS131E0x has CMOS inputs and therefore has negligible current noise. Table 3 shows the typical small-signal bandwidth values for various gain settings.

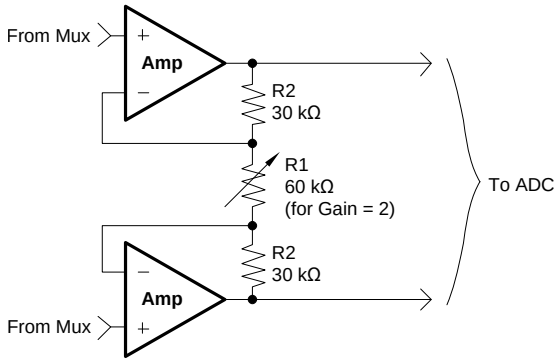

Figure 21. PGA Implementation

Table 3. PGA Gain versus Bandwidth

GAIN	NOMINAL BANDWIDTH AT T_A = 25°C (kHz)
1	237
2	146
4	96
8	48
12	32

The PGA resistor string that implements the gain has 120 kΩ of resistance for a gain of 2. This resistance provides a current path across the PGA outputs in the presence of a differential input signal. This current is in addition to the quiescent current specified for the device in the presence of a differential signal at the input.

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9.3.4.1 Input Common-Mode Range

The usable input common-mode range of the analog front-end depends on various parameters, including the maximum differential input signal, supply voltage, and PGA gain. The common-mode range, V_{CM}, is defined in Equation 4:

$$AVDD - 0.3\ V - \left(\frac{Gain \times V_{MAX_DIFF}}{2}\right) > V_{CM} > AVSS + 0.3\ V + \left(\frac{Gain \times V_{MAX_DIFF}}{2}\right) \quad (4)$$

where:

- V_{MAX_DIFF} = maximum differential signal at the PGA input and
- V_{CM} = common-mode voltage

For example:

If AVDD – AVSS = 3.3 V, gain = 2, and V_{MAX_DIFF} = 1000 mV,

Then 1.3 V < V_{CM} < 2.0 V

9.3.5 ΔΣ Modulator

Each ADS131E0x channel has its own delta-sigma (ΔΣ) ADC. The ΔΣ converters use second-order modulators optimized for low-power applications. The modulator samples the input signal at the modulator rate of (f_{MOD} = f_{CLK} / 2). As with any ΔΣ modulator, the ADS131E0x noise is shaped until f_{MOD} / 2, as shown in Figure 22.

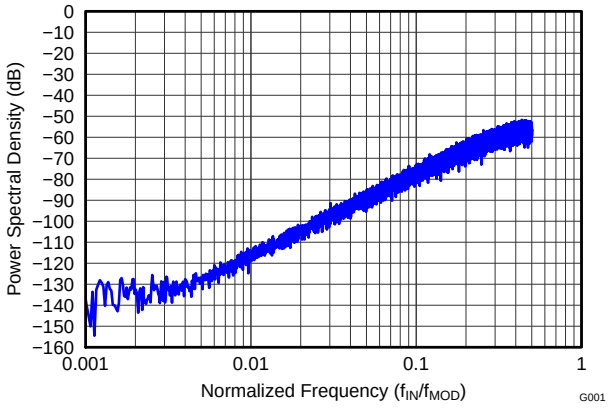

Figure 22. Modulator Noise Spectrum Up to 0.5 × f_{MOD}

9.3.6 Clock

The ADS131E0x provides two different device clocking methods: internal and external. Internal clocking using the internal oscillator is ideally-suited for non-synchronized, low-power systems. The internal oscillator is trimmed for accuracy at room temperature. The accuracy of the internal oscillator varies over the specified temperature range; see the *Electrical Characteristics* table for details. External clocking is recommended when synchronizing multiple ADS131E0x devices or when synchronizing to an external event because the internal oscillator clock performance can vary over temperature. Clock selection is controlled by the CLKSEL pin and the CLK_EN register bit. Provide the external clock any time after the analog and digital supplies are present.

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The CLKSEL pin selects either the internal oscillator or external clock. The CLK_EN bit in the CONFIG1 register enables and disables the oscillator clock to be output on the CLK pin. A truth table for the CLKSEL pin and the CLK_EN bit is shown in Table 4. The CLK_EN bit is useful when multiple devices are used in a daisy-chain configuration. During power-down, the external clock is recommended to be shut down to save power.

Table 4. CLKSEL Pin and CLK_EN Bit

CLKSEL PIN	CLK_EN BIT	CLOCK SOURCE	CLK PIN STATUS
0	X	External clock	Input: external clock
1	0	Internal oscillator	3-state
1	1	Internal oscillator	Output: internal oscillator

9.3.7 Digital Decimation Filter

The digital filter receives the modulator output bit stream and decimates the data stream. The decimation ratio determines the number of samples taken to create the output data word, and is set by the modulator rate divided by the data rate (f_{MOD} / f_{DR}). By adjusting the decimation ratio, a tradeoff can be made between resolution and data rate: higher decimation allows for higher resolution (thus creating lower data rates) and lower decimation decreases resolution but enables wider bandwidths with higher data rates. Higher data rates are typically used in power applications that implement software re-sampling techniques to help with channel-to-channel phase adjustment for voltage and current.

The digital filter on each channel consists of a third-order sinc filter. An input step change takes three conversion cycles for the filter to settle. Adjust the decimation ratio of the $sinc^3$ filters using the DR[2:0] bits in the CONFIG1 register (see the *Register Map* section for details). The data rate setting is a global setting that sets all channels to the same data rate.

The sinc filter is a variable decimation rate, third-order, low-pass filter. Data are supplied to this section of the filter from the modulator at the rate of f_{MOD}. The $sinc^3$ filter attenuates the high-frequency modulator noise, then decimates the data stream into parallel data. The decimation rate affects the overall converter data rate.

Equation 5 shows the scaled $sinc^3$ filter Z-domain transfer function.

$$\left|H(z)\right| = \left|\frac{1 - Z^{-N}}{1 - Z^{-1}}\right|^3 \tag{5}$$

The $sinc^3$ filter frequency domain transfer function is shown in Equation 6.

$$\left|H(f)\right| = \left|\frac{\sin\left(\frac{N\pi f}{f_{MOD}}\right)}{N \times \sin\left(\frac{\pi f}{f_{MOD}}\right)}\right|^3 \tag{6}$$

where:

- N = decimation ratio

The $sinc^3$ filter has notches (or zeroes) that occur at the output data rate and multiples thereof. At these frequencies, the filter has infinite attenuation. Figure 23 illustrates the sinc filter frequency response and Figure 24 illustrates the sinc filter roll-off. Figure 25 and Figure 26 illustrate the filter transfer function until f_{MOD} / 2 and f_{MOD} / 16, respectively, at different data rates. Figure 27 illustrates the transfer function extended until 4 f_{MOD}. Figure 27 illustrates that the ADS131E0x passband repeats itself at every f_{MOD}. Note that the digital filter response and filter notches are proportional to the master clock frequency.

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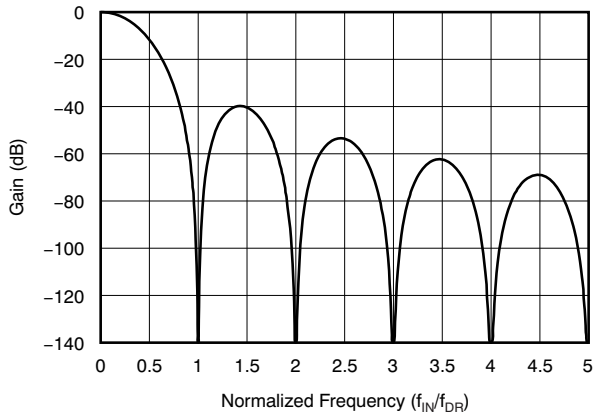

Figure 23. Sinc Filter Frequency Response

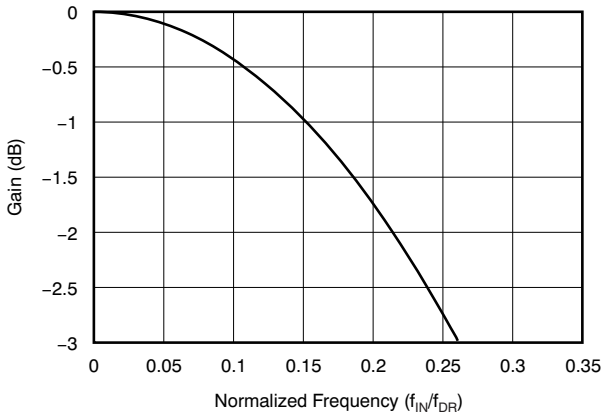

Figure 24. Sinc Filter Roll-Off

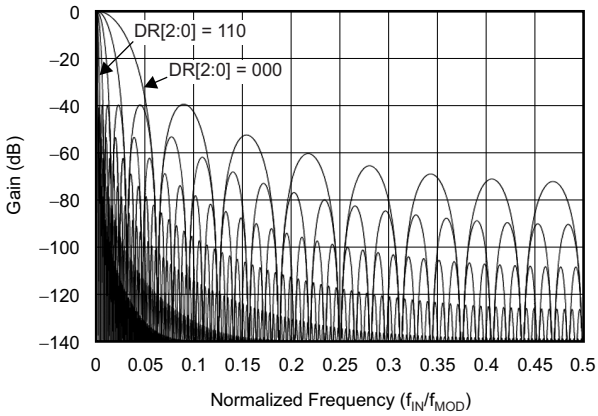

Figure 25. Transfer Function of Decimation Filters Until f_{MOD} / 2

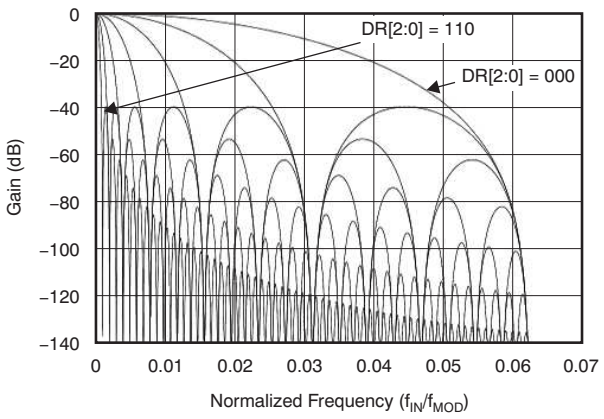

Figure 26. Transfer Function of Decimation Filters Until f_{MOD} / 16

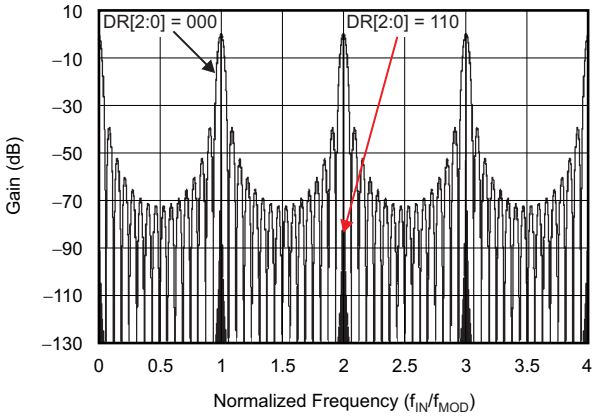

Figure 27. Transfer Function of Decimation Filters Until 4 f_{MOD} for DR[2:0] = 000 and DR[2:0] = 110

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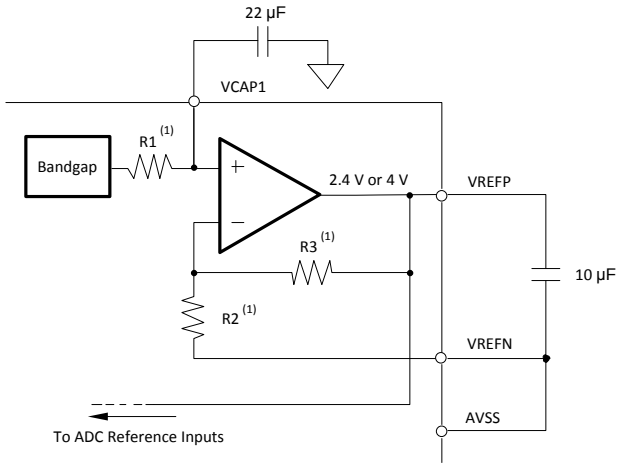
9.3.8 Voltage Reference

Figure 28 shows a simplified block diagram of the internal ADS131E0x reference. The reference voltage is generated with respect to AVSS. When using the internal voltage reference, connect VREFN to AVSS.



For V_{REF} = 2.4 V: R1 = 12.5 kΩ, R2 = 25 kΩ, and R3 = 25 kΩ.

For V_{REF} = 4 V: R1 = 10.5 kΩ, R2 = 15 kΩ, and R3 = 35 kΩ.

Figure 28. Internal Reference

The external band-limiting capacitors determine the amount of reference noise contribution. For high-end systems, the capacitor values should be chosen such that the bandwidth is limited to less than 10 Hz, so that the reference noise does not dominate the system noise. When using a 3-V analog supply, the internal reference must be set to 2.4 V. In case of a 5-V analog supply, the internal reference can be set to 4 V by setting the VREF_4V bit in the CONFIG2 register.

Alternatively, the internal reference buffer can be powered down and VREFP can be driven externally. Figure 29 shows a typical external reference drive circuit. Power-down is controlled by the PD_REFBUF bit in the CONFIG3 register. This power-down is also used to share internal references when two devices are cascaded. By default, the device wakes up in external reference mode.

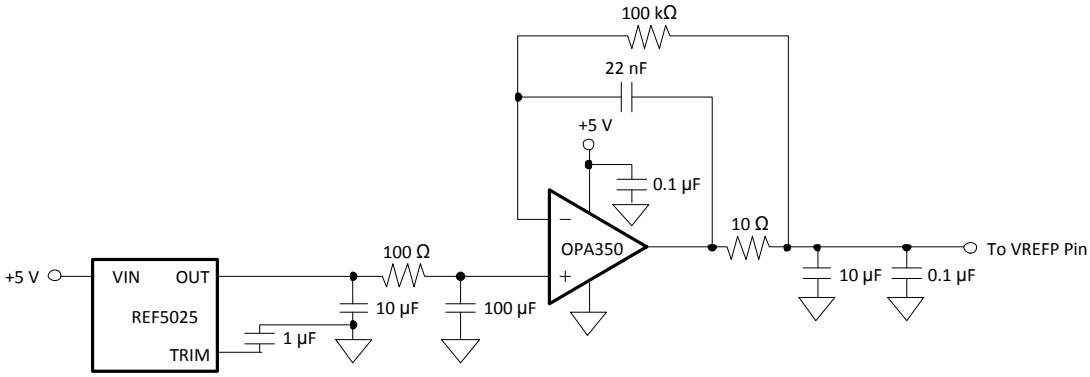


Figure 29. External Reference Driver

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9.3.9 Input Out-of-Range Detection

The ADS131E0x has integrated comparators to detect out-of-range conditions on the input signals. The basic principle is to compare the input voltage against a threshold voltage set by a 3-bit digital-to-analog converter (DAC) based off the analog power supply. The comparator trigger threshold level is set by the COMP_TH[2:0] bits in the FAULT register.

If the ADS131E0x is powered from a ±2.5-V supply and COMP_TH[2:0] = 000 (95% and 5%), the high-side trigger threshold is set at 2.25 V [equal to AVSS + (AVDD – AVSS) × 95%] and the low-side threshold is set at –2.25 V [equal to AVSS + (AVDD – AVSS) × 5%]. The threshold calculation formula applies to unipolar as well as to bipolar supplies.

A fault condition can be detected by setting the appropriate threshold level using the COMP_TH[2:0] bits. To determine which of the inputs is out of range, read the FAULT_STATP and FAULT_STATN registers individually or read the FAULT_STATx bits as part of the output data stream; see the *Data Output (DOUT)* section.

9.3.10 General-Purpose Digital I/O (GPIO)

The ADS131E0x has a total of four general-purpose digital I/O (GPIO) pins available. Configure the digital I/O pins as either inputs or outputs through the GPIOC bits. The GPIOD bits in the GPIO register indicate the level of the pins. The GPIO logic high voltage level is set by the voltage level of DVDD. When reading the GPIOD bits, the data returned are the logic level of the pins, whether they are programmed as inputs or outputs. When the GPIO pin is configured as an input, a write to the corresponding GPIOD bit has no effect. When configured as an output, a write to the GPIOD bit sets the output level.

If configured as inputs, the GPIO pins must be driven to a defined state. The GPIO pins are set as inputs after power up or after a reset. Figure 30 shows the GPIO pin structure. Connect unused GPIO pins directly to DGND through 10-kΩ resistors.

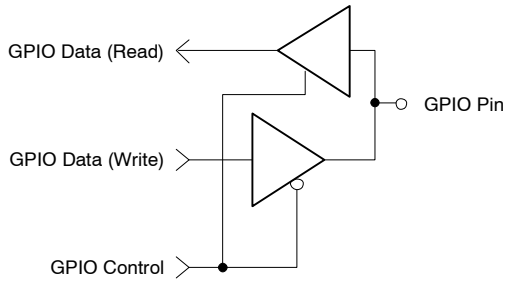

Figure 30. GPIO Pin Implementation

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9.4 Device Functional Modes

9.4.1 Start

Pull the START pin high for at least 2 t_{CLK} periods, or send the START command to begin conversions. When START is low and the START command has not been sent, the device does not issue a $\overline{DRDY}$ signal (conversions are halted).

When using the START command to control conversions, hold the START pin low. In multiple device configurations, the START pin is used to synchronize devices (see the *Multiple Device Configuration* subsection for more details).

9.4.1.1 Settling Time

The settling time (t_{SETTLE}) is the time required for the converter to output fully-settled data when the START signal is pulled high. When START is pulled high, $\overline{DRDY}$ is also pulled high. The next $\overline{DRDY}$ falling edge indicates that data are ready. Figure 31 shows the timing diagram and Table 5 shows the settling time for different data rates as a function of t_{CLK}. The settling time depends on f_{CLK} and the decimation ratio (controlled by the DR[2:0] bits in the CONFIG1 register). When the initial settling time has passed, the $\overline{DRDY}$ falling edge occurs at the set data rate, t_{DR}. If data is not read back on DOUT and the output shift register needs to update, $\overline{DRDY}$ goes high for 4 t_{CLK} before returning back low indicating new data is ready. Note that when START is held high and there is a step change in the input signal, 3 × t_{DR} is required for the filter to settle to the new value. Settled data are available on the fourth $\overline{DRDY}$ pulse.

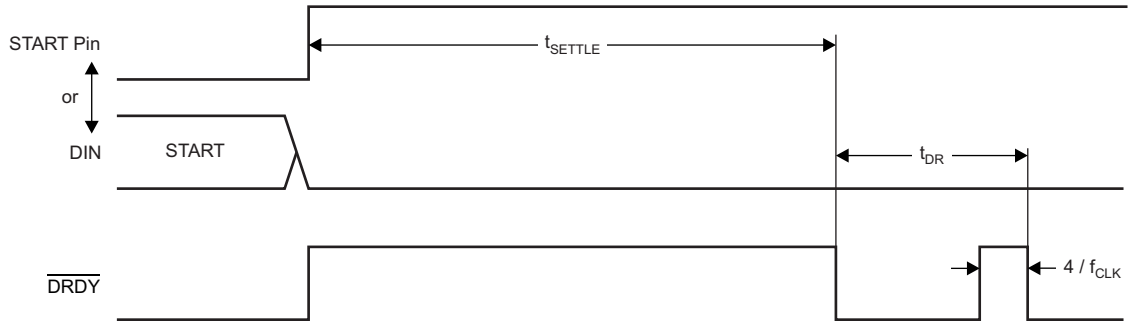

Figure 31. Settling Time

Table 5. Settling Time for Different Data Rates

DR[2:0]	NORMAL MODE	UNIT
000	152	t_{CLK}
001	296	t_{CLK}
010	584	t_{CLK}
011	1160	t_{CLK}
100	2312	t_{CLK}
101	4616	t_{CLK}
110	9224	t_{CLK}

9.4.1.2 Input Signal Step

When the device is converting and there is a step change on the input signal, a delay of 3 t_{DR} is required for the output data to settle. Settled data are available on the fourth $\overline{DRDY}$ pulse. Data are available to read at each $\overline{DRDY}$ low transition prior to the 4th $\overline{DRDY}$ pulse, but are recommended to be ignored. Figure 32 shows the required wait time for complete settling for an input step or input transient event on the analog input.

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Device Functional Modes (continued)

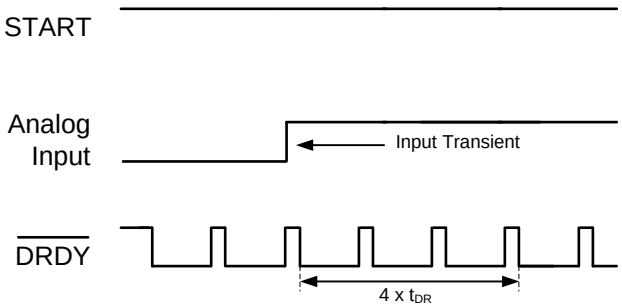


Figure 32. Settling Time for the Input Transient

9.4.2 Reset ($\overline{\text{RESET}}$)

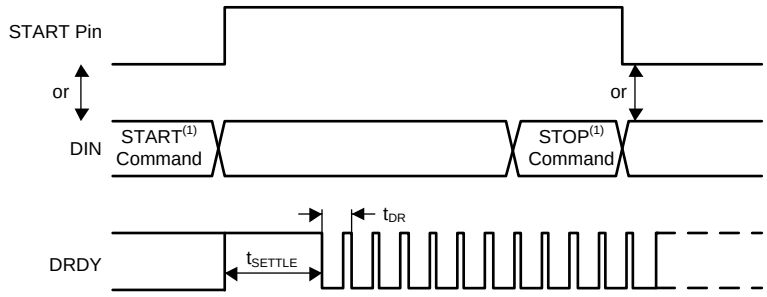
There are two methods to reset the ADS131E0x: pull the $\overline{\text{RESET}}$ pin low, or send the RESET command. When using the $\overline{\text{RESET}}$ pin, make sure to follow the minimum pulse duration timing specifications before taking the pin back high. The RESET command takes effect on the eighth SCLK falling edge of the command. After a reset, 18 t_{CLK} cycles are required to complete initialization of the configuration registers to default states and start the conversion cycle. Note that an internal reset is automatically issued to the digital filter whenever the CONFIG1 register is set to a new value with a WREG command.

9.4.3 Power-Down ($\overline{\text{PWDN}}$)

When $\overline{\text{PWDN}}$ is pulled low, all on-chip circuitry is powered down. To exit power-down mode, take the $\overline{\text{PWDN}}$ pin high. Upon exiting from power-down mode, the internal oscillator and the reference require time to wake up. During power-down, the external clock is recommended to be shut down to save power.

9.4.4 Continuous Conversion Mode

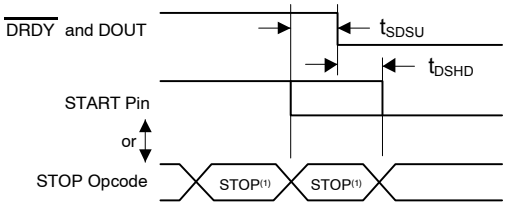
Conversions begin when the START pin is taken high or when the START command is sent. As shown in Figure 33, the DRDY output goes high when conversions are started and goes low when data are ready. Conversions continue indefinitely until the START pin is taken low or the STOP command is transmitted. When the START pin is pulled low or the STOP command is issued, the conversion in progress is allowed to complete. Figure 34 and Table 6 show the required DRDY timing to the START pin or the START and STOP commands when controlling conversions in this mode. The t_{SDSU} timing indicates when to take the START pin low or when to send the STOP command before the DRDY falling edge to halt further conversions. The t_{DSHD} timing indicates when to take the START pin low or send the STOP command after a DRDY falling edge to complete the current conversion and halt further conversions. To keep the converter running continuously, the START pin can be permanently tied high.



(1) START and STOP commands take effect on the seventh SCLK falling edge.

Figure 33. Continuous Conversion Mode

Device Functional Modes (continued)



(1) START and STOP commands take effect on the seventh SCLK falling edge at the end of the transmission.

Figure 34. START to DRDY Timing

Table 6. Timing Characteristics for Figure 34(1)

		MIN	UNIT
t_{SDSU}	Setup time: START pin low or STOP command before the DRDY falling edge to halt further conversions	16	t_{CLK}
t_{DSHD}	Delay time: START pin low or STOP command to complete the current conversion and halt further conversions	16	t_{CLK}

(1) START and STOP commands take effect on the seventh SCLK falling edge at the end of the transmission.

9.4.5 Data Retrieval

9.4.5.1 Data Ready (DRDY)

DRDY is an output signal which transitions from high to low indicating new conversion data are ready. The CS signal has no effect on the data ready signal. DRDY behavior is determined by whether the device is in RDATAC mode or the RDATA command is used to read data on demand. (See the *RDATAC: Start Read Data Continuous Mode* and *RDATA: Read Data* subsections of the *SPI Command Definitions* section for further details).

When reading data with the RDATA command, the read operation can overlap the next DRDY occurrence without data corruption.

The START pin or the START command places the device either in normal data capture mode or pulse data capture mode.

Figure 35 shows the relationship between CS, DRDY, DOUT, and SCLK during data retrieval (in case of an ADS131E0x). DOUT is latched out at the SCLK rising edge. DRDY is pulled high at the SCLK falling edge. Note that DRDY goes high on the first SCLK falling edge, regardless of whether data are being retrieved from the device or a command is being sent through the DIN pin.

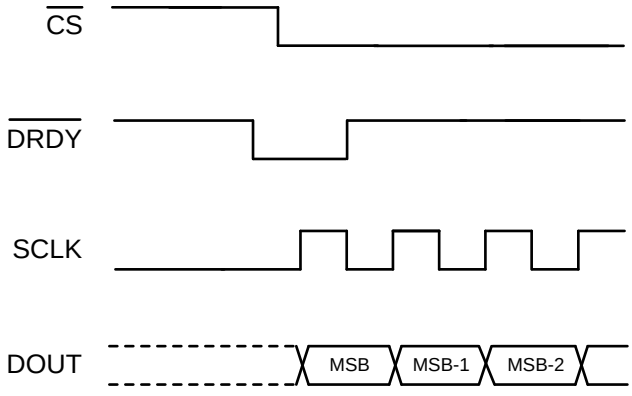


Figure 35. DRDY Behavior with Data Retrieval

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The $\overline{\text{DRDY}}$ signal is cleared on the first SCLK falling edge regardless of the state of $\overline{\text{CS}}$. This condition must be taken into consideration if the SPI bus is used to communicate with other devices on the same bus. Figure 36 shows a behavior diagram for $\overline{\text{DRDY}}$ when SCLKs are sent with $\overline{\text{CS}}$ high. Figure 36 shows that no data are clocked out, but the $\overline{\text{DRDY}}$ signal is cleared.

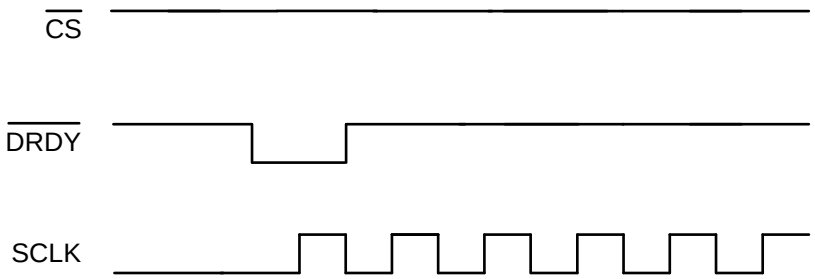

Figure 36. $\overline{\text{DRDY}}$ and SCLK Behavior when $\overline{\text{CS}}$ is High

9.4.5.2 Reading Back Data

Data retrieval can be accomplished in one of two methods:

1. RDATAC: the read data continuous command sets the device in a mode that reads data continuously without sending commands. See the *RDATAC: Start Read Data Continuous Mode* section for more details.
2. RDATA: the read data command requires that a command is sent to the device to load the output shift register with the latest data. See the *RDATA: Read Data* section for more details.

Conversion data are read by shifting data out on DOUT. The MSB of the data on DOUT is clocked out on the first SCLK rising edge. $\overline{\text{DRDY}}$ returns high on the first SCLK falling edge. DIN should remain low for the entire read operation.

9.4.5.3 Status Word

A status word precedes data readback and provides information on the state of the ADS131E0x. The status word is 24 bits long and contains the values for FAULT_STATP, FAULT_STATN, and the GPIO data bits. The content alignment is shown in Figure 37.

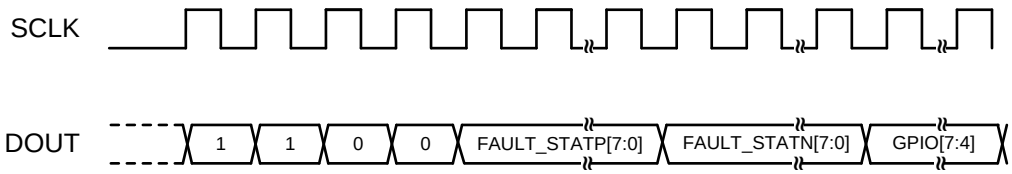

Figure 37. Status Word Content

NOTE

The status word length is always 24 bits. The length does not change for 32-kSPS and 64-kSPS data rates.

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9.4.5.4 Readback Length

The number of bits in the data output depends on the number of channels and the number of bits per channel. The data format for each channel data are twos complement and MSB first.

For the ADS131E0x with 32-kSPS and 64-kSPS data rates, the number of data bits is: 24 status bits + 16 bits per channel × 8 channels = 152 bits.

For all other data rates, the number of data bits is: 24 status bits + 24 bits per channel × 8 channels = 216 bits.

When channels are powered down using the user register setting, the corresponding channel output is set to 0. However, the sequence of channel outputs remains the same.

The ADS131E0x also provides a multiple data readback feature. Data can be read out multiple times by simply providing more SCLKs, in which case the MSB data byte repeats after reading the last byte. The DAISY_IN bit in the CONFIG1 register must be set to 1 for multiple read backs.

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9.5 Programming

9.5.1 Data Format

The DR[2:0] bits in the CONFIG1 register sets the output resolution for the ADS131E0x. When DR[2:0] = 000 or 001, the 16 bits of data per channel are sent in binary twos complement format, MSB first. The size of one code (LSB) is calculated using Equation 7.

$$1\ LSB = (2 \times V_{REF} / Gain) / 2^{16} = FS / 2^{15} \quad (7)$$

A positive full-scale input [$V_{IN} \geq (FS - 1\ LSB) = (V_{REF} / Gain - 1\ LSB)$] produces an output code of 7FFFh and a negative full-scale input ($V_{IN} \leq -FS = -V_{REF} / Gain$) produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale.

Table 7 summarizes the ideal output codes for different input signals.

Table 7. 16-Bit Ideal Output Code versus Input Signal

INPUT SIGNAL, V_{IN} $V_{(IN \times P)} - V_{(IN \times N)}$	IDEAL OUTPUT CODE(1)
≥ FS ($2^{15} - 1$) / 2^{15}	7FFFh
FS / 2^{15}	0001h
0	0000h
–FS / 2^{15}	FFFFh
≤ –FS	8000h

(1) Excludes the effects of noise, INL, offset, and gain errors.

When DR[2:0] = 010, 011, 100, 101, or 110, the ADS131E0x outputs 24 bits of data per channel in binary twos complement format, MSB first. The size of one code (LSB) is calculated using Equation 8.

$$1\ LSB = (2 \times V_{REF} / Gain) / 2^{24} = FS / 2^{23} \quad (8)$$

A positive full-scale input [$V_{IN} \geq (FS - 1\ LSB) = (V_{REF} / Gain - 1\ LSB)$] produces an output code of 7FFFFFh and a negative full-scale input ($V_{IN} \leq -FS = -V_{REF} / Gain$) produces an output code of 800000h. The output clips at these codes for signals that exceed full-scale.

Table 8 summarizes the ideal output codes for different input signals.

Table 8. 24-Bit Ideal Output Code versus Input Signal

INPUT SIGNAL, V_{IN} $V_{(INxP)} - V_{(INxN)}$	IDEAL OUTPUT CODE(1)
≥ FS ($2^{23} - 1$) / 2^{23}	7FFFFFh
FS / 2^{23}	000001h
0	000000h
–FS / 2^{23}	FFFFFFh
≤ –FS	800000h

(1) Excludes the effects of noise, INL, offset, and gain errors.

9.5.2 SPI Interface

The SPI-compatible serial interface consists of four signals: $\overline{CS}$, SCLK, DIN, and DOUT. The interface is used to read conversion data, read and write registers, and control the ADS131E0x operation. The $\overline{DRDY}$ output is used as a status signal to indicate when ADC data are ready for readback. $\overline{DRDY}$ goes low when new data are available.

9.5.2.1 Chip Select ($\overline{CS}$)

The $\overline{CS}$ pin activates SPI communication. $\overline{CS}$ must be low before data transactions and must stay low for the entire SPI communication period. When $\overline{CS}$ is high, the DOUT pin enters a high-impedance state. Therefore, reading and writing to the serial interface are ignored and the serial interface is reset. $\overline{DRDY}$ pin operation is independent of $\overline{CS}$. $\overline{DRDY}$ still indicates that a new conversion has completed and is forced high as a response to SCLK, even if $\overline{CS}$ is high.

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Taking $\overline{CS}$ high deactivates only the SPI communication with the device and the serial interface is reset. Data conversion continues and the $\overline{DRDY}$ signal can be monitored to check if a new conversion result is ready. A master device monitoring the $\overline{DRDY}$ signal can select the appropriate slave device by pulling the $\overline{CS}$ pin low. After the serial communication is finished, always wait four or more t_{CLK} cycles before taking $\overline{CS}$ high.

9.5.2.2 Serial Clock (SCLK)

SCLK provides the clock for serial communication. SCLK is a Schmitt-trigger input, but TI recommends keeping SCLK as free from noise as possible to prevent glitches from inadvertently shifting the data. Data are shifted into DIN on the falling edge of SCLK and shifted out of DOUT on the rising edge of SCLK.

The absolute maximum SCLK limit is specified in Figure 1. When shifting in commands with SCLK, make sure that the entire set of SCLKs is issued to the device. Failure to do so can result in the device serial interface being placed into an unknown state requiring $\overline{CS}$ to be taken high to recover.

For a single device, the minimum speed required for SCLK depends on the number of channels, number of bits of resolution, and output data rate. (For multiple devices, see the *Multiple Device Configuration* section.)

For example, if the ADS131E0x is used with an 8-kSPS mode (24-bit resolution), the minimum SCLK speed is 1.755 MHz to shift out all the data.

Data retrieval can be accomplished either by placing the device in RDATAC mode or by issuing an RDATA command for data on demand. The SCLK rate limitation in Equation 9 applies to RDATAC. For the RDATA command, the limitation applies if data must be read in between two consecutive $\overline{DRDY}$ signals. Equation 9 assumes that there are no other commands issued in between data captures.

$$t_{SCLK} < (t_{DR} - 4\ t_{CLK}) / (N_{BITS} \times 8 + 24) \quad (9)$$

where

- N_{BITS} = resolution of data for the current data rate; 16 or 24

9.5.2.3 Data Input (DIN)

DIN is used along with SCLK to send data to the device. Data on DIN are shifted into the device on the falling edge of SCLK.

The communication of this device is full-duplex in nature. The device monitors commands shifted in even when data are being shifted out. Data that are present in the output shift register are shifted out when sending in a command. Therefore, make sure that whatever is being sent on the DIN pin is valid when shifting out data. When no command is to be sent to the device when reading out data, send the NOP command on DIN. Make sure that the $t_{SDECODE}$ timing is met in the *Sending Multibyte Commands* section when sending multiple byte commands on DIN.

9.5.2.4 Data Output (DOUT)

DOUT is used with SCLK to read conversion and register data from the device. Data are clocked out on the rising edge of SCLK, MSB first. DOUT goes to a high-impedance state when $\overline{CS}$ is high. In read data continuous mode (see the *SPI Command Definitions* section for more details), the DOUT output line can also be used to indicate when new data are available. If $\overline{CS}$ is low when new data are ready, a high-to-low transition on the DOUT line occurs synchronously with a high-to-low transition on $\overline{DRDY}$, as shown in Figure 38. This feature can be used to minimize the number of connections between the device and system controller.

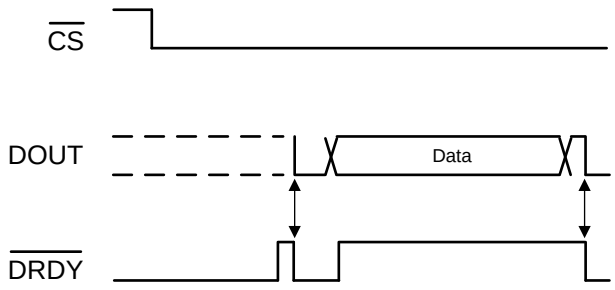

Figure 38. Using DOUT as $\overline{DRDY}$

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9.5.3 SPI Command Definitions

The ADS131E0x provides flexible configuration control. The commands, summarized in Table 9, control and configure device operation. The commands are stand-alone, except for the register read and register write operations that require a second command byte to include additional data. $\overline{CS}$ can be taken high or held low between commands but must stay low for the entire command operation (including multibyte commands). System commands and the RDATA command are decoded by the ADS131E0x on the seventh SCLK falling edge. The register read and write commands are decoded on the eighth SCLK falling edge. Be sure to follow the SPI timing requirements when pulling $\overline{CS}$ high after issuing a command.

Table 9. Command Definitions

COMMAND	DESCRIPTION	FIRST BYTE	SECOND BYTE
SYSTEM COMMANDS			
WAKEUP	Wake-up from standby mode	0000 0010 (02h)	
STANDBY	Enter standby mode	0000 0100 (04h)	
RESET	Reset the device	0000 0110 (06h)	
START	Start or restart (synchronize) conversions	0000 1000 (08h)	
STOP	Stop conversions	0000 1010 (0Ah)	
OFFSETCAL	Channel offset calibration	0001 1010 (1Ah)	
DATA READ COMMANDS			
RDATAC	Enable read data continuous mode. This mode is the default mode at power-up.(1)	0001 0000 (10h)	
SDATAC	Stop read data continuous mode	0001 0001 (11h)	
RDATA	Read data by command	0001 0010 (12h)	
REGISTER READ COMMANDS			
RREG	Read *n nnnn* registers starting at address *r rrrr*	001*r rrrr* (2xh)(2)	000*n nnnn*(2)
WREG	Write *n nnnn* registers starting at address *r rrrr*	010*r rrrr* (4xh)(2)	000*n nnnn*(2)

(1) When in RDATAC mode, the RREG command is ignored.
(2) *n nnnn* = number of registers to be read or written – 1. For example, to read or write three registers, set *n nnnn* = 0 (0010). *r rrrr* = the starting register address for read and write commands.

9.5.3.1 Sending Multibyte Commands

The ADS131E0x serial interface decodes commands in bytes and requires 4 t_{CLK} cycles to decode and execute each command. Therefore, when sending multi-byte commands (such as RREG or WREG), a 4 t_{CLK} period must separate the end of one byte (or command) and the next.

Assuming CLK is 2.048 MHz, then $t_{SDECODE}$ (4 t_{CLK}) is 1.96 µs. When SCLK is 16 MHz, one byte can be transferred in 0.5 µs. This byte transfer time does not meet the $t_{SDECODE}$ specification; therefore, a delay of 1.46 µs (1.96 µs – 0.5 µs) must be inserted after the first byte and before the second byte. If SCLK is 4 MHz, one byte is transferred in 2 µs. Because this transfer time exceeds the $t_{SDECODE}$ specification (2 µs > 1.96 µs), the processor can send subsequent bytes without delay.

9.5.3.2 WAKEUP: Exit STANDBY Mode

The WAKEUP command exits the low-power standby mode; see the *STANDBY: Enter STANDBY Mode* section. Be sure to allow enough time for all circuits in standby mode to power-up (see the *Electrical Characteristics* table for details). There are no SCLK rate restrictions for this command and it can be issued at any time. There are no SCLK rate restrictions for this command and can be issued at any time. Any following commands must be sent after a delay of 4 t_{CLK} cycles.

9.5.3.3 STANDBY: Enter STANDBY Mode

The STANDBY command enters low-power standby mode. All circuits in the device are powered down except for the reference section. The standby mode power consumption is specified in the *Electrical Characteristics* table. There are no SCLK rate restrictions for this command and can be issued at any time. Do not send any other commands other than the WAKEUP command after the device enters standby mode.

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9.5.3.4 RESET: Reset Registers to Default Values

The RESET command resets the digital filter and returns all register settings to their default values; see the *Reset (RESET)* section for more details. There are no SCLK rate restrictions for this command and can be issued at any time. 18 t_{CLK} cycles are required to execute the RESET command. Avoid sending any commands during this time.

9.5.3.5 START: Start Conversions

The START command starts data conversions. Tie the START pin low to control conversions by the START and STOP commands. If conversions are in progress, this command has no effect. The STOP command is used to stop conversions. If the START command is immediately followed by a STOP command, then there must be a gap of 4 t_{CLK} cycle delay between them. The current conversion completes before further conversions are halted. There are no SCLK rate restrictions for this command and can be issued at any time.

9.5.3.6 STOP: Stop Conversions

The STOP command stops conversions. Tie the START pin low to control conversions by command. When the STOP command is sent, the conversion in progress completes and further conversions are stopped. If conversions are already stopped, this command has no effect. There are no SCLK rate restrictions for this command and can be issued at any time.

9.5.3.7 OFFSETCAL: Channel Offset Calibration

The OFFSETCAL command cancels the offset of each channel. The OFFSETCAL command is recommended to be issued every time there is a change in PGA gain settings.

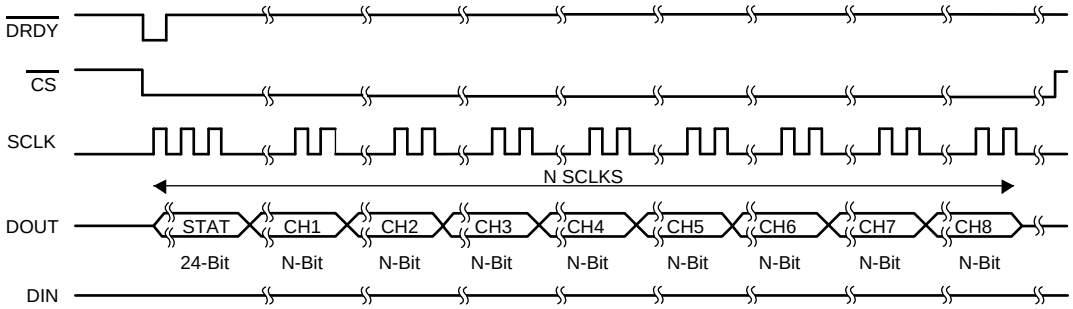
When the OFFSETCAL command is issued, the device configures itself to the lowest data rate (DR[2:0] = 110, 1 kSPS) and performs the following steps for each channel:

- Short the analog inputs of each channel together and connect them to mid-supply [(AVDD + AVSS) / 2]
- Reset the digital filter (requires a filter settling time = 4 t_{DR})
- Collect 16 data points for calibration = 15 t_{DR}

Total calibration time = (19 t_{DR} × 8) + 1 ms = 153 ms.

9.5.3.8 RDATAC: Start Read Data Continuous Mode

The RDATAC command enables read data continuous mode. In this mode, conversion data are retrieved from the device without the need to issue subsequent RDATA commands. This mode places the conversion data in the output register with every $\overline{\text{DRDY}}$ falling edge so that the data can be shifted out directly with the following SCLKs. Shift out all data from the device before data are updated with a new $\overline{\text{DRDY}}$ falling edge to avoid losing data. The read data continuous mode is the device default mode; the device defaults to this mode on powerup. Figure 39 shows the ADS131E0x data output protocol when using RDATAC mode.



NOTE: X SCLKs = (N bits)(8 channels) + 24 bits. N-bit is dependent upon the DR[2:0] registry bit settings (N = 16 or 24).

Figure 39. ADS131E0x SPI Bus Data Output (Eight Channels)

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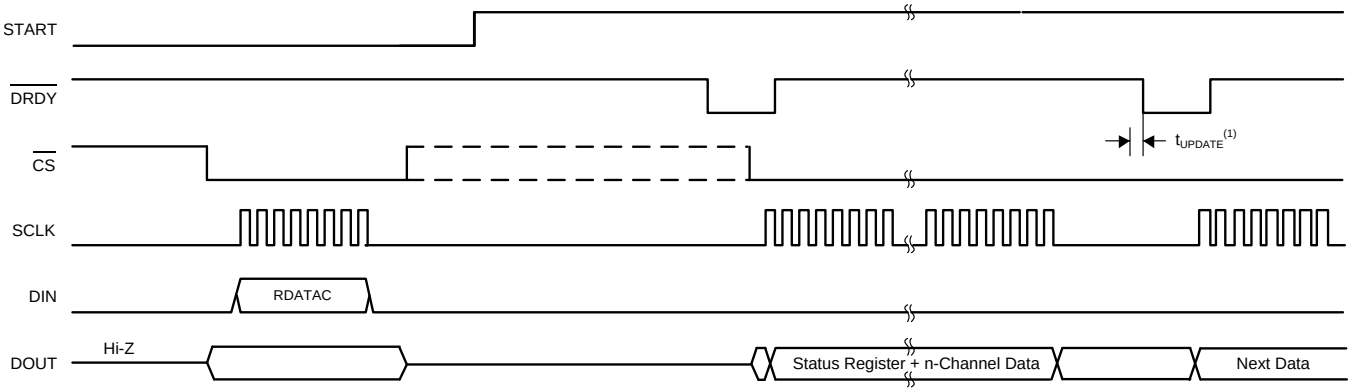
RDATAC mode is cancelled by the Stop Read Data Continuous command. If the device is in RDATAC mode, a SDATAC command must be issued before any other commands can be sent to the device. There are no SCLK rate restrictions for this command. However, subsequent data retrieval SCLKs or the SDATAC command should wait at least 4 t_{CLK} cycles before completion. RDATAC timing is shown in Figure 40. There is a *keep out* zone of 4 t_{CLK} cycles around the DRDY pulse where this command cannot be issued in. If no data are retrieved from the device and CS is held low, a high-to-low DOUT transition occurs synchronously with DRDY. To retrieve data from the device after the RDATAC command is issued, make sure either the START pin is high or the START command is issued. Figure 40 shows the recommended way to use the RDATAC command. Read data continuous mode is ideally-suited for applications such as data loggers or recorders where registers are set one time and do not need to be reconfigured.



(1) $t_{UPDATE} = 4 / f_{CLK}$. Do not read data during this time.

Figure 40. Reading Data in RDATAC Mode

9.5.3.9 SDATAC: Stop Read Data Continuous Mode

The SDATAC command cancels the Read Data Continuous mode. There are no SCLK rate restrictions for this command, but the next command must wait for 4 t_{CLK} cycles before completion.

9.5.3.10 RDATA: Read Data

The RDATA command loads the output shift register with the latest data when not in Read Data Continuous mode. Issue this command after DRDY goes low to read the conversion result. There are no SCLK rate restrictions for this command, and there is no wait time needed for the subsequent commands or data retrieval SCLKs. To retrieve data from the device after the RDATA command is issued, make sure either the START pin is high or the START command is issued. When reading data with the RDATA command, the read operation can overlap the next DRDY occurrence without data corruption. RDATA can be sent multiple times after new data are available, thus supporting multiple data readback. Figure 41 illustrates the recommended way to use the RDATA command. RDATA is best suited for systems where register settings must be read or the user does not have precise control over timing. Reading data using the RDATA command is recommended to avoid data corruption when the DRDY signal is not monitored.

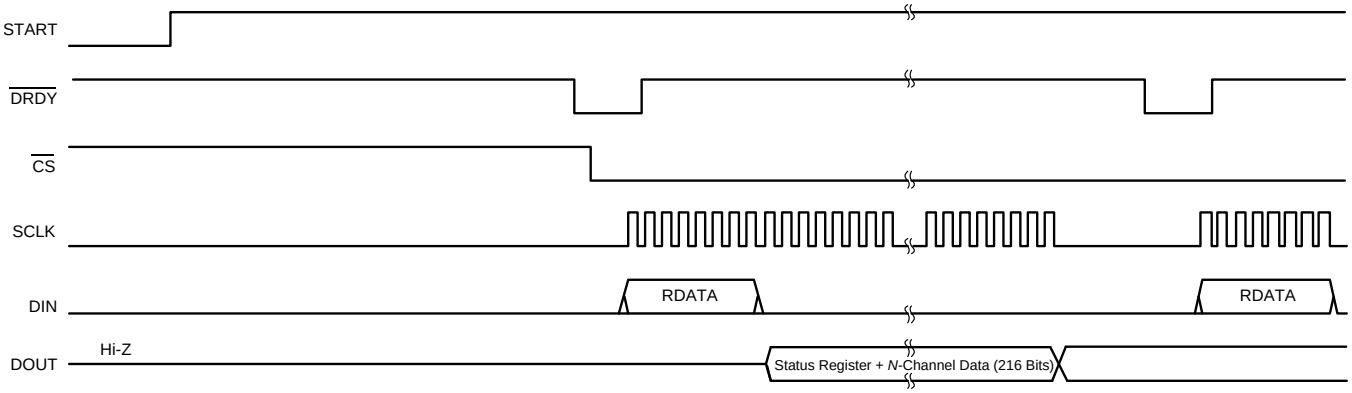


Figure 41. RDATA Usage

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9.5.3.11 RREG: Read from Register

The RREG command reads the contents of one or more device configuration registers. The Register Read command is a two-byte command followed by the register data output. The first byte contains the command and register address. The second command byte specifies the number of registers to read – 1.

First command byte: 001*r rrrr*, where *r rrrr* is the starting register address.

Second command byte: 000*n nnnn*, where *n nnnn* is the number of registers to read – 1.

The 17th SCLK rising edge of the operation clocks out the MSB of the first register, as shown in Figure 42. When the device is in read data continuous mode, an SDATAC command must be issued before the RREG command can be issued. The RREG command can be issued any time. However, because this command is a multi-byte command, there are SCLK rate restrictions depending on how the SCLKs are issued to meet the $t_{SDECODE}$ timing. See the *Serial Clock (SCLK)* subsection of the *SPI Interface* section for more details. Note that $\overline{CS}$ must be low for the entire command.

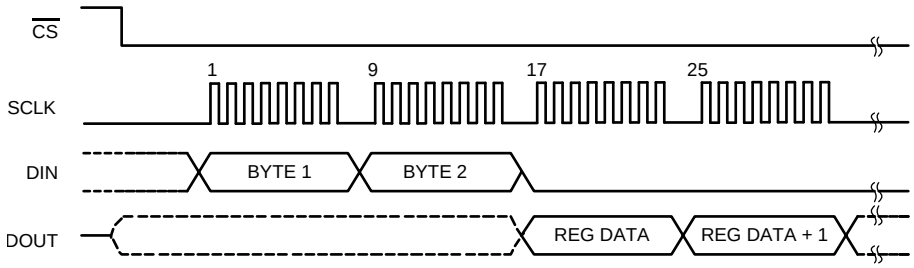

Figure 42. RREG Command Example: Read Two Registers Starting from Register 00h (ID Register) (BYTE 1 = 0010 0000, BYTE 2 = 0000 0001)

9.5.3.12 WREG: Write to Register

The WREG command writes data to one or more device configuration registers. The Register Write command is a two-byte command followed by the register data input. The first byte contains the command and register address. The second command byte specifies the number of registers to write – 1.

First command byte: 010*r rrrr*, where *r rrrr* is the starting register address.

Second command byte: 000*n nnnn*, where *n nnnn* is the number of registers to write – 1.

After the command bytes, the register data follows (in MSB-first format), as shown in Figure 43. For multiple register writes across reserved registers (0Dh–11h), these registers must be included in the register count and the default setting of the reserved register must be written. The WREG command can be issued at any time. However, because this command is a multi-byte command, there are SCLK rate restrictions depending on how the SCLKs are issued to meet the $t_{SDECODE}$ timing. See the Figure 1 for more details. $\overline{CS}$ must be low for the entire command.

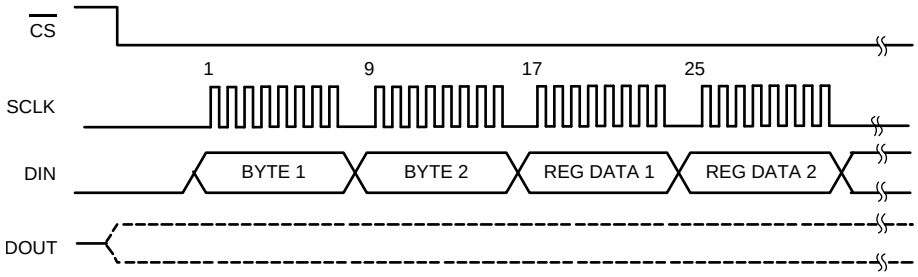

Figure 43. WREG Command Example: Write Two Registers Starting from 00h (ID Register) (BYTE 1 = 0100 0000, BYTE 2 = 0000 0001)

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9.6 Register Map

Table 10 describes the various ADS131E0x registers.

Table 10. Register Map(1)

ADDRESS	REGISTER	RESET VALUE (HEX)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DEVICE SETTINGS (READ-ONLY REGISTERS)										
00h	ID	xx	REV_ID2	REV_ID1	REV_ID0	1	0	0	NU_CH2	NU_CH1
GLOBAL SETTINGS ACROSS CHANNELS										
01h	CONFIG1	91	1	DAISY_IN	CLK_EN	1	0	DR[2:0]		
02h	CONFIG2	E0	1	1	1	INT_TEST	0	TEST_AMP0	TEST_FREQ[1:0]	
03h	CONFIG3	40	PDB_REFBUF	1	VREF_4V	0	OPAMP_REF	PDB_OPAMP	0	0
04h	FAULT	00	COMP_TH[2:0]			0	0	0	0	0
CHANNEL-SPECIFIC SETTINGS										
05h	CH1SET	10	PD1	GAIN1[2:0]			0	MUX1[2:0]		
06h	CH2SET	10	PD2	GAIN2[2:0]			0	MUX2[2:0]		
07h	CH3SET	10	PD3	GAIN3[2:0]			0	MUX3[2:0]		
08h	CH4SET	10	PD4	GAIN4[2:0]			0	MUX4[2:0]		
09h	CH5SET	10	PD5	GAIN5[2:0]			0	MUX5[2:0]		
0Ah	CH6SET	10	PD6	GAIN6[2:0]			0	MUX6[2:0]		
0Bh	CH7SET	10	PD7	GAIN7[2:0]			0	MUX7[2:0]		
0Ch	CH8SET	10	PD8	GAIN8[2:0]			0	MUX8[2:0]		
FAULT DETECT STATUS REGISTERS (READ-ONLY REGISTERS)										
12h	FAULT_STATP	00	IN8P_FAULT	IN7P_FAULT	IN6P_FAULT	IN5P_FAULT	IN4P_FAULT	IN3P_FAULT	IN2P_FAULT	IN1P_FAULT
13h	FAULT_STATN	00	IN8N_FAULT	IN7N_FAULT	IN6N_FAULT	IN5N_FAULT	IN4N_FAULT	IN3N_FAULT	IN2N_FAULT	IN1N_FAULT
GPIO SETTINGS										
14h	GPIO	0F	GPIOD4	GPIOD3	GPIOD2	GPIOD1	GPIOC4	GPIOC3	GPIOC2	GPIOC1

(1) When using multiple register write commands, registers 0Dh, 0Eh, 0Fh, 10h, and 11h must be written to 00h.

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9.6.1 Register Descriptions

9.6.1.1 ID: ID Control Register (Factory-Programmed, Read-Only) (address = 00h) [reset = xxh]

This register is programmed during device manufacture to indicate device characteristics.

Figure 44. ID: ID Control Register

7	6	5	4	3	2	1	0
REV_ID2	REV_ID1	REV_ID0	1	0	0	NU_CH2	NU_CH1
R-1h	R-1h	R-0h	R-1h	R-0h	R-0h	R-xh	R-xh

LEGEND: R = Read only; -n = value after reset

Table 11. ID: ID Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	REV_ID[2:0]	R	6h	**Device family identification.** This bit indicates the device family. 110 : ADS131E0x 000, 001, 010, 011, 100, 101, 111 : Reserved
4	Reserved	R	1h	**Reserved.** Always reads 1.
3:2	Reserved	R	0h	**Reserved.** Always reads 0.
1:0	NU_CH[2:0]	R	xh	**Device identification bits.** 00 : 4-channel device 01 : 6-channel device 10 : 8-channel device 11 : Reserved

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9.6.1.2 CONFIG1: Configuration Register 1 (address = 01h) [reset = 91h]

This register configures daisy chain, the clock setting, and each ADC channel sample rate.

Figure 45. CONFIG1: Configuration Register 1

7	6	5	4	3	2	1	0
1	DAISY_IN	CLK_EN	1	0	DR[2:0]		
R/W-1h	R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-4h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 12. CONFIG1: Configuration Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W	1h	**Reserved.** Must be set to 1. This bit reads high.
6	DAISY_IN	R/W	0h	**Daisy-chain and multiple data readback mode.** This bit determines which mode is enabled. 0 : Daisy-chain mode 1 : Multiple data readback mode
5	CLK_EN	R/W	0h	**CLK connection**(1). This bit determines if the internal oscillator signal is connected to the CLK pin when the CLKSEL pin = 1. 0 : Oscillator clock output disabled 1 : Oscillator clock output enabled
4	Reserved	R/W	1h	**Reserved.** Must be set to 1. This bit reads high.
3	Reserved	R/W	0h	**Reserved.** Must be set to 0. This bit reads low.
2:0	DR[2:0]	R/W	1h	**Output data rate.** These bits determine the output data rate and resolution; see Table 13 for details.

(1) Additional power is consumed when driving external devices.

Table 13. Data Rate Settings

DR[2:0]	RESOLUTION	DATA RATE (kSPS)(1)
000	16-bit output	64
001	16-bit output	32 (default)
010	24-bit output	16
011	24-bit output	8
100	24-bit output	4
101	24-bit output	2
110	24-bit output	1
111	Do not use	NA

(1) Where f_{CLK} = 2.048 MHz. Data rates scale with master clock frequency.

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9.6.1.3 CONFIG2: Configuration Register 2 (address = 02h) [reset = E0h]

This register configures the test signal generation; see the *Input Multiplexer* section for more details.

Figure 46. CONFIG2: Configuration Register 2

7	6	5	4	3	2	1	0
1	1	1	INT_TEST	0	TEST_AMP	TEST_FREQ[1:0]	
R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 14. CONFIG2: Configuration Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	Reserved	R/W	7h	**Reserved.** Must be set to 1. This bit reads high.
4	INT_TEST	R/W	0h	**Test signal source.** This bit determines the source for the test signal. 0 : Test signals are driven externally 1 : Test signals are generated internally
3	Reserved	R/W	0h	**Reserved.** Must be set to 0. This bit reads low.
2	TEST_AMP	R/W	0h	**Test signal amplitude.** These bits determine the calibration signal amplitude. 0 : $1 \times -(V_{VREFP} - V_{VREFN}) / 2400$ 1 : $2 \times -(V_{VREFP} - V_{VREFN}) / 2400$
1:0	TEST_FREQ[1:0]	R/W	0h	**Test signal frequency.** These bits determine the test signal frequency. 00 : Pulsed at $f_{CLK} / 2^{21}$ 01 : Pulsed at $f_{CLK} / 2^{20}$ 10 : Not used 11 : At dc

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9.6.1.4 CONFIG3: Configuration Register 3 (address = 03h) [reset = 40]

This register configures the reference and internal amplifier operation.

Figure 47. CONFIG3: Configuration Register 3

7	6	5	4	3	2	1	0
PDB_REFBUF	1	VREF_4V	0	OPAMP_REF	PDB_OPAMP	0	0
R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15. CONFIG3: Configuration Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
7	PDB_REFBUF	R/W	0h	**PDB_REFBUF: Power-down reference buffer** This bit determines the power-down reference buffer state. 0 : Power-down internal reference buffer 1 : Enable internal reference buffer
6	Reserved	R/W	1h	**Reserved.** Must be set to 1. This bit reads high.
5	VREF_4V	R/W	0h	**Internal reference voltage.** This bit determines the internal reference voltage, VREF. 0 : VREF is set to 2.4 V 1 : VREF is set to 4 V
4	Reserved	R/W	0h	**Reserved.** Must be set to 0. This bit reads low.
3	OPAMP_REF	R/W	0h	**Op amp reference.** This bit determines whether the op amp noninverting input connects to the OPAMPP pin or to the internally-derived supply (AVDD + AVSS) / 2. 0 : Noninverting input connected to the OPAMPP pin 1 : Noninverting input connected to (AVDD + AVSS) / 2
2	PDB_OPAMP	R/W	0h	**Op amp power-down.** This bit powers down the op amp. 0 : Power-down op amp 1 : Enable op amp
1	Reserved	R/W	0h	**Reserved.** Must be set to 0. Reads back as 0.
0	Reserved	R	0h	**Reserved.** Reads back as either 1 or 0.

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9.6.1.5 FAULT: Fault Detect Control Register (address = 04h) [reset = 00h]

This register configures the fault detection operation.

Figure 48. FAULT: Fault Detect Control Register

7	6	5	4	3	2	1	0
COMP_TH[2:0]			0	0	0	0	0
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 16. FAULT: Fault Detect Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	COMP_TH[2:0]	R/W	0h	**Fault detect comparator threshold.** These bits determine the fault detect comparator threshold level setting. See the *Input Out-of-Range Detection* section for a detailed description. **Comparator high-side threshold.** 000 : 95% 001 : 92.5% 010 : 90% 011 : 87.5% 100 : 85% 101 : 80% 110 : 75% 111 : 70% **Comparator low-side threshold.** 000 : 5% 001 : 7.5% 010 : 10% 011 : 12.5% 100 : 15% 101 : 20% 110 : 25% 111 : 30%
4:0	Reserved	R/W	00h	**Reserved.** Must be set to 0. This bit reads low.

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9.6.1.6 CHnSET: Individual Channel Settings (address = 05h to 0Ch) [reset = 10h]

This register configures the power mode, PGA gain, and multiplexer settings for the channels; see the *Input Multiplexer* section for details. CHnSET are similar to CH1SET, corresponding to the respective channels (see Table 10).

Figure 49. CHnSET(1): Individual Channel Settings

7	6	5	4	3	2	1	0
PDn	GAINn[2:0]			0	MUXn[2:0]		
R/W-0h	R/W-1h			R/W-0h	R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

(1) n = 1 to 8.

Table 17. CHnSET: Individual Channel Settings Field Descriptions

Bit	Field	Type	Reset	Description
7	PDn	R/W	0h	**Power-down (n = individual channel number).** This bit determines the channel power mode for the corresponding channel. 0 : Normal operation 1 : Channel power-down
6:4	GAINn[2:0]	R/W	1h	**PGA gain (n = individual channel number).** These bits determine the PGA gain setting. 000 : Do not use 001 : 1 010 : 2 011 : Do not use 100 : 4 101 : 8 110 : 12 111 : Do not use
3	Reserved	R/W	0h	**Reserved.** Must be set to 0. This bit reads low.
2:0	MUXn[2:0]	R/W	0h	**Channel input (n = individual channel number).** These bits determine the channel input selection. 000 : Normal input 001 : Input shorted to (AVDD + AVSS) / 2 (for offset or noise measurements) 010 : Do not use 011 : MVDD for supply measurement 100 : Temperature sensor 101 : Test signal 110 : Do not use 111 : Do not use

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9.6.1.7 FAULT_STATP: Fault Detect Positive Input Status (address = 12h) [reset = 00h]

This register stores the status of whether the positive input on each channel has a fault or not. Faults are determined by comparing the input pin to a threshold set by Table 16; see the *Input Out-of-Range Detection* section for details.

Figure 50. FAULT_STATP: Fault Detect Positive Input Status

7	6	5	4	3	2	1	0
IN8P_FAULT	IN7P_FAULT	IN6P_FAULT	IN5P_FAULT	IN4P_FAULT	IN3P_FAULT	IN2P_FAULT	IN1P_FAULT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read only; -n = value after reset

Table 18. FAULT_STATP: Fault Detect Positive Input Status Field Descriptions

Bit	Field	Type	Reset	Description
7	IN8P_FAULT	R	0h	**IN8P threshold detect.** 0 : Channel 8 positive input pin does not exceed threshold set 1 : Channel 8 positive input pin exceeds threshold set
6	IN7P_FAULT	R	0h	**IN7P threshold detect.** 0 : Channel 7 positive input pin does not exceed threshold set 1 : Channel 7 positive input pin exceeds threshold set
5	IN6P_FAULT	R	0h	**IN6P threshold detect.** 0 : Channel 6 positive input pin does not exceed threshold set 1 : Channel 6 positive input pin exceeds threshold set
4	IN5P_FAULT	R	0h	**IN5P threshold detect.** 0 : Channel 5 positive input pin does not exceed threshold set 1 : Channel 5 positive input pin exceeds threshold set
3	IN4P_FAULT	R	0h	**IN4P threshold detect.** 0 : Channel 4 positive input pin does not exceed threshold set 1 : Channel 4 positive input pin exceeds threshold set
2	IN3P_FAULT	R	0h	**IN3P threshold detect.** 0 : Channel 3 positive input pin does not exceed threshold set 1 : Channel 3 positive input pin exceeds threshold set
1	IN2P_FAULT	R	0h	**IN2P threshold detect.** 0 : Channel 2 positive input pin does not exceed threshold set 1 : Channel 2 positive input pin exceeds threshold set
0	IN1P_FAULT	R	0h	**IN1P threshold detect.** 0 : Channel 1 positive input pin does not exceed threshold set 1 : Channel 1 positive input pin exceeds threshold set

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9.6.1.8 FAULT_STATN: Fault Detect Negative Input Status (address = 13h) [reset = 00h]

This register stores the status of whether the negative input on each channel has a fault or not. Faults are determined by comparing the input pin to a threshold set by Table 16; see the *Input Out-of-Range Detection* section for details.

Figure 51. FAULT_STATN: Fault Detect Negative Input Status

7	6	5	4	3	2	1	0
IN8N_FAULT	IN7N_FAULT	IN6N_FAULT	IN5N_FAULT	IN4N_FAULT	IN3N_FAULT	IN2N_FAULT	IN1N_FAULT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read only; -n = value after reset

Table 19. FAULT_STATN: Fault Detect Negative Input Status Field Descriptions

Bit	Field	Type	Reset	Description
7	IN8N_FAULT	R	0h	**IN8N threshold detect.** 0 : Channel 8 negative input pin does not exceed threshold set 1 : Channel 8 negative input pin exceeds threshold set
6	IN7N_FAULT	R	0h	**IN7N threshold detect.** 0 : Channel 7 negative input pin does not exceed threshold set 1 : Channel 7 negative input pin exceeds threshold set
5	IN6N_FAULT	R	0h	**IN6N threshold detect.** 0 : Channel 6 negative input pin does not exceed threshold set 1 : Channel 6 negative input pin exceeds threshold set
4	IN5N_FAULT	R	0h	**IN5N threshold detect.** 0 : Channel 5 negative input pin does not exceed threshold set 1 : Channel 5 negative input pin exceeds threshold set
3	IN4N_FAULT	R	0h	**IN4N threshold detect.** 0 : Channel 4 negative input pin does not exceed threshold set 1 : Channel 4 negative input pin exceeds threshold set
2	IN3N_FAULT	R	0h	**IN3N threshold detect.** 0 : Channel 3 negative input pin does not exceed threshold set 1 : Channel 3 negative input pin exceeds threshold set
1	IN2N_FAULT	R	0h	**IN2N threshold detect.** 0 : Channel 2 negative input pin does not exceed threshold set 1 : Channel 2 negative input pin exceeds threshold set
0	IN1N_FAULT	R	0h	**IN1N threshold detect.** 0 : Channel 1 negative input pin does not exceed threshold set 1 : Channel 1 negative input pin exceeds threshold set

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9.6.1.9 GPIO: General-Purpose IO Register (address = 14h) [reset = 0Fh]

This register controls the format and state of the four GPIO pins.

Figure 52. GPIO: General-Purpose IO Register

7	6	5	4	3	2	1	0
GPIOD[4:1]				GPIOC[4:1]			
R/W-0h				R/W-Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 20. GPIO: General-Purpose IO Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	GPIOD[4:1]	R/W	0h	**GPIO data.** These bits are used to read and write data to the GPIO ports. When reading the register, the data returned correspond to the state of the GPIO external pins, whether they are programmed as inputs or outputs. As outputs, a write to the GPIOD sets the output value. As inputs, a write to the GPIOD has no effect.
3:0	GPIOC[4:1]	R/W	Fh	**GPIO control (corresponding to GPIOD).** These bits determine if the corresponding GPIOD pin is an input or output. 0 : Output 1 : Input

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Unused Inputs and Outputs

Power down unused analog inputs and connect them directly to AVDD.

Power down the Bias amplifier if unused and float OPAMPOUT and OPAMPN. Tie OPAMPP directly to AVSS or leave floating if unused.

Tie TESTN and TESTP to AVDD through individual 10-kΩ resistors or leave them floating if unused and the internal test signal is not used. If the internal test signal is used, leave TESTP and TESTN floating. If an external test signal is used, connect to external test circuitry.

Do not float unused digital inputs because excessive power-supply leakage current might result. Set the two-state mode setting pins high to DVDD or low to DGND through ≥10-kΩ resistors.

Pull $\overline{\text{DRDY}}$ to supply using weak pull-up resistor if unused.

If not daisy-chaining devices, tie DAISYIN directly to DGND.

10.1.2 Setting the Device Up for Basic Data Capture

This section outlines the procedure to configure the device in a basic state and capture data. This procedure is intended to put the device in a data sheet condition to check if the device is working properly in the user system. It is recommended that this procedure be followed initially to get familiar with the device settings. When this procedure is verified, the device can be configured as needed. For details on the timings for commands refer to the appropriate sections in the data sheet. The flow chart of Figure 53 details the initial ADS131E0x configuration and setup.

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Application Information (continued)

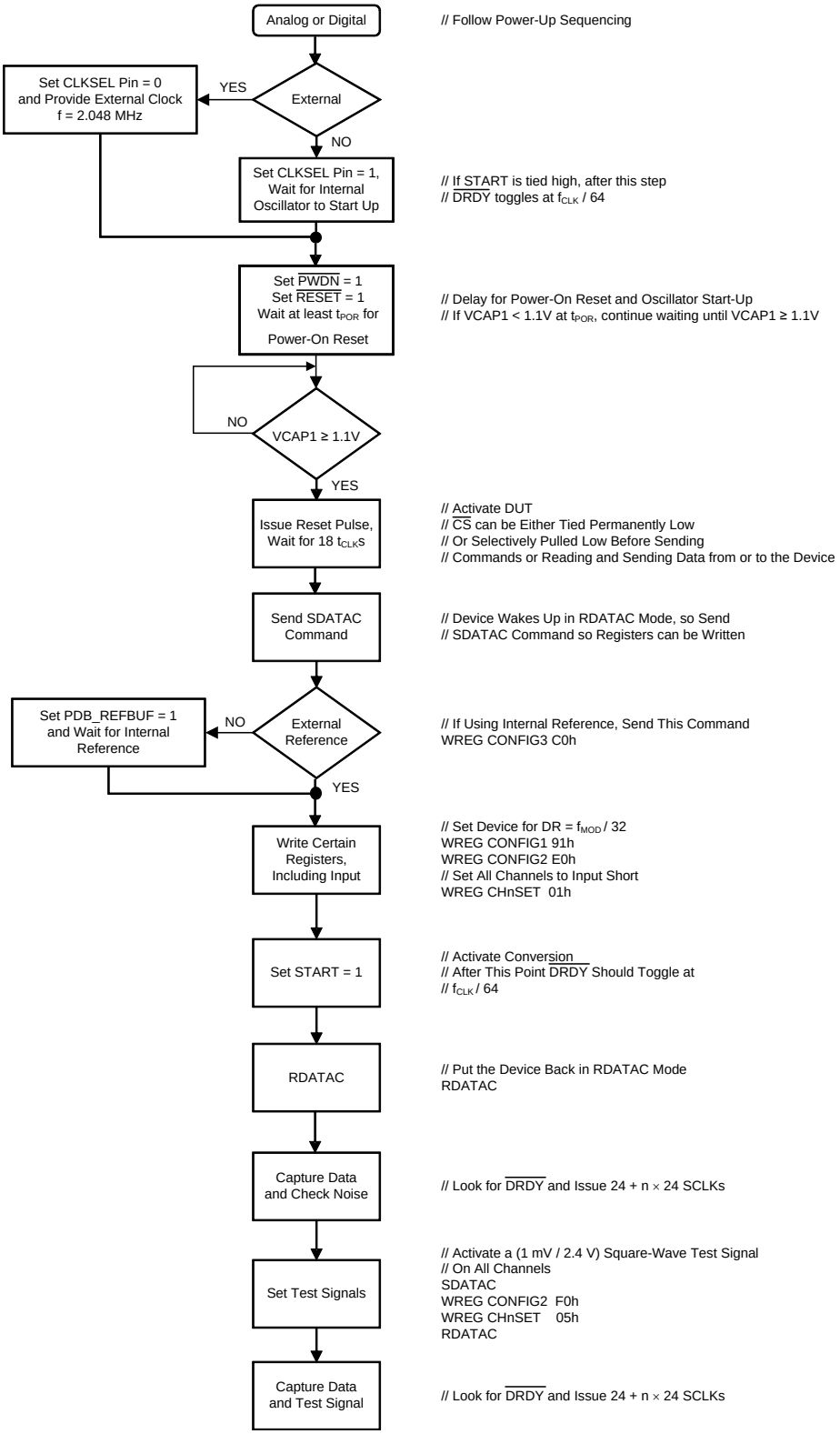

Figure 53. Initial Flow at Power Up

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Application Information (continued)

10.1.3 Multiple Device Configuration

The ADS131E0x provides configuration flexibility when multiple devices are used in a system. The serial interface typically needs four signals: DIN, DOUT, SCLK, and $\overline{CS}$. With one additional chip select signal per device, multiple devices can be operated on the same SPI bus. The number of signals needed to interface to *N* devices is 3 + *N*.

10.1.3.1 Synchronizing Multiple Devices

When using multiple devices, the devices can be synchronized using the START signal. The delay time from the rising edge of the START signal to the falling edge of the $\overline{DRDY}$ signal is fixed for a given data rate (see the *Start* section for more details on the settling times). Figure 54 shows the behavior of two devices when synchronized with the START signal.

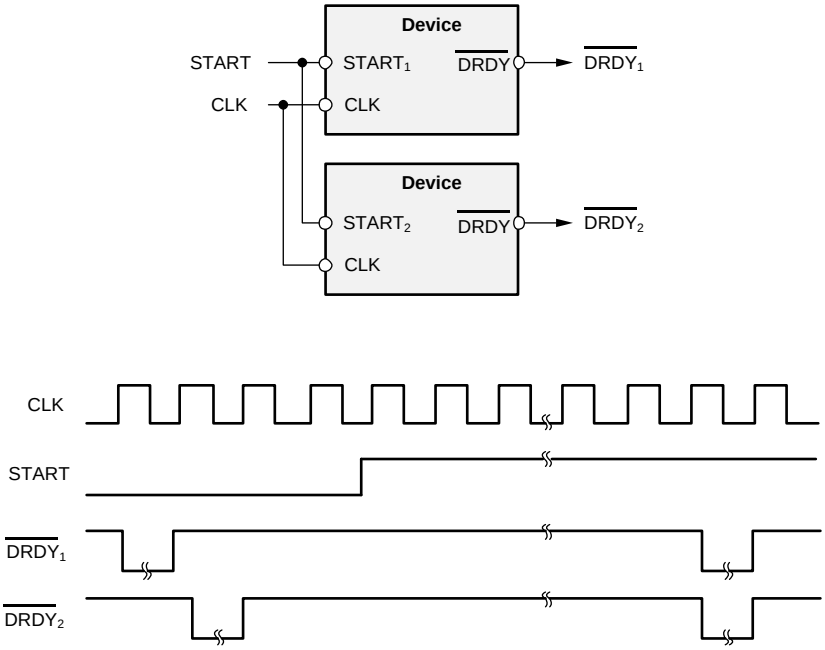

Figure 54. Synchronizing Multiple Converters

To use the internal oscillator in a daisy-chain configuration, one device must be set as the master for the clock source with the internal oscillator enabled (CLKSEL pin = 1) and the internal oscillator clock must be brought out of the device by setting the $\overline{CLK_EN}$ register bit to 1. The master device clock is used as the external clock source for the other devices.

There are two ways to connect multiple devices with an optimal number of interface pins: standard configuration and daisy-chain configuration.

10.1.3.2 Standard Configuration

Figure 55a shows a configuration with two ADS131E0x devices cascaded. Together, the devices create a system with up to 16 channels. DOUT, SCLK, and DIN are shared. Each device has its own chip select. When a device is not selected by the corresponding $\overline{CS}$ being driven to logic 1, the DOUT pin of this device is high-impedance. This structure allows the other device to take control of the DOUT bus. This configuration method is suitable for the majority of applications where extra I/O pins are available.

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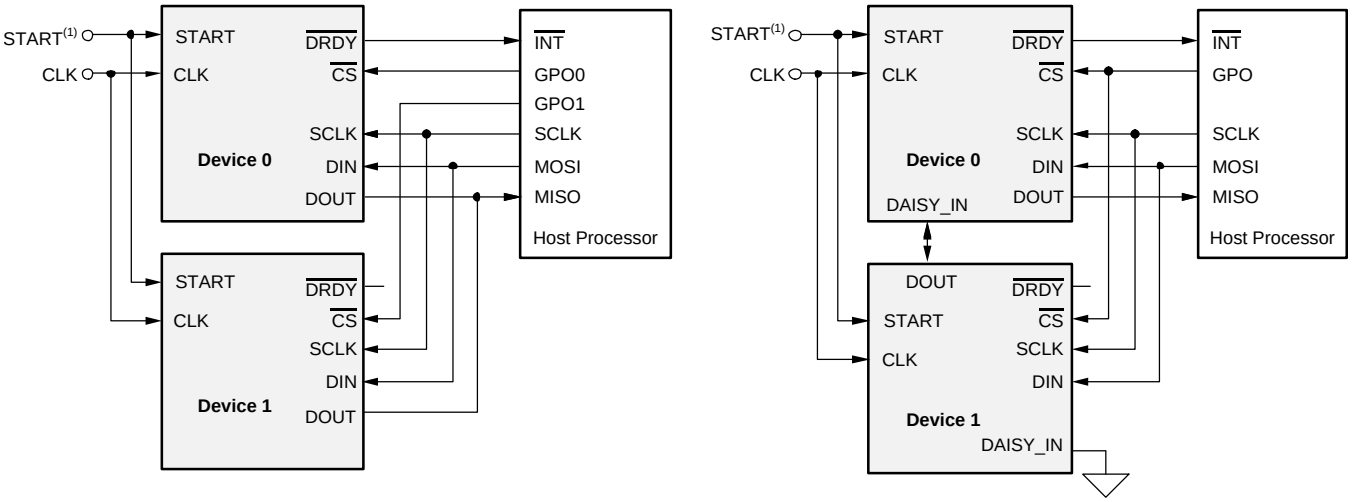
Application Information (continued)

10.1.3.3 Daisy-Chain Configuration

Daisy-chain mode is enabled by setting the DAISY_IN bit in the CONFIG1 register. Figure 55b shows the daisy-chain configuration. In this mode SCLK, DIN, and $\overline{CS}$ are shared across multiple devices. The DOUT pin of device 1 is connected to the DAISY_IN pin of device 0, thereby creating a daisy-chain for the data. Connect the DAISY_IN pin of device 1 to DGND if not used. The daisy-chain timing requirements for the SPI interface are illustrated in Figure 2. Data from the ADS131E0x device 0 appear first on DOUT, followed by a *don't care* bit, and then the status and data words from the ADS131E0x device 1.

The internal oscillator output cannot be enabled because all devices in the chain operate by sharing the same DIN pin, thus an external clock must be used.



a) Standard Configuration

b) Daisy-Chain Configuration

(1) To reduce pin count, set the START pin low and use the START command to synchronize and start conversions.

Figure 55. Multiple Device Configurations

There are several items to be aware of when using daisy-chain mode:

1. One extra SCLK must be issued between each data set (see Figure 56)
2. All devices are configured to the same register values because the $\overline{CS}$ signal is shared
3. Device register readback is only valid for device 0 in the daisy-chain. Only ADC conversion data can be read back from device 1 through device *N*, where *N* is the last device in the chain.

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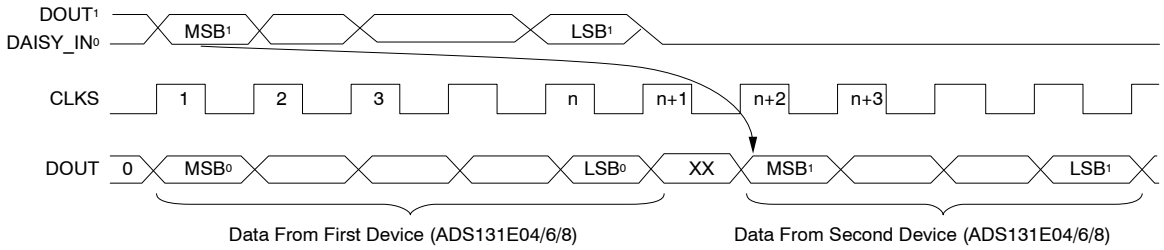
Application Information (continued)

The more devices in the chain, the more challenging adhering to setup and hold times becomes. A star-pattern connection of SCLK to all devices, minimizing the trace length of DOUT, and other printed circuit board (PCB) layout techniques helps to mitigate this challenge with signal delays. Placing delay circuits (such as buffers) between DOUT and DAISY_IN are options to help reduce signal delays. One other option is to insert a *D* flip-flop between DOUT and DAISY_IN clocked on an inverted SCLK. Figure 56 shows a timing diagram for daisy-chain mode.



NOTE: n = (number of channels) × (resolution) + 24 bits. The number of channels is 8. Resolution is 16 bits or 24 bits.

Figure 56. Daisy-Chain Data Word

The maximum number of devices that can be daisy-chained depends on the data rate that the devices are operated at. The maximum number of devices can be calculated with Equation 10.

$$N_{DEVICES} = \frac{f_{SCLK}}{f_{DR}\,(N_{BITS})(N_{CHANNELS}) + 24} \quad (10)$$

where:

- N_{BITS} = device resolution (depends on DR[2:0] setting)
- $N_{CHANNELS}$ = number of channels powered up in the device

For example, when the ADS131E0x is operated in 24-bit, 8-kSPS data rate with f_{SCLK} = 10 MHz, up to six devices can be daisy-chained together.

10.1.4 Power Monitoring Specific Applications

All channels of the ADS131E0x are exactly identical, yet independently configurable, thus giving the user the flexibility of selecting any channel for voltage or current monitoring. An overview of a system configured to monitor voltage and current is illustrated in Figure 57. Also, the simultaneously sampling capability of the device allows the user to monitor both the current and the voltage at the same time. The full-scale differential input voltage of each channel is determined by the PGA gain setting (see the *CHnSET: Individual Channel Settings* section) for the respective channel and V_{REF} (see the *CONFIG3: Configuration Register 3* section).

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Application Information (continued)

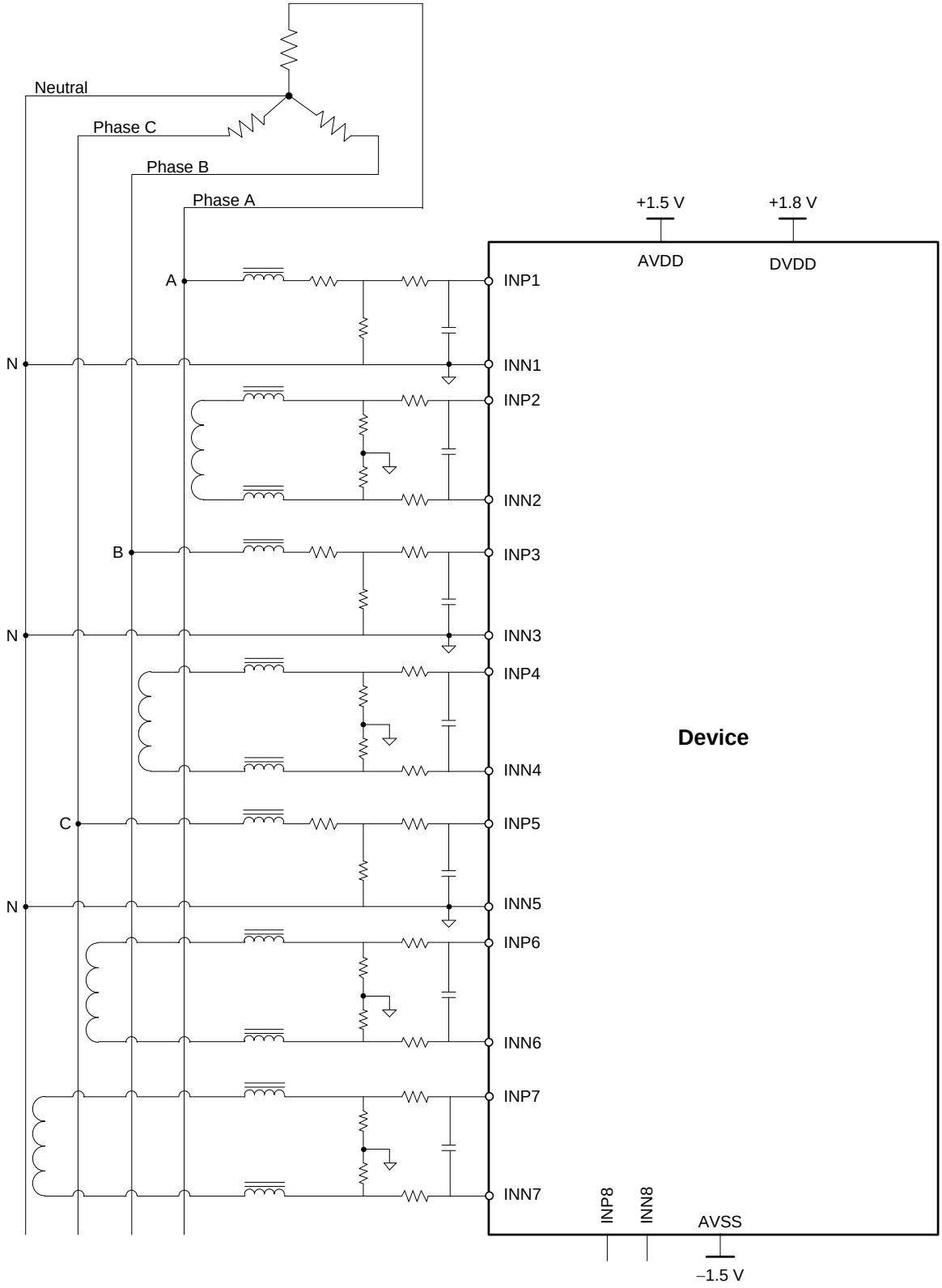

Figure 57. Overview of a Power-Monitoring System

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Application Information (continued)

10.1.5 Current Sensing

Figure 58 illustrates a simplified diagram of typical configurations used for current sensing with a Rogowski coil, current transformer (CT), or an air coil that outputs a current or voltage. In the case of a current output transformer, the burden resistors (R1) are used for current-to-voltage conversion. The output of the burden resistors is connected to the ADS131E0x INxP and INxN inputs through an antialiasing RC filter for current sensing. In the case of a voltage output transformer for current sensing (such as certain types of Rogowski coils), the output terminals of the transformer are directly connected to the ADS131E0x INxP and INxN inputs through an antialiasing RC filter. The input network must be biased to mid-supply if using a unipolar-supply analog configuration (AVSS = 0 V, AVDD = 2.7 V to 5.5 V). The common-mode bias voltage [(AVDD + AVSS) / 2] can be obtained from the ADS131E0x by either configuring the internal op amp in a unity-gain configuration using the R_F resistor and setting the OPAMP_REF bit of the CONFIG3 register to 1, or generated externally with a resistor divider network between the positive and negative supplies.

Select the value of resistor R1 for the current output transformer and turns ratio of the transformer such that the ADS131E0x full-scale differential input voltage range is not exceeded. Likewise, select the output voltage for the voltage output transformer to not exceed the full-scale differential input voltage range. In addition, the selection of the resistors (R1 and R2) and turns ratio must not saturate the transformer over the full operating dynamic range. Figure 58a illustrates differential input current sensing and Figure 58b illustrates single-ended input voltage sensing. Use separate external op amps to source and sink current because the internal op amp has very limited current sink and source capability. Additionally, separate op amps for each channel help isolate individual phases from one another to limit crosstalk.

10.1.6 Voltage Sensing

Figure 59 illustrates a simplified diagram of commonly-used differential and single-ended methods of voltage sensing. A resistor divider network is used to step down the line voltage to within the acceptable ADS131E0x input range and then connect to the inputs (INxP and INxN) through an antialiasing RC filter formed by resistor R3 and capacitor C. The common-mode bias voltage [(AVDD + AVSS) / 2] can be obtained from the ADS131E0x by either configuring the internal op amp in a unity-gain configuration using the R_F resistor and setting the OPAMP_REF bit of the CONFIG3 register, or generated externally by using a resistor divider network between the positive and negative supplies.

In either of the cases illustrated in Figure 59 (Figure 59a for a differential input and Figure 59b for a single-ended input), the line voltage is divided down by a factor of [R2 / (R1 + R2)]. Values of R1 and R2 must be carefully chosen so that the voltage across the ADS131E0x inputs (INxP and INxN) does not exceed the range of the ADS131E0x over the full operating dynamic range. Use separate external op amps to source and sink current because the internal op amp has very limited current sink and source capability. Additionally, separate op amps for each channel help isolate individual phases from one another to limit crosstalk.

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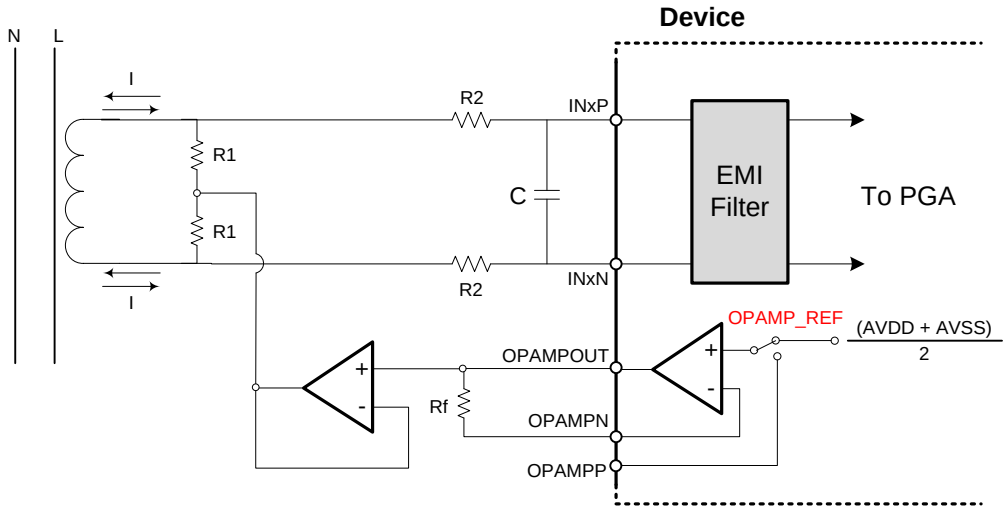
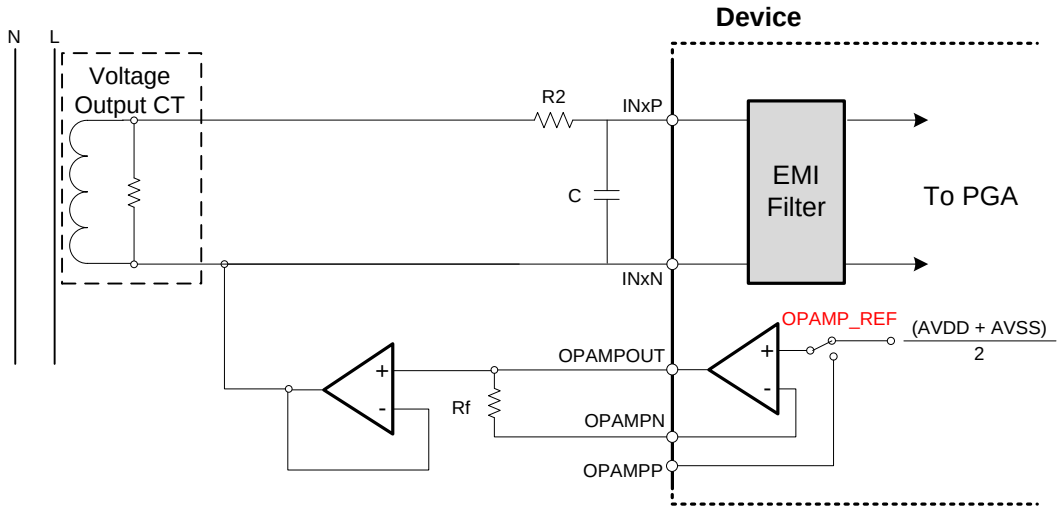
Application Information (continued)



(a) Current Output CT with Differential Input



(b) Voltage Output CT with Single-Ended Input

Figure 58. Simplified Current-Sensing Connections

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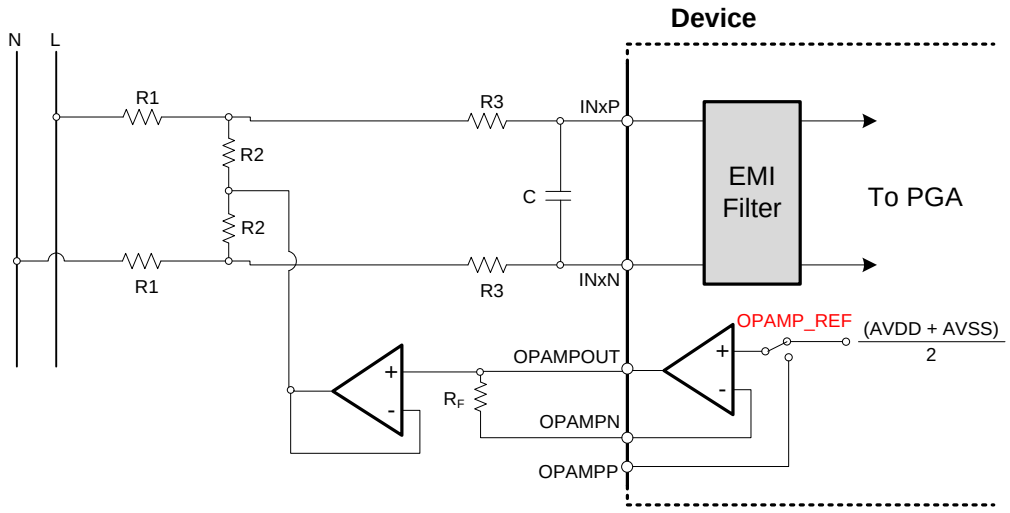
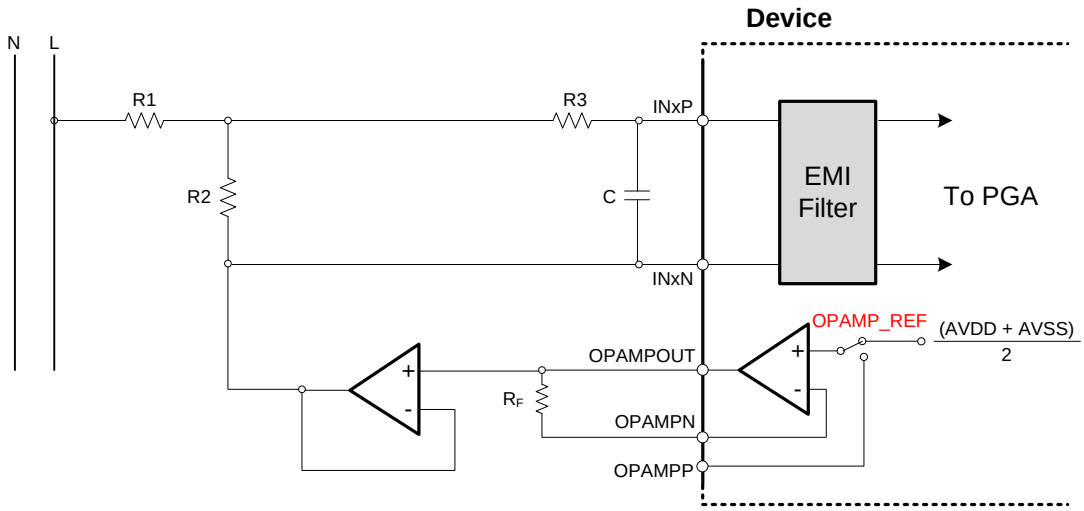
Application Information (continued)



(a) Voltage Sensing with Differential Input



(b) Voltage Sensing with Single-Ended Input

Figure 59. Simplified Voltage-Sensing Connections

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10.2 Typical Application

Figure 60 shows the ADS131E0x being used as part of an electronic trip unit (ETU) in a circuit breaker or protection relay. Delta-sigma (ΔΣ), analog-to-digital converters (ADCs), such as the ADS131E0x, are ideal for this application because these devices provide a wide dynamic range.

The system measures voltages and currents output from a breaker enclosure. In this example, the first three inputs measure line voltage and the remaining five inputs measure line current from the secondary winding of a current transformer (CT). A voltage divider steps down the voltage from the output of the breaker. Several resistors are used to break up power consumption and are used as a form of fault protection against any potential resistor short-circuit. After the voltage step down, RC filters are used for antialiasing and diodes protect the inputs from overrange.

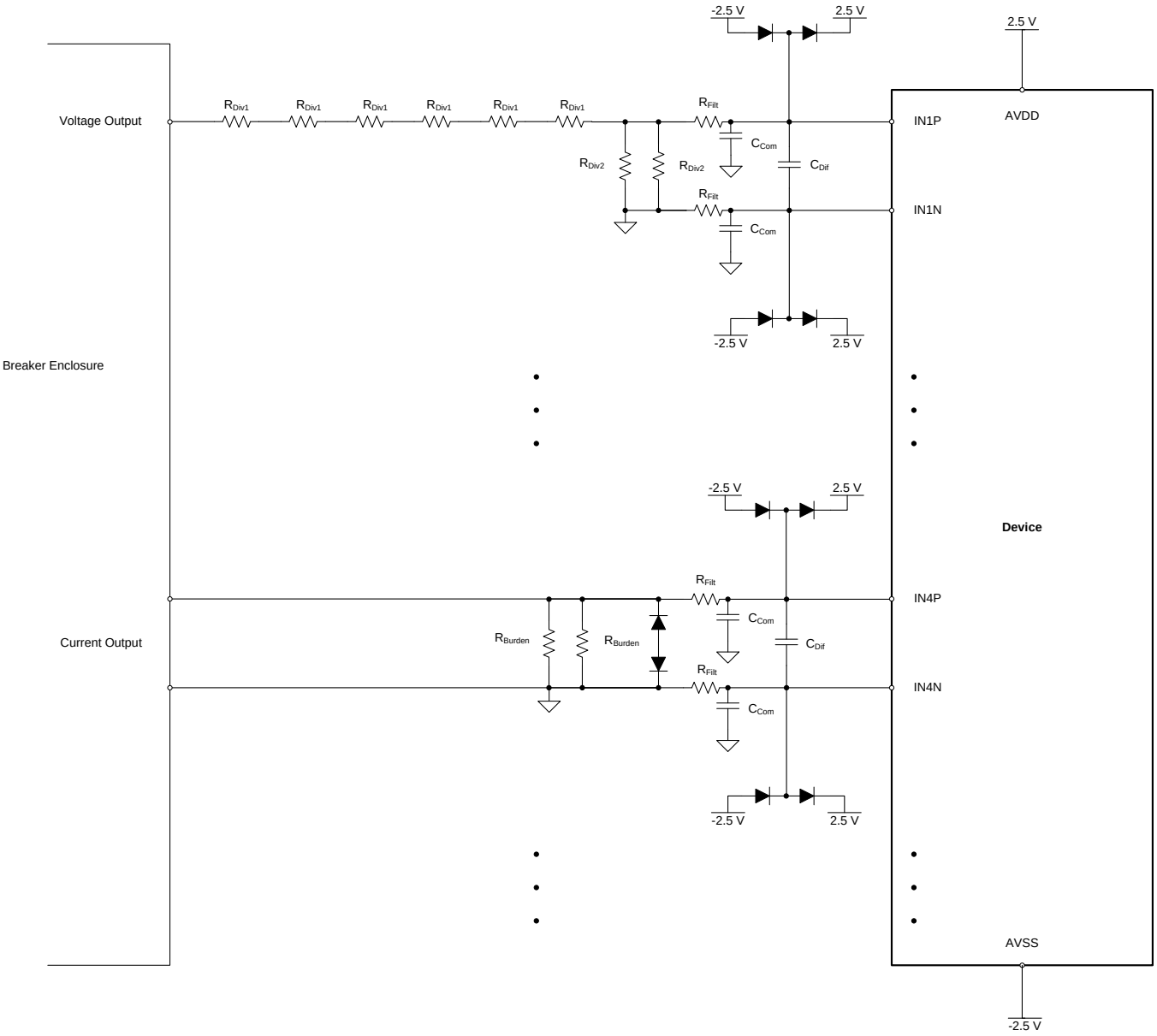

Figure 60. ETU Block Diagram: High-Resolution and Fast Power-Up Analog Front-End for Air Circuit Breaker or Molded Case Circuit Breaker and Protection Relay

10.2.1 Design Requirements

Table 21 summarizes the design requirements for the circuit breaker front-end application.

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Table 21. ETU Circuit Breaker Design Requirements

DESIGN PARAMETER	VALUE
Number of voltage inputs	3
Voltage input range	10 V to 750 V
Number of current inputs	5
Current input range	50 mA to 25 A
Dynamic range with fixed gain	> 500:1
Accuracy	±1%

10.2.2 Detailed Design Procedure

The line voltage is stepped down to a voltage range within the measurable range of the ADC. The reference voltage determines the range in which the ADC can measure signals. The ADS131E0x has two integrated low-drift reference voltage options: 2.4 V and 4 V.

Equation 11 describes the transfer function for the voltage divider at the input in Figure 60. Using multiple series resistors, R_{DIV1}, and multiple parallel resistors, R_{DIV2}, allows for power and heat to be dissipated among several circuit elements and serves as protection against a potential short-circuit across a single resistor. The number of resistors trade off with nominal accuracy because each additional element introduces an additional source of tolerance.

$$V_{IN} = V_{Phase} \times \left(\frac{0.5 \times R_{Div2}}{6 \times R_{Div1} + 0.5 \times R_{Div2}} \right) \tag{11}$$

The step-down resistor, R_{Div2}, dominates the measurement error produced by the resistor network. Using input PGAs on the ADS131E0x helps to mitigate this error source by allowing R_{Div2} to be made smaller and then amplifying the signal to near full-scale using the ADS131E0x PGA.

For this design, R_{Div1} is set to 200 kΩ and R_{Div2} is set to 2.4 kΩ to provide proper signal attenuation at a sufficient power level across each resistor. The input saturates at values greater than ±750 V when using the ADS131E0x internal 2.4-V reference and a PGA gain of 2.

The ADS131E0x measures the line current by creating a voltage across the burden resistance (R_{Burden} in Figure 60) in parallel with the secondary winding of a CT. As with the voltage measurement front-end, multiple resistors (R_{Div1}) that are used to step down a voltage share the duty of dissipating power. In this design, R_{BURDEN} is set to 33 Ω. Used with a 1:500 turns ratio CT, the ADC input saturates with a line current over 25 A when the ADC is configured using the internal 2.4-V reference and a PGA gain of 2.

Diodes protect the ADS131E0x inputs from overvoltage and current. Diodes on each input shunt to either supply if the input voltage exceeds the safe range for the device. On current inputs, a diode shunts the inputs if current on the secondary winding of the CT threatens to damage the device.

The combination of R_{Filt}, C_{Com}, and C_{Dif} form the antialiasing filters for each of the inputs. The differential capacitor C_{Dif} improves the common-mode rejection of the system by sharing its tolerance between the positive and negative input. The antialiasing filter requirement is not strict because the nature of a ΔΣ converter (with oversampling and digital filter) attenuates a significant proportion of out-of-band noise. In addition, the input PGAs have intentionally low bandwidth to provide additional antialiasing. The component values used in this design are R_{Filt} = 1 kΩ, C_{Com} = 47 pF, and C_{Dif} = 0.015 μF. This first-order filter produces a relatively flat frequency response beyond 2 kHz, capable of measuring greater than 30 harmonics at a 50-Hz or 60-Hz fundamental frequency. The 3-dB cutoff frequency of the filter is 5.3 kHz for each input channel.

Each analog system block introduces errors from input to output. Protection CTs in the 5P accuracy class can introduce as much as ±1% current error from input to output. CTs in the 10P accuracy class can introduce as much as ±3% error. The burden resistor also introduces errors in the form of resistor tolerance and temperature drift. For the voltage input, error comes from the divider network in the form of resistor tolerance and temperature drift. Finally, the converter introduces errors in the form of offset error, gain error, and reference error. All of these specifications can drift over temperature.

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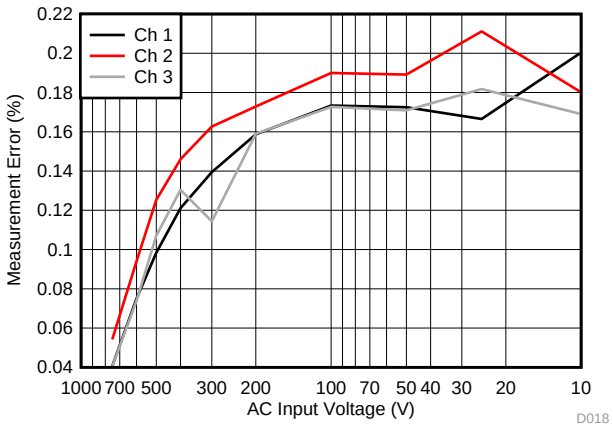
10.2.3 Application Curves

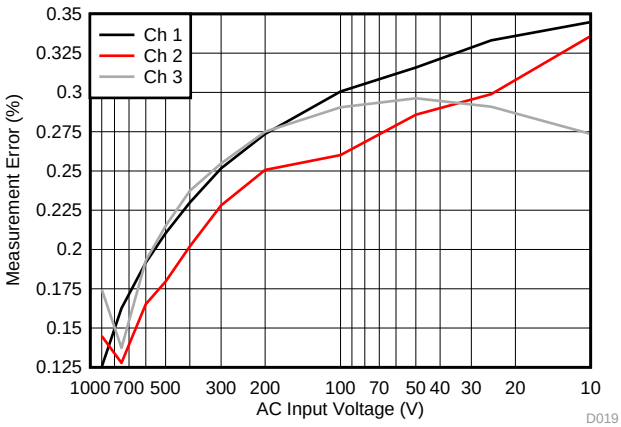
Accuracy is measured using a system designed in a similar way to that illustrated in Figure 60. The CT used for the current input is CT1231 (a 0.3 class, solid core, 5:2500 turns transformer). In each case, data are taken for three channels over one cycle of the measured waveform and the RMS input-referred signal is compared to the output to calculate the error. The equation used to derive the measurement error is shown in Equation 12. Data are taken using both the 2.4-V and 4-V internal reference voltages. In all cases, measured accuracy is within ±1%.

$$\text{Measurement Accuracy}(\%) = \left(\frac{\text{Measured} - \text{Actual}}{\text{Actual}}\right) \times 100 \tag{12}$$



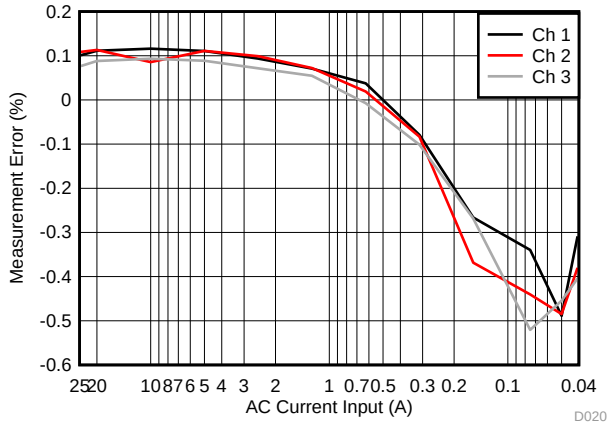
One 50-Hz line cycle , 4-kSPS data rate, 80 samples, gain = 2, V_{REF} = 2.4 V, measurement accuracy is absolute value

Figure 61. Input Voltage vs ADC Measurement Error: 2.4-V Reference



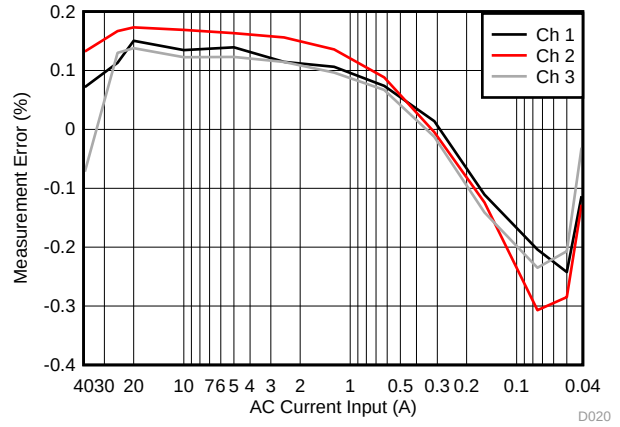
One 50-Hz line cycle , 4-kSPS data rate, 80 samples, gain = 2, V_{REF} = 4 V, measurement accuracy is absolute value

Figure 62. Input Voltage vs ADC Measurement Error: 4-V Reference



One 50-Hz line cycle , 4-kSPS data rate, 80 samples, gain = 2, V_{REF} = 2.4 V

Figure 63. Input Current vs ADC Measurement Error: 2.4-V Reference



One 50-Hz line cycle , 4-kSPS data rate, 80 samples, gain = 2, V_{REF} = 4 V

Figure 64. Input Current vs ADC measurement Error: 4-V Reference

TI Precision Designs

For a step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, see *High Resolution, Fast Startup Analog Front End for Air Circuit Breaker Design Guide* (TIDUB80).

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11 Power Supply Recommendations

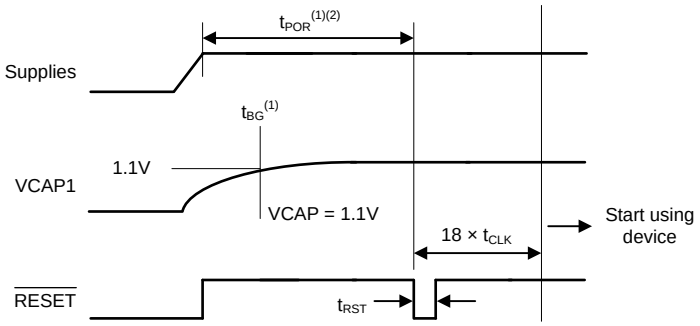
11.1 Power-Up Timing

Before device power up, all digital and analog inputs must be low. At the time of power up, keep all of these signals low until the power supplies have stabilized, as shown in Figure 65.

Allow time for the supply voltages to reach their final value, and then begin supplying the master clock signal to the CLK pin. Wait for time t_{POR}, then transmit a reset pulse using either the RESET pin or RESET command to initialize the digital portion of the chip. Issue the reset after t_{POR} or after the VCAP1 voltage is greater than 1.1 V, whichever time is longer. Note that:

- t_{POR} is described in Table 22.
- The VCAP1 pin charge time is set by the RC time constant set by the capacitor value on VCAP1; see Figure 28.

After releasing RESET, the configuration registers must be programmed (see the *CONFIG1: Configuration Register 1 (address = 01h) [reset = 91h]* subsection of the *Register Map* section for details) to the desired settings. The power-up sequence timing is shown in Table 22.



(1) Timing to reset pulse is t_{POR} or after t_{BG}, whichever is longer.

(2) When using an external clock, t_{POR} timing does not start until CLK is present and valid.

Figure 65. Power-Up Timing Diagram

Table 22. Timing Requirements for Figure 65

		MIN	MAX	UNIT
t_{POR}	Wait after power up until reset	2^{18}		t_{CLK}
t_{RST}	Reset low duration	1		t_{CLK}

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11.2 Recommended External Capacitor Values

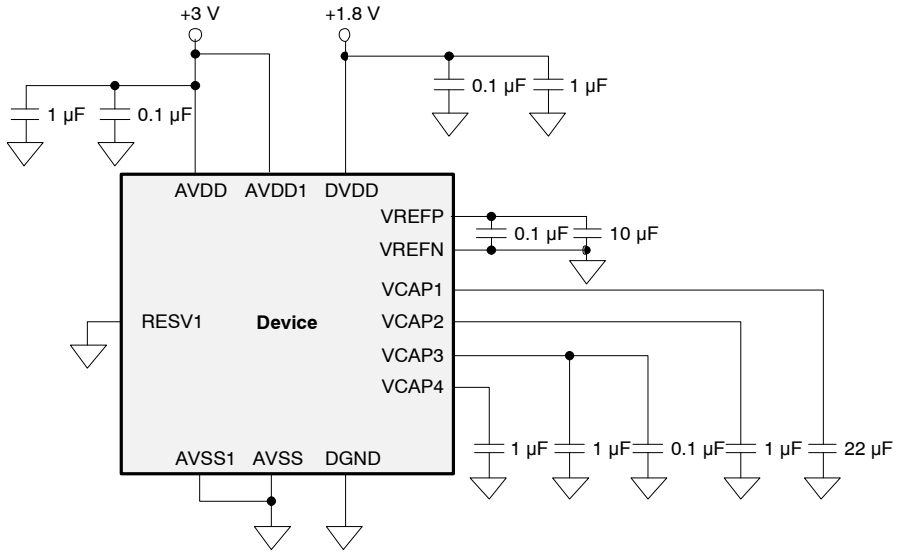
The ADS131E0x power-up time is set by the time required for the critical voltage nodes to settle to their final values. The analog supplies (AVDD and AVSS), digital supply (DVDD), and internal node voltages (VCAPx pins) must be up and stable when the data converter samples are taken to ensure performance. The combined current sourcing capability of the supplies and size of the bypass capacitors dictate the ramp rate of AVDD, AVSS, and DVDD. The VCAPx voltages are charged internally using the supply voltages. Table 23 lists the internal node voltages, their function, and recommended capacitor values to optimize the power-up time.

Table 23. Recommended External Capacitor Values

PIN		FUNCTION	RECOMMENDED CAPACITOR VALUE
NAME	NO.		
VCAP1	28	Band-gap voltage for the ADC	22 µF to AVSS
VCAP2	30	Modulator common-mode	1 µF to AVSS
VCAP3	55	PGA charge pump	0.1 µF || 1 µF to AVSS
VCAP4	26	Reference common-mode	1 µF to AVSS
VREFP	24	Reference voltage after the internal buffer	0.1 µF || 10 µF to AVSS
AVDD	19, 21, 22, 56, 59	Analog supply	0.1 µF || 1 µF each to AVSS
AVDD1	54	Internal PGA charge pump analog supply	0.1 µF || 1 µF to AVSS1
DVDD	48, 50	Digital supply	0.1 µF || 1 µF each to DGND

11.3 Device Connections for Unipolar Power Supplies

Figure 66 shows the ADS131E0x connected to a unipolar supply. In this example, the analog supply (AVDD) is referenced to the analog ground (AVSS) and the digital supply (DVDD) is referenced to the digital ground (DGND). The ADS131E0x supports an analog supply range of AVDD = 2.7 V to 5.25 V when operated in unipolar supply mode.



NOTE: Place the supply, reference, and VCAP1 to VCAP4 capacitors as close to the package as possible.

Figure 66. Unipolar Power Supply Operation

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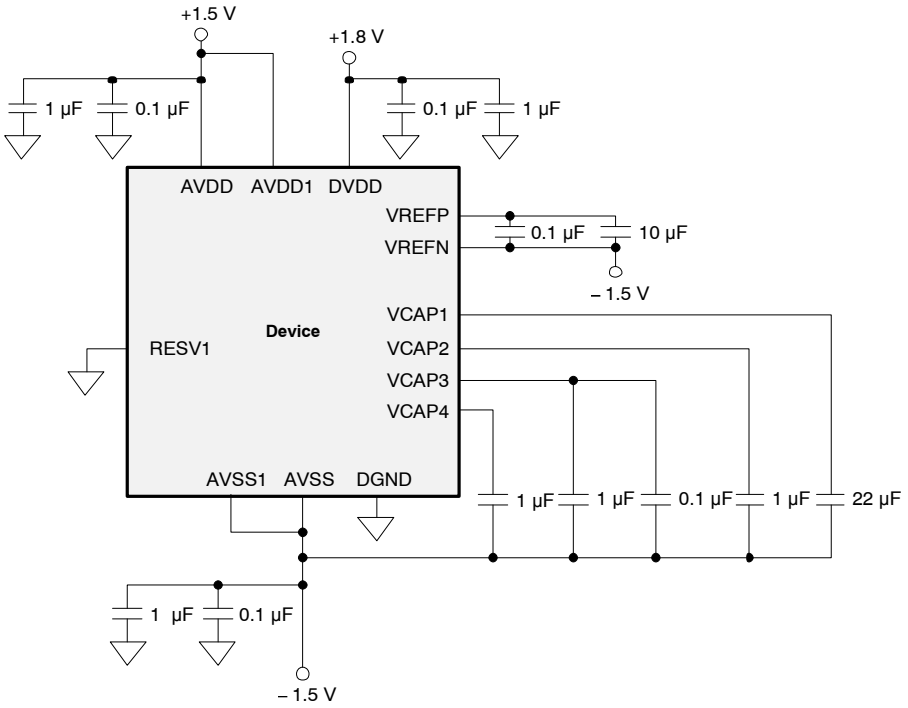
11.4 Device Connections for Bipolar Power Supplies

Figure 67 shows the ADS131E0x connected to a bipolar supply. In this example, the analog supply (AVDD) is referenced to the analog ground (AVSS) and the digital supply (DVDD) is referenced to the digital ground (DGND). The ADS131E0x supports an analog supply range of AVDD and AVSS = ±1.5 V to ±2.5 V when operated in bipolar supply mode.



NOTE: Place the supply, reference, and VCAP1 to VCAP4 capacitors as close to the package as possible.

Figure 67. Bipolar Power Supply Operation

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12 Layout

12.1 Layout Guidelines

TI recommends employing best design practices when laying out a printed-circuit board (PCB) for both analog and digital components. This recommendation generally means that the layout separates analog components (such as ADCs, amplifiers, references, digital-to-analog converters (DACs), and analog MUXs) from digital components (such as microcontrollers, complex programmable logic devices (CPLDs), field-programmable gate arrays (FPGAs), radio frequency (RF) transceivers, universal serial bus (USB) transceivers, and switching regulators). An example of good component placement is shown in Figure 68. Although Figure 68 provides a good example of component placement, the best placement for each application is unique to the geometries, components, and PCB fabrication capabilities employed. That is, there is no single layout that is perfect for every design and careful consideration must always be used when designing with any analog component.

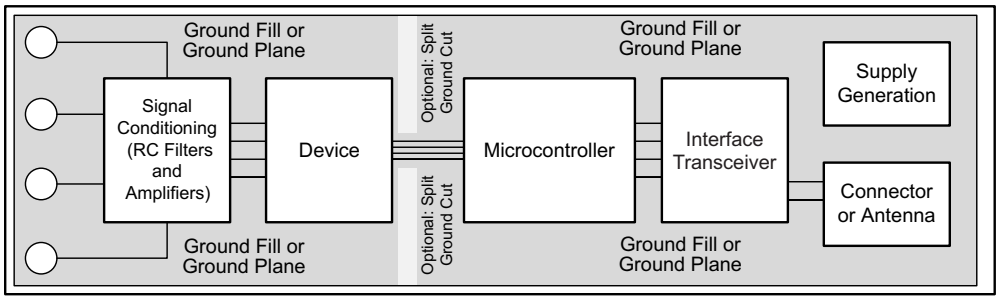

Figure 68. System Component Placement

The following outlines some basic recommendations for the layout of the ADS131E0x to get the best possible performance of the ADC. A good design can be ruined with a bad circuit layout.

- Separate analog and digital signals. To start, partition the board into analog and digital sections where the layout permits. Route digital lines away from analog lines. This configuration prevents digital noise from coupling back into analog signals.
- The ground plane can be split into an analog plane (AGND) and digital plane (DGND), but is not necessary. Place digital signals over the digital plane, and analog signals over the analog plane. As a final step in the layout, the split between the analog and digital grounds must be connected together at the ADC.
- Fill void areas on signal layers with ground fill.
- Provide good ground return paths. Signal return currents flow on the path of least impedance. If the ground plane is cut or has other traces that block the current from flowing right next to the signal trace, then the current must find another path to return to the source and complete the circuit. If current is forced into a longer path, the chances that the signal radiates increases. Sensitive signals are more susceptible to EMI interference.
- Use bypass capacitors on supplies to reduce high-frequency noise. Do not place vias between bypass capacitors and the active device. Placing the bypass capacitors on the same layer as close to the active device yields the best results.
- Analog inputs with differential connections must have a capacitor placed differentially across the inputs. The differential capacitors must be of high quality. The best ceramic chip capacitors are C0G (NPO), which have stable properties and low noise characteristics.

12.2 Layout Example

Figure 69 shows an example layout of the ADS131E0x requiring a minimum of two PCB layers. The example circuit is shown for either a unipolar analog supply connection or a bipolar analog supply connection. In this example, polygon pours are used as supply connections around the device. If a three- or four-layer PCB is used, the additional inner layers can be dedicated to route power traces. The PCB is partitioned with analog signals routed from the left, digital signals routed to the right, and power routed above and below the device.

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Layout Example (continued)

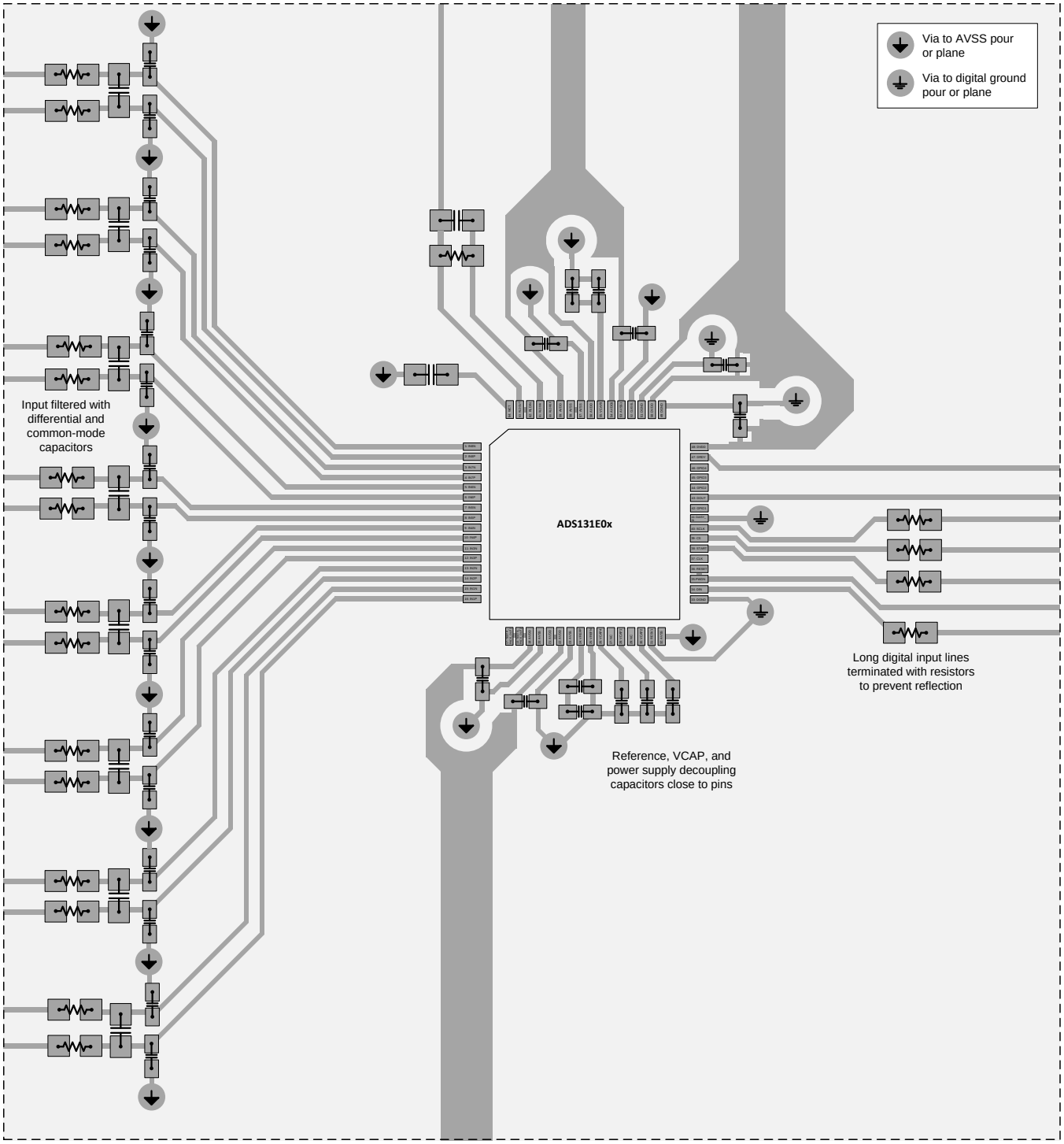

Figure 69. ADS131E0x Layout Example

13 器件和文档支持

13.1 器件支持

13.1.1 Third-Party Products Disclaimer

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13.2 相关链接

表 24 列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，以及样片或购买的快速访问。

表 **24.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持与社区
ADS131E04	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ADS131E06	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ADS131E08	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

13.3 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

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13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS131E04IPAG	Active	Production	TQFP (PAG) | 64	160 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ADS131E04
ADS131E04IPAG.A	Active	Production	TQFP (PAG) | 64	160 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ADS131E04
ADS131E04IPAG.B	Active	Production	TQFP (PAG) | 64	160 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ADS131E04
ADS131E04IPAGR	Active	Production	TQFP (PAG) | 64	1500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ADS131E04
ADS131E04IPAGR.A	Active	Production	TQFP (PAG) | 64	1500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ADS131E04
ADS131E04IPAGR.B	Active	Production	TQFP (PAG) | 64	1500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ADS131E04
ADS131E06IPAG	Active	Production	TQFP (PAG) | 64	160 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ADS131E06
ADS131E06IPAG.A	Active	Production	TQFP (PAG) | 64	160 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ADS131E06
ADS131E06IPAG.B	Active	Production	TQFP (PAG) | 64	160 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ADS131E06
ADS131E06IPAGR	Active	Production	TQFP (PAG) | 64	1500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ADS131E06
ADS131E06IPAGR.A	Active	Production	TQFP (PAG) | 64	1500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ADS131E06
ADS131E06IPAGR.B	Active	Production	TQFP (PAG) | 64	1500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ADS131E06
ADS131E06IPAGRG4	Active	Production	TQFP (PAG) | 64	1500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ADS131E06
ADS131E06IPAGRG4.A	Active	Production	TQFP (PAG) | 64	1500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ADS131E06
ADS131E06IPAGRG4.B	Active	Production	TQFP (PAG) | 64	1500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ADS131E06
ADS131E08IPAG	Active	Production	TQFP (PAG) | 64	160 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ADS131E08
ADS131E08IPAG.A	Active	Production	TQFP (PAG) | 64	160 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ADS131E08
ADS131E08IPAG.B	Active	Production	TQFP (PAG) | 64	160 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ADS131E08
ADS131E08IPAGR	Active	Production	TQFP (PAG) | 64	1500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ADS131E08
ADS131E08IPAGR.A	Active	Production	TQFP (PAG) | 64	1500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ADS131E08
ADS131E08IPAGR.B	Active	Production	TQFP (PAG) | 64	1500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ADS131E08

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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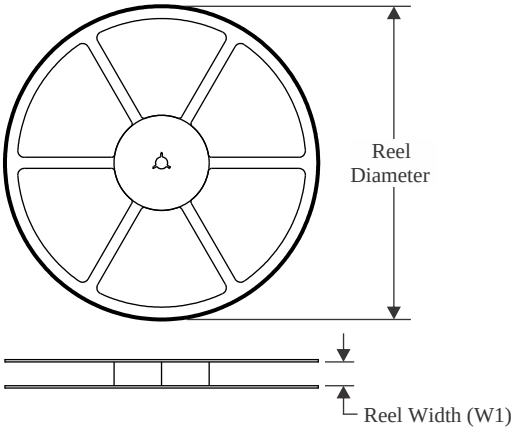
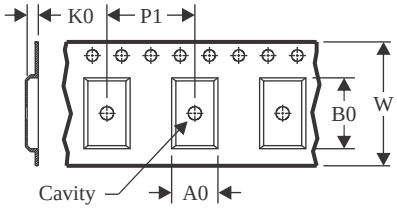
TAPE AND REEL INFORMATION

REEL DIMENSIONS

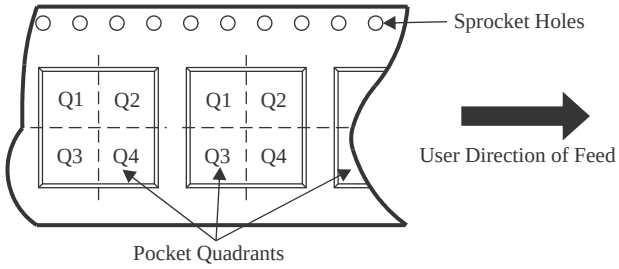


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

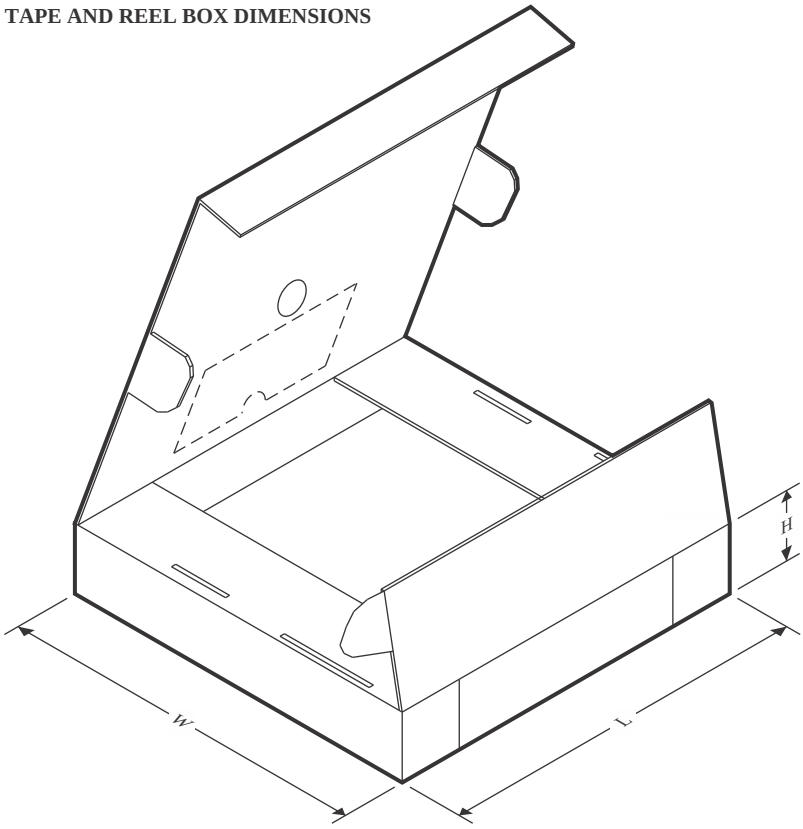
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS131E04IPAGR	TQFP	PAG	64	1500	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2
ADS131E06IPAGR	TQFP	PAG	64	1500	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2
ADS131E06IPAGRG4	TQFP	PAG	64	1500	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2
ADS131E08IPAGR	TQFP	PAG	64	1500	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

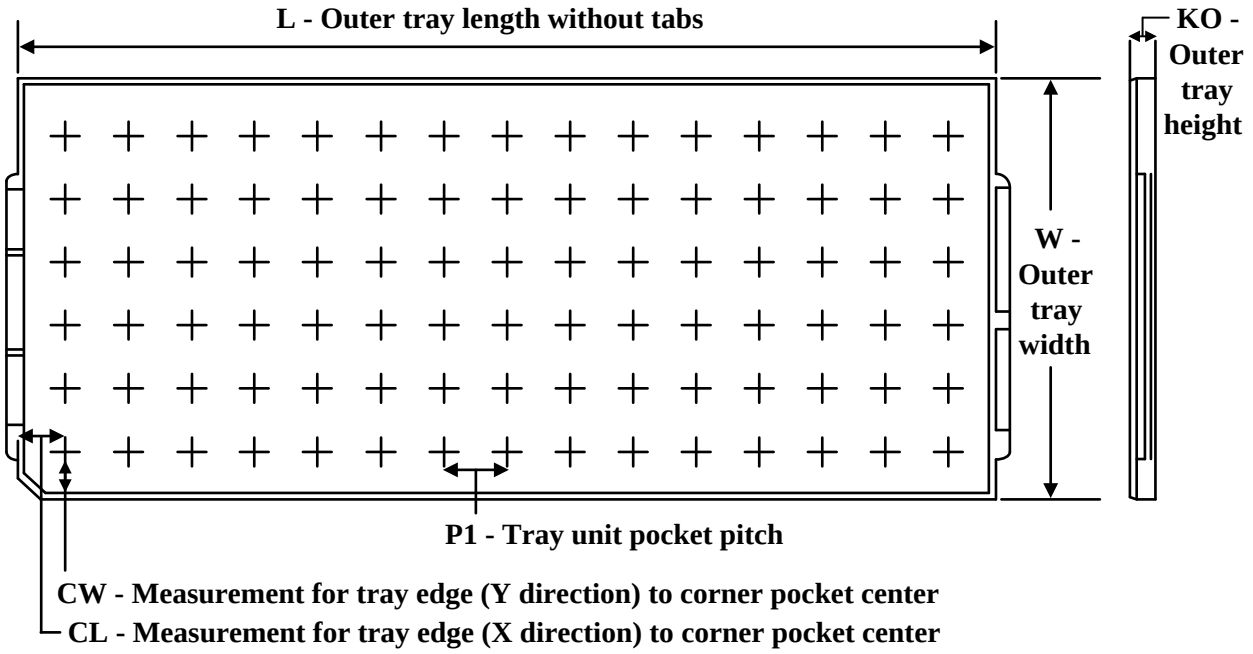
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS131E04IPAGR	TQFP	PAG	64	1500	350.0	350.0	43.0
ADS131E06IPAGR	TQFP	PAG	64	1500	350.0	350.0	43.0
ADS131E06IPAGRG4	TQFP	PAG	64	1500	350.0	350.0	43.0
ADS131E08IPAGR	TQFP	PAG	64	1500	350.0	350.0	43.0

TRAY

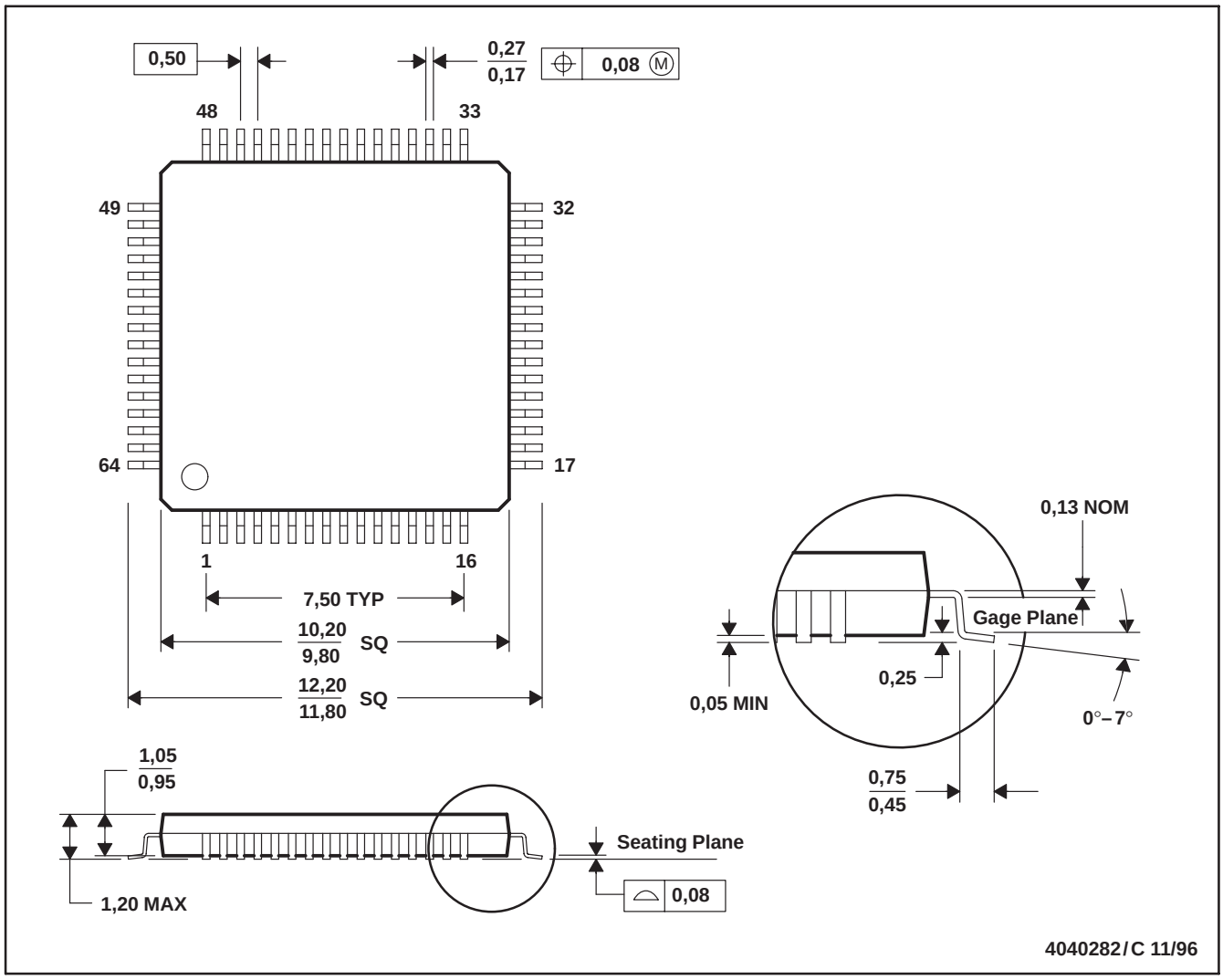


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

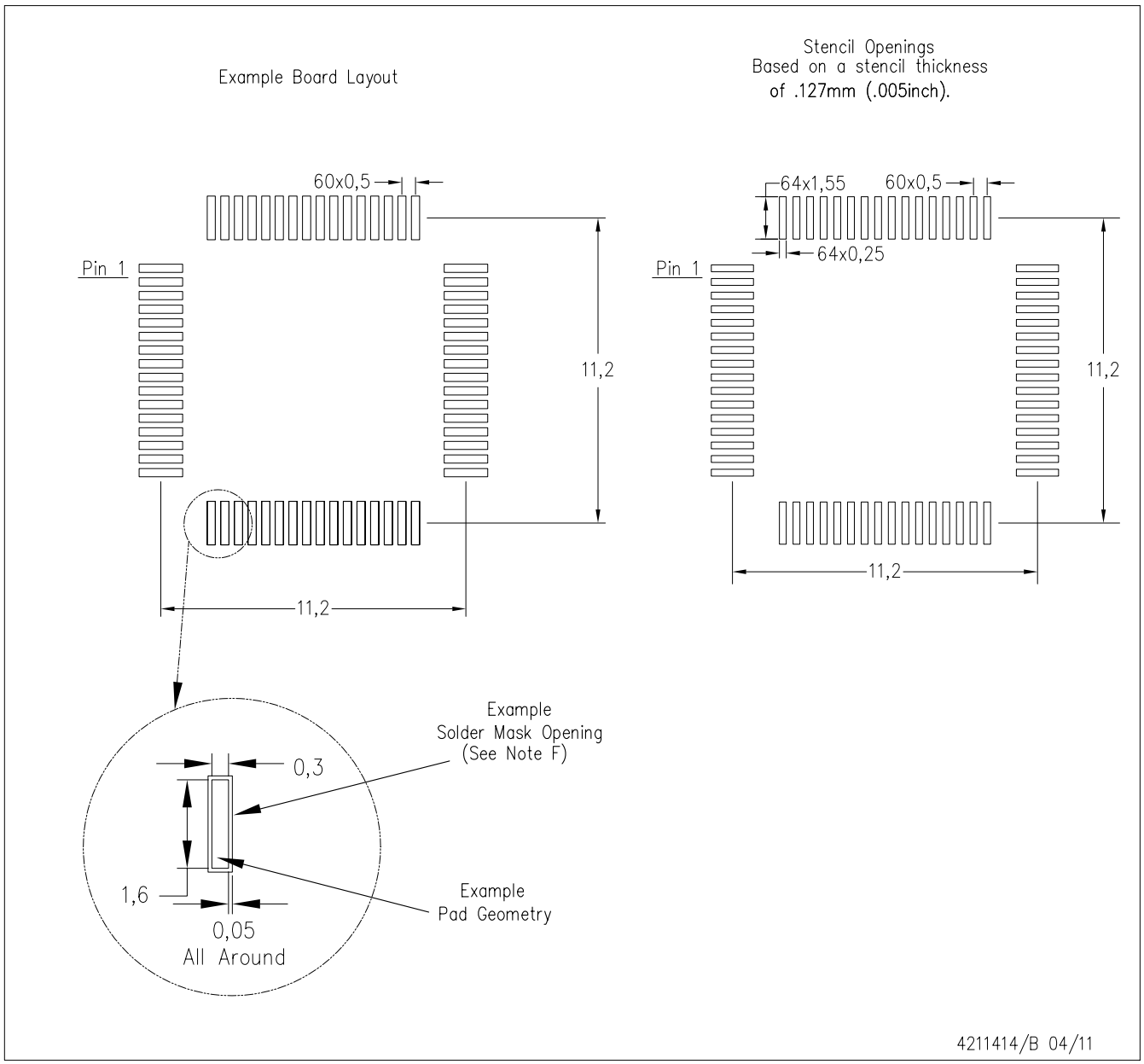
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADS131E04IPAG	PAG	TQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
ADS131E04IPAG.A	PAG	TQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
ADS131E04IPAG.B	PAG	TQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
ADS131E06IPAG	PAG	TQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
ADS131E06IPAG.A	PAG	TQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
ADS131E06IPAG.B	PAG	TQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
ADS131E08IPAG	PAG	TQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
ADS131E08IPAG.A	PAG	TQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
ADS131E08IPAG.B	PAG	TQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13

PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



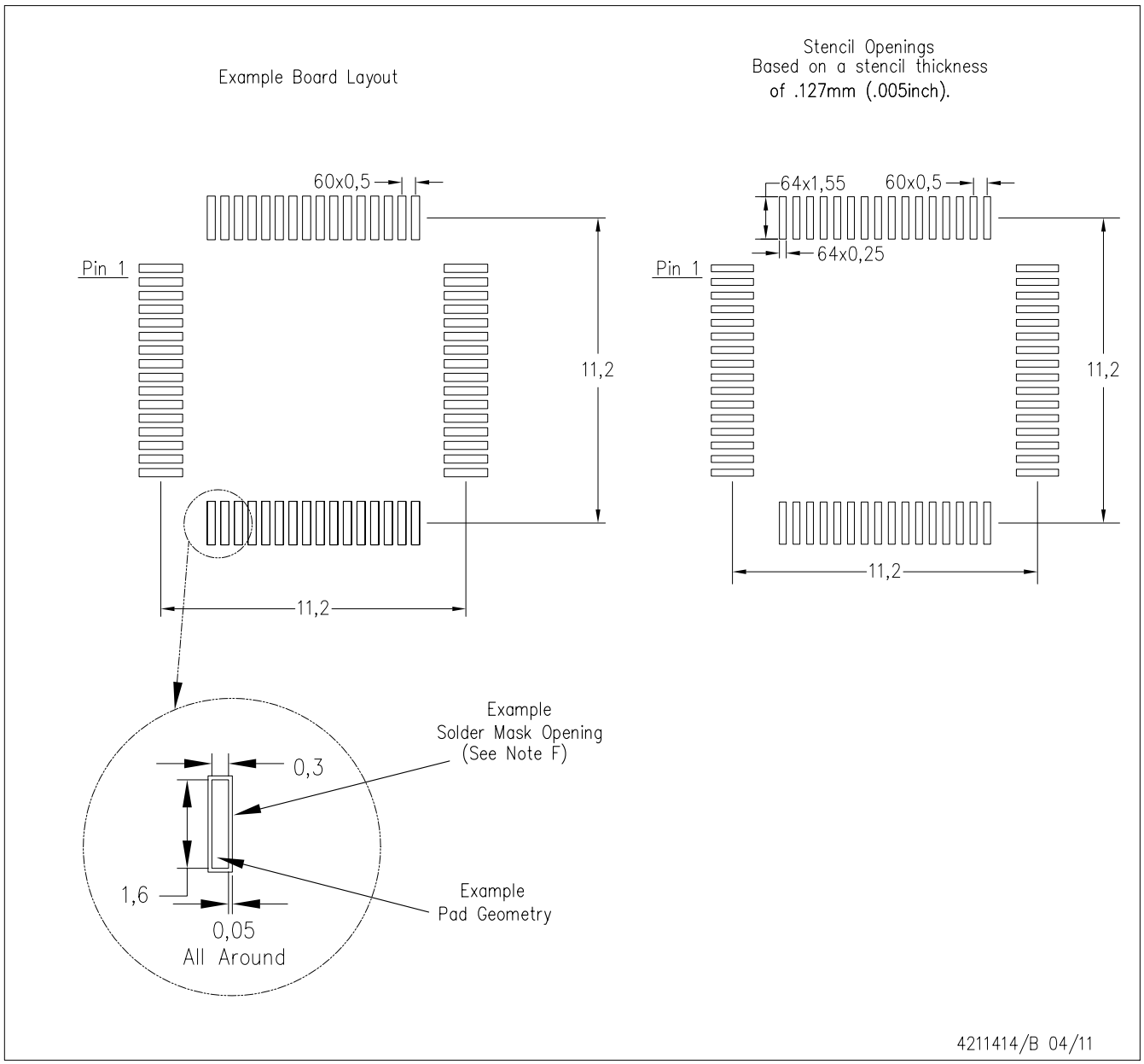
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PAG (S–PQFP–G64) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PAG (S–PQFP–G64) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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