ADS1282-HT 高温度、高分辨率 Δ-Σ ADC

1 特性

- 高分辨率：124dB 信噪比 (SNR) (1000SPS)
- 高精度：总谐波失真 (THD)：–102dB
  积分非线性 (INL)：0.5ppm
- 低噪声可编程增益放大器 (PGA)
- 双通道输入多路复用器 (MUX)
- 固有稳定性的调制器，支持快速响应超范围检测
- 灵活的数字滤波器：
  - 正弦 + 有限脉冲响应 (FIR) + 无限脉冲响应 (IIR)（可选）
  - 线性或最小相位响应
  - 可编程的高通滤波器
  - 可选的 FIR 数据速率： 250SPS 至 4kSPS
- 滤波器旁路选项
- 低功耗：25mW (210°C)
- 偏移和增益校准引擎
- SYNC 输入
- 模拟电源：单极 (5V) 或双极 (±2.5V)
- 数字电源：1.75V 至 3.3V
- 支持极端温度 应用 (1)
  - 可控基线
  - 一个组装/测试场所
  - 一个制造场所
  - 在极端（–55°C 至 210°C）温度范围内可用
  - 延长的产品生命周期
  - 延长产品的变更通知
  - 产品可追溯性

(1) 德州仪器 (TI) 高温产品利用高度优化的硅（芯片）解决方案，通过设计和制造工艺方面的改进，能够在广泛的温度范围内最大限度提升性能。

2 应用

- 能量勘探
- 地震监测
- 高精度仪器
- 潜孔打钻
- 高温环境

3 说明

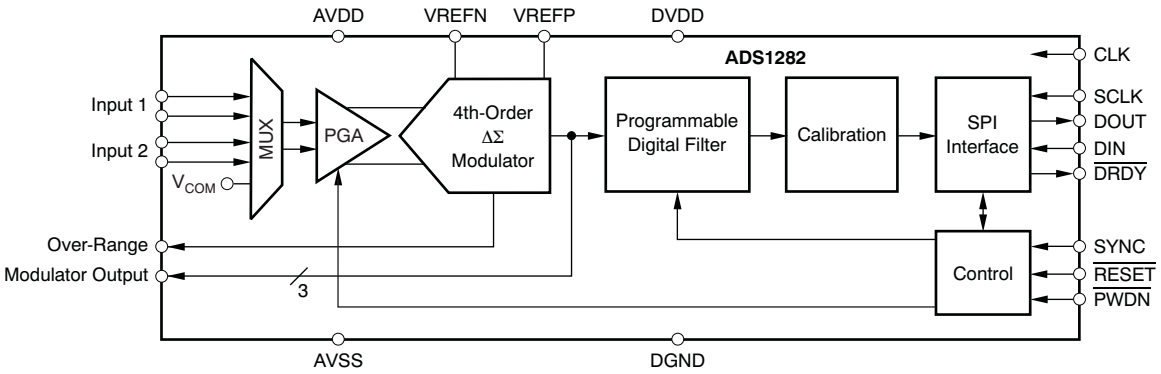
ADS1282-HT 器件是一款超高性能的单芯片模数转换器 (ADC)，具有集成式低噪声可编程增益放大器 (PGA) 和双通道输入多路复用器 (MUX)。ADS1282-HT 器件适用于能量勘探和地震监测等应用的苛刻环境。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ADS1282-HT	CDIP SB (28)	7.49mm x 35.56mm
	TSSOP (28)	4.40mm x 9.70mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision G (May 2015) to Revision H **Page**

- Relaxed current for standby and power mode from "110 µA" to "250 µA" ... 7

Changes from Revision F (August 2011) to Revision G **Page**

- 已添加 *ESD 额定值*表，*特性 描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1
- Removed data in *Specifications* for low-power modes ... 6
- Removed low-power mode data from graphs in *Typical Characteristics* ... 12
- Remove low-power mode information from Figure 35 ... 24

Changes from Revision C (August 2010) to Revision D **Page**

- Changed $f_{CLK}/128$ to $f_{CLK}/512$ in *Modulator* ... 21
- Updated *Modulator Input Impedance* ... 23
- Updated Figure 36 ... 25
- Updated Table 9 and added footnote ... 34
- Updated *Modulator Output Mode* ... 36
- Updated Figure 56 and added footnote ... 36
- Updated Figure 75 ... 46

5 说明 （续）

此转换器使用一个固有稳定性的四阶 Δ-Σ 调制器来获得出色的抗噪性能和线性度。该调制器可与片上数字滤波器搭配使用，也可通过旁路与后处理滤波器结合使用。

输入 MUX 可灵活提供附加的外部输入用于测量以及内部自检连接。PGA 具有 出色的低噪声性能 (5nV/$\sqrt{Hz}$) 和高输入阻抗，能够与较宽增益范围内的地震检波器和水中检波器轻松连接。

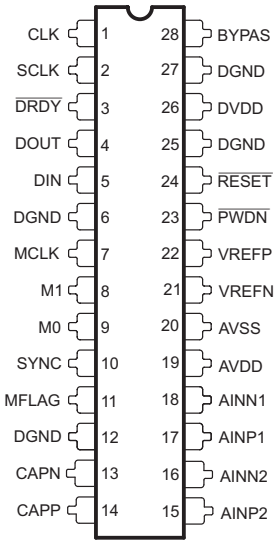
数字滤波器提供 250SPS 至 4000SPS 的可选数据速率。高通滤波器 (HPF) 具有 可调节的角频率。片上增益和偏移调节寄存器支持系统校准。

同步输入 (SYNC) 可用于对多个 ADS1282 的转换操作进行同步。SYNC 输入还接受外部时钟源输入，用于对转换操作进行持续校准。

该器件具有两种工作模式，对噪声性能和功耗进行了优化。放大器、调制器和滤波器三者的总功耗为 30mW。ADS1282-SP 在 –55°C 至 210°C（或 –55°C 至 175°C，对于 PW 封装） 温度范围内完全额定运行。

6 Pin Configuration and Functions

JDJ or PW Package
28-Pin CDIP SB or TSSOP
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	CDIP SB	TSSOP		
CLK	1	1	Digital input	Master clock input
SCLK	2	2	Digital input	Serial clock input
$\overline{\text{DRDY}}$	3	3	Digital output	Data ready output: read data on falling edge
DOUT	4	4	Digital output	Serial data output
DIN	5	5	Digital input	Serial data input
MCLK	7	7	Digital I/O	Modulator clock output; if in modulator mode: MCLK: Modulator clock output Otherwise, the pin is an unused input (must be tied).
M1	8	8	Digital I/O	Modulator data output 1; if in modulator mode: M1: Modulator data output 1 Otherwise, the pin is an unused input (must be tied).
M0	9	9	Digital I/O	Modulator data output 0; if in modulator mode: M0: Modulator data output 0 Otherwise, the pin is an unused input (must be tied).
SYNC	10	10	Digital input	Synchronize input
MFLAG	11	11	Digital output	Modulator Over-Range flag: 0 = normal, 1 = modulator over-range
DGND	6	6	Digital ground	Digital ground, pin 12 is the key ground point
	12	12		
	27	25		
	29	27		
CAPN	13	13	Analog	PGA outputs: Connect 10-nF capacitor from CAPP to CAPN
CAPP	14	14	Analog	PGA outputs: Connect 10-nF capacitor from CAPP to CAPN
AINP2	15	15	Analog input	Positive analog input 2
AINN2	16	16	Analog input	Negative analog input 2
AINP1	17	17	Analog input	Positive analog input 1
AINN1	18	18	Analog input	Negative analog input 1

Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	CDIP SB	TSSOP		
AVDD	19	19	Analog supply	Positive analog power supply
	20			
AVSS	21	20	Analog supply	Negative analog power supply
	22			
VREFN	23	21	Analog input	Negative reference input
VREFP	24	22	Analog input	Positive reference input
$\overline{\text{PWDN}}$	25	23	Digital input	Power-down input, active low
$\overline{\text{RESET}}$	26	24	Digital input	Reset input, active low
DVDD	28	26	Digital supply	Digital power supply: 1.8 V to 3.3 V
BYPAS	30	28	Analog	Sub-regulator output: Connect 1-µF capacitor to DGND

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

	MIN	MAX	UNIT
AVDD to AVSS	–0.3	5.5	V
AVSS to DGND	–2.8	0.3	V
DVDD to DGND	–0.3	3.9	V
Input current		100, momentary	mA
Input current		10, continuous	mA
Analog input voltage (AINP1, AINN1, AINP2, AINN2, VREFN, VREFP, CAPP, CAPN)	AVSS – 0.3	AVDD + 0.3	V
Digital input voltage to DGND (CLK, SCLK, $\overline{\text{DRDY}}$, DOUT, DIN, MCLK, M1, M0, MFLAG, SYNC, $\overline{\text{PWDN}}$, $\overline{\text{RESET}}$)	–0.3	DVDD + 0.3	V
Storage temperature, T_{stg}	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Operating temperature	–55		125	°C

7.3 Thermal Information

THERMAL METRIC(1)		ADS1282-HT		UNIT
		JDJ (CDIP SB)	PW (TSSOP)	
		28 PINS	28 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.1	54.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.03	11.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.2	13	°C/W
ψ_{JT}	Junction-to-top characterization parameter	N/A	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	N/A	12.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.98	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.4 Electrical Characteristics

Limit specifications at –55°C to 210°C. Typical specifications at 25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK} (1) = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, CAPN – CAPP = 10 nF, PGA = 1, and f_{DATA} = 1000 SPS, unless otherwise noted.

PARAMETER		TEST CONDITIONS	T_A = –55°C to 125°C			T_A = 210°C (2)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUTS									
Full-scale input voltage		V_{IN} = (AINP – AINN)		±V_{REF}/(2 × PGA)					V
Absolute input range	AINP or AINN		AVSS + 0.7		AVDD – 1.25	AVSS + 0.7		AVDD – 1.25	V
PGA input voltage noise density				5					nV/√Hz
Differential input impedance (3)				1					GΩ
Common-mode input impedance				100					MΩ
Input bias current				1			1000		nA
Crosstalk		f = 31.25 Hz		–128			–123		dB
MUX ON-resistance				30			45		Ω
PGA OUTPUT (CAPP, CAPN)									
Absolute output range			AVSS + 0.4		AVDD – 0.4	AVSS + 0.4		AVDD – 0.4	V
PGA differential output impedance				600			600		Ω
Output impedance tolerance				±10%			±10%		
External bypass capacitance				10	100		10		nF
Modulator differential input impedance				55					kΩ
AC PERFORMANCE									
Signal-to-noise ratio (4)	SNR		112	124		110	122		dB
Total harmonic distortion (5)	THD	PGA = 1...16		–122	–99		–102	–99	dB
		PGA = 32		–117	–99		–98	–94	
		PGA = 64		–115			–93		
Spurious-free dynamic range	SFDR			123					dB
DC PERFORMANCE									
Resolution		No missing codes	31			31			bits
Data rate	f_{DATA}	FIR filter mode	250		4000	250		4000	SPS
		Sinc filter mode	8000		128000	8000		128000	SPS
Integral nonlinearity (INL) (6)		Differential input		0.00005	0.0090		0.002	0.01	% FSR (7)
Offset error		Shorted input		50	200		99	250	µV
Offset error after calibration (8)				1			2		µV
Offset drift				0.02			0.19		µV/°C
Gain error (9)			–1.5%	–1%	–0.5%	–1.5%	–1%	–0.5%	
Gain error after calibration (8)				0.0002%			0.0002%		
Gain drift		PGA = 1		2			3		ppm/°C
		PGA = 16		9			11		ppm/°C
Gain matching (10)				0.3%	0.8%			0.8%	
Common-mode rejection		f_{CM} = 60 Hz (11)	82	110		82	137		dB

(1) f_{CLK} = system clock.
(2) Minimum and maximum parameters are characterized for operation at T_A = 210°C, but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.
(3) Input impedance is improved by disabling input chopping (CHOP bit = 0).
(4) V_{IN} = 20mV_{DC}/PGA, see Table 1.
(5) V_{IN} = 31.25 Hz, –0.5 dBFS.
(6) Best-fit method.
(7) FSR: Full-scale range = ±V_{REF} / (2 × PGA).
(8) Calibration accuracy is on the level of noise reduced by 4 (calibration averages 16 readings).
(9) The PGA output impedance and the modulator input impedance results in –1% systematic gain error.
(10) Gain match relative to PGA = 1.
(11) f_{CM} is the input common-mode frequency. f_{PS} is the power-supply frequency.

Electrical Characteristics (continued)

Limit specifications at –55°C to 210°C. Typical specifications at 25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK}(1) = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, CAPN – CAPP = 10 nF, PGA = 1, and f_{DATA} = 1000 SPS, unless otherwise noted.

PARAMETER		TEST CONDITIONS	T_A = –55°C to 125°C			T_A = 210°C(2)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Power-supply rejection	AVDD, AVSS	f_{PS} = 60 Hz(11)	80	90			83		dB
	DVDD		90	115			101		
VOLTAGE REFERENCE INPUTS									
Reference input voltage		(V_{REF} = VREFP – VREFN)	0.5	5	(AVDD – AVSS) + 0.2	0.5		(AVDD – AVSS) + 0.2	V
Negative reference input	VREFN		AVSS – 0.1		VREFP – 0.5	AVSS – 0.1		VREFP – 0.5	V
Positive reference input	VREFP		VREFN + 0.5		AVDD + 0.1	VREFN + 0.5		AVDD + 0.1	V
Reference input impedance				85			85		kΩ
DIGITAL FILTER RESPONSE									
Passband ripple					±0.003				dB
Passband (–0.01 dB)				0.375 × f_{DATA}					Hz
Bandwidth (–3 dB)				0.413 × f_{DATA}					Hz
High-pass filter corner			0.1		10				Hz
Stop band attenuation(12)			135						dB
Stop band				0.500 × f_{DATA}					Hz
Group delay		Minimum phase filter		5 / f_{DATA}					s
		Linear phase filter		31 / f_{DATA}					
Settling time (latency)		Minimum phase filter		62 / f_{DATA}					s
		Linear phase filter		62 / f_{DATA}					s
DIGITAL INPUT/OUTPUT									
V_{IH}			0.8 × DVDD		DVDD	0.8 × DVDD		DVDD	V
V_{IL}			DGND		0.2 × DVDD	DGND		0.2 × DVDD	V
V_{OH}		I_{OH} = 1 mA	0.8 × DVDD			0.8 × DVDD			V
V_{OL}		I_{OL} = 1 mA			0.2 × DVDD			0.2 × DVDD	V
Input leakage		0 < $V_{DIGITAL\ IN}$ < DVDD			±10			±10	µA
POWER SUPPLY									
AVSS			–2.6		0	–2.6		0	V
AVDD			AVSS + 4.75		AVSS + 5.25	AVSS + 4.75		AVSS + 5.25	V
DVDD			1.75		3.6	1.75		3.6	V
AVDD, AVSS current		High-resolution mode		4.5	7.2		5.2	10	|mA|
		Standby mode		68	250		3000	3700	|µA|
		Power-down mode		68	250		3000	3700	|µA|
DVDD current		All modes		0.6	1.5		1.2	2	mA
		Modulator mode		0.1			1.1		mA
		Standby mode		73	175		576	950	µA
		Power-down mode(13)		32	120		186	240	µA

(12) Input frequencies in the range of Nf_{CLK} / 512 ± f_{DATA} / 2 (N = 1, 2, 3...) can mix with the modulator chopping clock. In these frequency ranges intermodulation = 120 dB, typ.
(13) CLK input stopped.

Electrical Characteristics (continued)

Limit specifications at –55°C to 210°C. Typical specifications at 25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK} (1) = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, CAPN – CAPP = 10 nF, PGA = 1, and f_{DATA} = 1000 SPS, unless otherwise noted.

PARAMETER	TEST CONDITIONS	T_A = –55°C to 125°C			T_A = 210°C (2)			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Power dissipation	High-resolution mode		25	41		29.7	56.1	mW
	Standby mode		0.58	1.1		16.9	21.6	mW
	Power-down mode		0.45	0.95		15.6	19.3	mW

7.5 Electrical Characteristics (PW Package)

Limit specifications at –55°C to 175°C. Typical specifications at 25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK} (1) = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, CAPN – CAPP = 10 nF, PGA = 1, and f_{DATA} = 1000 SPS, unless otherwise noted.

PARAMETER		TEST CONDITIONS	T_A = –55°C to 125°C			T_A = 175°C (2)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUTS									
Full-scale input voltage		V_{IN} = (AINP – AINN)		±V_{REF} / (2 × PGA)			±V_{REF} / (2 × PGA)		V
Absolute input range	AINP or AINN		AVSS + 0.7		AVDD – 1.25	AVSS + 0.7		AVDD – 1.25	V
PGA input voltage noise density				5			5		nV/√Hz
Differential input impedance (3)				1			1		GΩ
Common-mode input impedance				100			100		MΩ
Input bias current				1			1000		nA
Crosstalk		f = 31.25 Hz		–128			–123		dB
MUX on-resistance				30			45		Ω
PGA OUTPUT (CAPP, CAPN)									
Absolute output range			AVSS + 0.4		AVDD – 0.4	AVSS + 0.4		AVDD – 0.4	V
PGA differential output impedance				600			600		Ω
Output impedance tolerance				±10%			±10%		
External bypass capacitance				10	100		10		nF
Modulator differential input impedance				55			55		kΩ
AC PERFORMANCE									
Signal-to-noise ratio (4)	SNR		112	124		112	122		dB
Total harmonic distortion (5)	THD	PGA = 1...16		–122	–99		–112	–99	dB
		PGA = 32		–117	–99		–106	–94	
		PGA = 64		–115			–102		
Spurious-free dynamic range	SFDR			123					dB
DC PERFORMANCE									
Resolution		No missing codes	31			31			bits
Data rate	f_{DATA}	FIR filter mode	250		4000	250		4000	SPS
		Sinc filter mode	8000		128000	8000		128000	SPS

(1) f_{CLK} = System clock
(2) Minimum and maximum parameters are characterized for operation at T_A = 175°C, but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.
(3) Input impedance is improved by disabling input chopping (CHOP bit = 0).
(4) V_{IN} = 20 mV_{DC} / PGA, see Table 1.
(5) V_{IN} = 31.25 Hz, –0.5 dBFS.

Electrical Characteristics (PW Package) (continued)

Limit specifications at –55°C to 175°C. Typical specifications at 25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK}[1] = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, CAPN – CAPP = 10 nF, PGA = 1, and f_{DATA} = 1000 SPS, unless otherwise noted.

PARAMETER		TEST CONDITIONS	T_A = –55°C to 125°C			T_A = 175°C[2]			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Integral nonlinearity (INL)[6]		Differential input		0.00005	0.009		0.00004	0.009	% FSR[7]
Offset error		Shorted input		50	200		50	200	µV
Offset error after calibration[8]				1			2		µV
Offset drift				0.02			0.19		µV/°C
Gain error[9]			–1.5%	–1%	–0.5%	–1.5%	–1%	–0.5%	
Gain error after calibration[8]				0.0002%			0.0002%		
Gain drift		PGA = 1		2			2		ppm/°C
		PGA = 16		9			11		ppm/°C
Gain matching[10]				0.3%	0.8%		0.4%	0.8%	
Common-mode rejection		f_{CM} = 60 Hz[11]	82	110		82	114		dB
Power-supply rejection	AVDD, AVSS	f_{PS} = 60 Hz[11]	80	90			84		dB
	DVDD		90	115			106		
VOLTAGE REFERENCE INPUTS									
Reference input voltage		(V_{REF} = VREFP – VREFN)	0.5	5	(AVDD – AVSS) + 0.2	0.5		(AVDD – AVSS) + 0.2	V
Negative reference input	VREFN		AVSS – 0.1		VREFP – 0.5	AVSS – 0.1		VREFP – 0.5	V
Positive reference input	VREFP		VREFN + 0.5		AVDD + 0.1	VREFN + 0.5		AVDD + 0.1	V
Reference input impedance				85			85		kΩ
DIGITAL FILTER RESPONSE									
Passband ripple					±0.003			±0.003	dB
Passband (–0.01 dB)				0.375 × f_{DATA}			0.375 × f_{DATA}		Hz
Bandwidth (–3 dB)				0.413 × f_{DATA}			0.413 × f_{DATA}		Hz
High-pass filter corner			0.1		10	0.1		10	Hz
Stop band attenuation[12]			135			135			dB
Stop band				0.500 × f_{DATA}			0.500 × f_{DATA}		Hz
DIGITAL INPUT/OUTPUT									
V_{IH}			0.8 × DVDD		DVDD	0.8 × DVDD		DVDD	V
V_{IL}			DGND		0.2 × DVDD	DGND		0.2 × DVDD	V
V_{OH}		I_{OH} = 1 mA	0.8 × DVDD			0.8 × DVDD			V
V_{OL}		I_{OL} = 1 mA			0.2 × DVDD			0.2 × DVDD	V
Input leakage		0 < $V_{DIGITAL\ IN}$ < DVDD			±10			±10	µA
POWER SUPPLY									
AVSS			–2.6		0	–2.6		0	V
AVDD			AVSS + 4.75		AVSS + 5.25	AVSS + 4.75		AVSS + 5.25	V
DVDD			1.75		3.6	1.75		3.6	V

(6) Best-fit method.
(7) FSR: Full-scale range = ±V_{REF} / (2 × PGA).
(8) Calibration accuracy is on the level of noise reduced by 4 (calibration averages 16 readings).
(9) The PGA output impedance and the modulator input impedance results in –1% systematic gain error.
(10) Gain match relative to PGA = 1.
(11) f_{CM} is the input common-mode frequency. f_{PS} is the power-supply frequency.
(12) Input frequencies in the range of Nf_{CLK} / 512 ± f_{DATA} / 2 (N = 1, 2, 3...) can mix with the modulator chopping clock. In these frequency ranges intermodulation = 120 dB, typ.

Electrical Characteristics (PW Package) (continued)

Limit specifications at –55°C to 175°C. Typical specifications at 25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK}(1) = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, CAPN – CAPP = 10 nF, PGA = 1, and f_{DATA} = 1000 SPS, unless otherwise noted.

PARAMETER	TEST CONDITIONS	T_A = –55°C to 125°C			T_A = 175°C(2)			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
AVDD, AVSS current	High-resolution mode		4.5	7.2		5.2	9.2	|mA|
	Standby mode		68	110		52	900	|µA|
	Power-down mode		68	110		52	900	|µA|
DVDD current	All modes		0.6	1.5		0.7	1.5	mA
	Modulator mode		0.1			1.05		mA
	Standby mode		73	175		255	600	µA
	Power-down mode(13)		32	120		118	220	µA
Power dissipation	High-resolution mode		25	41		31	41	mW
	Standby mode		0.58	1.1		2.5	5	mW
	Power-down mode		0.45	0.95		2.06	4.5	mW

(13) CLK input stopped.

7.6 Timing Requirements

At T_A = –55°C to 210°C and DVDD = 1.65 to 3.6 V, unless otherwise noted.

		T_A = –55°C to 125°C		T_A = 175°C		T_A = 210°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{SCLK}	SCLK period	2	16	2	16	2	16	1 / f_{CLK}
$t_{SPWH, L}$	SCLK pulse width, high and low(1)	0.8	10	0.8	10	0.8	10	1 / f_{CLK}
t_{DIST}	DIN valid to SCLK rising edge: setup time	50		50		50		ns
t_{DIHD}	Valid DIN to SCLK rising edge: hold time	50		50		50		ns
t_{DOPD}	SCLK falling edge to valid new DOUT: propagation delay(2)		100		100		100	ns
t_{DOHD}	SCLK falling edge to DOUT invalid: hold time	0		0		0		ns
t_{SCDL}	Final SCLK rising edge of command to first SCLK rising edge for register read/write data	24		24		24		1 / f_{CLK}
DIGITAL INPUT/OUTPUT								
Clock input	f_{CLK}	1	4.096			1	4.096	MHz
Serial clock rate	f_{SCLK}		$f_{CLK/2}$				$f_{CLK/2}$	MHz

(1) Holding SCLK low for 64 $\overline{DRDY}$ falling edges resets the serial interface.
(2) Load on DOUT = 20 pF || 100 kΩ.

7.7 Pulse-Sync Timing Requirements

See Figure 46 and Figure 47 for timing diagrams.

		MIN	MAX	UNIT
t_{SYNC}	SYNC period(1)	1	Infinite	n / f_{DATA}
t_{CSHD}	CLK to SYNC hold time to not latch on CLK edge	10		ns
t_{SCSU}	SYNC to CLK setup time to latch on CLK edge	10		ns
$t_{SPWH, L}$	SYNC pulse width, high or low	2		1 / f_{CLK}
t_{DR}	Time for data ready (SINC filter)	See *器件支持*, 表 20		
	Time for data ready (FIR filter)	62.98046875 / f_{DATA} + 466 / f_{CLK}		

(1) Continuous-Sync mode; a free-running SYNC clock input without causing re-synchronization.

7.8 Reset Timing Requirements

See Figure 48 for timing diagram.

		MIN	MAX	UNIT
t_{CRHD}	CLK to RESET hold time	10		ns
t_{RCSU}	RESET to CLK setup time	10		ns
t_{RST}	RESET low	2		1 / f_{CLK}
t_{DR}	Time for data ready	62.98046875 / f_{DATA} + 468 / f_{CLK}		s

7.9 Read Data Timing Requirements

		MIN	MAX	UNIT
t_{DDPD}	$\overline{DRDY}$ to valid MSB on DOUT propagation delay (see Figure 54)(1)		100	ns
t_{DR}	Time for new data after data read command (see Figure 55)	0	1	f_{DATA}

(1) Load on DOUT = 20 pF || 100 kΩ.

7.10 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Group delay(1)	Minimum phase filter		5 / f_{DATA}		s
	Linear phase filter		31 / f_{DATA}		s
Settling time (latency)	Minimum phase filter		62 / f_{DATA}		s
	Linear phase filter		62 / f_{DATA}		s

(1) At DC. See Figure 42.

7.11 Modulator Switching Characteristics

See Figure 56.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{MCD0}, 1	MCLK rising edge to M0, M1 valid propagation delay(1)				100	ns
t_{CMD}	CLK rising edge (after SYNC rising edge) to MCLK rising edge CMD			5		1/f_{CLK}
t_{CSHD}	CLK to SYNC hold time to not latch on CLK edge		10			ns
t_{SCSU}	SYNC to CLK setup time to latch on CLK edge		10			ns
t_{SYMD}	SYNC to stable bit stream				16	1/f_{MOD}

(1) Load on M0 and M1 = 20 pF || 100 kΩ.

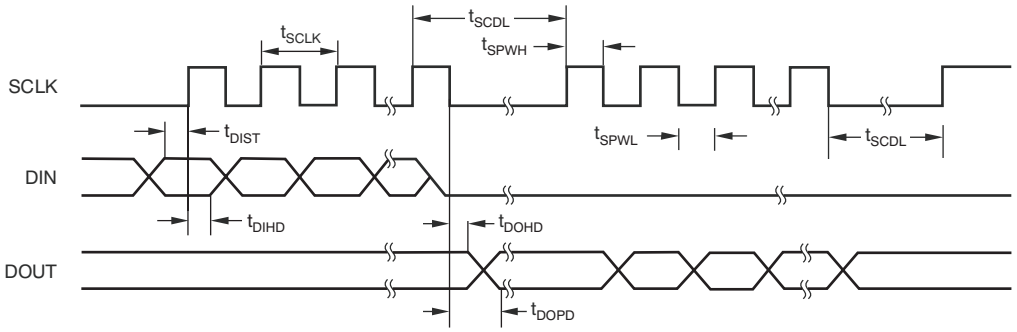


Figure 1. Timing Diagram

7.12 Typical Characteristics

At 25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK} = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, CAPN – CAPP = 10 nF, PGA = 1, and f_{DATA} = 1000 SPS, unless otherwise noted.

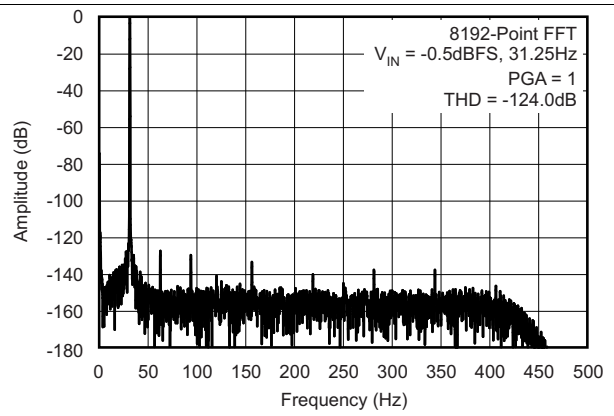


Figure 2. Output Spectrum

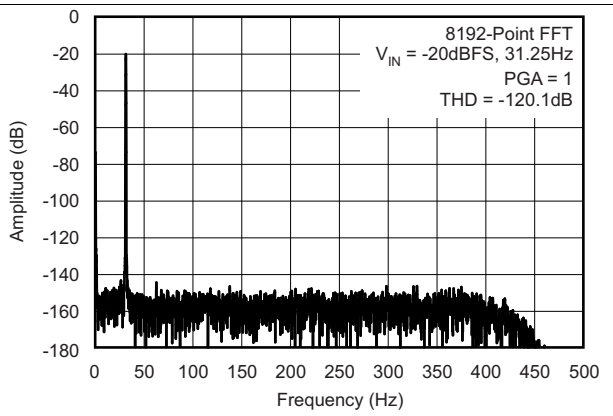


Figure 3. Output Spectrum

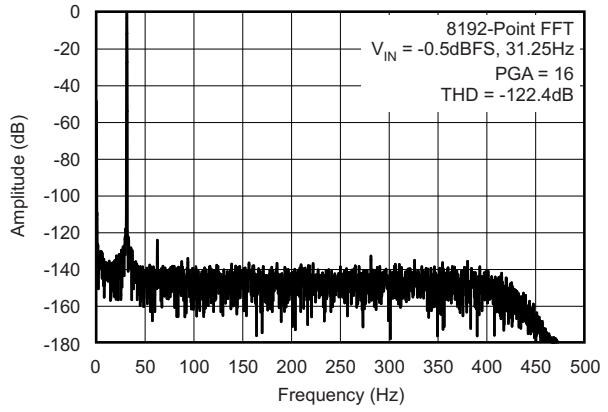


Figure 4. Output Spectrum

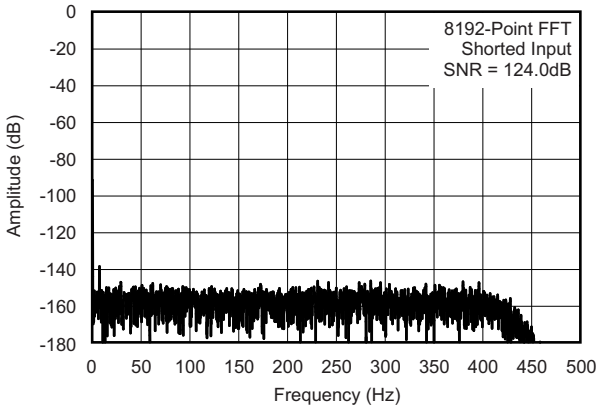


Figure 5. Output Spectrum

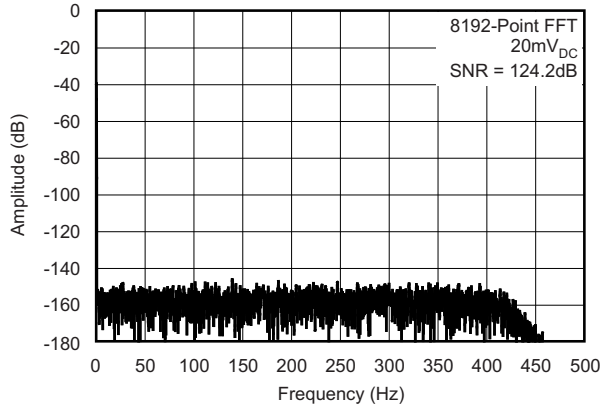


Figure 6. Output Spectrum

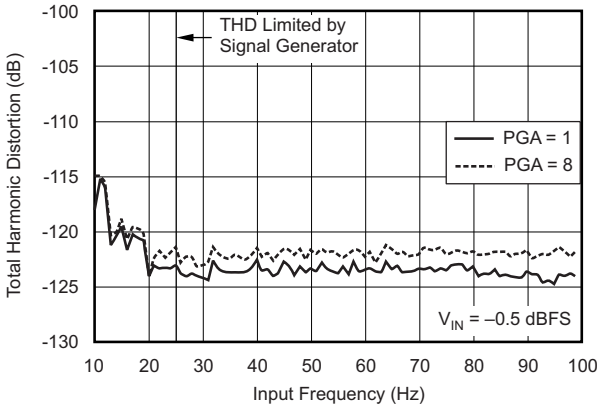


Figure 7. THD vs Input Frequency

Typical Characteristics (continued)

At 25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK} = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, CAPN – CAPP = 10 nF, PGA = 1, and f_{DATA} = 1000 SPS, unless otherwise noted.

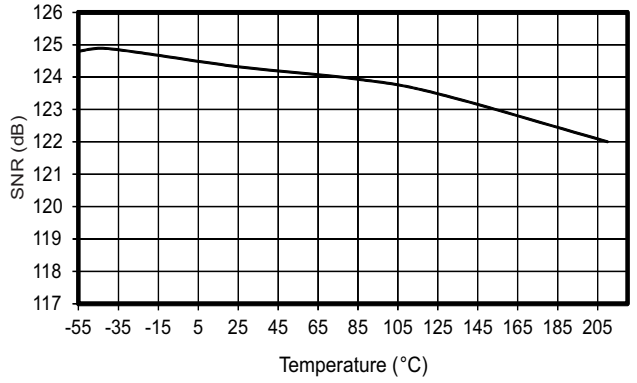


Figure 8. SNR (1000 SPS) vs Temperature

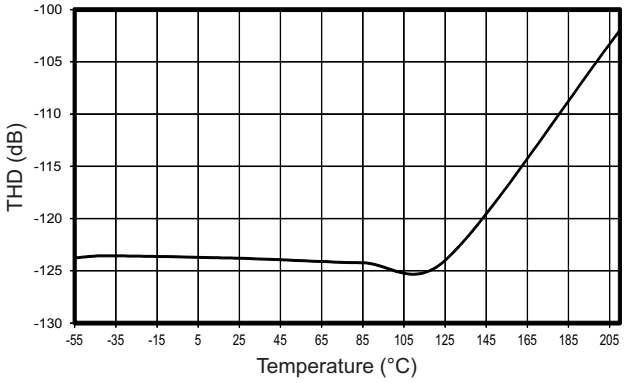


Figure 9. THD (G = 8) vs Temperature

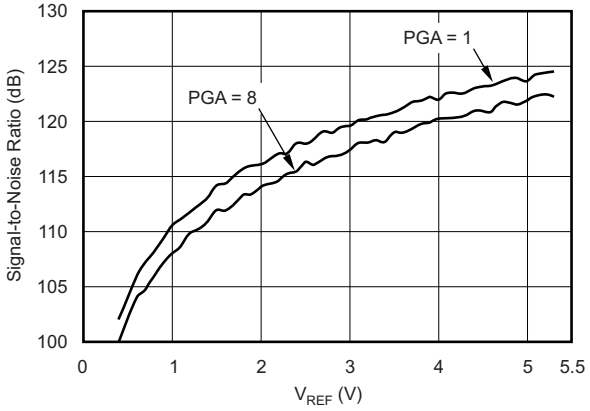


Figure 10. SNR vs Reference Voltage

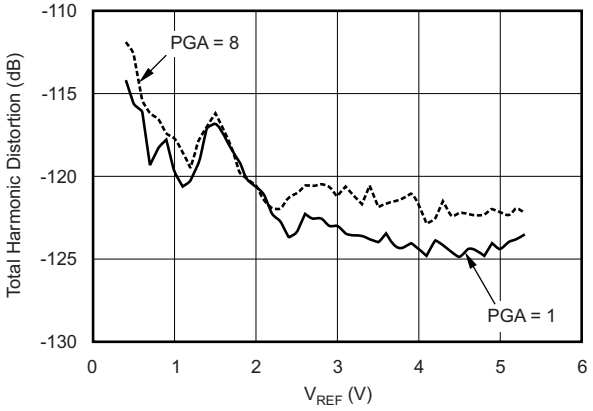


Figure 11. THD vs Reference Voltage

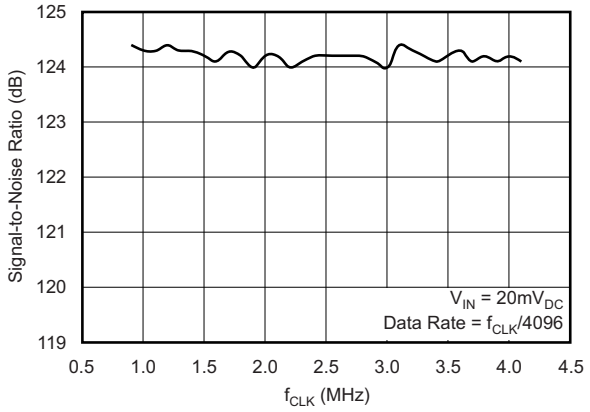


Figure 12. SNR vs Clock Frequency

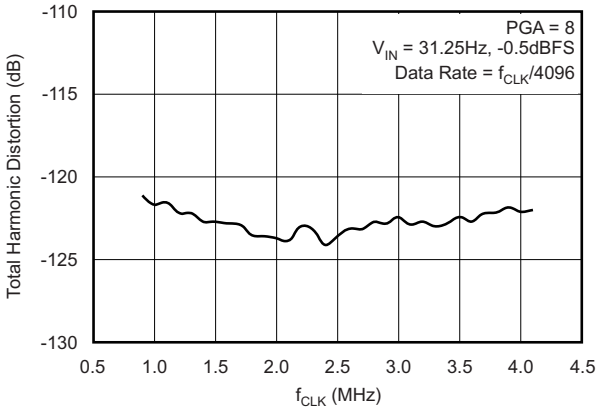


Figure 13. THD vs Clock Frequency

Typical Characteristics (continued)

At 25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK} = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, CAPN – CAPP = 10 nF, PGA = 1, and f_{DATA} = 1000 SPS, unless otherwise noted.

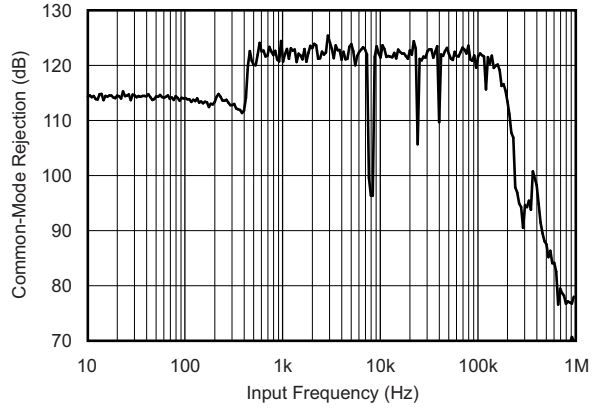


Figure 14. CMR vs Input Frequency

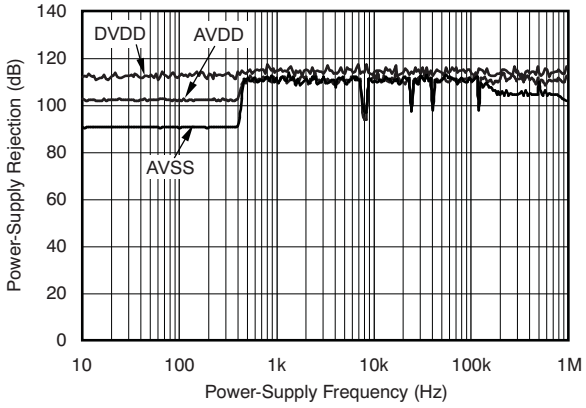


Figure 15. Power-Supply Rejection vs Frequency

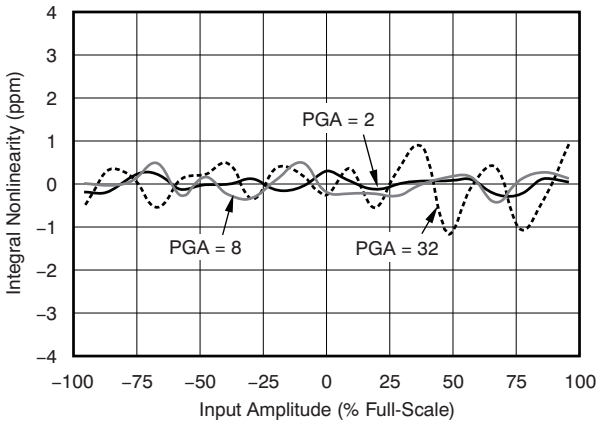


Figure 16. INL vs Input Amplitude

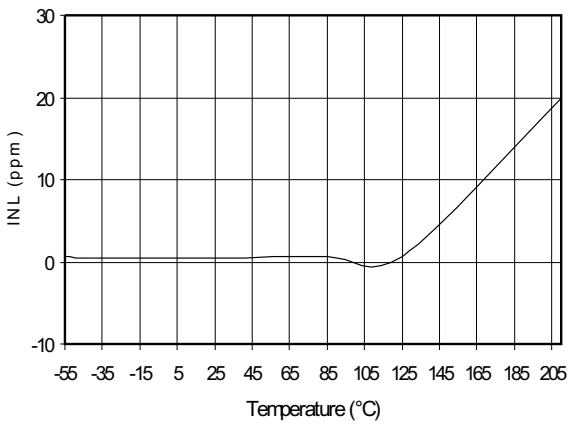


Figure 17. INL vs Temperature

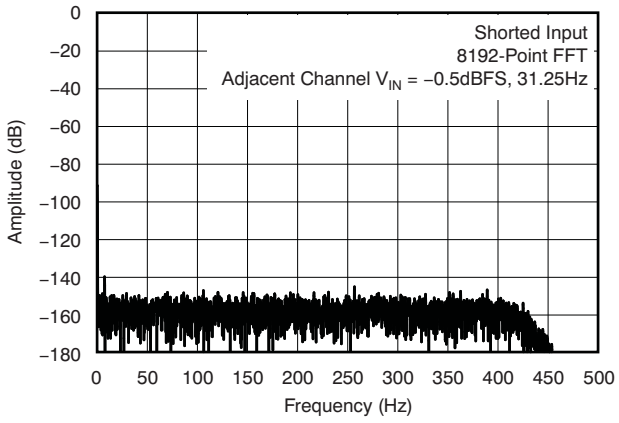


Figure 18. Crosstalk Output Spectrum

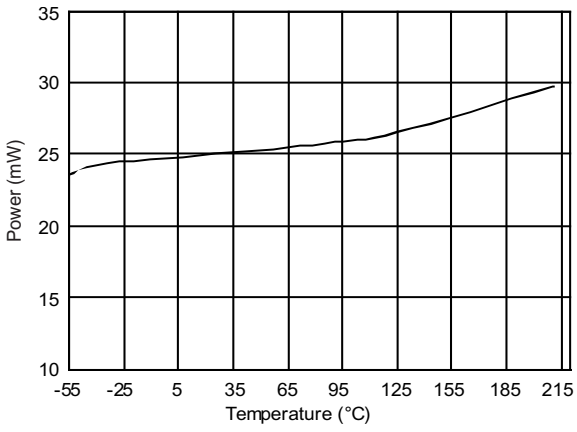


Figure 19. Power vs Temperature

Typical Characteristics (continued)

At 25°C, AVDD = 2.5 V, AVSS = –2.5 V, f_{CLK} = 4.096 MHz, VREFP = 2.5 V, VREFN = –2.5 V, DVDD = 3.3 V, CAPN – CAPP = 10 nF, PGA = 1, and f_{DATA} = 1000 SPS, unless otherwise noted.

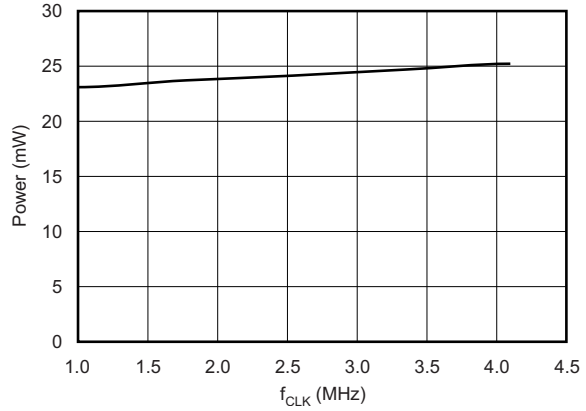


Figure 20. Power vs Clock Frequency

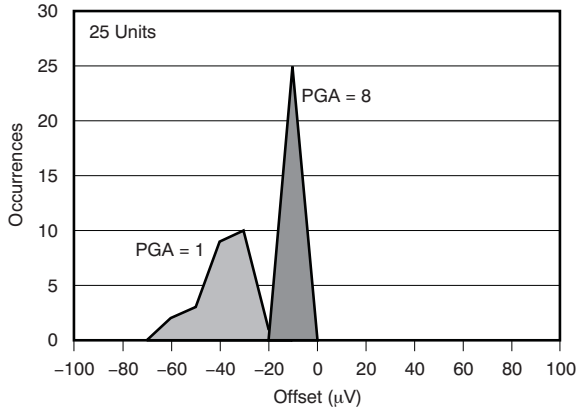


Figure 21. Offset Histogram

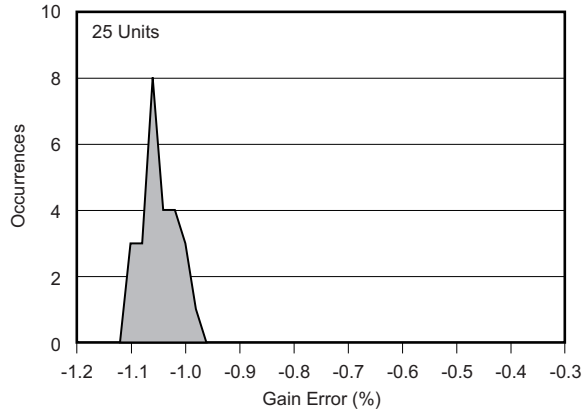


Figure 22. Gain Error Histogram

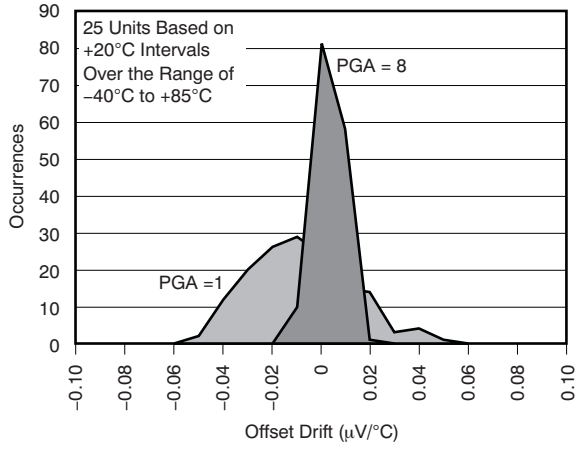


Figure 23. Offset Drift Histogram

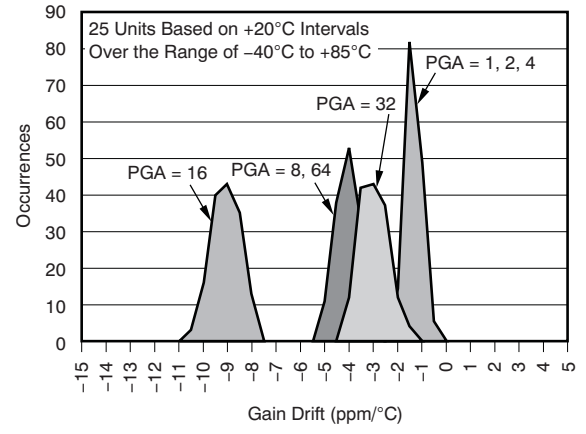


Figure 24. Gain Drift Histogram

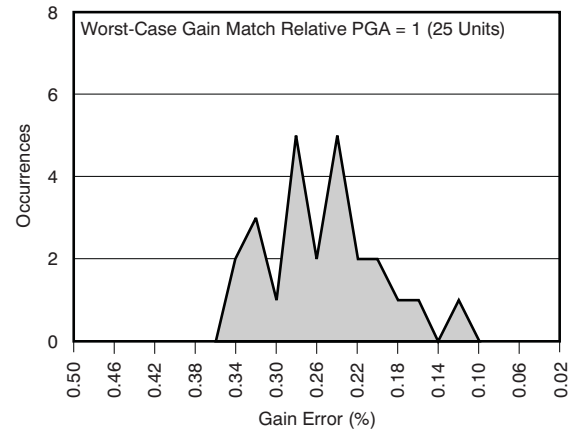


Figure 25. Gain Match Histogram

8 Detailed Description

8.1 Overview

The ADS1282-HT is a high-performance analog-to-digital converter (ADC) intended for energy exploration, seismic monitoring, chromatography, and other exacting applications. The converter provides 24- or 32-bit output data in data rates from 250 SPS to 4000 SPS. The *Functional Block Diagram* shows the block diagram of the ADS1282-HT.

The two-channel input MUX allows five configurations: Input 1; Input 2; Input 1 and Input 2 shorted together; shorted with 400-Ω test; and common-mode test. The input MUX is followed by a continuous time PGA, featuring very low noise of 5 nV/√Hz. The PGA is controlled by register settings, allowing gains of 1 to 64.

The inherently-stable, fourth-order, delta-sigma modulator measures the differential input signal V_{IN} = (AINP – AINN) × PGA against the differential reference V_{REF} = (VREFP – VREFN). A digital output (MFLAG) indicates that the modulator is in overload as a result of an overdrive condition. The modulator output is available directly on the MCLK, M0, and M1 output pins when in modulator mode. The modulator connects to an on-chip digital filter that provides the output code readings.

The digital filter consists of a variable decimation rate, fifth-order sinc filter followed by a variable phase, decimate-by-32, finite-impulse response (FIR) low-pass filter with programmable phase, and then by an adjustable high-pass filter for DC removal of the output reading. The output of the digital filter can be taken from the sinc, the FIR low-pass, or the infinite impulse response (IIR) high-pass sections.

Gain and offset registers scale the digital filter output to produce the final code value. The scaling feature can be used for calibration and sensor gain matching. The output data word is provided as either a 24-bit word or a full 32-bit word, allowing complete utilization of the inherently high resolution.

The SYNC input resets the operation of both the digital filter and the modulator, allowing synchronization conversions of multiple ADS1282-HT devices to an external event. The SYNC input supports a continuously-toggled input mode that accepts an external data frame clock locked to the conversion rate.

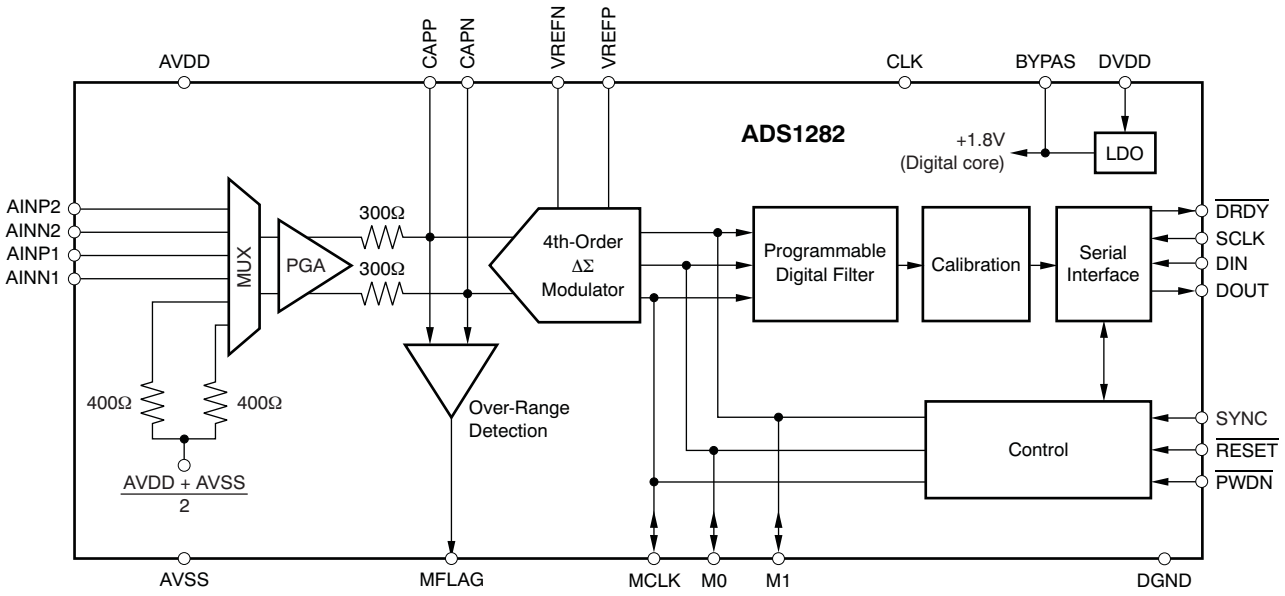
The $\overline{\text{RESET}}$ input resets the register settings and also restarts the conversion process. The $\overline{\text{PWDN}}$ input sets the device into a micro-power state. The register settings are not retained in $\overline{\text{PWDN}}$ mode. Use the STANDBY command in its place if it is desired to retain register settings (the quiescent current in the Standby mode is slightly higher).

Noise-immune Schmitt-trigger and clock-qualified inputs ($\overline{\text{RESET}}$ and SYNC) provide increased reliability in high-noise environments. The serial interface is used to read conversion data, in addition to reading from and writing to the configuration registers.

The device features unipolar and bipolar analog power supplies (AVDD and AVSS, respectively) for input range flexibility and a digital supply accepting 1.8 V to 3.3 V. The analog supplies may be set to 5 V to accept unipolar signals (with input offset) or set lower in the range of ±2.5 V to accept true bipolar input signals (ground referenced).

An internal sub-regulator is used to supply the digital core from DVDD. The BYPAS pin (pin 28) is the sub-regulator output and requires a 1-µF capacitor for noise reduction. BYPAS should not be used to drive external circuitry.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Noise Performance

The ADS1282-HT device offers outstanding noise performance (SNR). SNR depends on the data rate, the PGA setting, and the mode. As the bandwidth is reduced by decreasing the data rate, the SNR improves correspondingly. Similarly, as the PGA gain is increased, the SNR decreases. Table 1 summarizes the noise performance versus data rate, PGA setting, and mode.

8.3.2 Input-Referred Noise

The input-referred noise is related to SNR by Equation 1:

$$SNR = 20\log \frac{FSR_{RMS}}{N_{RMS}}$$

where:

- FSR_{RMS} = Full-scale range RMS = (VREFP – VREFN)/(2 × √2 × PGA)
- N_{RMS} = Noise RMS (input-referred) (1)

8.3.3 Idle Tones

The ADS1282-HT modulator incorporates an internal dither signal that randomizes the idle tone energy. Low-level idle tones may still be present, typically –137-dB less than full-scale. The low-level idle tones can be shifted out of the passband with an external offset = 20 mV/PGA. See the *Application Information* section for the recommended offset circuit.

Feature Description (continued)

8.3.4 Operating Mode

The default mode is high-resolution.

Table 1. Signal-to-Noise Ratio (dB)(1)

DATA RATE (SPS)	PGA						
	1	2	4	8	16	32	64
250	130	130	129	128	125	119	114
500	127	127	126	125	122	116	111
1000	124	124	123	122	119	113	108
2000	121	121	120	119	116	111	106
4000	118	118	117	116	113	108	103

(1) V_{IN} = 20 mV_{DC} / PGA.

8.3.5 Analog Inputs and Multiplexer

Figure 26 shows a diagram of the input multiplexer.

ESD diodes protect the multiplexer inputs. If either input is taken less than AVSS – 0.3 V or greater than AVDD + 0.3 V, the ESD protection diodes may turn on. If these conditions are possible, external Schottky clamp diodes and/or series resistors may be required to limit the input current to safe values (see the *Absolute Maximum Ratings*).

Also, overdriving one unused input may affect the conversions of the other input. If overdriven inputs are possible, TI recommends clamping the signal with external Schottky diodes.

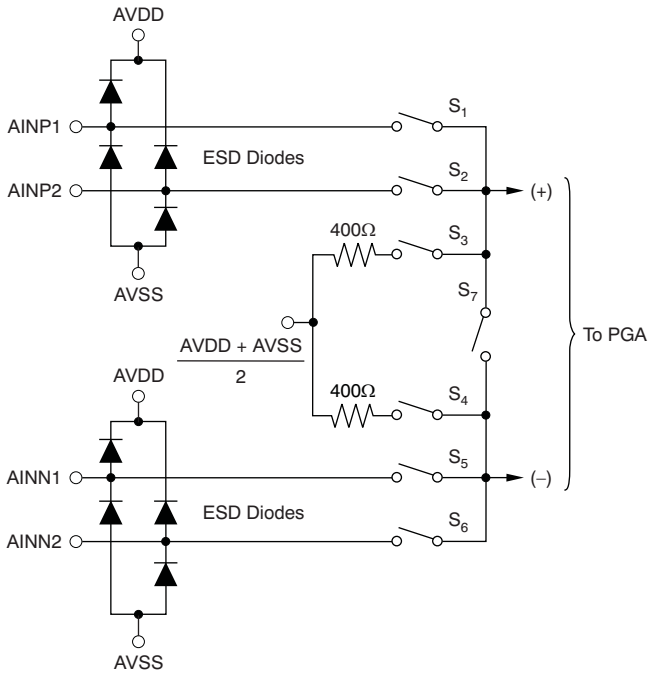


Figure 26. Analog Inputs and Multiplexer

The specified input operating range of the PGA is shown in Equation 2:

AVSS + 0.7 V < (AINN or AINP) < AVDD – 1.25 V (2)

Absolute input levels (input signal level and common-mode level) should be maintained within these limits for best operation.

The multiplexer connects one of the two external differential inputs to the preamplifier inputs, in addition to internal connections for various self-test modes. Table 2 summarizes the multiplexer configurations for Figure 26.

Table 2. Multiplexer Modes

MUX[2:0]	SWITCHES	DESCRIPTION
000	S_1, S_5	AINP1 and AINN1 connected to preamplifier
001	S_2, S_6	AINP2 and AINN2 connected to preamplifier
010	S_3, S_4	Preamplifier inputs shorted together through 400Ω internal resistors
011	S_1, S_5, S_2, S_6	AINP1, AINN1 and AINP2, AINN2 connected together and to the preamplifier
100	S_6, S_7	External short, preamplifier inputs shorted to AINN2 (common-mode test)

The typical on-resistance (R_{ON}) of the multiplexer switch is 30 Ω. When the multiplexer is used to drive an external load on one input by a signal generator on the other input, on-resistance and on-resistance amplitude dependency can lead to measurement errors. Figure 27 shows THD versus load resistance and amplitude. THD improves with high-impedance loads and with lower amplitude drive signals. The data are measured with the circuit from Figure 28 with MUX[2:0] = 011.

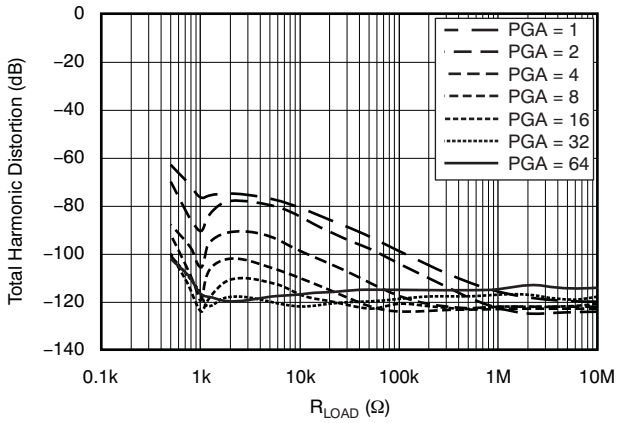


Figure 27. THD vs External Load and Signal Magnitude (PGA) (See Figure 28)

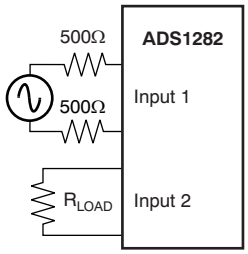


Figure 28. Driving an External Load Through the MUX

8.3.6 PGA (Programmable Gain Amplifier)

The PGA of the ADS1282-HT is a low-noise, continuous-time, differential-in/differential-out CMOS amplifier. The gain is programmable from 1 to 64, set by register bits, PGA[2:0]. The PGA differentially drives the modulator through 300-Ω internal resistors. A COG capacitor (10 nF typical) must be connected to CAPP and CAPN to filter modulator sampling glitches. The external capacitor also serves as an anti-alias filter. The corner frequency is given in Equation 3:

$$f_P = \frac{1}{6.3 \times 600 \times C} \quad (3)$$

Referring to Figure 29, amplifiers A_1 and A_2 are chopped to remove the offset, offset drift, and the 1/f noise. Chopping moves the effects to $f_{CLK}/128$ (8 kHz), which is safely out of the passband. Chopping can be disabled by setting the CHOP register bit = 0. With chopping disabled, the impedance of the PGA increases substantially (>> 1 GΩ). As shown in Figure 30, chopping maintains flat noise density; if chopping is disabled, however, it results in a rising 1/f noise profile.

The PGA has programmable gains from 1 to 64. Table 3 shows the register bit setting for the PGA and resulting full-scale differential range.

The specified output operating range of the PGA is shown in Equation 4:

$$AVSS + 0.4\ V < (CAPN \text{ or } CAPP) < AVDD - 0.4\ V \quad (4)$$

PGA output levels (signal plus common-mode) should be maintained within these limits for best operation.

Table 3. PGA Gain Settings

PGA[2:0]	GAIN	DIFFERENTIAL INPUT RANGE (V)(1)
000	1	±2.5
001	2	±1.25
010	4	±0.625
011	8	±0.312
100	16	±0.156
101	32	±0.078
110	64	±0.039

(1) V_{REF} = VREFP – VREFN = 5 V

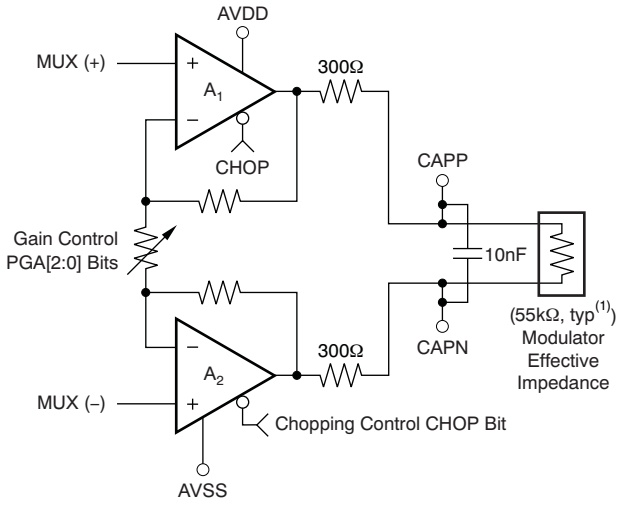


Figure 29. PGA Block Diagram

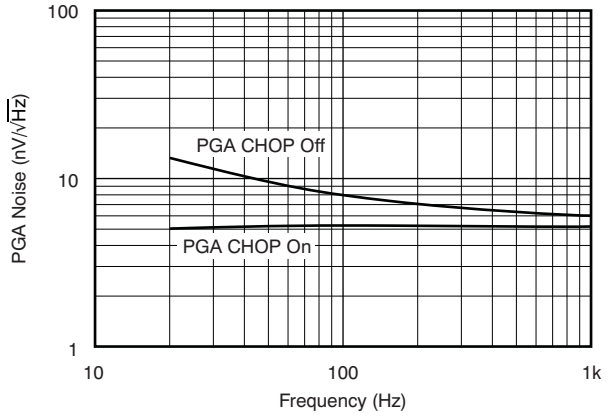


Figure 30. PGA Noise

8.3.7 ADC

The ADC block of the ADS1282-HT is composed of two sections: a high-accuracy modulator and a programmable digital filter.

8.3.8 Modulator

The high-performance modulator is an inherently-stable, fourth-order, ΔΣ, 2 + 2 pipelined structure, as Figure 31 shows. It shifts the quantization noise to a higher frequency (out of the passband) where digital filtering can easily remove it. The modulator can be filtered either by the on-chip digital filter or by use of post-processing filters.

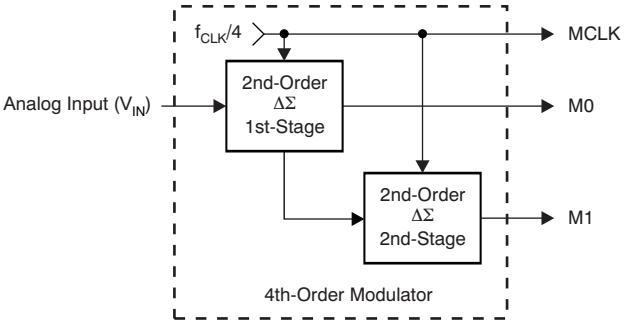


Figure 31. Fourth-Order Modulator

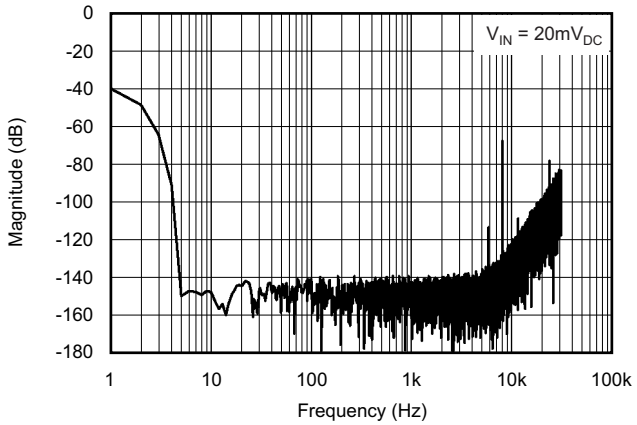
The modulator first stage converts the analog input voltage into a pulse-code modulated (PCM) stream. When the level of differential analog input (AINP – AINN) is near one-half the level of the reference voltage 1/2 × (VREFP – VREFN), the '1' density of the PCM data stream is at its highest. When the level of the differential analog input is near zero, the PCM '0' and '1' densities are nearly equal. At the two extremes of the analog input levels (+FS and –FS), the '1' density of the PCM streams is approximately 90% and 10%, respectively.

The modulator second stage produces a '1' density data stream designed to cancel the quantization noise of the first stage. The data streams of the two stages are then combined before the digital filter stage, as shown in Equation 5.

$$Y[n] = 3M0[n – 2] – 6M0[n –3] + 4M0[n – 4] + 9(M1[n] – 2M1[n – 1] + M1[n – 2]) \quad (5)$$

M0[n] represents the most recent first-stage output while M0[n – 1] is the previous first-stage output. When the modulator output is enabled, the digital filter shuts down to save power.

The modulator is optimized for input signals within a 4-kHz passband. As Figure 32 shows, the noise shaping of the modulator results in a sharp increase in noise greater than 6 kHz. The modulator has a chopped input structure that further reduces noise within the passband. The noise moves out of the passband and appears at the chopping frequency (f_{CLK} / 512 = 8 kHz). The component at 5.8 kHz is the tone frequency, shifted out of band by an external 20 mV/PGA offset. The frequency of the tone is proportional to the applied DC input and is given by PGA × V_{IN}/0.003 (in kHz).



1-Hz resolution

Figure 32. Modulator Output Spectrum

8.3.9 Modulator Over-Range

The ADS1282-HT modulator is inherently stable, and therefore, has predictable recovery behavior resulting from an input overdrive condition. The modulator does not exhibit self-resetting behavior, which often results in an unstable output data stream.

The ADS1282-HT modulator outputs a 1s density data stream at 90% duty cycle with the positive full-scale input signal applied (10% duty cycle with the negative full-scale signal). If the input is overdriven past 90% modulation, but less than 100% modulation (10% and 0% for negative overdrive, respectively), the modulator remains stable and continues to output the 1s density data stream. The digital filter may or may not clip the output codes to +FS or –FS, depending on the duration of the overdrive. When the input returns to the normal range from a long duration overdrive (worst case), the modulator returns immediately to the normal range, but the group delay of the digital filter delays the return of the conversion result to within the linear range (31 readings for linear phase FIR). 31 additional readings (62 total) are required for completely settled data.

If the inputs are sufficiently overdriven to drive the modulator to full duty cycle, all 1s or all 0s, the modulator enters a stable saturated state. The digital output code may clip to +FS or –FS, again depending on the duration. A small duration overdrive may not always clip the output code. When the input returns to the normal range, the modulator requires up to 12 modulator clock cycles (f_{MOD}) to exit saturation and return to the linear region. The digital filter requires an additional 62 conversions for fully settled data (linear phase FIR).

In the extreme case of over-range, either input is overdriven, exceeding the voltage of either analog supply voltage plus an internal ESD diode drop. The internal diodes begin to conduct and the signal on the input is clipped. When the input overdrive is removed, the diodes recover quickly. Keep in mind that the input current must be limited to 100-mA peak or 10-mA continuous if an overvoltage condition is possible.

8.3.10 Modulator Input Impedance

The modulator samples the buffered input voltage with an internal capacitor to perform conversions. The charging of the input sampling capacitor draws a transient current from the PGA output. The average value of the current can be used to calculate an effective input impedance of:

$$R_{EFF} = 1 / (f_{MOD} \times C_S) \quad (6)$$

where

- f_{MOD} = Modulator sample frequency, Mode = CLK / 4
- C_S = Input sampling capacitor (17 pF, typ)

The resulting modulator input impedance for CLK = 4.096 MHz is 55 kΩ. The modulator input impedance and the PGA output resistors result in a systematic gain error of –1%. C_S can vary ±20% over production lots, affecting the gain error.

8.3.11 Modulator Over-Range Detection (MFLAG)

The ADS1282-HT has a fast-responding over-range detection that indicates when the differential input exceeds ±100% full scale. The threshold tolerance is ±2.5%.The MFLAG output asserts high when in an over-range condition. As Figure 33 and Figure 34 illustrate, the absolute differential input is compared to 100% of range. The output of the comparator is sampled at the rate of f_{MOD} / 2, yielding the MFLAG output. The minimum MFLAG pulse width is f_{MOD} / 2.

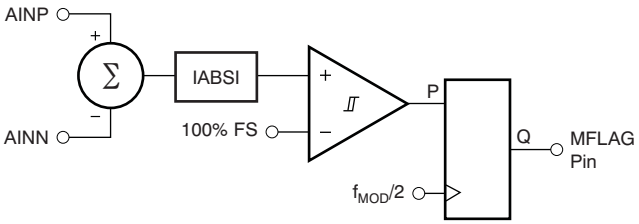


Figure 33. Modulator Over-Range Block Diagram

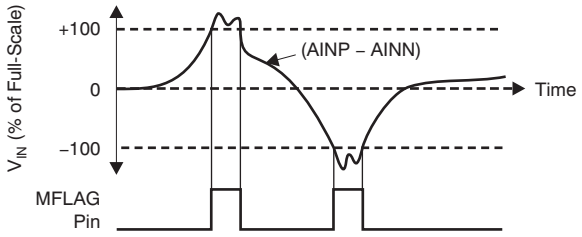


Figure 34. Modulator Over-Range Flag Operation

8.3.12 Voltage Reference Inputs (VREFP, VREFN)

The voltage reference for the ADS1282-HT is the differential voltage between VREFP and VREFN: V_{REF} = VREFP – VREFN. The reference inputs use a structure similar to that of the analog inputs with the circuitry of the reference inputs shown in Figure 35. The average load presented by the switched capacitor reference input can be modeled with an effective differential impedance of $R_{EFF} = t_{SAMPLE} / C_{IN}$ ($t_{SAMPLE} = 1/f_{MOD}$). The effective impedance of the reference inputs loads the external reference.

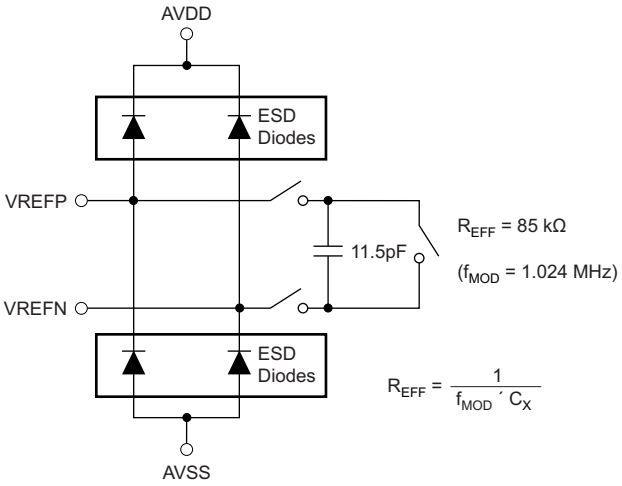


Figure 35. Simplified Reference Input Circuit

The ADS1282-HT reference inputs are protected by ESD diodes. In order to prevent these diodes from turning on, the voltage on either input must stay within the range shown in Equation 7:

$$AVSS - 300\ mV < (VREFP \text{ or } VREFN) < AVDD + 300\ mV \quad (7)$$

The minimum valid input for VREFN is AVSS – 0.1 V and maximum valid input for VREFP is AVDD + 0.1 V.

A high-quality 5 V reference voltage is necessary for achieving the best performance from the ADS1282-HT. Noise and drift on the reference degrade overall system performance, and it is critical that special care be given to the circuitry generating the reference voltages in order to achieve full performance. See *Application Information* for reference recommendations.

8.3.13 Digital Filter

The digital filter receives the modulator output and decimates the data stream. By adjusting the amount of filtering, tradeoffs can be made between resolution and data rate: filter more for higher resolution, filter less for higher data rate.

The digital filter is comprised of three cascaded filter stages: a variable-decimation, fifth-order sinc filter; a fixed-decimation FIR, low-pass filter (LPF) with selectable phase; and a programmable, first-order, high-pass filter (HPF), as shown in Figure 36.

The output can be taken from one of the three filter blocks, as Figure 36 shows. To implement the digital filter completely off-chip, select the filter bypass setting (modulator output). For partial filtering by the ADS1282-HT, select the sinc filter output. For complete on-chip filtering, activate both the sinc and FIR stages. The HPF can then be included to remove DC and low frequencies from the data. Table 4 shows the filter options.

Table 4. Digital Filter Selection

FILTR[1:0] BITS	DIGITAL FILTERS SELECTED
00	Bypass; modulator output mode
01	Sinc
10	Sinc + FIR
11	Sinc + FIR + HPF (low-pass and high-pass)

8.3.13.1 Sinc Filter Stage (Sinx/X)

The sinc filter is a variable decimation rate, fifth-order, low-pass filter. Data are supplied to this section of the filter from the modulator at the rate of f_{MOD} (f_{CLK}/4). The sinc filter attenuates the high-frequency noise of the modulator, then decimates the data stream into parallel data. The decimation rate affects the overall data rate of the converter; it is set by the DR[2:0] register bits, as shown in Table 5.

Equation 8 shows the scaled Z-domain transfer function of the sinc filter.

$$H(Z) = \left[\frac{1 - Z^{-N}}{N(1 - Z^{-1})} \right]^5 \quad (8)$$

Table 5. Sinc Filter Data Rates (Clk = 4.096 MHz)

DR[2:0] REGISTER	DECIMATION RATIO (N)	SINC DATA RATE (SPS)
000	128	8000
001	64	16000
010	32	32000
011	16	64000
100	8	128000

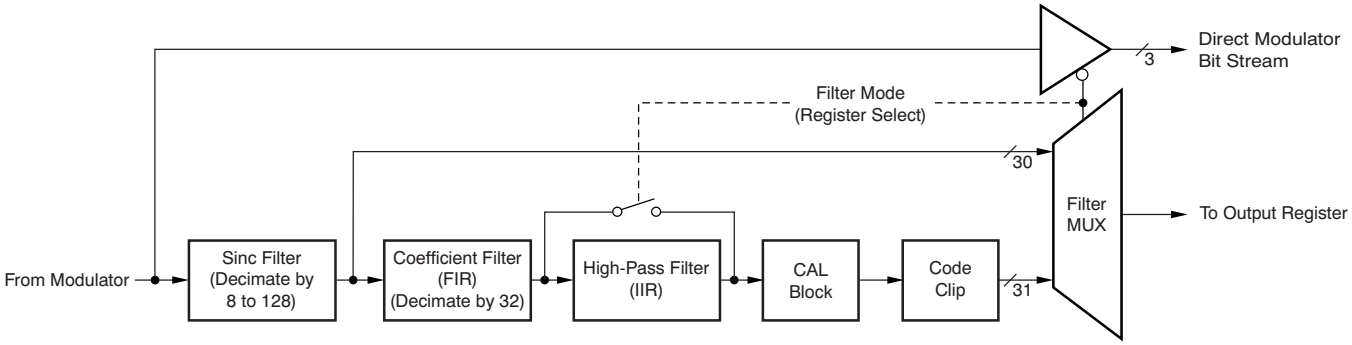


Figure 36. Digital Filter and Output Code Processing

Equation 9 shows the frequency domain transfer function of the sinc filter.

$$|H(f)| = \left| \frac{\sin\left(\frac{\pi N \times f}{f_{MOD}}\right)}{N \sin\left(\frac{\pi \times f}{f_{MOD}}\right)} \right|^5 \quad (9)$$

where

- N = Decimation ratio (see Table 5)

The sinc filter has notches (or zeroes) that occur at the output data rate and multiples thereof. At these frequencies, the filter has zero gain. Figure 37 shows the frequency response of the sinc filter and Figure 38 shows the roll-off of the sinc filter.

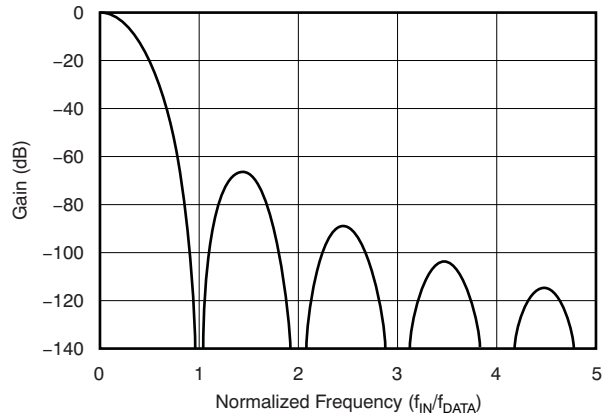


Figure 37. Sinc Filter Frequency Response

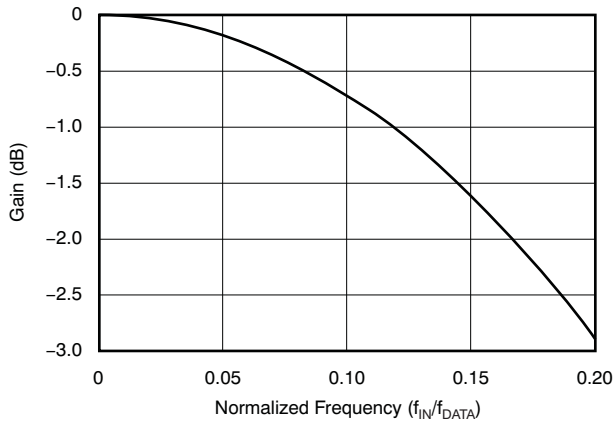


Figure 38. Sinc Filter Roll-Off

8.3.13.2 FIR Stage

The second stage of the ADS1282-HT digital filter is an FIR low-pass filter. Data are supplied to this stage from the sinc filter. The FIR stage is segmented into four sub-stages, as shown in Figure 39. The first two sub-stages are half-band filters with decimation ratios of 2. The third sub-stage decimates by 4 and the fourth sub-stage decimates by 2. The overall decimation of the FIR stage is 32. Two coefficient sets are used for the third and fourth sections, depending on the phase selection. 表 19 (in *器件支持*) lists the FIR stage coefficients. Table 6 lists the data rates and overall decimation ratio of the FIR stage.

Table 6. Fir Filter Data Rates

DR[2:0] REGISTER	DECIMATION RATIO (N)	FIR DATA RATE (SPS)
000	4096	250
001	2048	500
010	1024	1000
011	512	2000
100	256	4000

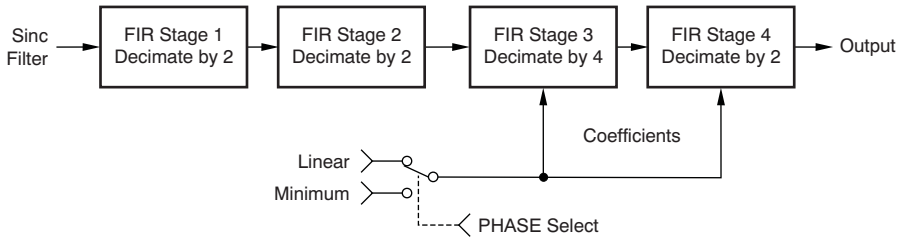


Figure 39. Fir Filter Sub-Stages

As shown in Figure 40, the FIR frequency response provides a flat passband to 0.375 of the data rate (±0.003-dB passband ripple). Figure 41 shows the transition from passband to stop band.

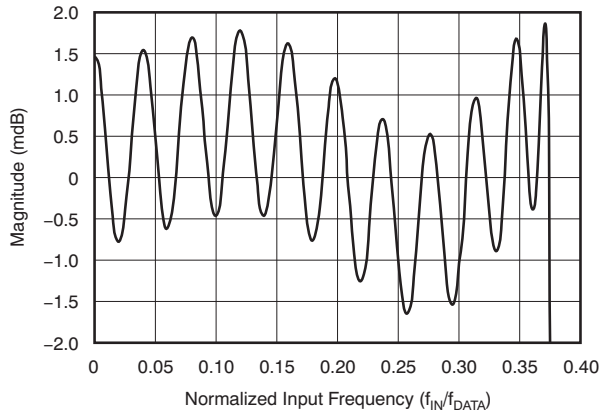


Figure 40. FIR Passband Magnitude Response (F_{DATA} = 500 Hz)

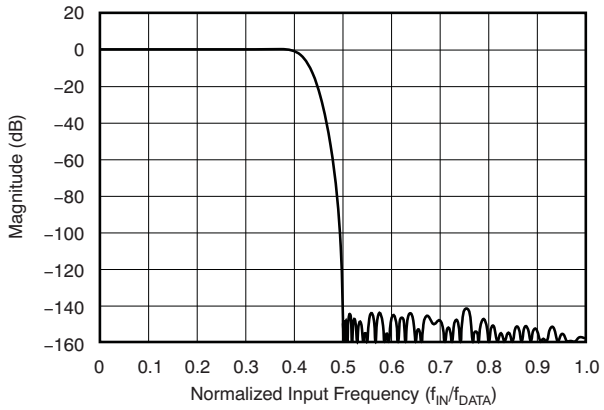


Figure 41. FIR Transition Band Magnitude Response

Although not shown in Figure 41, the passband response repeats at multiples of the modulator frequency ($Nf_{MOD} - f_0$ and $Nf_{MOD} + f_0$, where N = 1, 2, and so forth, and f_0 = passband). These image frequencies, if present in the signal and not externally filtered, fold back (or alias) into the passband and cause errors. A low-pass signal filter reduces the effect of aliasing. Often, the RC low-pass filter provided by the PGA output resistors and the external capacitor connected to CAPP and CAPN provides sufficient signal attenuation.

8.3.13.3 Group Delay and Step Response

The FIR block is implemented as a multi-stage FIR structure with selectable linear or minimum phase response. The passband, transition band, and stop band responses of the filters are nearly identical but differ in the respective phase responses.

8.3.13.3.1 Linear Phase Response

Linear phase filters exhibit constant delay time versus input frequency (that is, constant group delay). Linear phase filters have the property that the time delay from any instant of the input signal to the same instant of the output data is constant and is independent of the signal nature. This filter behavior results in essentially zero phase error when analyzing multi-tone signals. However, the group delay and settling time of the linear phase filter are somewhat larger than the minimum phase filter, as shown in Figure 42.

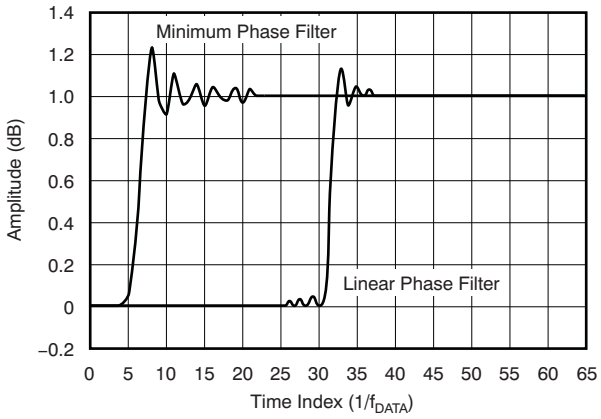


Figure 42. FIR Step Response

8.3.13.3.2 Minimum Phase Response

The minimum phase filter provides a short delay from the arrival of an input signal to the output, but the relationship (phase) is not constant versus frequency, as shown in Figure 43. The filter phase is selected by the PHS bit, as Table 7 shows.

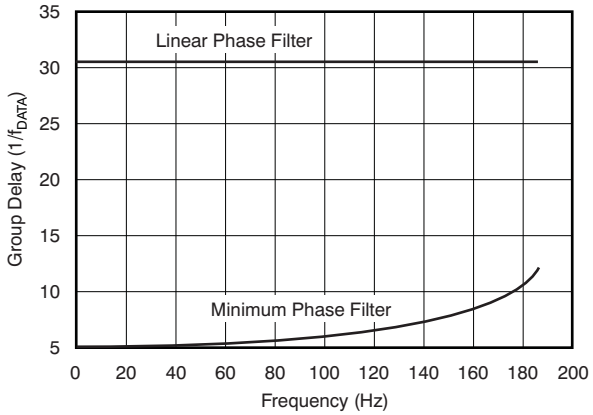


Figure 43. FIR Group Delay (F_{DATA} = 500 Hz)

Table 7. Fir Phase Selection

PHS BIT	FILTER PHASE
0	Linear
1	Minimum

8.3.13.4 HPF Stage

The last stage of the ADS1282-HT filter block is a first-order HPF implemented as an IIR structure. This filter stage blocks DC signals and rolls off low-frequency components below the cut-off frequency. The transfer function for the filter is shown in 公式 16 of the *器件支持*.

The high-pass corner frequency is programmed by registers HPF[1:0], in hexadecimal. Equation 10 is used to set the high-pass corner frequency. Table 8 lists example values for the high-pass filter.

$$HPF[1:0] = 65{,}536 \left[1 - \sqrt{1 - 2\frac{\cos \omega_N + \sin \omega_N - 1}{\cos \omega_N}} \right] \quad (10)$$

where

- HPF = High-pass filter register value (converted to hexadecimal)
- $\omega_N = 2\pi f_{HP}/f_{DATA}$ (normalized frequency, radians)
- f_{HP} = High-pass corner frequency (Hz)
- f_{DATA} = Data rate (Hz)

Table 8. High-Pass Filter Value Examples

f_{HP} (Hz)	DATA RATE (SPS)	HPF[1:0]
0.5	250	0337h
1	500	0337h
1	1000	019Ah

The HPF causes a small gain error, in which case the magnitude of the error depends on the ratio of f_{HP}/f_{DATA}. For many common values of (f_{HP}/f_{DATA}), the gain error is negligible. Figure 44 shows the gain error of the HPF. The gain error factor is illustrated in 公式 15 (see *器件支持*).

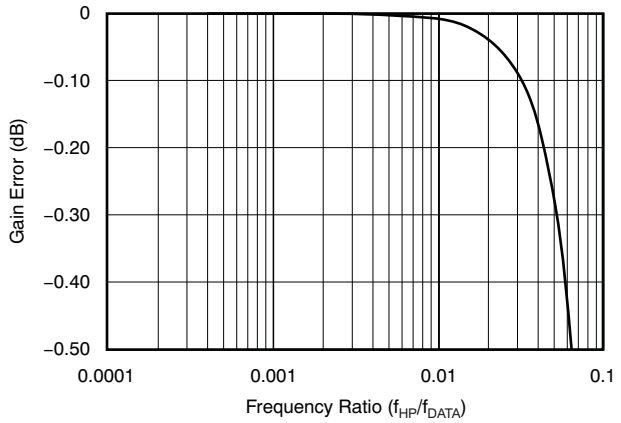


Figure 44. HPF Gain Error

Figure 45 shows the first-order amplitude and phase response of the HPF. In the case of applying step inputs or synchronizing, the settling time of the filter should be taken into account.

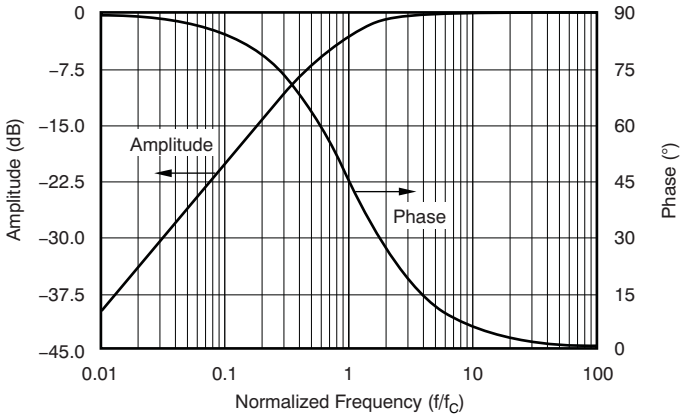


Figure 45. HPF Amplitude and Phase Response

8.3.14 Master Clock Input (CLK)

The ADS1282-HT requires a clock input for operation. The clock is applied to the CLK pin. The data conversion rate scales directly with the CLK frequency. Power consumption versus CLK frequency is relatively constant (see the *Typical Characteristics*).

As with any high-speed data converter, a high-quality, low-jitter clock is essential for optimum performance. Crystal clock oscillators are the recommended clock source. Make sure to avoid excess ringing on the clock input; keep the clock trace as short as possible and use a 50-Ω series resistor close to the source.

8.3.15 Synchronization (SYNC Pin and Sync Command)

The ADS1282-HT can be synchronized to an external event, as well as synchronized to other ADS1282-HT devices if the sync event is applied simultaneously.

The ADS1282-HT has two sources for synchronization: the SYNC input pin and the SYNC command. The ADS1282-HT also has two synchronizing modes: Pulse-sync and Continuous-sync. In Pulse-sync mode, the ADS1282-HT synchronizes to a single sync event. In Continuous-sync mode, either a single SYNC event is used to synchronize conversions or a continuous clock is applied to the pin with a period equal to integer multiples of the data rate. When the periods of the sync input and the $\overline{\text{DRDY}}$ output do not match, the ADS1282-HT re-synchronizes and conversions are restarted.

8.3.16 Pulse-Sync Mode

In pulse-sync mode, the ADS1282-HT stops and restarts the conversion process when a sync event occurs (by pin or command). When the sync event occurs, the device resets the internal memory; $\overline{\text{DRDY}}$ goes high (pulse SYNC mode) otherwise in Continuous SYNC mode, $\overline{\text{DRDY}}$ continues to toggle, and after the digital filter has settled, new conversion data are available, as shown in Figure 46 and *Pulse-Sync Timing Requirements*.

Resynchronization occurs on the next rising CLK edge after the rising edge of the SYNC pin or after the eighth rising SCLK edge for opcode SYNC commands. To be effective, the SYNC opcode should be broadcast to all devices simultaneously.

8.3.17 Continuous-Sync Mode

In Continuous-sync mode, either a single sync pulse or a continuous clock may be applied. When a single sync pulse is applied (rising edge), the device behaves similar to the Pulse-sync mode. However, in this mode, $\overline{\text{DRDY}}$ continues to toggle unaffected but the DOUT output is held low until data are ready, 63 $\overline{\text{DRDY}}$ periods later. When the conversion data are non-zero, new conversion data are ready (as shown in Figure 46).

When a continuous clock is applied to the SYNC pin, the period must be an integral multiple of the output data rate or the device re-synchronizes. Synchronization results in the restarting of the digital filter and an interruption of 63 readings (refer to *Pulse-Sync Timing Requirements*).

When the sync input is first applied, the device re-synchronizes (under the condition $t_{SYNC} \neq N / f_{DATA}$). $\overline{DRDY}$ continues to output but DOUT is held low until the new data are ready. Then, if SYNC is applied again and the period matches an integral multiple of the output data rate, the device freely runs without re-synchronization. The phase of the applied clock and output data rate ($\overline{DRDY}$) are not matched because of the initial delay of $\overline{DRDY}$ after SYNC is first applied. Figure 47 shows the timing for Continuous-Sync mode.

A SYNC clock input should be applied after the Continuous-Sync mode is set. The first rising edge of SYNC then causes a synchronization.

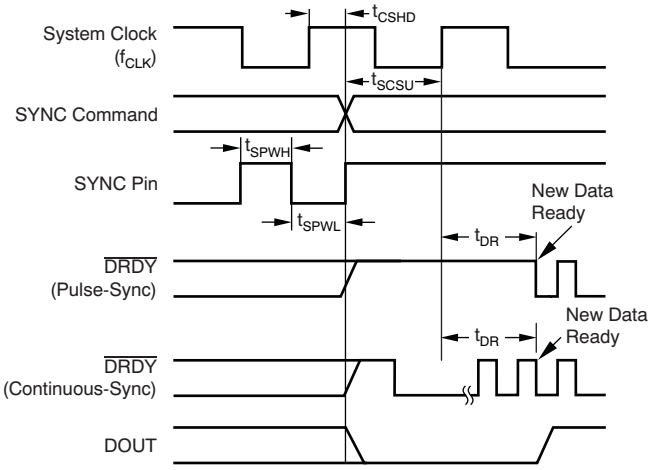


Figure 46. Pulse-Sync Timing, Continuous-Sync Timing With Single Sync

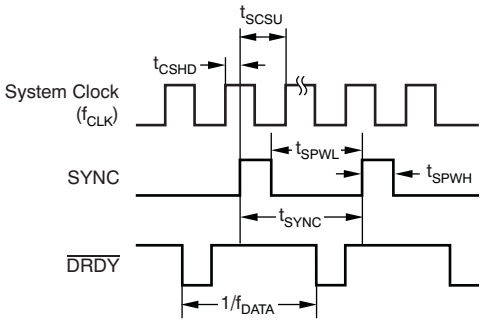


Figure 47. Continuous-Sync Timing With Sync Clock

8.3.18 Reset ($\overline{RESET}$ Pin and Reset Command)

The ADS1282-HT may be reset in two ways: toggle the $\overline{RESET}$ pin low or send a Reset command. When using the $\overline{RESET}$ pin, take it low and hold for at least $2 / f_{CLK}$ to force a reset. The ADS1282-HT is held in reset until the pin is released. By command, RESET takes effect on the next rising edge of f_{CLK} after the eighth rising edge of SCLK of the command. To ensure the Reset command can function, the SPI interface may require resetting itself; see *Serial Interface*.

In reset, registers are set to default and the conversions are synchronized on the next rising edge of CLK. New conversion data are available, as shown in Figure 48 and *Reset Timing Requirements*.

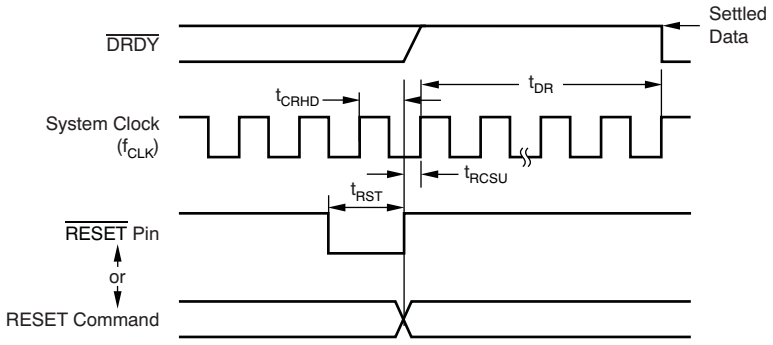


Figure 48. Reset Timing

8.3.19 Power-Down ($\overline{\text{PWDN}}$ Pin and Standby Command)

There are two ways to power-down the ADS1282-HT: take the $\overline{\text{PWDN}}$ pin low or send a Standby command. When the $\overline{\text{PWDN}}$ pin is pulled low, the internal circuitry is disabled to minimize power and the contents of the register settings are reset.

In power-down, the device outputs remain active and the device inputs must not float. When the Standby command is sent, the SPI port and the configuration registers are kept active. Figure 49 and Pulse-Sync Timing Requirements show the timing.

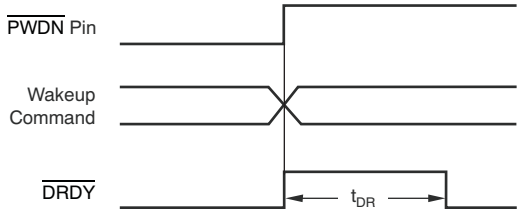


Figure 49. $\overline{\text{PWDN}}$ Pin and Wake-Up Command Timing (Pulse-Sync Timing Requirements Shows t_{DR})

8.3.20 Power-On Sequence

The ADS1282-HT has three power supplies: AVDD, AVSS, and DVDD. Figure 50 shows the power-on sequence of the ADS1282-HT. The power supplies can be sequenced in any order. The supplies [the difference of (AVDD – AVSS) and DVDD] generate an internal reset whose outputs are summed to generate a global internal reset. After the supplies have crossed the minimum thresholds, 2^{16} f_{CLK} cycles are counted before releasing the internal reset. After the internal reset is released, new conversion data are available, as shown in Figure 50 and *Pulse-Sync Timing Requirements*.

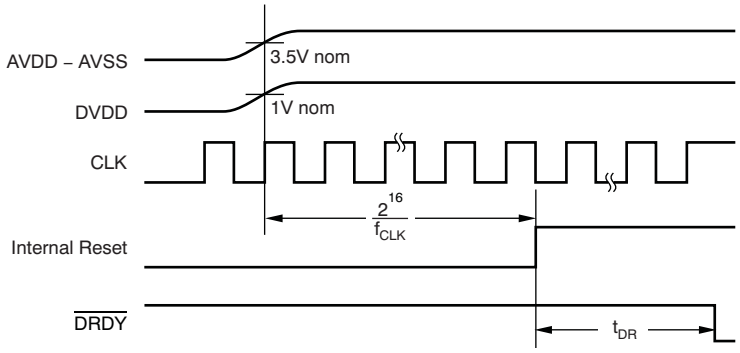


Figure 50. Power-On Sequence

8.3.21 Serial Interface

A serial interface is used to read the conversion data and access the configuration registers. The interface consists of three basic signals: SCLK, DIN, and DOUT. An additional output, $\overline{\text{DRDY}}$, transitions low in Read Data Continuous mode when data are ready for retrieval. Figure 51 shows the connection when multiple converters are used.

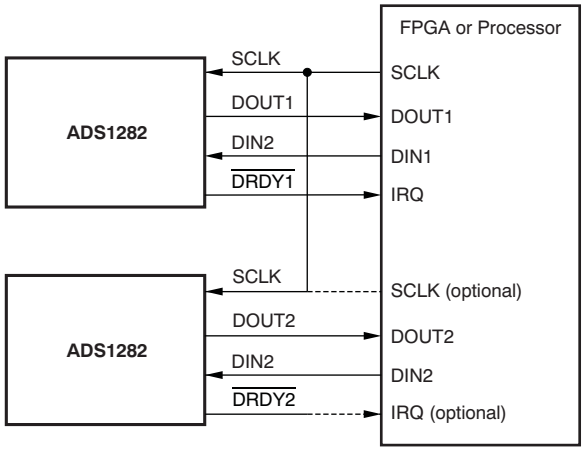


Figure 51. Interface for Multiple Devices

8.3.21.1 Serial Clock (SCLK)

The serial clock (SCLK) is an input that is used to clock data into (DIN) and out of (DOUT) the ADS1282-HT. This input is a Schmitt-trigger input that has a high degree of noise immunity. However, TI recommends keeping SCLK as clean as possible to prevent possible glitches from inadvertently shifting the data.

Data are shifted into DIN on the rising edge of SCLK and data are shifted out of DOUT on the falling edge of SCLK. If SCLK is held low for 64 $\overline{\text{DRDY}}$ cycles, data transfer or commands in progress terminate and the SPI interface resets. The next SCLK pulse starts a new communication cycle. This time-out feature can be used to recover the interface when a transmission is interrupted or SCLK inadvertently glitches. SCLK should remain low when not active.

8.3.21.2 Data Input (DIN)

The data input pin (DIN) is used to input register data and commands to the ADS1282-HT. Keep DIN low when reading conversion data in the Read Data Continuous mode (except when issuing a STOP Read Data Continuous command). Data on DIN are shifted into the converter on the rising edge of SCLK. In Pin mode, DIN is not used.

8.3.21.3 Data Output (DOUT)

The data output pin (DOUT) is used to output data from the ADS1282-HT. Data are shifted out on DOUT on the falling edge of SCLK.

8.3.21.4 Data Ready ($\overline{\text{DRDY}}$)

$\overline{\text{DRDY}}$ is an output; when it transitions low, this transition indicates new conversion data are ready, as shown in Figure 52. When reading data by the continuous mode, the data must be read within four CLK periods before $\overline{\text{DRDY}}$ goes low again or the data are overwritten with new conversion data. When reading data by the command mode, the read operation can overlap the occurrence of the next $\overline{\text{DRDY}}$ without data corruption.

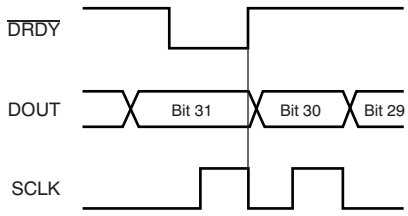


Figure 52. $\overline{\text{DRDY}}$ With Data Retrieval

$\overline{\text{DRDY}}$ resets high on the first falling edge of SCLK. Figure 52 and Figure 53 show the function of $\overline{\text{DRDY}}$ with and without data readback, respectively.

If data are not retrieved (no SCLK provided), $\overline{\text{DRDY}}$ pulses high for four f_{CLK} periods during the update time, as shown in Figure 53.

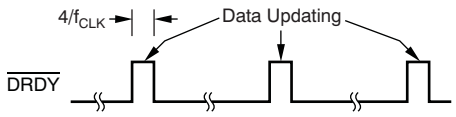


Figure 53. $\overline{\text{DRDY}}$ With No Data Retrieval

8.3.22 Data Format

The ADS1282-HT provides 32 bits of conversion data in binary twos complement format, as shown in Table 9. The LSB of the data is a redundant sign bit: '0' for positive numbers and '1' for negative numbers. However, when the output is clipped to +FS, the LSB = 1; when the output is clipped to –FS, the LSB = 0. If desired, the data readback may be stopped at 24 bits. In sinc filter mode, the output data are scaled by 1/2.

Table 9. Ideal Output Code Versus Input Signal

INPUT SIGNAL V_{IN} (AINP – AINN)	32-BIT IDEAL OUTPUT CODE(1)	
	FIR FILTER	SINC FILTER(2)
$> \frac{V_{REF}}{2 \times PGA}$	7FFFFFFFh	(3)
$\frac{V_{REF}}{2 \times PGA}$	7FFFFFFEh	3FFFFFFFh
$\frac{V_{REF}}{2PGA \times (2^{30} - 1)}$	00000002h	00000001h
0	00000000h	00000000h
$\frac{-V_{REF}}{2PGA \times (2^{30} - 1)}$	FFFFFFFFh	FFFFFFFFh
$\frac{-V_{REF}}{2PGA} \times \frac{2^{30}}{2^{30} - 1}$	80000001h	C0000000h
$< \frac{-V_{REF}}{2PGA} \times \frac{2^{30}}{2^{30} - 1}$	80000000h	(3)

(1) Excludes effects of noise, linearity, offset, and gain errors.
(2) Due to the reduction in oversampling ratio (OSR) related to the sinc filter high data rates, full 32-bit available resolution is reduced.
(3) In sinc filter mode, the output does not clip at half-scale code when the full-scale range is exceeded.

8.3.23 Reading Data

The ADS1282-HT has two ways to read conversion data: Read Data Continuous and Read Data By Command.

8.3.23.1 Read Data Continuous

In the Read Data Continuous mode, the conversion data are shifted out directly from the device without the need for sending a read command. This mode is the default mode at power-on. This mode is also enabled by the RDATAC command. When $\overline{\text{DRDY}}$ goes low, indicating that new data are available, the MSB of data appears on DOUT, as shown in Figure 54. The data are normally read on the rising edge of SCLK, at the occurrence of the first falling edge of SCLK, $\overline{\text{DRDY}}$ returns high. After 32 bits of data have been shifted out, further SCLK transitions cause DOUT to go low. If desired, the read operation may be stopped at 24 bits. The data shift operation must be completed within four CLK periods before $\overline{\text{DRDY}}$ falls again or the data may be corrupted.

When a Stop Read Data Continuous command is issued, the $\overline{\text{DRDY}}$ output is blocked but the ADS1282-HT continues conversions. In stop continuous mode, the data can only be read by command.

8.3.23.2 Read Data by Command

The Read Data Continuous mode is stopped by the SDATAC command. In this mode, conversion data are read by command. In the Read Data By Command mode, a read data command must be sent to the device for each data conversion (as shown in Figure 55). When the read data command is received (on the eighth SCLK rising edge), data are available to read only when $\overline{\text{DRDY}}$ goes low (t_{DR}). When $\overline{\text{DRDY}}$ goes low, conversion data appear on DOUT. The data may be read on the rising edge of SCLK.

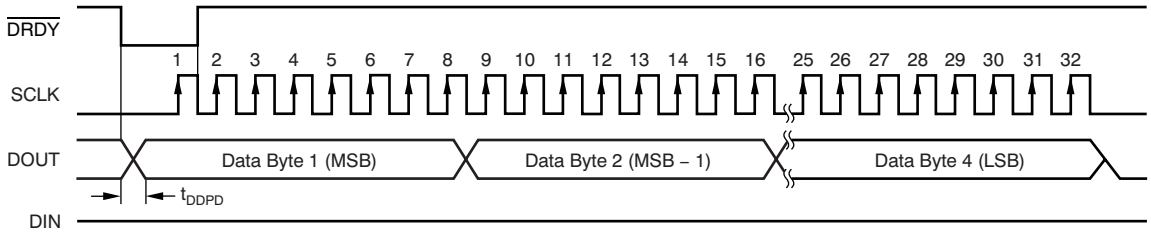


Figure 54. Read Data Continuous

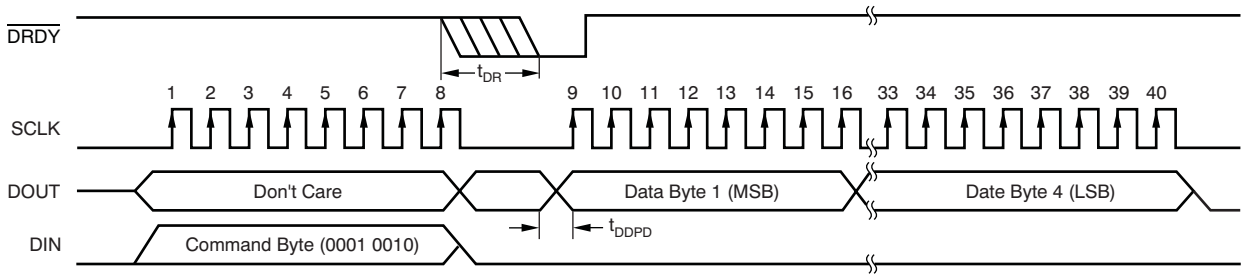


Figure 55. Read Data By Command, Rdata (T_{DDPD} Timing Is Given In *Read Data Timing Requirements*)

8.3.24 One-Shot Operation

The ADS1282-HT can perform very power-efficient, one-shot conversions using the STANDBY command while under software control. Figure 73 shows this sequence. First, issue the STANDBY command to set the Standby mode.

When ready to make a measurement, issue the WAKEUP command. Monitor $\overline{\text{DRDY}}$; when it goes low, the fully settled conversion data are ready and may be read directly in Read Data Continuous mode. Afterwards, issue another STANDBY command. When ready for the next measurement, repeat the cycle starting with another WAKEUP command.

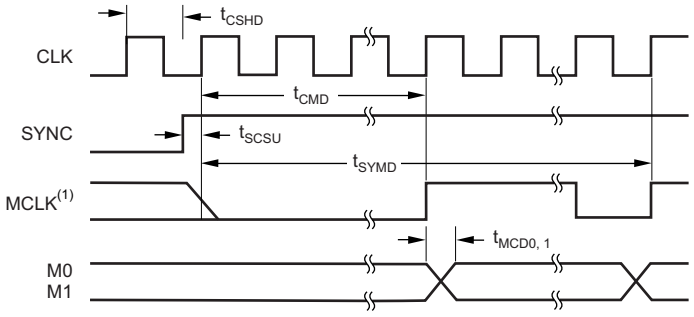
8.4 Device Functional Modes

8.4.1 Modulator Output Mode

The modulator digital stream output is accessible directly, bypassing and disabling the internal digital filter. The modulator output mode is activated by setting the CONFIG0 register bits FILTR[1:0] = 00. Pins M0 and M1 then become the modulator data outputs and the MCLK becomes the modulator clock output. When not in the modulator mode, these pins are inputs and must be tied.

The modulator output is composed of three signals: one output for the modulator clock (MCLK) and two outputs for the modulator data (M0 and M1). The modulator clock output rate is f_{MOD} (f_{CLK} / 4). The SYNC input resets the MCLK phase, as shown in Figure 56. The SYNC input is latched on the rising edge of CLK. The MCLK resets and the next rising edge of MCLK occurs five CLK periods later.

The modulator output data are two bits wide, which must be merged together before being filtered. Use the time domain equation of Equation 5 to merge the data outputs.



(1) MCLK = f_{CLK} / 4.

Figure 56. Modulator Mode Timing

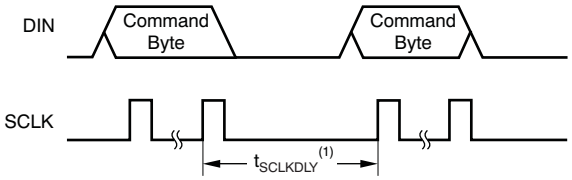
8.5 Programming

8.5.1 Commands

The commands listed in Table 10 control the operation of the ADS1282-HT. Most commands are stand-alone (that is, 1 byte in length); the register reads and writes require a second command byte in addition to the actual data bytes.

A delay of 24 f_{CLK} cycles between commands and between bytes within a command is required, starting from the last SCLK rising edge of one command to the first SCLK rising edge of the following command. This delay is shown in Figure 57.

In Read Data Continuous mode, the ADS1282-HT places conversion data on the DOUT pin as SCLK is applied. As a consequence of the potential conflict of conversion data on DOUT and data placed on DOUT resulting from a register or Read Data By Command operation, it is necessary to send a STOP Read Data Continuous command before Register or Data Read By Command. The STOP Read Data Continuous command disables the direct output of conversion data on the DOUT pin.



(1) $t_{SCLKDLY}$ = 24/f_{CLK} (min).

Figure 57. Consecutive Commands

Programming (continued)

Table 10. Command Descriptions

COMMAND	TYPE	DESCRIPTION	1st COMMAND BYTE(1)(2)	2nd COMMAND BYTE(3)
WAKEUP	Control	Wake-up from Standby mode	0000 000X (00h or 01h)	
STANDBY	Control	Enter Standby mode	0000 001X (0 h or 03h)	
SYNC	Control	Synchronize the A/D conversion	0000 010X (04h or 5h)	
$\overline{\text{RESET}}$	Control	Reset registers to default values	0000 011X (06h or 07h)	
RDATAC	Control	Read data continuous	0001 0000 (10h)	
SDATAC	Control	Stop read data continuous	0001 0001 (11h)	
RDATA	Data	Read data by command(4)	0001 0010 (12h)	
RREG	Register	Read *nnnnn* register(s) at address *rrrrr*(4)	00r rrrr (20h + 000r rrrr)	000n nnnn (00h + n nnnn)
WREG	Register	Write *nnnnn* register(s) at address *rrrrr*	010r rrrr (40h + 000r rrrr)	000n nnnn (00h + n nnnn)
OFSCAL	Calibration	Offset calibration	0110 0000 (60h)	
GANCAL	Calibration	Gain calibration	0110 0001 (61h)	

(1) X = Don't care.
(2) rrrrr = starting address for register read and write commands.
(3) nnnnn = number of registers to be read/written – 1. For example, to read/write three registers, set *nnnnn* = 2 (00010).
(4) Required to cancel Read Data Continuous mode before sending a command.

8.5.1.1 WAKEUP: Wake-Up from Standby Mode

This command is used to exit the standby mode. Upon sending the command, the time for the first data to be ready is illustrated in Figure 49 and Table 9. Sending this command during normal operation has no effect; for example, reading data by the Read Data Continuous method with DIN held low.

8.5.1.2 STANDBY: Standby Mode

This command places the ADS1282-HT into Standby mode. In Standby, the device enters a reduced power state where a low quiescent current remains to keep the register settings and SPI interface active. For complete device shutdown, take the $\overline{\text{PWDN}}$ pin low (register settings are not saved). To exit Standby mode, issue the WAKEUP command. The operation of Standby mode is shown in Figure 58.

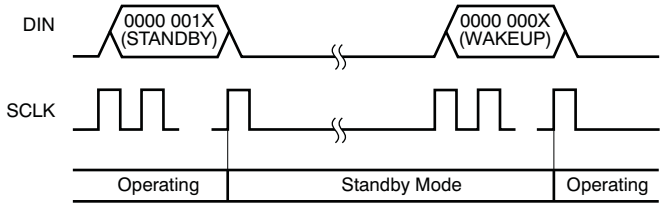


Figure 58. Standby Command Sequence

8.5.1.3 SYNC: Synchronize the A/D Conversion

This command synchronizes the A/D conversion. Upon receipt of the command, the reading in progress is cancelled and the conversion process is re-started. In order to synchronize multiple ADS1282-HTs, the command must be sent simultaneously to all devices. The SYNC pin must be high for this command.

8.5.1.4 RESET: Reset the Device

The RESET command resets the registers to default values, enables the Read Data Continuous mode, and restarts the conversion process; the RESET command is functionally the same as the $\overline{\text{RESET}}$ pin. See Figure 48 for the RESET command timing.

8.5.1.5 RDATAC: Read Data Continuous

This command enables the Read Data Continuous mode (default mode). In this mode, conversion data can be read from the device directly without the need to supply a data read command. Each time $\overline{\text{DRDY}}$ falls low, new data are available to read. See *Read Data Continuous* for more details.

8.5.1.6 SDATAC: Stop Read Data Continuous

This command stops the Read Data Continuous mode. Exiting the Read Data Continuous mode is required before sending Register and Data read commands. This command suppresses the $\overline{\text{DRDY}}$ output, but the ADS1282-HT continues conversions.

8.5.1.7 RDATA: Read Data By Command

This command reads the conversion data. See *Read Data by Command* for more details.

8.5.1.8 RREG: Read Register Data

This command is used to read single or multiple register data. The command consists of a two-byte op-code argument followed by the output of register data. The first byte of the op-code includes the starting address, and the second byte specifies the number of registers to read – 1.

First command byte: 001r rrrr, where *rrrrr* is the starting address of the first register.

Second command byte: 000n nnnn, where *nnnnn* is the number of registers – 1 to read.

Starting with the 16th falling edge of SCLK, the register data appear on DOUT.

The RREG command is illustrated in Figure 59. The a delay of 24 f_{CLK} cycles is required between each byte transaction.

8.5.1.9 WREG: Write to Register

This command writes single or multiple register data. The command consists of a two-byte op-code argument followed by the input of register data. The first byte of the op-code contains the starting address and the second byte specifies the number of registers to write – 1.

First command byte: 001r rrrr, where *rrrrr* is the starting address of the first register.

Second command byte: 000n nnnn, where *nnnnn* is the number of registers – 1 to write.

Data byte(s): one or more register data bytes, depending on the number of registers specified.

Figure 60 illustrates the WREG command.

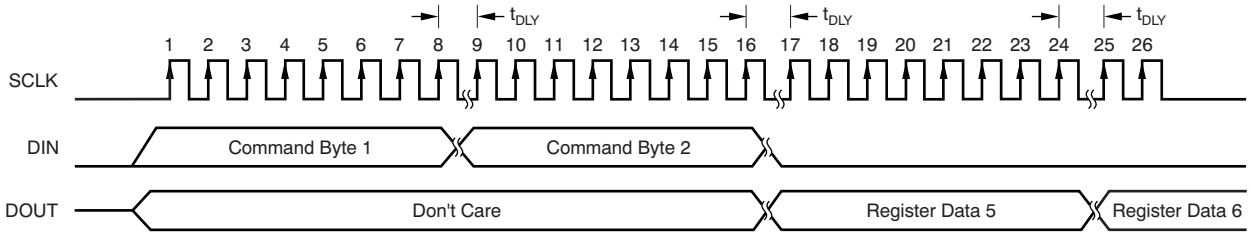
A delay of 24 f_{CLK} cycles is required between each byte transaction.

8.5.1.10 OFSCAL: Offset Calibration

This command performs an offset calibration. The inputs to the converter (or the inputs to the external pre-amplifier) should be zeroed and allowed to stabilize before sending this command. The offset calibration register updates after this operation. See *Calibration Commands* for more details.

8.5.1.11 GANCAL: Gain Calibration

This command performs a gain calibration. The inputs to the converter should have a stable DC input, preferably close to (but not exceeding) positive full-scale. The gain calibration register updates after this operation. See *Calibration Commands* for more details.



Example: Read six registers, starting at register 05h (OFC0)
Command Byte 1 = 0010 0101
Command Byte 2 = 0000 0101

Figure 59. Read Register Data (Shows t_{DLY})

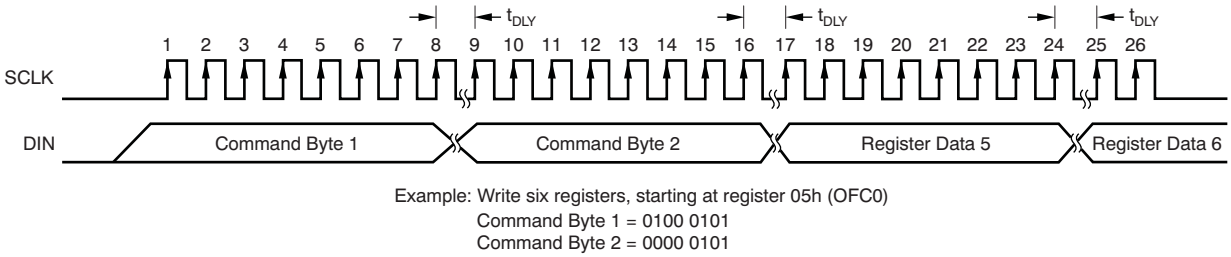


Figure 60. Write Register Data (Shows t_{DLY})

$$t_{DLY} = 24 / f_{CLK} \quad (11)$$

8.5.2 Calibration Commands

Calibration commands may be sent to the ADS1282-HT to calibrate the conversion data. The values of the offset and gain calibration registers are internally written to perform calibration. The appropriate input signals must be applied to the ADS1282-HT inputs before sending the commands. Use slower data rates to achieve more consistent calibration results; this effect is a byproduct of the lower noise that these data rates provide. Also, if calibrating at power-on, be sure the reference voltage is fully settled.

Figure 61 shows the calibration command sequence. After the analog input voltage (and reference) have stabilized, send the Stop Data Continuous command followed by the SYNC and Read Data Continuous commands. 64 data periods later, $\overline{DRDY}$ goes low. After $\overline{DRDY}$ goes low, send the Stop Data Continuous, then the Calibrate command followed by the Read Data Continuous command. After 16 data periods, calibration is complete and conversion data may be read at this time. The SYNC input must remain high during the calibration sequence.

The calibration commands apply to specific PGA settings. If the PGA is changed, recalibration is necessary. Calibration is bypassed in the sinc filter mode.

8.5.2.1 OFSCAL Command

The OFSCAL command performs an offset calibration. Before sending the offset calibration command, a *zero* input signal must be applied to the ADS1282-HT and the inputs allowed to stabilize. When the command is sent, the ADS1282-HT averages 16 readings and then writes this value to the OFC register. The contents of the OFC register may be subsequently read or written. During offset calibration, the full-scale correction is bypassed.

8.5.2.2 GANCAL Command

The GANCAL command performs a gain calibration. Before sending the GANCAL command, a DC input signal must be applied that is in the range of, but not exceeding, positive or negative full-scale. After the signal has stabilized, the command can be sent. The ADS1282-HT averages 16 readings, then computes the value that compensates for the gain error. The gain correction value is then written to the FSC register. The contents of the GANCAL register may be subsequently read or written. While the gain calibration command corrects for gain errors greater than 1 (gain correction <1), to avoid input overload, the analog inputs cannot exceed full-scale range. The gain calibration should be performed after the offset calibration.

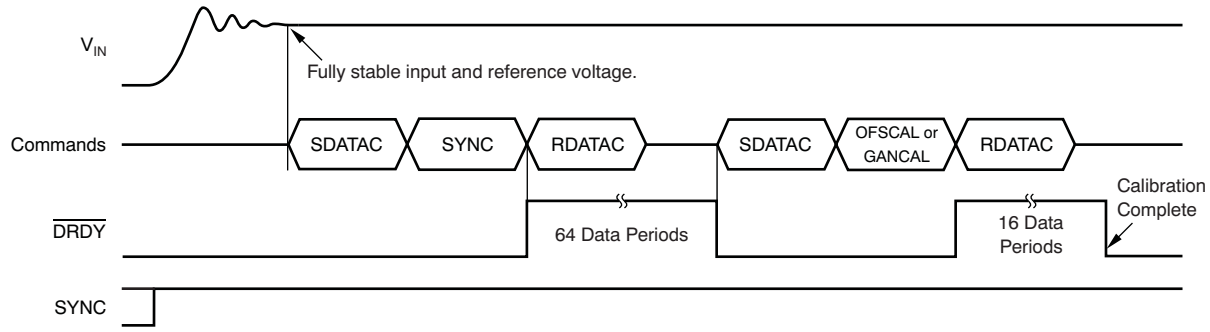


Figure 61. Offset/Gain Calibration Timing

8.5.3 User Calibration

System calibration of the ADS1282-HT can be performed without using the calibration commands. This procedure requires the calibration values to be externally calculated and then written to the calibration registers. The steps for this procedure are:

1. Set the OFSCAL[2:0] register = 0h and GANCAL[2:0] = 400000h. These values set the offset and gain registers to 0 and 1, respectively.
2. Apply a *zero* differential input to the input of the system. Wait for the system to settle and then average *n* output readings. Higher numbers of averaged readings result in more consistent calibration. Write the averaged value to the OFC register.
3. Apply a differential positive or negative DC signal, or an AC signal, less than the *full-scale* input to the system. Wait for the system to settle and then average the *n* output readings.

The value written to the FSC registers is calculated by Equation 12.

DC signal calibration is shown in Equation 12. The expected output code is based on 31-bit output data.

$$\text{FSC[2:0]} = 400000\text{h} \times \left(\frac{\text{Expected Output Code}}{\text{Actual Output Code}} \right) \tag{12}$$

For AC signal calibration, use an RMS value of collected data (as shown in Equation 13).

$$\text{FSC[2:0]} = 400000\text{h} \times \frac{\text{Expected RMS Value}}{\text{Actual RMS Value}} \tag{13}$$

8.5.4 Configuration Guide

After RESET or power-on, the registers can be configured using the following procedure:

1. **Reset the serial interface.** Before using the serial interface, it may be necessary to recover the serial interface (undefined I/O power-up sequencing may cause false SCLK detection). To reset the SPI interface, toggle the $\overline{\text{RESET}}$ pin or, when in Read Data Continuous mode, hold SCLK low for 64 $\overline{\text{DRDY}}$ periods.
2. **Configure the registers.** The registers are configured by either writing to them individually or as a group. Software may be configured in either mode. The SDATAC command must be sent before register read/write operations to cancel the Read Data Continuous mode.
3. **Verify register data.** The register may be read back for verification of device communications.
4. **Set the data mode.** After register configuration, the device may be configured for Read Data Continuous mode, either by the Read Data Continuous command or configured in Read Data By Register mode using SDATAC command.
5. **Synchronize readings.** Whenever SYNC is high, the ADS1282-HT freely runs the data conversions. To stop and re-sync the conversions, take SYNC low and then high.
6. **Read data.** If the Read Data Continuous mode is active, the data are read directly after $\overline{\text{DRDY}}$ falls by applying SCLK pulses. If the Read Data Continuous mode is inactive, the data can only be read by Read Data By Command. The Read Data opcode command must be sent in this mode to read each conversion result ($\overline{\text{DRDY}}$ only asserts after each read data command is sent).

8.6 Register Maps

8.6.1 ADS1282-HT Register Map Information

Collectively, the registers contain all the information needed to configure the part, such as data rate, filter selection, calibration, and so forth. The registers are accessed by the RREG and WREG commands. The registers can be accessed individually or as a block of registers by sending or receiving consecutive bytes. After a register write operation the ADC resets, resulting in an interruption of 63 readings.

Table 11. ADS1282-HT Register Map

ADDRESS	REGISTER	RESET VALUE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	ID	X0h	ID3	ID2	ID1	ID0	0	0	0	0
01h	CONFIG0	52h	SYNC	MODE	DR2	DR1	DR0	PHS	FILTR1	FILTR0
02h	CONFIG1	08h	0	MUX2	MUX1	MUX0	CHOP	PGA2	PGA1	PGA0
03h	HPF0	32h	HPF07	HPF06	HPF05	HPF04	HPF03	HPF02	HPF01	HPF00
04h	HPF1	03h	HPF15	HPF14	HPF13	HPF12	HPF11	HPF10	HPF09	HPF08
05h	OFC0	00h	OFC07	OFC06	OFC05	OFC04	OFC03	OFC02	OFC01	OFC00
06h	OFC1	00h	OFC15	OFC14	OFC13	OFC12	OFC11	OFC10	OFC09	OFC08
07h	OFC2	00h	OFC23	OFC22	OFC21	OFC20	OFC19	OFC18	OFC17	OFC16
08h	FSC0	00h	FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00
09h	FSC1	00h	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08
0Ah	FSC2	40h	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16

8.6.2 ID Register

Figure 62. ID: ID Register (Address 00h)

7	6	5	4	3	2	1	0
ID3	ID2	ID1	ID0	Reserved			
				0	0	0	0

Reset value = X0h

Table 12. ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	ID[3:0]			Factory-programmed identification bits (read-only)
3:0	Reserved			Always write '0'

8.6.3 Configuration Registers

8.6.3.1 Configuration Register 0

Figure 63. CONFIG0: Configuration Register 0 (Address 01h)

7	6	5	4	3	2	1	0
SYNC	MODE	DR2	DR1	DR0	PHASE	FILTR1	FILTR0

Reset value = 52h

Table 13. Configuration Register 0 Field Descriptions

Bit	Field	Type	Reset	Description
7	SYNC			Synchronization mode 0: Pulse SYNC mode (default) 1: Continuous SYNC mode
6	MODE			1: High-resolution mode (default)
5:3	DR[2:0]			Data Rate Select(1) 000: 250SPS 001: 500SPS 010: 1000SPS (default) 011: 2000SPS 100: 4000SPS
2	PHASE			FIR Phase Response 0: Linear phase (default) 1: Minimum phase
1:0	FILTR[1:0]			Digital Filter Select Digital filter configuration 00: On-chip filter bypassed, modulator output mode 01: Sinc filter block only 10: Sinc + LPF filter blocks (default) 11: Sinc + LPF + HPF filter blocks

(1) Sample rate based on 4.096-Mhz clock.

8.6.3.2 Configuration Register 1

Figure 64. CONFIG1: Configuration Register 1 (Address 02h)

7	6	5	4	3	2	1	0
RSVD	MUX2	MUX1	MUX0	CHOP	PGA2	PGA1	PGA0
0							

Reset value = 08h

Table 14. Configuration Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved			Always write '0'
6:4	MUX[2:0]			MUX Select 000: AINP1 and AINN1 (default) 001: AINP2 and AINN2 010: Internal short via 400Ω 011:AINP1 and AINN1 connected to AINP2 and AINN2 100: External short to AINN2
3	CHOP			PGA Chopping Enable 0: PGA chopping disabled 1: PGA chopping enabled (default)
2:0	PGA[2:0]			PGA Gain Select 000: G = 1 (default) 001: G = 2 010: G = 4 011: G = 8 100: G = 16 101: G = 32 110: G = 64

8.6.4 HPF1 and HPF0

These two bytes (high-byte and low-byte, respectively) set the corner frequency of the high-pass filter.

8.6.4.1 High-Pass Filter Corner Frequency, Low Byte

Figure 65. HPF0: High-Pass Filter Corner Frequency, Low Byte (Address 03h)

7	6	5	4	3	2	1	0
HP07	HP06	HP05	HP04	HP03	HP02	HP01	HP00

Reset value = 32h

8.6.4.2 High-Pass Filter Corner Frequency, High Byte

Figure 66. HPF1: High-Pass Filter Corner Frequency, High Byte (Address 04h)

7	6	5	4	3	2	1	0
HP15	HP14	HP13	HP12	HP11	HP10	HP09	HP08

Reset value = 03h

8.6.5 OFC2, OFC1, OFC0

These three bytes set the offset calibration value.

8.6.5.1 Offset Calibration, Low Byte

Figure 67. OFC0: Offset Calibration, Low Byte (Address 05h)

7	6	5	4	3	2	1	0
OC07	OC06	OC05	OC04	OC03	OC02	OC01	OC00

Reset value = 00h

8.6.5.2 Offset Calibration, Mid Byte

Figure 68. OFC1: Offset Calibration, Mid Byte (Address 06h)

7	6	5	4	3	2	1	0
OC15	OC14	OC13	OC12	OC11	OC10	OC09	OC08

Reset value = 00h

8.6.5.3 Offset Calibration, High Byte

Figure 69. OFC2: Offset Calibration, High Byte (Address 07h)

7	6	5	4	3	2	1	0
OC23	OC22	OC21	OC20	OC19	OC18	OC17	OC16

Reset value = 00h

8.6.6 FSC2, FSC1, FSC0

These three bytes set the full-scale calibration value.

8.6.6.1 Full-Scale Calibration, Low Byte

Figure 70. FSC0: Full-Scale Calibration, Low Byte (Address 08h)

7	6	5	4	3	2	1	0
FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00

Reset value = 00h

8.6.6.2 Full-Scale Calibration, Mid Byte

Figure 71. FSC1: Full-Scale Calibration, Mid Byte (Address 09h)

7	6	5	4	3	2	1	0
FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08

Reset value = 00h

8.6.6.3 Full-Scale Calibration, High Byte

Figure 72. FSC2: Full-Scale Calibration, High Byte (Address 0Ah)

7	6	5	4	3	2	1	0
FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16

Reset value = 40h

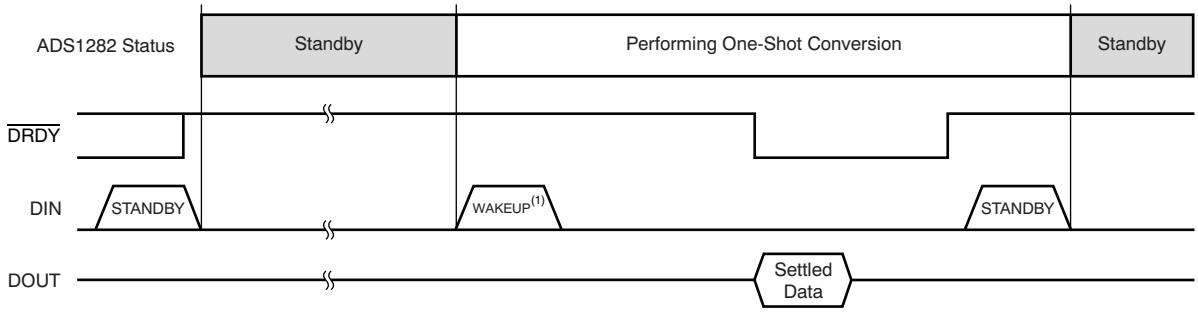
8.6.7 Offset and Full-Scale Calibration Registers

The conversion data can be scaled for offset and gain before yielding the final output code. As shown in Figure 74, the output of the digital filter is first subtracted by the offset register (OFC) and then multiplied by the full-scale register (FSC). Equation 14 shows the scaling:

$$\text{Final Output Data} = (\text{Input} - \text{OFC}[2:0]) \times \frac{\text{FSC}[2:0]}{400000\text{h}} \quad (14)$$

The values of the offset and full-scale registers are set by writing to them directly, or they are set automatically by calibration commands.

The offset and full-scale calibrations apply to specific PGA settings. When the PGA changes, the contents of these registers may have to be recalculated. Calibration is bypassed in the sinc filter mode.



(1) See Figure 49 and for time to new data.

Figure 73. One-Shot Conversions Using the Standby Command

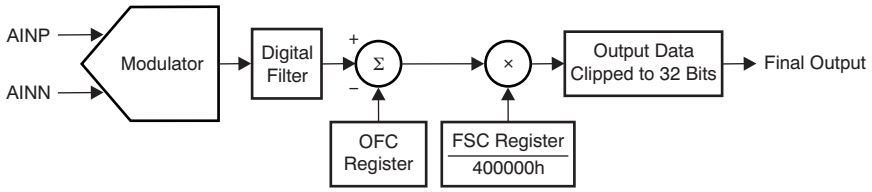


Figure 74. Calibration Block Diagram

8.6.7.1 OFC[2:0] Registers

The offset calibration is a 24-bit word, composed of three 8-bit registers, as shown in Table 17. The offset register is left-justified to align with the 32-bits of conversion data. The offset is in twos complement format with a maximum positive value of 7FFFFFh and a maximum negative value of 800000h. This value is subtracted from the conversion data. A register value of 00000h has no offset correction (default value). While the offset calibration register value can correct offsets ranging from –FS to +FS (as shown in Table 15), to avoid input overload, the analog inputs cannot exceed the full-scale range.

Table 15. Offset Calibration Values

OFC REGISTER	FINAL OUTPUT CODE(1)
7FFFFFh	80000000h
000001h	FFFFFF00h
000000h	00000000h
FFFFFFh	00000100h
800000h	7FFFFF00h

(1) Full 32-bit final output code with zero code input.

8.6.7.2 FSC[2:0] Registers

The full-scale calibration is a 24-bit word, composed of three 8-bit registers, as shown in Table 18. The full-scale calibration value is 24-bit, straight offset binary, normalized to 1 at code 400000h. Table 16 summarizes the scaling of the full-scale register. A register value of 400000h (default value) has no gain correction (gain = 1). While the gain calibration register value corrects gain errors greater than 1 (gain correction <1), the full-scale range of the analog inputs cannot be exceeded to avoid input overload.

Table 16. Full-Scale Calibration Register Values

FSC REGISTER	GAIN CORRECTION
800000h	2
400000h	1
200000h	0.5
000000h	0

Table 17. Offset Calibration Word

REGISTER	BYTE	BIT ORDER							
OFC0	LSB	7	6	5	4	3	2	1	0 (LSB)
OFC1	MID	15	14	13	12	11	10	9	8
OFC2	MSB	23 (MSB)	22	21	20	19	18	17	16

Table 18. Full-Scale Calibration Word

REGISTER	BYTE	BIT ORDER							
FSC0	LSB	7	6	5	4	3	2	1	0 (LSB)
FSC1	MID	15	14	13	12	11	10	9	8
FSC2	MSB	23 (MSB)	22	21	20	19	18	17	16

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

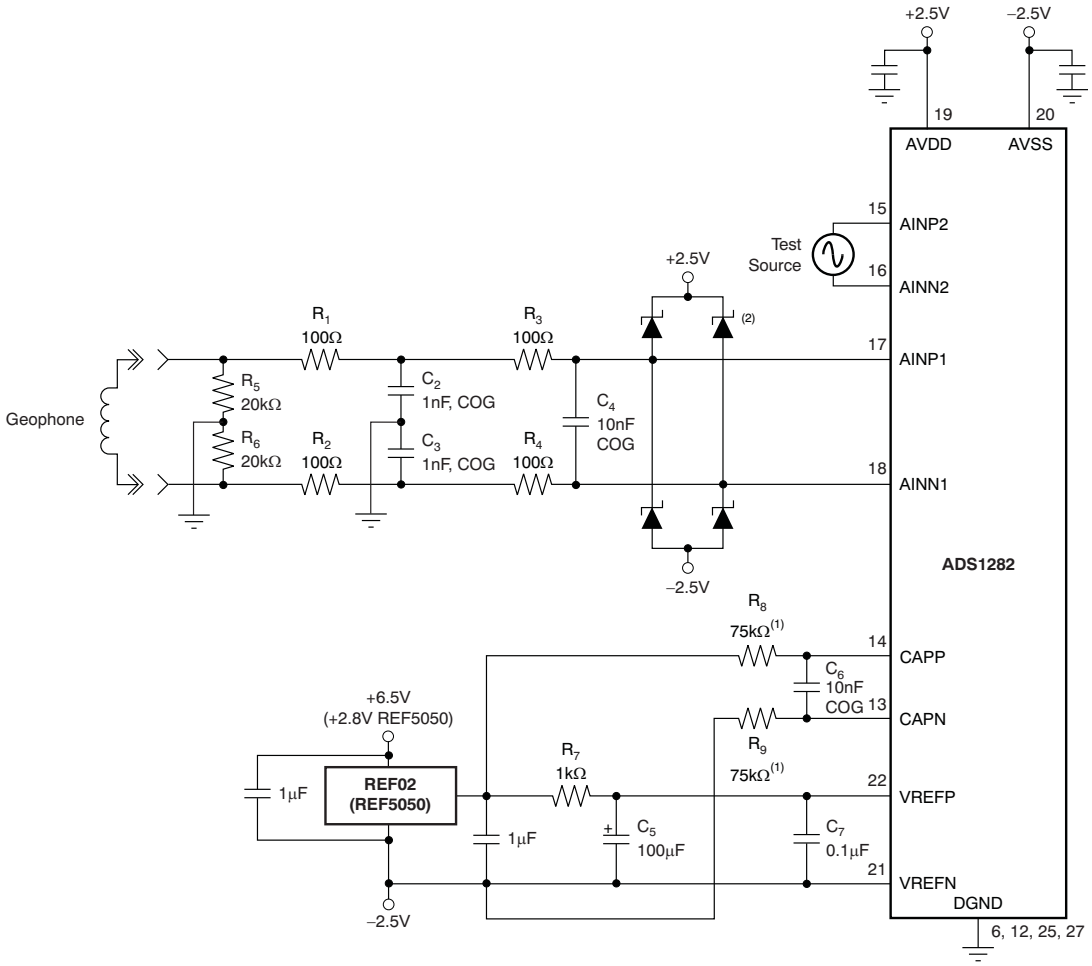
9.1 Application Information

The ADS1282-HT is a very-high-resolution ADC. Optimal performance requires giving special attention to the support circuitry and PCB design. Locate noisy digital components, such as microcontrollers, oscillators, and so forth, in an area of the PCB away from the converter or front-end components. Locating the digital components close to the power-entry point keeps the digital current path short and separate from sensitive analog components.

9.2 Typical Application

9.2.1 Geophone Interface Typical Application

Figure 75 shows a typical geophone front-end application. The application shows the ADS1282-HT operation with dual ±2.5-V analog supplies. The ADS1282-HT can also operate with a single 5-V analog supply.



(1) Optional 20-mV offset. Match to 0.1% to maintain CMR.

Figure 75. Geophone Interface Application

Typical Application (continued)

9.2.1.1 Detailed Design Procedure

The geophone input signal is filtered both differentially, by components C_4 and R_1 to R_4 and filtered independently by components C_2, C_3 and R_1, R_2. The differential filter removes high-frequency normal mode components from the input signal. The independent filters remove high-frequency components that are common to both input signals leads (common-mode filter). The recommended input filters may not be required for all applications depending on the system requirements.

Resistors R_5 and R_6 bias the signals inputs to midsupply (ground), and also provide the bias current return path for the ADS1282-HT inputs. For single-supply operation, set the bias to a low impedance 2.5 V (AVDD/2). Resistors R_5 and R_6 can also influence common-mode attenuation. To maintain good CMR performance, resistors R_5 and R_6 may require matching.

Diode clamps protect the ADS1282-HT inputs from voltage transients and overloads.

The REF02 5-V reference provides the reference to the ADS1282-HT. The reference output is filtered by the optional R_7 and C_5 filter network. The filter requires several seconds to settle after power-on. Capacitor C_7 provides high-frequency bypassing of the reference inputs and should be placed close to the ADS1282-HT pins. R_7 (1-kΩ) results in a systematic gain error (–1.2%).

Alternatively, the REF5050 (5-V) or REF5045 (4.5-V) reference can be used. The REF5045 reference has the advantage of operating from the 5-V power supply. The REF5050 requires 5.2-V minimum power supply.

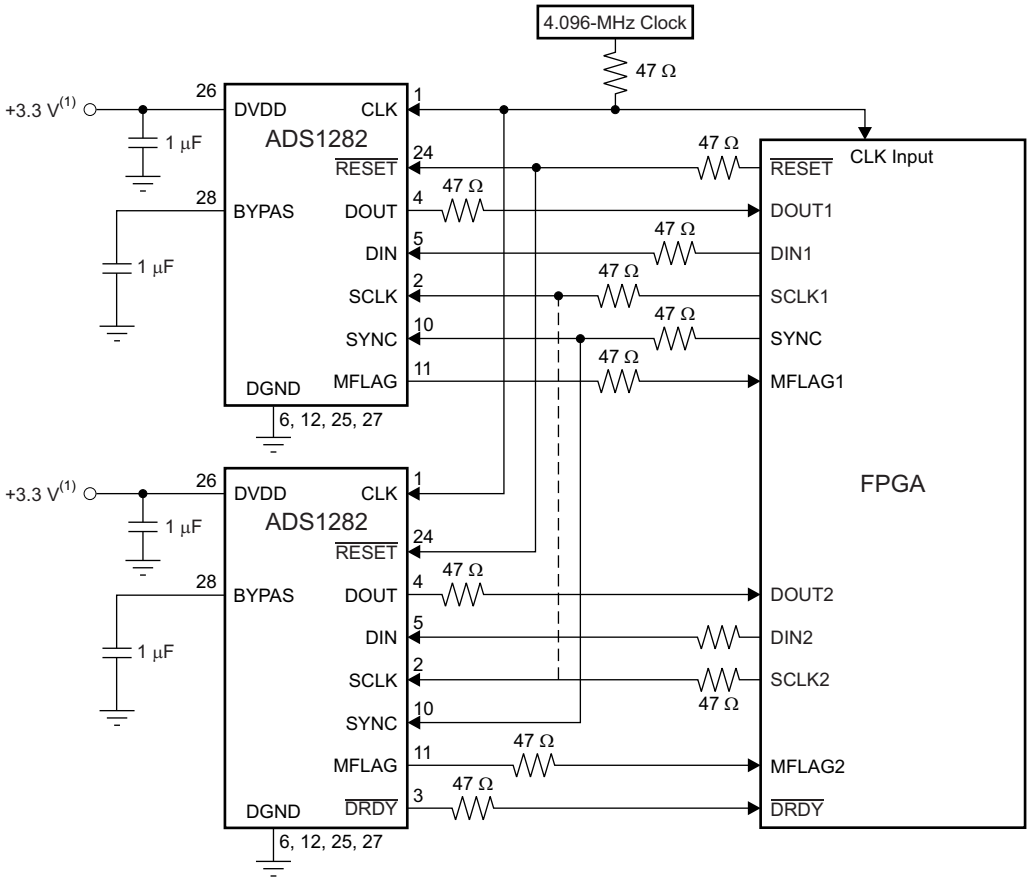
Optional components R_8, and R_9 provides a 20mV offset to the ADS1282-HT. The internal 300-Ω resistors form a voltage divider with the external resistors to provide the offset. The offset moves the low level idle tones out of the passband. The offset is independent of the PGA setting. To maintain good CMR performance, R_{10} and R_{11} should be matched to 0.1%, and the traces routed back directly to the reference.

Capacitor C_6 (10-nF) filters the PGA output glitches caused by sampling of the modulator. The capacitor also forms a low-pass filter on the input signal with a cut-off frequency ≠ 25 kHz.

9.2.2 Digital Connection to a Field Programmable Gate Array (FPGA) Device Typical Application

Figure 76 shows the digital connection to a field programmable gate array (FPGA) device. In this example, two ADS1282-HT devices are shown connected. The $\overline{\text{DRDY}}$ output from each ADS1282-HT device can be used; however, when the devices are synchronized, the $\overline{\text{DRDY}}$ output from only one device is sufficient. A shared SCLK line between the devices is optional.

Typical Application (continued)



NOTE: Dashed line is optional.

(1) For DVDD < 2.25 V, see the *Power Supply Recommendations*.

Figure 76. Microcontroller Interface With Dual ADS1282-HTs

9.2.2.1 Detailed Design Procedure

The modulator over-range flag (MFLAG) from each device ties to the FPGA. For synchronization, one SYNC control line connects all ADS1282-HT devices. The RESET line also connects to all ADS1282-HT devices.

For best performance, the FPGA and the ADS1282-HTs should operate from the same clock. Avoid ringing on the digital inputs. 47-Ω resistors in series with the digital traces can help to reduce ringing by controlling impedances. Place the resistors at the source (driver) end of the trace. Unused digital inputs should not float; use pullups or pulldowns to DVDD or GND. This includes the modulator data pins, M0, M1, and MCLK.

10 Power Supply Recommendations

The DVDD power supply operates over the range of 1.75 to 3.6 V. If DVDD is operated at less than 2.25 V, connect the DVDD pin to the BYPAS pin. If DVDD is greater than or equal to 2.25 V, do not connect DVDD to the BYPAS pin. Figure 77 shows this connection.

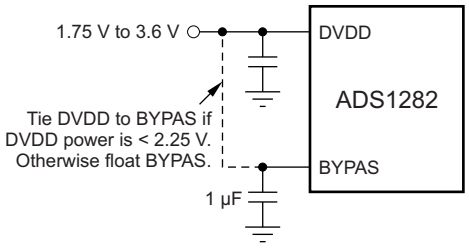


Figure 77. DVDD Power

11 器件和文档支持

11.1 器件支持

表 **19. FIR** 级系数

系数	第 **1** 部分	第 **2** 部分	第 **3** 部分		第 **4** 部分	
	换算系数 **= 1 / 8388608**		换算系数 **= 134217728**		换算系数 **= 134217728**	
			线性相位	最小相位	线性相位	最小相位
b_0	–10944	–774	–73	819	–132	11767
b_1	0	0	–874	8211	–432	133882
b_2	103807	8994	–4648	44880	–75	769961
b_3	0	0	–16147	174712	2481	2940447
b_4	–507903	–51663	–41280	536821	6692	8262605
b_5	0	0	–80934	1372637	7419	17902757
b_6	2512192	199523	–120064	3012996	–266	30428735
b_7	4194304	0	–118690	5788605	–10663	40215494
b_8	2512192	–629120	–18203	9852286	–8280	39260213
b_9	0	0	224751	14957445	10620	23325925
b_{10}	–507903	2570188	580196	20301435	22008	–1757787
b_{11}	0	4194304	893263	24569234	348	–21028126
b_{12}	103807	2570188	891396	26260385	–34123	–21293602
b_{13}	0	0	293598	24247577	–25549	–3886901
b_{14}	–10944	–629120	–987253	18356231	33460	14396783
b_{15}		0	–2635779	9668991	61387	16314388
b_{16}		199523	–3860322	327749	–7546	1518875
b_{17}		0	–3572512	–7171917	–94192	–12979500
b_{18}		–51663	–822573	–10926627	–50629	–11506007
b_{19}		0	4669054	–10379094	101135	2769794
b_{20}		8994	12153698	–6505618	134826	12195551
b_{21}		0	19911100	–1333678	–56626	6103823
b_{22}		–774	25779390	2972773	–220104	–6709466
b_{23}			27966862	5006366	–56082	–9882714
b_{24}			只显示一半；从 b_{22} 开始对称。	4566808	263758	–353347
b_{25}				2505652	231231	8629331
b_{26}				126331	–215231	5597927
b_{27}				–1496514	–430178	–4389168
b_{28}				–1933830	34715	–7594158
b_{29}				–1410695	580424	–428064
b_{30}				–502731	283878	6566217
b_{31}				245330	–588382	4024593
b_{32}				565174	–693209	–3679749
b_{33}				492084	366118	–5572954
b_{34}				231656	1084786	332589
b_{35}				–9196	132893	5136333
b_{36}				–125456	–1300087	2351253
b_{37}				–122207	–878642	–3357202
b_{38}				–61813	1162189	–3767666
b_{39}				–4445	1741565	1087392
b_{40}				22484	–522533	3847821
b_{41}				22245	–2490395	919792

器件支持 (接下页)

表 19. FIR 级系数 (接下页)

系数	第 1 部分	第 2 部分	第 3 部分		第 4 部分	
	换算系数 = 1 / 8388608		换算系数 = 134217728		换算系数 = 134217728	
			线性相位	最小相位	线性相位	最小相位
b_{42}				10775	–688945	–2918303
b_{43}				940	2811738	–2193542
b_{44}				–2953	2425494	1493873
b_{45}				–2599	–2338095	2595051
b_{46}				–1052	–4511116	–79991
b_{47}				-43	641555	–2260106
b_{48}				214	6661730	–963855
b_{49}				132	2950811	1482337
b_{50}				33	–8538057	1480417
b_{51}					–10537298	–586408
b_{52}					9818477	–1497356
b_{53}					41426374	–168417
b_{54}					56835776	1166800
b_{55}					只显示一半；从 b_{53} 开始对称。	644405
b_{56}						–675082
b_{57}						–806095
b_{58}						211391
b_{59}						740896
b_{60}						141976
b_{61}						–527673
b_{62}						–327618
b_{63}						278227
b_{64}						363809
b_{65}						–70646
b_{66}						–304819
b_{67}						–63159
b_{68}						205798
b_{69}						124363
b_{70}						–107173
b_{71}						–131357
b_{72}						31104
b_{73}						107182
b_{74}						15644
b_{75}						–71728
b_{76}						–36319
b_{77}						38331
b_{78}						38783
b_{79}						–13557
b_{80}						–31453
b_{81}						–1230
b_{82}						20983
b_{83}						7729
b_{84}						–11463
b_{85}						–8791

器件支持 (接下页)

表 19. FIR 级系数 (接下页)

系数	第 1 部分	第 2 部分	第 3 部分		第 4 部分	
	换算系数 = 1 / 8388608		换算系数 = 134217728		换算系数 = 134217728	
			线性相位	最小相位	线性相位	最小相位
b_{86}						4659
b_{87}						7126
b_{88}						–732
b_{89}						–4687
b_{90}						–976
b_{91}						2551
b_{92}						1339
b_{93}						–1103
b_{94}						–1085
b_{95}						314
b_{96}						681
b_{97}						16
b_{98}						–349
b_{99}						–96
b_{100}						144
b_{101}						78
b_{102}						-46
b_{103}						–42
b_{104}						9
b_{105}						16
b_{106}						0
b_{107}						-4

$$\text{HPF Gain} = \frac{1 + \sqrt{1 - 2\left(\frac{\cos\omega_N + \sin\omega_N - 1}{\cos\omega_N}\right)}}{2 - \left(\frac{\cos\omega_N + \sin\omega_N - 1}{\cos\omega_N}\right)} \tag{15}$$

有关该公式的使用示例，请参见*HPF Stage*。

11.1.1 HPF 传递函数

$$\text{HPF}(Z) = \frac{2 - a}{2} \times \frac{1 - Z^{-1}}{1 - bZ^{-1}} \tag{16}$$

其中，*b* 的计算公式如公式 17 所示：

$$b = \frac{\left(1 + (1 - a)^2\right)^2}{2} \tag{17}$$

表 **20.** 数据就绪时间 t_{DR}（正弦滤波器）

f_{DATA}	f_{CLK} (1)
128k	440
64k	616
32k	968
16k	1672
8k	2824

(1) 对于同时有同步命令和唤醒命令的情况，f_{CLK} = 从第八个 SCLK 上升沿后紧接着的下一个 CLK 上升沿到 $\overline{DRDY}$ 下降沿的 CLK 周期数。对于仅有唤醒命令的情况，减去两个 f_{CLK} 周期。

表 20 被*Pulse-Sync Timing Requirements*引用。

11.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS1282HPW	Active	Production	TSSOP (PW) | 28	50 | BULK	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 175	ADS1282H
ADS1282HPW.A	Active	Production	TSSOP (PW) | 28	50 | BULK	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 175	ADS1282H
ADS1282HPWG4	Active	Production	TSSOP (PW) | 28	50 | BULK	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 210	ADS1282H
ADS1282HPWG4.A	Active	Production	TSSOP (PW) | 28	50 | BULK	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 210	ADS1282H
ADS1282SJDJ	Active	Production	CDIP SB (JDJ) | 28	12 | TUBE	Yes	Call TI	N/A for Pkg Type	0 to 0	ADS1282SJDJ
ADS1282SJDJ.A	Active	Production	CDIP SB (JDJ) | 28	12 | TUBE	Yes	Call TI	N/A for Pkg Type	0 to 0	ADS1282SJDJ
ADS1282SKGDA	Active	Production	XCEPT (KGD) | 0	80 | OTHER	Yes	Call TI	N/A for Pkg Type	-55 to 210	
ADS1282SKGDA.A	Active	Production	XCEPT (KGD) | 0	80 | OTHER	Yes	Call TI	N/A for Pkg Type	-55 to 210	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

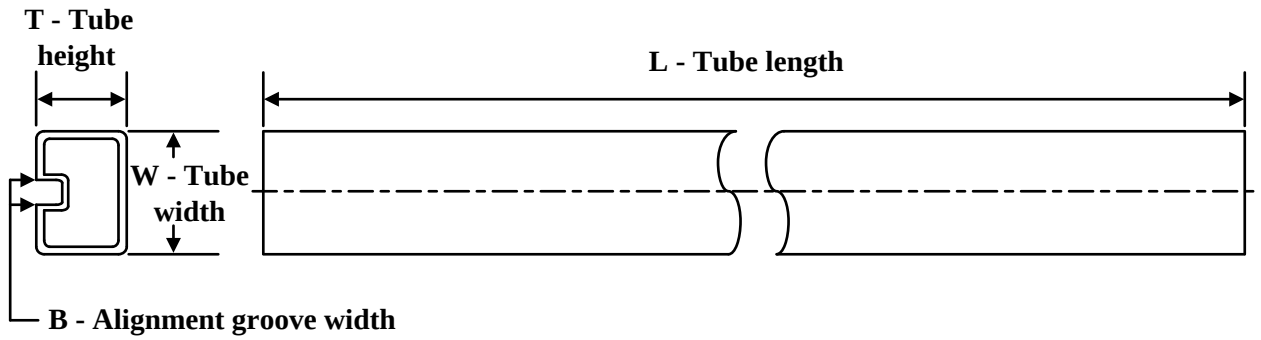
OTHER QUALIFIED VERSIONS OF ADS1282-HT :

- Catalog : ADS1282
- Space : ADS1282-SP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

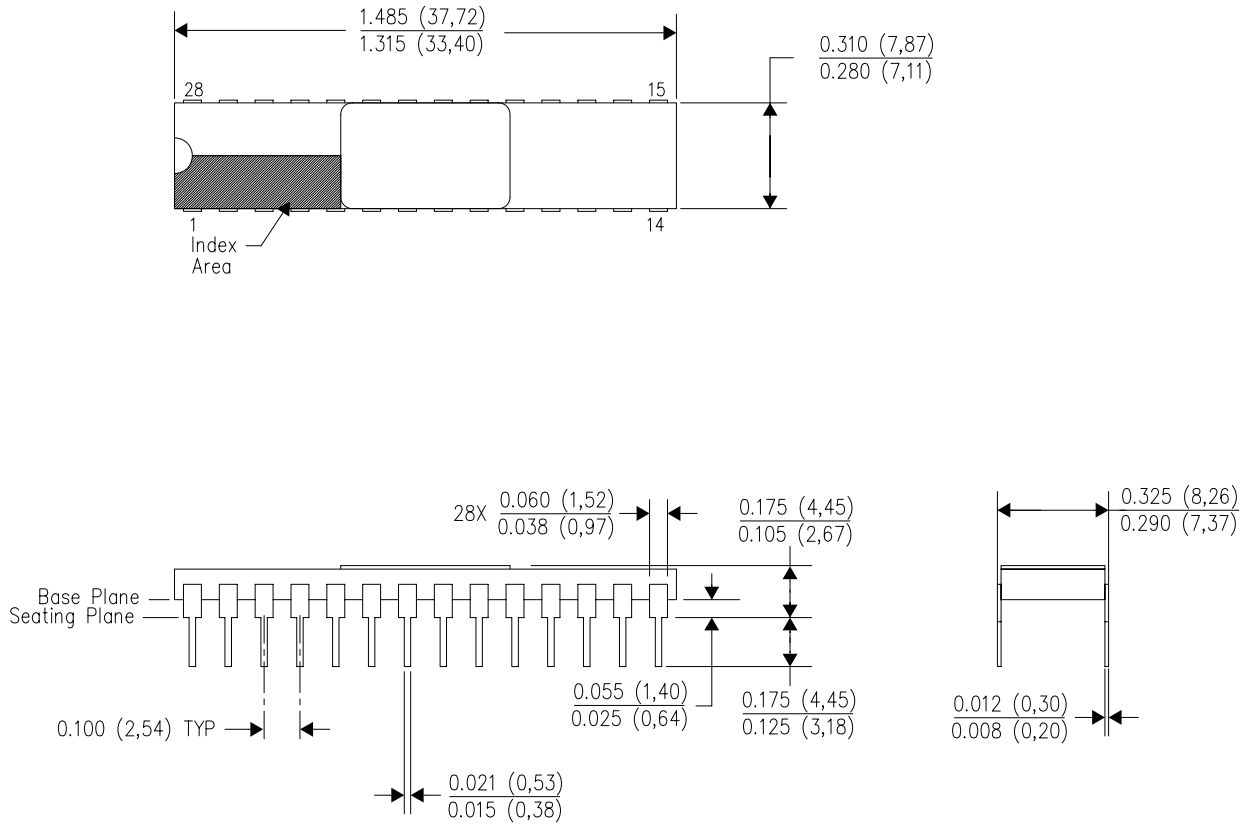
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ADS1282HPW	PW	TSSOP	28	50	530	10.2	3600	3.5
ADS1282HPW.A	PW	TSSOP	28	50	530	10.2	3600	3.5
ADS1282HPWG4	PW	TSSOP	28	50	530	10.2	3600	3.5
ADS1282HPWG4.A	PW	TSSOP	28	50	530	10.2	3600	3.5
ADS1282SJDJ	JDJ	CDIP SB	28	12	506.98	15.24	12290	NA
ADS1282SJDJ.A	JDJ	CDIP SB	28	12	506.98	15.24	12290	NA

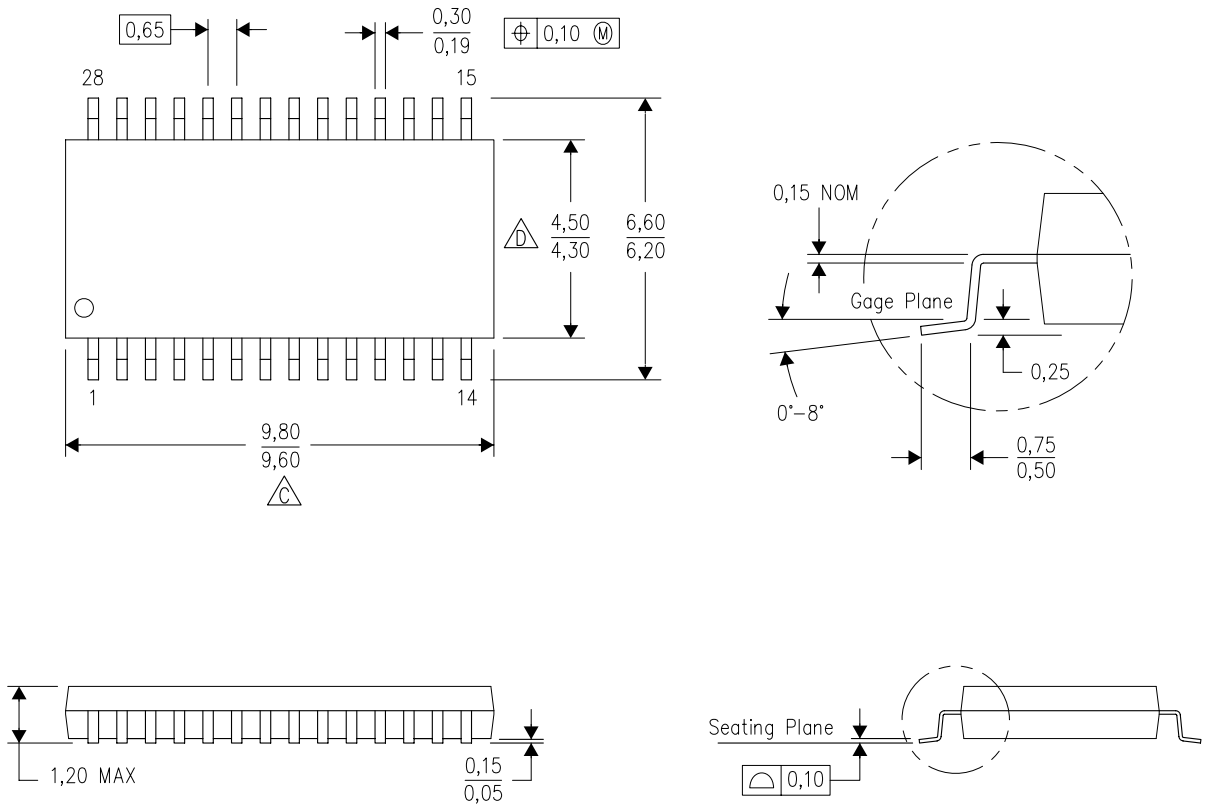
JDJ (R–CDIP–T28) CERAMIC DUAL IN–LINE PACKAGE



4202646–3/B 07/10

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Ceramic quad flatpack with flat leads brazed to non–conductive tie bar carrier.
D. This package is hermetically sealed with a metal lid.
E. The leads are gold plated and can be solderdipped.
F. Leads not shown for clarity purposes.
G. Lid and heat sink are connected to GND leads.

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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