ADC128S102-SEP 耐辐射 8 通道、50-kSPS 至 1-MSPS、12 位 ADC

1 特性

- 抗辐射：
  - 在 125°C 的环境温度下，单粒子锁定 (SEL) 抗扰度高达
    LET = 43 MeV-cm^2/mg
  - 单粒子功能中断 (SEFI) 的 LET 特征值高达 43 MeV-cm^2/mg
  - 电离辐射总剂量 (TID) RLAT/RHA 特征值高达 30 krad(Si)
- 增强型航天塑料（航天 EP）：
  - 符合 ASTM E595 释气规格要求
  - 供应商项目图 (VID) V62/22608
  - 军用温度范围：-55°C 至 125°C
  - 制造、组装和测试一体化基地
  - 金键合线，NiPdAu 铅涂层
  - 晶圆批次可追溯性
  - 延长了产品生命周期
  - 延长了产品变更通知
- 宽电源电压范围：
  - V_A：2.7V 至 5.25V
  - V_D：2.7V 至 V_A
- 兼容 SPI™、QSPI™、MICROWIRE®、DSP
- 转换速率：50 kSPS 至 1 MSPS
- DNL：+1.8 LSB 至 -0.99 LSB（最大值）
- INL：+1.6 LSB 至 -1.6 LSB（最大值）
- 功耗：
  - 3V 电源：2.7 mW（典型值）
  - 5V 电源：11 mW（典型值）

2 应用

- 卫星电力系统 (EPS)
- 命令和数据处理 (C&DH)
- 光学成像有效载荷
- 电压、电流和温度监控
- 加速器

3 说明

ADC128S102-SEP 是一款低功耗、8 通道、CMOS、12 位模数转换器 (ADC)，具有 50 kSPS 至 1 MSPS 的转换吞吐率。该转换器以逐次逼近寄存器 (SAR) 架构为基础，具有内部追踪保持电路。该器件经配置可接收多达八路输入信号（IN0 至 IN7）。

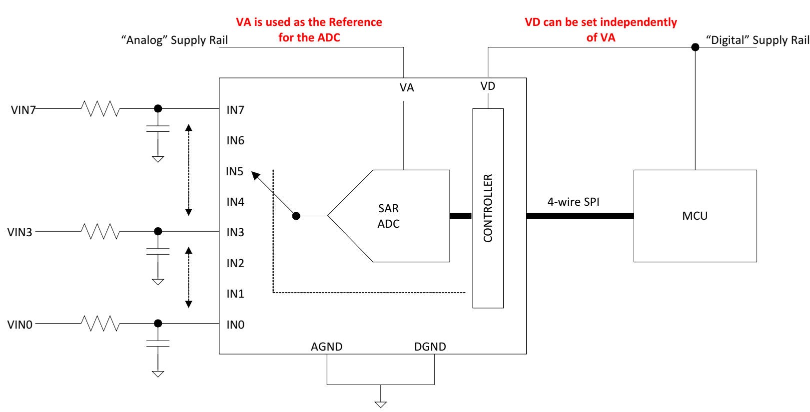
串行数据输出采用标准二进制，兼容多个标准（如 SPI、QSPI、MICROWIRE）和许多常见的 DSP 串行接口。

ADC128S102-SEP 可由独立的模拟和数字电源供电。模拟电源 (V_A) 的电压范围为 2.7V 至 5.25V，数字电源 (V_D) 的电压范围为 2.7V 至 V_A。使用 3V 或 5V 电源的正常功耗分别为 2.3 mW 和 10.7 mW。使用 3V 和 5V 电源时，断电特性可分别将功耗降至 16.5 μW 和 30 μW。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ADC128S102-SEP	TSSOP (16)	5.00mm × 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (December 2021) to Revision A (April 2022) **Page**

- 将文档状态从*预告信息*更改为*量产数据* 1

5 Pin Configuration and Functions

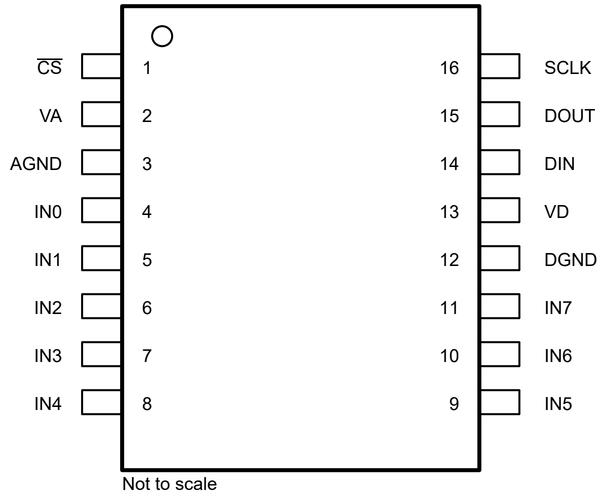


图 5-1. PW Package, 16-Pin TSSOP (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	$\overline{CS}$	IN	Chip select. On the falling edge of $\overline{CS}$, a conversion process begins. Conversions continue as long as $\overline{CS}$ is held low.
2	V_A	Supply	Positive analog supply pin. This voltage is also used as the reference voltage. Connect this pin to a quiet 2.7-V to 5.25-V source and bypass this pin to GND with 1-µF and 0.1-µF monolithic ceramic capacitors located within 1 cm of the power pin.
3	AGND	Supply	The ground return for the analog supply and signals.
4	IN0	IN	Analog input. This signal can range from 0 V to V_{REF}.
5	IN1	IN	Analog input. This signal can range from 0 V to V_{REF}.
6	IN2	IN	Analog input. This signal can range from 0 V to V_{REF}.
7	IN3	IN	Analog input. This signal can range from 0 V to V_{REF}.
8	IN4	IN	Analog input. This signal can range from 0 V to V_{REF}.
9	IN5	IN	Analog input. This signal can range from 0 V to V_{REF}.
10	IN6	IN	Analog input. This signal can range from 0 V to V_{REF}.
11	IN7	IN	Analog input. This signals can range from 0 V to V_{REF}.
12	DGND	Supply	The ground return for the digital supply and signals.
13	V_D	Supply	Positive digital supply pin. Connect this pin to a 2.7-V to V_A supply, and bypass this pin to GND with a 0.1-µF monolithic ceramic capacitor located within 1 cm of the power pin.
14	DIN	IN	Digital data input. The control register is loaded through this pin on rising edges of the SCLK pin.
15	DOUT	OUT	Digital data output. The output samples are clocked out of this pin on the falling edges of the SCLK pin.
16	SCLK	IN	Digital clock input. The specified performance range of frequencies for this input is 0.8 MHz to 16 MHz. This clock directly controls the conversion and readout processes.

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)[(1)]

	MIN	MAX	UNIT
Analog supply voltage (V_A)	–0.3	6.5	V
Digital supply voltage (V_D)[(2)]	–0.3	V_A + 0.3	V
Voltage on analog input pins to AGND[(2)]	AGND – 0.3	V_A + 0.3	V
Voltage on digital input and digital output pins to DGND[(2)]	DGND – 0.3	V_D + 0.3	V
DGND to AGND	–0.3	0.3	V
Input current at any pin	–10	10	mA
Package input current	–20	20	mA
Power-dissipation at T_A = 25°C		See[(3)]	
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The maximum voltage is not to exceed 6.5 V
(3) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by TJmax, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula P_DMAX = ($T_J$max − T_A)/ θ_{JA}. The values for maximum power dissipation listed above will be reached only when the device is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Such conditions should always be avoided.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_A	Analog power supply	V_A to AGND	2.7		5.25	V
V_D	Digital power supply	V_D to DGND	2.7		V_A	V
V_{IN}	Digital input voltage		0		V_A	V
FSR	Full-scale analog input range		0		V_A	V
	Clock frequency		0.8		16	MHz
T_A	Ambient temperature		–55	25	125	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		ADC128S102-SEP PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	55	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

at AGND = DGND = 0 V, f_{SCLK} = 0.8 MHz to 16 MHz, f_{SAMPLE} = 50 kSPS to 1 MSPS, and C_L = 50 pF (unless otherwise noted); minimum and maximum values at T_A = –55°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
I_{DCL}	Input leakage current		–1		1	µA
C_{IN}	Input capacitance[(1)]	Track mode		33		pF
		Hold mode		3		
DC PERFORMANCE						
	Resolution	No missing codes		12		Bits
DNL	Differential nonlinearity	$V_A = V_D$ = 3 V		0.5	1.8	LSB
			–0.99	–0.3		
		$V_A = V_D$ = 5 V		0.9	1.7	
			–0.99	–0.5		
INL	Integral nonlinearity	$V_A = V_D$ = 3 V	–1.6	±0.6	1.6	LSB
		$V_A = V_D$ = 5 V	–1.5	±0.9	1.5	
V_{OFF}	Input offset error	$V_A = V_D$ = 3 V	–2.3	0.8	2.3	LSB
		$V_A = V_D$ = 5 V	–2.3	1.1	2.3	
OEM	Offset error match	$V_A = V_D$ = 3 V	–1.5	±0.1	1.5	LSB
		$V_A = V_D$ = 5 V	–1.5	±0.3	1.5	
FSE	Full-scale error	$V_A = V_D$ = 3 V	–2.1	0.8	2.1	LSB
		$V_A = V_D$ = 5 V	–2.1	0.3	2.1	
FSEM	Full-scale error match	$V_A = V_D$ = 3 V	–1.6	±0.1	1.6	LSB
		$V_A = V_D$ = 5 V	–1.6	±0.3	1.6	
AC PERFORMANCE						
FPBW	Full-power bandwidth	$V_A = V_D$ = 3 V		6.8		MHz
		$V_A = V_D$ = 5 V		10		
SINAD	Signal-to-noise + distortion ratio	$V_A = V_D$ = 3 V, f_{IN} = 40.2 kHz, –0.02 dBFS	68	72		dB
		$V_A = V_D$ = 5 V, f_{IN} = 40.2 kHz, –0.02 dBFS	68	72		
SNR	Signal-to-noise ratio	$V_A = V_D$ = 3 V, f_{IN} = 40.2 kHz, –0.02 dBFS	68.5	72		dB
		$V_A = V_D$ = 5 V, f_{IN} = 40.2 kHz, –0.02 dBFS	68	72		
THD	Total harmonic distortion	$V_A = V_D$ = 3 V, f_{IN} = 40.2 kHz, –0.02 dBFS		–86	–72	dB
		$V_A = V_D$ = 5 V, f_{IN} = 40.2 kHz, –0.02 dBFS		–87	–72	
SFDR	Spurious-free dynamic range	$V_A = V_D$ = 3 V, f_{IN} = 40.2 kHz, –0.02 dBFS	75	91		dB
		$V_A = V_D$ = 5 V, f_{IN} = 40.2 kHz, –0.02 dBFS	75	90		
ENOB	Effective number of bits	$V_A = V_D$ = 3 V, f_{IN} = 40.2 kHz, –0.02 dBFS	11.1	11.6		Bits
		$V_A = V_D$ = 5 V, f_{IN} = 40.2 kHz, –0.02 dBFS	11	11.6		
ISO	Channel-to-channel isolation	$V_A = V_D$ = 3 V, f_{IN} = 20 kHz, –0.02 dBFS		84		dB
		$V_A = V_D$ = 5 V, f_{IN} = 20 kHz, –0.02 dBFS		85		

6.5 Electrical Characteristics (continued)

at AGND = DGND = 0 V, f_{SCLK} = 0.8 MHz to 16 MHz, f_{SAMPLE} = 50 kSPS to 1 MSPS, and C_L = 50 pF (unless otherwise noted); minimum and maximum values at T_A = –55°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IMD	Intermodulation distortion, second order terms	$V_A = V_D$ = 3 V, f_{IN} = 19.5 kHz, –0.02 dBFS		–93	–77	dB
		$V_A = V_D$ = 5 V, f_{IN} = 19.5 kHz, –0.02 dBFS		–93	–77	
	Intermodulation distortion, third order terms	$V_A = V_D$ = 3 V, f_{IN} = 19.5 kHz, –0.02 dBFS		–91	–70	
		$V_A = V_D$ = 5 V, f_{IN} = 19.5 kHz, –0.02 dBFS		–91	–70	
DIGITAL INPUTS						
V_{IH}	Input high logic level	$V_A = V_D$ = 2.7 V to 3.6 V	2.1			V
		$V_A = V_D$ = 4.75 V to 5.25 V	2.4			
V_{IL}	Input low logic level	$V_A = V_D$ = 2.7 V to 5.25 V			0.8	V
	Input current	V_{IN} = 0 V or V_D		±0.01	±2	µA
	Digital input capacitance(1)				3.5	pF
DIGITAL OUTPUTS						
	Output format		Straight binary			
V_{OH}	Output high logic level	I_{SOURCE} = 200 µA, $V_A = V_D$ = 2.7 V to 5.25 V	V_D - 0.5			V
V_{OL}	Output low logic level	I_{SOURCE} = 200 µA to 1 mA, $V_A = V_D$ = 2.7 V to 5.25 V			0.4	V
	Hiigh-impedance output leakage current	$V_A = V_D$ = 2.7 V to 5.25 V		±0.01	±1	µA
	Hiigh-impedance output capacitance(1)				3.5	pF
POWER SUPPLY						
$I_A + I_D$	Total supply current, normal mode ($\overline{CS}$ low)	$V_A = V_D$ = 2.7 V to 3.6 V f_{SAMPLE} = 1 MSPS, f_{IN} = 40 kHz		0.9	1.5	mA
		$V_A = V_D$ = 4.75 V to 5.25 V f_{SAMPLE} = 1 MSPS, f_{IN} = 40 kHz		2.2	3.2	
	Total supply current, shutdown mode ($\overline{CS}$ high)	$V_A = V_D$ = 2.7 V to 3.6 V f_{SAMPLE} = 0 kSPS		5.5	50	µA
		$V_A = V_D$ = 4.75 V to 5.25 V f_{SAMPLE} = 0 kSPS		6	70	
P_C	Power consumption, normal mode ($\overline{CS}$ low)	$V_A = V_D$ = 3 V f_{SAMPLE} = 1 MSPS, f_{IN} = 40 kHz		2.7	4.5	mW
		$V_A = V_D$ = 5 V f_{SAMPLE} = 1 MSPS, f_{IN} = 40 kHz		11	15.5	
	Power consumption, shutdown mode ($\overline{CS}$ high)	$V_A = V_D$ = 3 V f_{SAMPLE} = 0 kSPS		16.5	150	µW
		$V_A = V_D$ = 5 V f_{SAMPLE} = 0 kSPS		30	350	

(1) This parameter is specified by design and/or characterization and is not tested in production.

6.6 Timing Requirements

at V_A = V_D = 2.7 V to 5.25 V, AGND = DGND = 0 V, f_{SCLK} = 0.8 MHz to 16 MHz, f_{SAMPLE} = 50 kSPS to 1 MSPS, and C_L = 50 pF (unless otherwise noted); minimum and maximum values at T_A = –55°C to +125°C; typical values at T_A = 25°C.

			MIN	TYP	MAX	UNIT
CONVERSION CYCLE						
f_{SCLK}	Serial clock frequency	V_A = V_D = 2.7 V to 5.25 V	0.8		16	MHz
	Serial clock duty cycle	V_A = V_D = 2.7 V to 5.25 V	40%		60%	
f_S	Sample rate in continuous mode	V_A = V_D = 2.7 V to 5.25 V	50			kSPS
$t_{CONVERT}$	Conversion (hold) time	V_A = V_D = 2.7 V to 5.25 V			13	SCLK
t_{ACQ}	Acquisition (track) time	V_A = V_D = 2.7 V to 5.25 V			3	SCLK
t_{CYCLE}	Throughput time	(t_{CONV} + t_{ACQ}) at V_A = V_D = 2.7 V to 5.25 V			16	SCLK
SPI INTERFACE TIMINGS						
t_{CSH}	$\overline{CS}$ hold time after SCLK rising edge		10	2		ns
t_{CSS}	$\overline{CS}$ setup time prior to SCLK rising edge		10	4.5		ns
t_{DS}	DIN setup time prior to SCLK rising edge		10			ns
t_{DH}	DIN hold time after SCLK rising edge		10			ns
t_{CH}	SCLK high time			0.4 x t_{SCLK}		ns
t_{CL}	SCLK low time			0.4 x t_{SCLK}		ns

6.7 Switching Characteristics

at V_A = V_D = 2.7 V to 5.25 V, AGND = DGND = 0 V, f_{SCLK} = 0.8 MHz to 16 MHz, f_{SAMPLE} = 50 kSPS to 1 MSPS, and C_L = 50 pF (unless otherwise noted); minimum and maximum values at T_A = –55°C to +125°C; typical values at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPI INTERFACE TIMINGS						
t_{EN}	$\overline{CS}$ falling edge to DOUT enabled			5	30	ns
t_{DACC}	DOUT access time after SCLK falling edge			17	27	ns
t_{DHLD}	DOUT hold time after SCLK falling edge		7			ns
t_{DIS}	$\overline{CS}$ rising edge to DOUT high-impedance	DOUT falling		2.4	20	ns
		DOUT rising		0.9	20	ns

6.8 Timing Diagrams

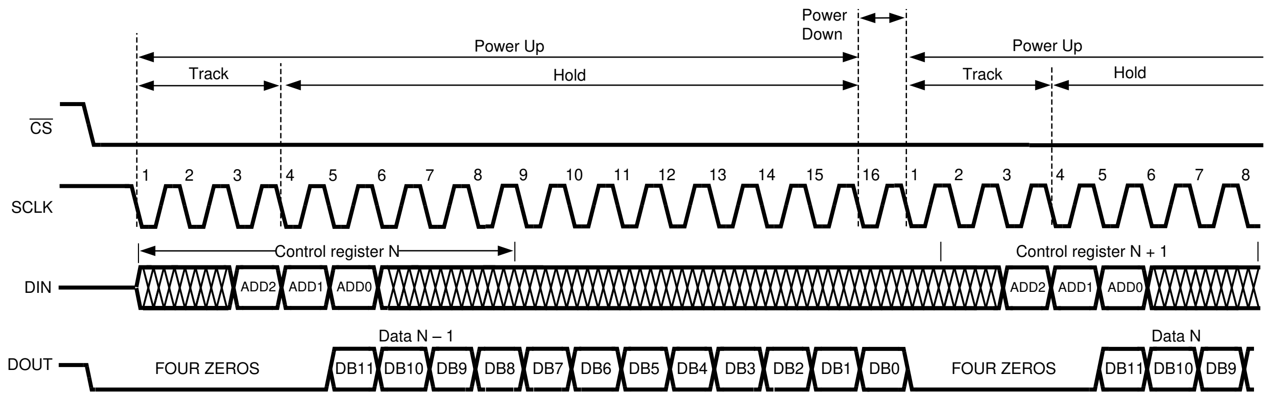


图 6-1. ADC128S102-SEP Operational Timing Diagram

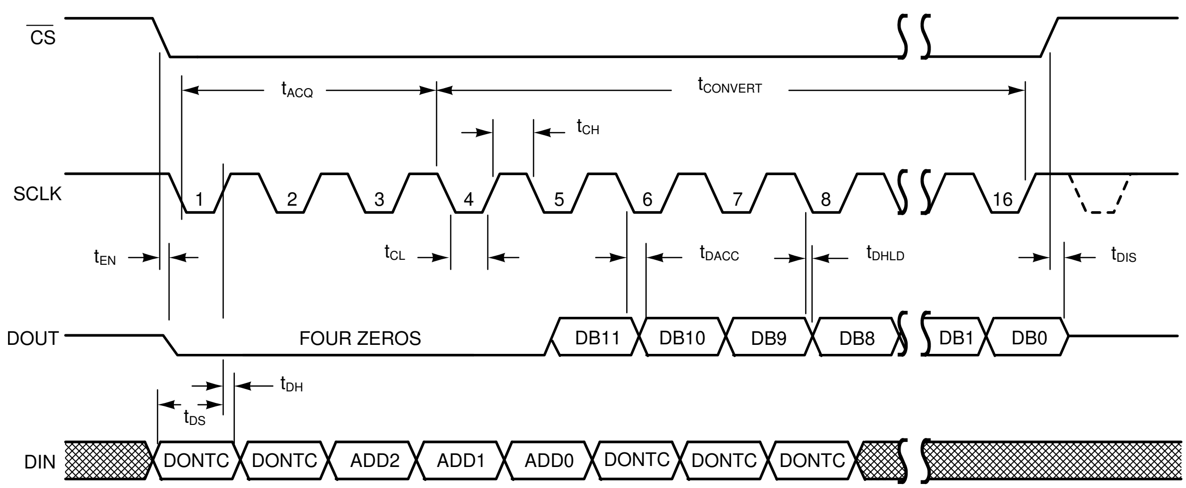


图 6-2. ADC128S102-SEP Serial Timing Diagram

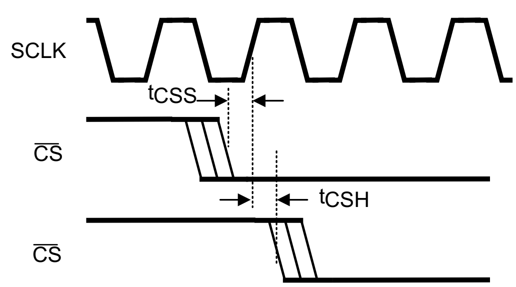


图 6-3. SCLK and $\overline{\text{CS}}$ Timing Parameters

6.9 Typical Characteristics

T_A = 25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, and f_{IN} = 40.2 kHz (unless otherwise noted)

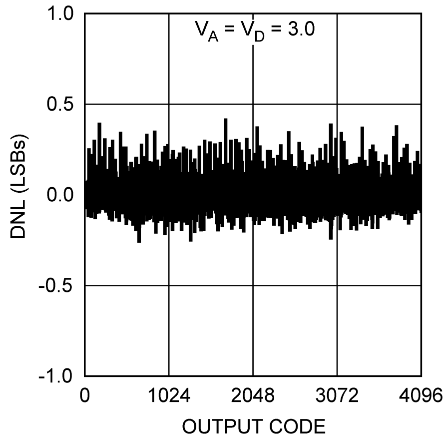


图 6-4. DNL

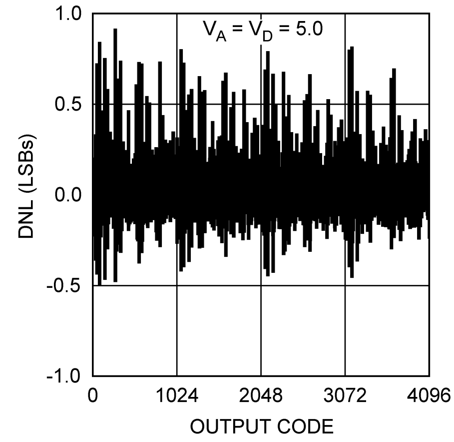


图 6-5. DNL

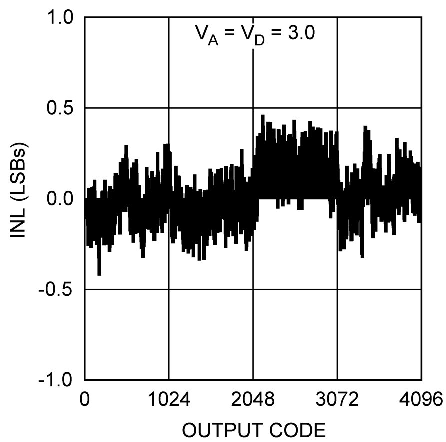


图 6-6. INL

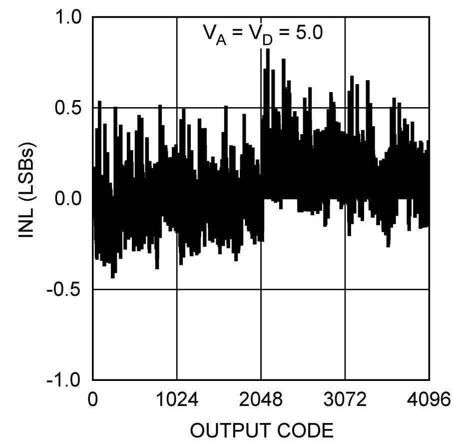


图 6-7. INL

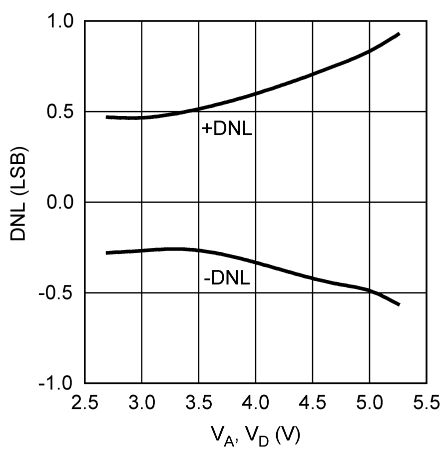


图 6-8. DNL vs Supply

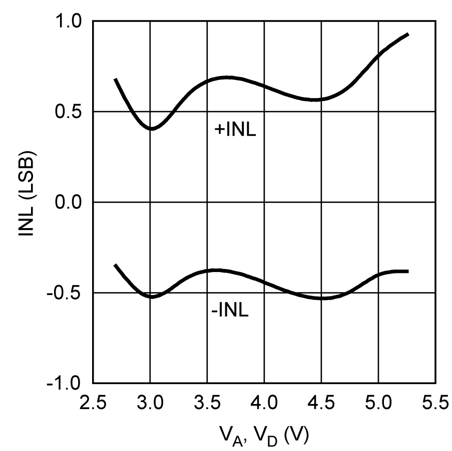


图 6-9. INL vs Supply

6.9 Typical Characteristics (continued)

T_A = 25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, and f_{IN} = 40.2 kHz (unless otherwise noted)

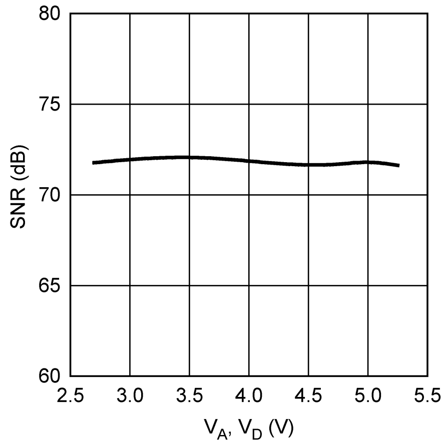


图 6-10. SNR vs Supply

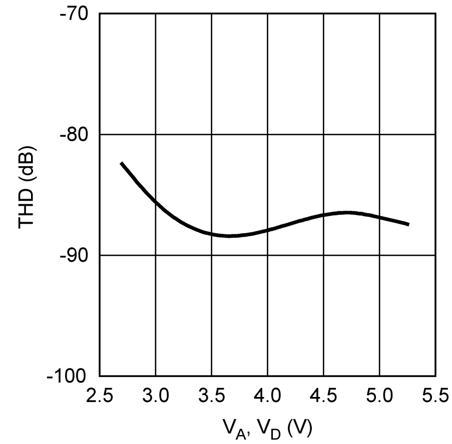


图 6-11. THD vs Supply

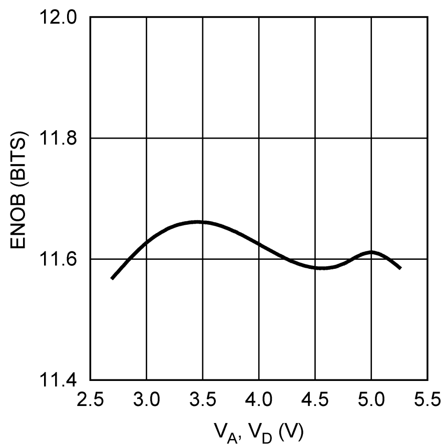


图 6-12. ENOB vs Supply

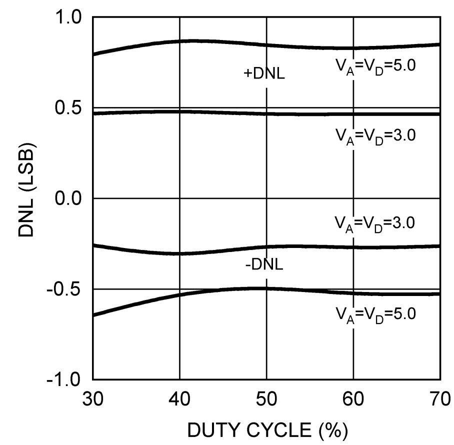


图 6-13. DNL vs SCLK Duty Cycle

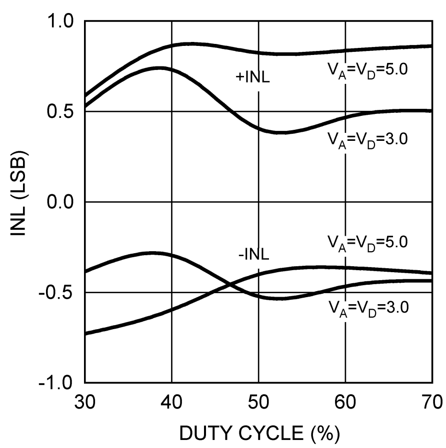


图 6-14. INL vs SCLK Duty Cycle

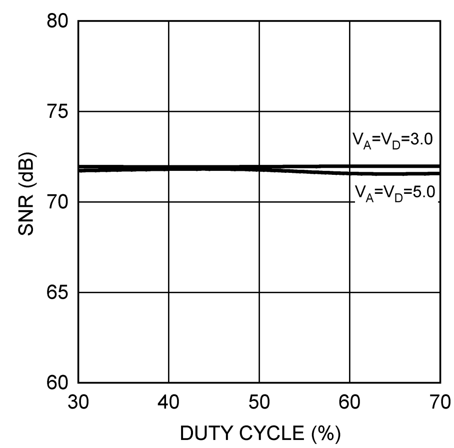


图 6-15. SNR vs SCLK Duty Cycle

6.9 Typical Characteristics (continued)

T_A = 25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, and f_{IN} = 40.2 kHz (unless otherwise noted)

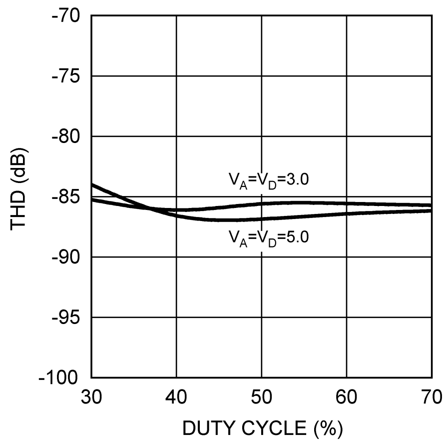


图 6-16. THD vs SCLK Duty Cycle

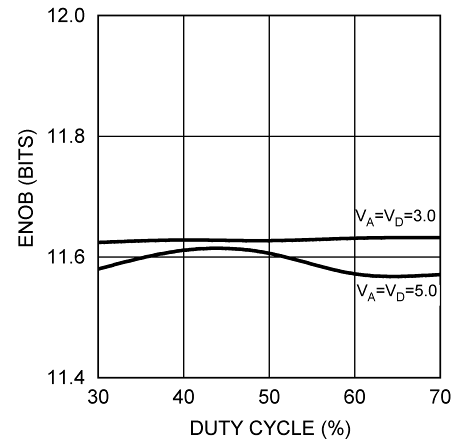


图 6-17. ENOB vs SCLK Duty Cycle

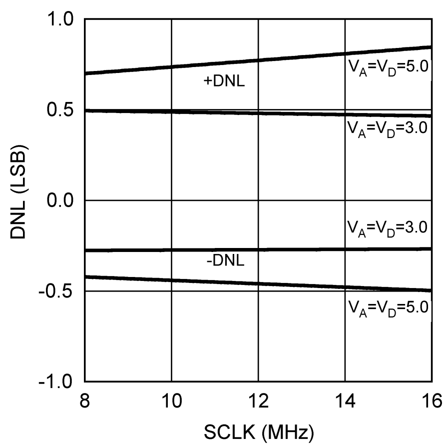


图 6-18. DNL vs SCLK

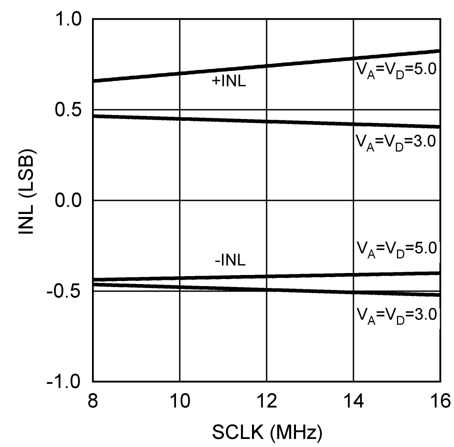


图 6-19. INL vs SCLK

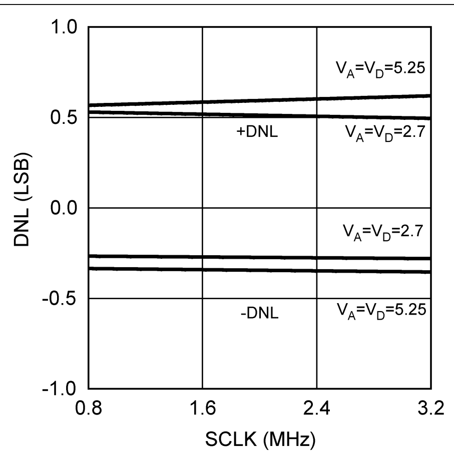


图 6-20. DNL vs SCLK

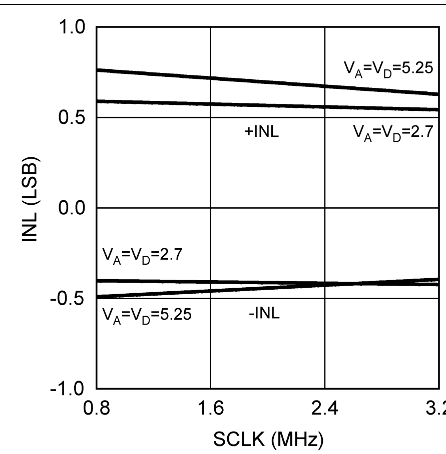


图 6-21. INL vs SCLK

6.9 Typical Characteristics (continued)

T_A = 25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, and f_{IN} = 40.2 kHz (unless otherwise noted)

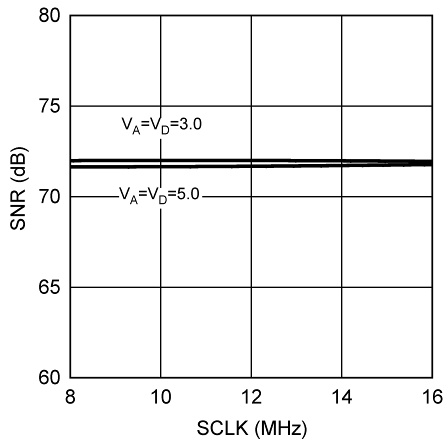


图 6-22. SNR vs SCLK

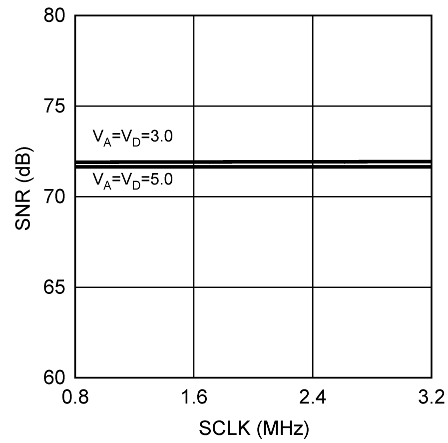


图 6-23. SNR vs SCLK

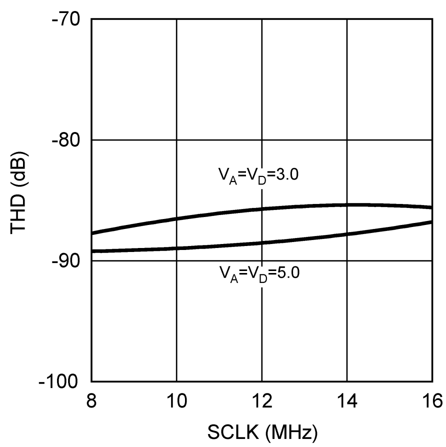


图 6-24. THD vs SCLK

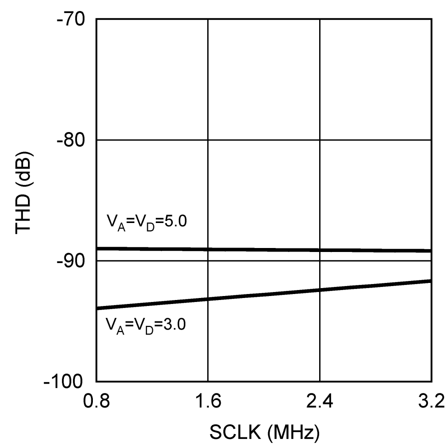


图 6-25. THD vs SCLK

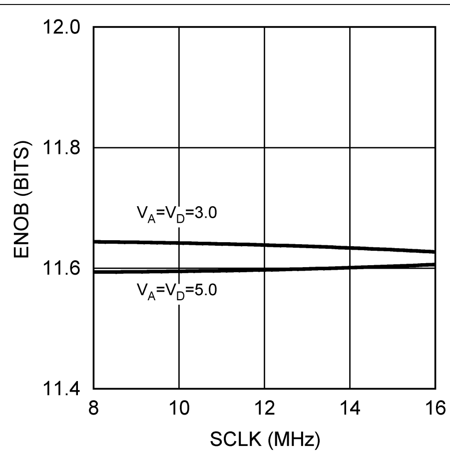


图 6-26. ENOB vs SCLK

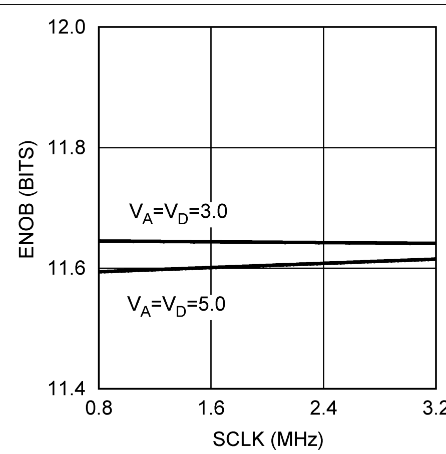


图 6-27. ENOB vs SCLK

6.9 Typical Characteristics (continued)

T_A = 25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, and f_{IN} = 40.2 kHz (unless otherwise noted)

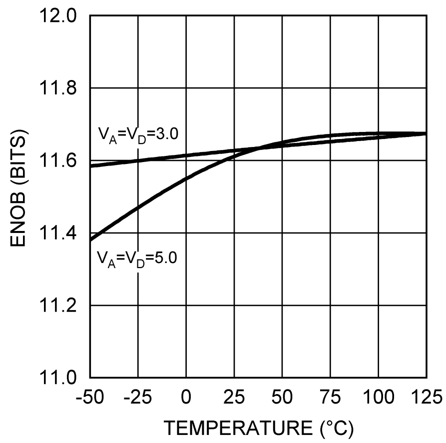


图 6-28. ENOB vs Temperature

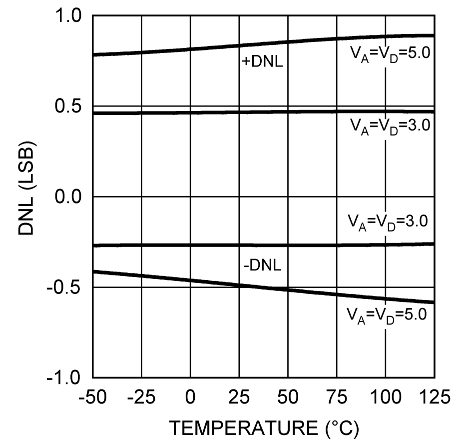


图 6-29. DNL vs Temperature

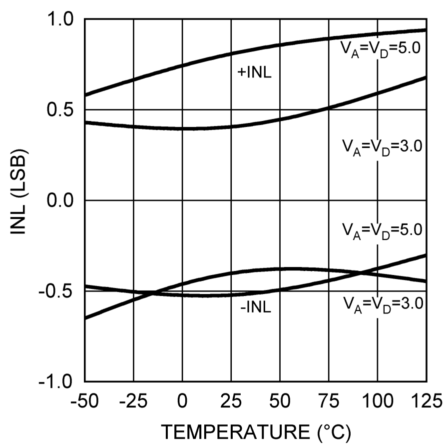


图 6-30. INL vs Temperature

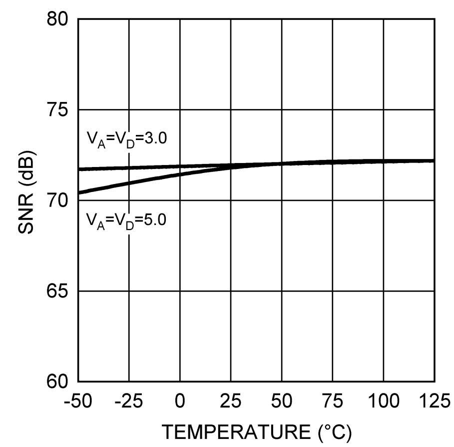


图 6-31. SNR vs Temperature

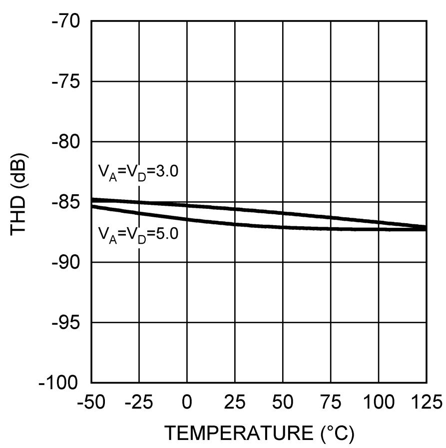


图 6-32. THD vs Temperature

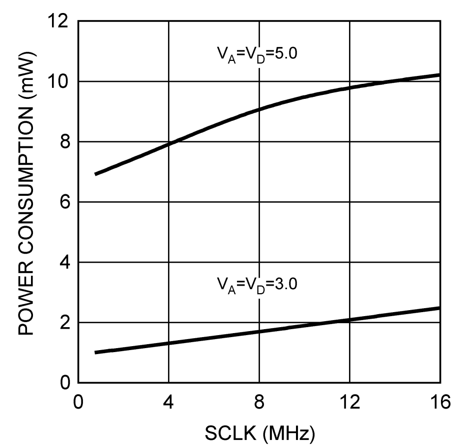


图 6-33. Power Consumption vs SCLK

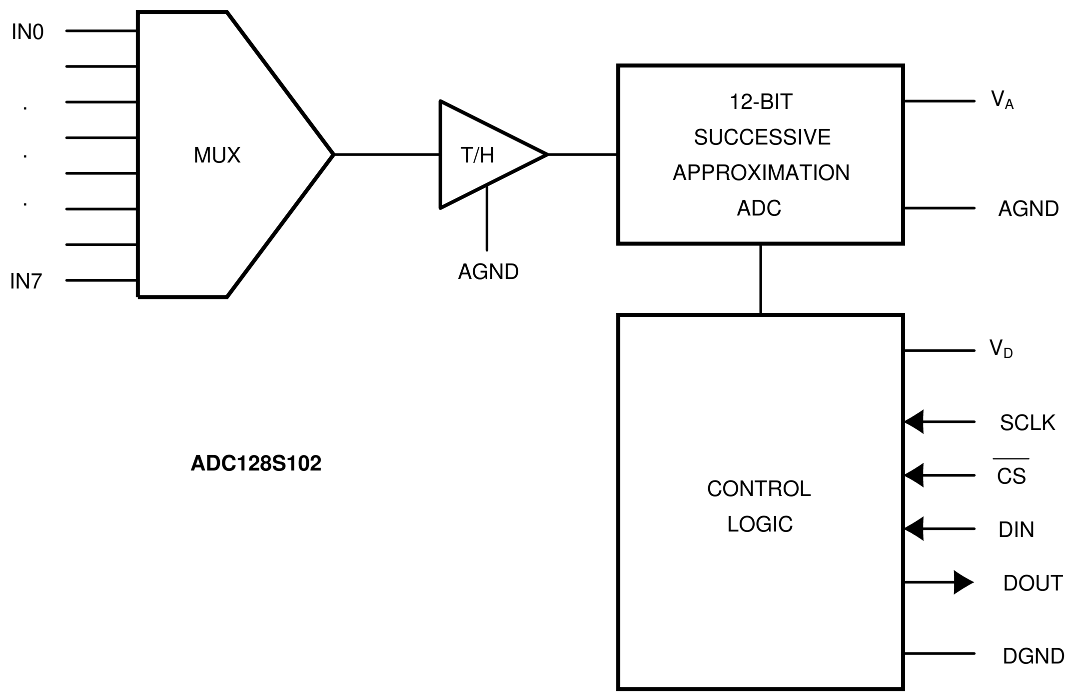
7 Detailed Description

7.1 Overview

The ADC128S102-SEP is a small, eight-channel, multiplexed, 12-bit, successive-approximation register analog-to-digital converter (SAR ADC) designed around a charge redistribution digital-to-analog converter (DAC). In addition to having 8 input channels, the ADC128S102-SEP can operate at sampling rates up to 1 MSPS.

The device provides an SPI-compatible serial interface.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 ADC128S102-SEP Transfer Function

The output format of the ADC128S102-SEP is straight binary. Code transitions occur midway between successive integer LSB values. The LSB width for the ADC128S102-SEP is V_A / 4096. 图 7-1 illustrates the ideal transfer characteristic. The transition from an output code of 0000 0000 0000 to a code of 0000 0000 0001 is at 1/2 LSB, or a voltage of V_A / 8192. Other code transitions occur at steps of one LSB.

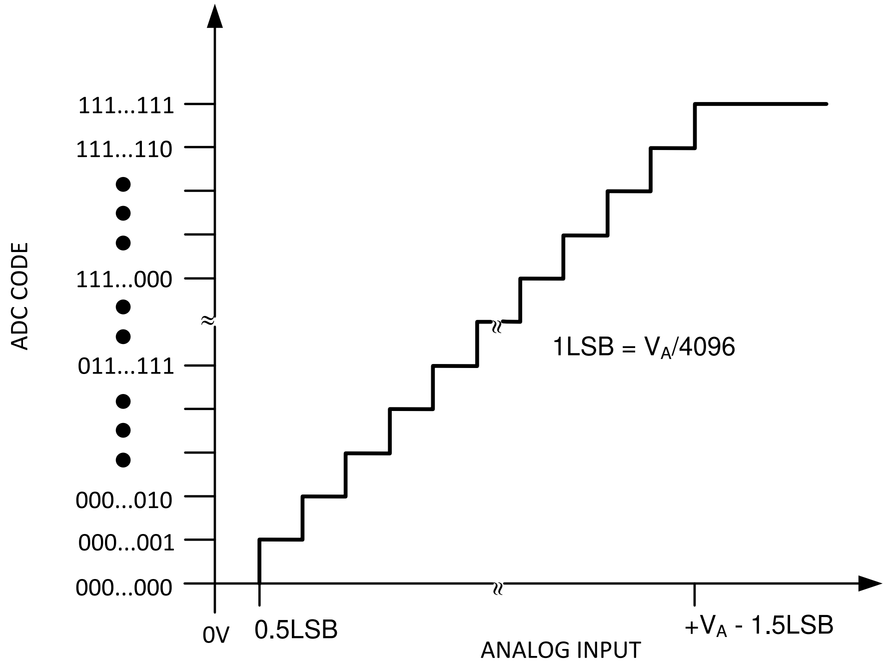


图 7-1. Ideal Transfer Characteristic

7.3.2 Analog Inputs

图 7-2 shows an equivalent circuit for one of the input channels of the ADC128S102-SEP. Diodes D1 and D2 provide ESD protection for the analog inputs. The operating range for the analog inputs is 0 V to V_A. Going beyond this range causes the ESD diodes to conduct and results in erratic operation.

Capacitor C1 in 图 7-2 has a typical value of 3 pF and is mainly the package pin capacitance. Resistor R1 is the ON-resistance of the multiplexer and track-and-hold switch and is typically 500 Ω. Capacitor C2 is the ADC128S102-SEP sampling capacitor, and is typically 30 pF. The ADC128S102-SEP delivers best performance when driven by a low-impedance source (less than 100 Ω). This source is especially important when using the ADC128S102-SEP to sample dynamic signals. Also important when sampling dynamic signals is a band-pass or low-pass filter, which reduces harmonics and noise in the input. These filters are often referred to as antialiasing filters.

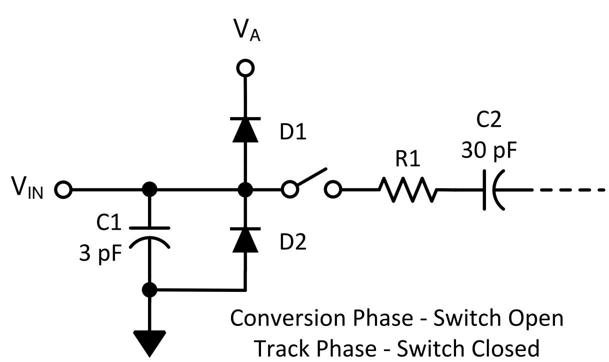


图 7-2. Equivalent Input Circuit

7.3.3 Digital Inputs and Outputs

The digital inputs of the ADC128S102-SEP (SCLK, $\overline{CS}$, and DIN) have an operating range of 0 V to V_A. The inputs are not prone to latch-up and can be asserted before the digital supply (V_D) without any risk. The digital output (DOUT) operating range is controlled by V_D. The output high voltage is V_D – 0.5 V (minimum) when the output low voltage is 0.4 V (maximum).

7.3.4 Radiation Environments

Careful consideration must be given to environmental conditions when using a product in a radiation environment.

7.3.4.1 Total Ionizing Dose

Testing and qualification of these products is done on a wafer level according to *MIL-STD-883G, Test Method 1019.7*. Testing is done according to condition A and the extended room temperature anneal test described in section 3.11 for application environment dose rates less than 51.61 rad(Si)/s. Wafer level TID data are available with lot shipments.

7.3.4.2 Single Event Latch-Up

One-time single event latch-up (SEL) was preformed according to EIA/JEDEC Standard, EIA/JEDEC57. The linear energy transfer threshold (LET_{th}) shown in the *特性* section is the maximum LET tested. A test report is available upon request.

7.4 Device Functional Modes

7.4.1 ADC128S102-SEP Operation

Simplified schematics of the ADC128S102-SEP in both track and hold operation are provided in 图 7-3 and 图 7-4, respectively. In 图 7-3, the ADC128S102-SEP is in track mode: switch SW1 connects the sampling capacitor to one of eight analog input channels through the multiplexer, and SW2 balances the comparator inputs. The ADC128S102-SEP is in this state for the first three SCLK cycles after $\overline{CS}$ is brought low.

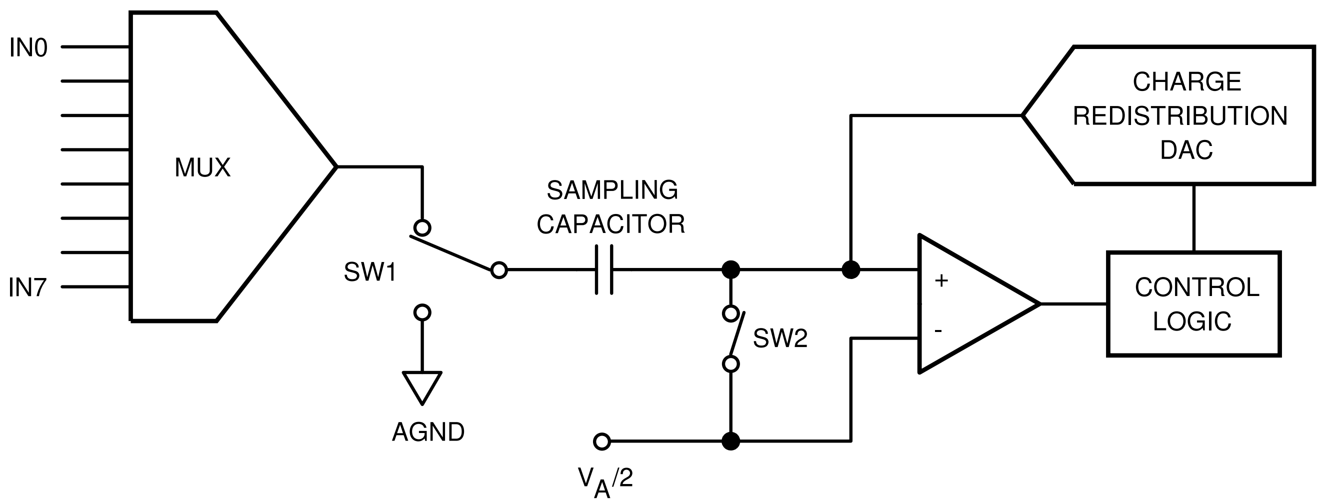


图 7-3. ADC128S102-SEP in Track Mode

图 7-4 shows the ADC128S102-SEP in hold mode: switch SW1 connects the sampling capacitor to ground, maintaining the sampled voltage, and switch SW2 unbalances the comparator. The control logic then instructs the charge-redistribution DAC to add or subtract fixed amounts of charge to or from the sampling capacitor until the comparator is balanced. When the comparator is balanced, the digital word supplied to the DAC is the digital representation of the analog input voltage. The ADC128S102-SEP is in this state for the last 13 SCLK cycles after $\overline{CS}$ is brought low.

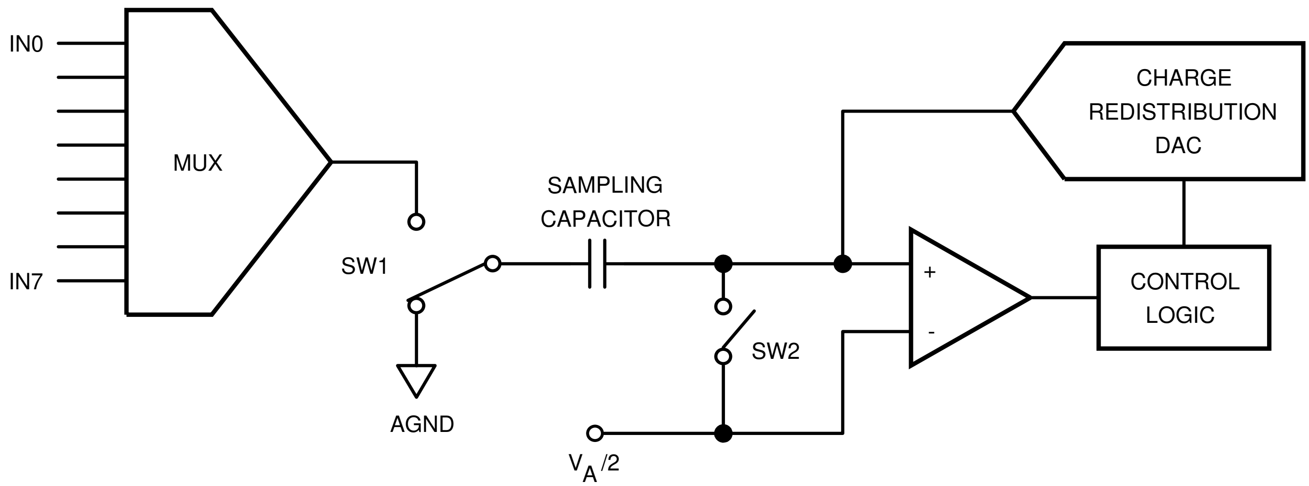


图 7-4. ADC128S102-SEP in Hold Mode

7.5 Programming

7.5.1 Serial Interface

An operational timing diagram and a serial interface timing diagram for the ADC128S102-SEP are illustrated in the *Timing Diagrams* section. $\overline{CS}$, chip select, initiates conversions and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of serial data. DOUT is the serial data output pin, where a conversion result is sent as a serial data stream, MSB first. Data to be written to the control register are placed on DIN, the serial data input pin. New data are written to DIN with each conversion.

A serial frame is initiated on the falling edge of $\overline{CS}$ and ends on the rising edge of $\overline{CS}$. Each frame must contain an integer multiple of 16 rising SCLK edges. The ADC DOUT pin is in a high-impedance state when $\overline{CS}$ is high and is active when $\overline{CS}$ is low. $\overline{CS}$ is asynchronous and therefore functions as an output enable. Similarly, SCLK is internally gated off when $\overline{CS}$ is brought high.

During the first three SCLK cycles, the ADC is in track mode, acquiring the input voltage. For the next 13 SCLK cycles the conversion is accomplished and the data are clocked out. SCLK falling edges 1 through 4 clock out leading zeros and falling edges 5 through 16 clock out the conversion result, MSB first. If there is more than one conversion in a frame (continuous conversion mode), the ADC re-enters track mode on the SCLK falling edge after the N × 16th SCLK rising edge and re-enters the hold/convert mode on the N × 16 + 4th SCLK falling edge. *N* is an integer value.

The ADC128S102-SEP enters track mode under three different conditions. In 图 6-1, $\overline{CS}$ goes low with SCLK high and the ADC enters track mode on the first SCLK falling edge. In the second condition, $\overline{CS}$ goes low with SCLK low. Under this condition, the ADC automatically enters track mode and the $\overline{CS}$ falling edge is taken as the first SCLK falling edge. In the third condition, $\overline{CS}$ and SCLK go low simultaneously and the ADC enters track mode. Although there is no timing restriction with respect to the falling edges of $\overline{CS}$ and SCLK, see 图 6-3 for setup and hold time requirements for the $\overline{CS}$ falling edge with respect to the SCLK rising edge.

During each conversion, data are clocked into a control register through the DIN pin on the first eight SCLK rising edges after the fall of $\overline{CS}$. As given in 表 7-1, 表 7-2, and 表 7-3, the control register is loaded with data indicating the input channel to be converted on the subsequent conversion.

Although the ADC128S102-SEP can acquire the input signal to full resolution in the first conversion immediately following power up, the first conversion result after power up is that of a randomly selected channel. Therefore, incorporate a dummy conversion to set the required channel to be used on the subsequent conversion.

表 7-1. Control Register Bits

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DONTC	DONTC	ADD2	ADD1	ADD0	DONTC	DONTC	DONTC

表 7-2. Control Register Bit Descriptions

BIT	SYMBOL	DESCRIPTION
7, 6, 2, 1, 0	DONTC	Don't care. The values of these bits do not affect the device.
5	ADD2	These three bits determine which input channel is sampled and converted at the next conversion cycle. The mapping between codes and channels is given in 表 7-3.
4	ADD1	
3	ADD0	

表 7-3. Input Channel Selection

ADD2	ADD1	ADD0	INPUT CHANNEL
0	0	0	IN0
0	0	1	IN1
0	1	0	IN2
0	1	1	IN3
1	0	0	IN4
1	0	1	IN5
1	1	0	IN6
1	1	1	IN7

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ADC128S102-SEP is a low-power, eight-channel, 12-bit ADC with specified performance specifications from 50 kSPS to 1 MSPS. The ADC128S102-SEP can be used at sample rates below 50 kSPS by powering the device down (deasserting $\overline{CS}$) in between conversions. The *Electrical Characteristics* table highlights the clock frequency where ADC performance is specified. There is no limitation on periods of time for shutdown between conversions.

8.2 Typical Application

图 8-1 shows a typical application block diagram. The split analog and digital supply pins are both powered in this example by the Texas Instruments' LP2950-N low-dropout voltage regulator. The analog supply is bypassed with a capacitor network located close to the ADC128S102-SEP. The digital supply is separated from the analog supply by an isolation resistor and bypassed with additional capacitors. The ADC128S102-SEP uses the analog supply (V_A) as its reference voltage; thus, V_A must be kept as clean as possible. Because of the low power requirements of the ADC128S102-SEP, a precision reference can also be used as a power supply.

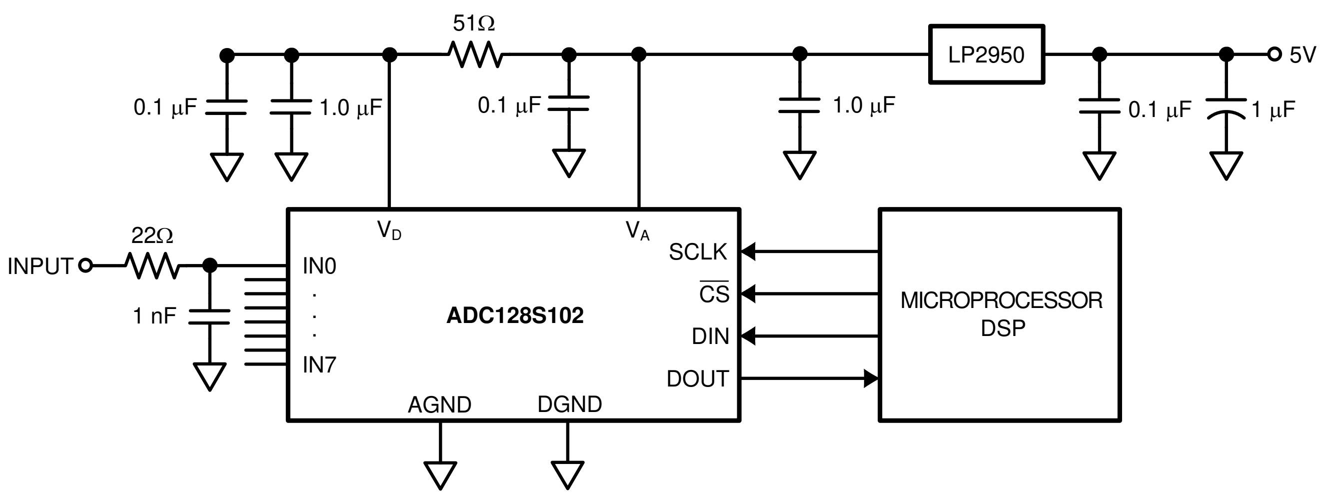


图 8-1. Typical Application Circuit

8.2.1 Design Requirements

A positive-supply-only data acquisition (DAQ) system is capable of digitizing up to eight single-ended input signals ranging from 0 V to 5 V with BW = 10 kHz and a throughput up to 500 kSPS. The ADC128S102-SEP must interface to an MCU whose supply is set at 5 V. To interface with an MCU that operates at 3.3 V or lower, V_A and V_D must be separated and care must be taken to ensure that V_A is powered before V_D.

8.2.2 Detailed Design Procedure

The signal range requirement forces the design to use a 5-V analog supply at V_A, the analog supply. This requirement stems from the fact that V_A is also a reference potential for the ADC. If the requirement of interfacing to the MCU changes to 3.3 V, the V_D supply voltage must also change to 3.3 V. The maximum sampling rate of the ADC128S102-SEP when all channels (eight) are enabled is $f_S = f_{SCLK} / (16 \times 8)$.

Faster sampling rates can be achieved when fewer channels are sampled. A single channel can be sampled at the maximum rate of f_S (single) = f_{SCLK} / 16.

The V_A and V_D pins are separated by a 51-Ω resistor to minimize digital noise from corrupting the analog reference input. If additional filtering is required, the resistor can be replaced by a ferrite bead, thus achieving a second-order filter response. Further noise consideration can be provided to the SPI interface, especially when the controller MCU is capable of producing fast rising edges on the digital bus signals. Inserting small resistances in the digital signal path can help reduce ground bounce, and thus improve overall noise performance of the system. Care must be taken when the signal source is capable of producing voltages beyond V_A. In such instances, the internal ESD diodes can start conducting. The ESD diodes are not intended as input signal clamps. To provide the desired clamping action, use Schottky diodes.

8.2.3 Application Curve

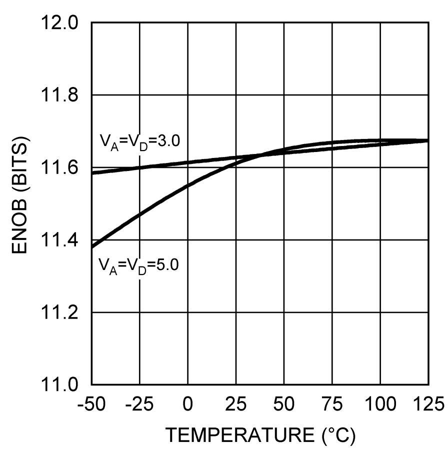


图 8-2. ENOB vs Temperature

9 Power Supply Recommendations

There are three major power supply concerns with this product: power-supply sequencing, power management, and the effect of digital supply noise on the analog supply.

9.1 Power-Supply Sequence

The ADC128S102-SEP is a dual-supply device. The two supply pins share ESD resources, so care must be exercised to ensure that power is applied in the correct sequence. To avoid turning on the ESD diodes, the digital supply (V_D) cannot exceed the analog supply (V_A) by more than 300 mV. Therefore, V_A must ramp up before or concurrently with V_D.

9.2 Power Management

The ADC128S102-SEP is fully powered up when $\overline{CS}$ is low and is fully powered down when $\overline{CS}$ is high, with one exception. If operating in continuous conversion mode, the ADC128S102-SEP automatically enters power-down mode between the 16th SCLK falling edge of a conversion and the 1st SCLK falling edge of the subsequent conversion (see 图 6-1).

In continuous conversion mode, the ADC128S102-SEP can perform multiple conversions back to back. Each conversion requires 16 SCLK cycles and the ADC128S102-SEP performs conversions continuously as long as $\overline{CS}$ is held low. Continuous mode offers maximum throughput.

In burst mode, throughput can be traded off for power consumption by performing fewer conversions per unit time. In other words, more time is spent in power-down mode and less time is spent in normal mode. By using this technique, very low sample rates can be achieved while still using an SCLK frequency within the electrical specifications. To calculate the power consumption (P_C), simply multiply the fraction of time spent in normal mode (t_N) by the normal mode power consumption (P_N), as shown in 方程式 1, and add the fraction of time spent in shutdown mode (t_S) multiplied by the shutdown mode power consumption (P_S).

$$P_C = \frac{t_N}{t_N + t_S} \times P_N + \frac{t_S}{t_N + t_S} \times P_S \quad (1)$$

9.3 Power-Supply Noise Considerations

The charging of any output load capacitance requires current from the digital supply, V_D. The current pulses required from the supply to charge the output capacitance cause voltage variations on the digital supply. If these variations are large enough, they can degrade SNR and SINAD performance of the ADC. Furthermore, if the analog and digital supplies are tied directly together, the noise on the digital supply is coupled directly into the analog supply, causing greater performance degradation than noise alone causes on the digital supply. Similarly, discharging the output capacitance when the digital output goes from a logic high to a logic low dumps current into the die substrate, which is resistive. Load discharge currents cause *ground bounce* noise in the substrate that degrades noise performance if that current is large enough. The larger the output capacitance, the more current flows through the die substrate and the greater the noise coupled into the analog channel.

The first solution to keeping digital noise out of the analog supply is to decouple the analog and digital supplies from each other or use separate supplies for them. To keep noise out of the digital supply, keep the output load capacitance as small as practical. If the load capacitance is greater than 50 pF, use a 100-Ω series resistor at the ADC output, located as close to the ADC output pin as practical. This resistor limits the charge and discharge current of the output capacitance and improves noise performance. Because the series resistor and the load capacitance form a low-frequency pole, verify signal integrity when the series resistor is added.

10 Layout

10.1 Layout Guidelines

Capacitive coupling between the noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry and the clock line as short as possible.

Digital circuits create substantial supply and ground current transients. The logic noise generated can have significant impact upon system noise performance. To avoid performance degradation of the ADC128S102-SEP resulting from supply noise, do not use the same supply for the ADC128S102-SEP that is used for digital logic.

Generally, analog and digital lines cross each other at 90° to avoid crosstalk. However, to maximize accuracy in high-resolution systems, avoid crossing analog and digital lines altogether. Clock lines must be kept as short as possible and isolated from ***all*** other lines, including other digital lines. In addition, the clock line must be treated as a transmission line and be properly terminated.

Isolate the analog input from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (for example, a filter capacitor) connected between the converter input pins and ground or to the reference input pin and ground must be connected to a very clean point in the ground plane.

Use a single, uniform ground plane and split power planes. The power planes must be located within the same board layer. Place all analog circuitry (input amplifiers, filters, reference components, and so forth) over the analog power plane. Place all digital circuitry and I/O lines over the digital power plane. Furthermore, all components in the reference circuitry and the input signal chain that are connected to ground must be connected together with short traces and enter the analog ground plane at a single, quiet point.

10.2 Layout Example

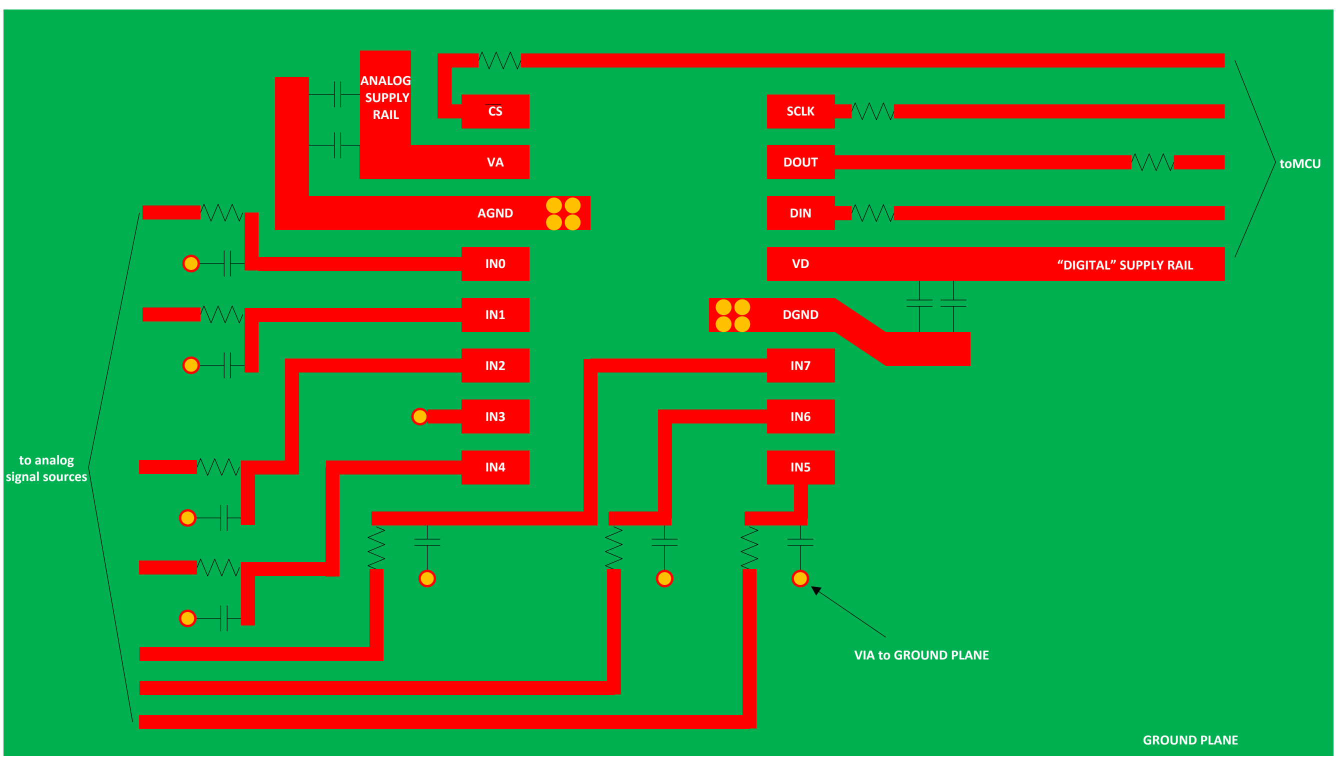


图 10-1. Layout Diagram

11 Device and Documentation Support

11.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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TI E2E™ is a trademark of Texas Instruments.
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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Engineering Samples

Engineering samples are available for order and are identified by *MPR* in the orderable device name (see *Packaging Information* at the end of this document). Engineering (MPR) samples meet the performance specifications of the data sheet at room temperature only and have not received the full space production flow or testing. Engineering samples may be QCI rejects that failed tests that do not impact the performance at room temperature, such as radiation or reliability testing.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADC128S102PWTSEP	Active	Production	TSSOP (PW) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	128S102
ADC128S102PWTSEP.A	Active	Production	TSSOP (PW) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	128S102

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

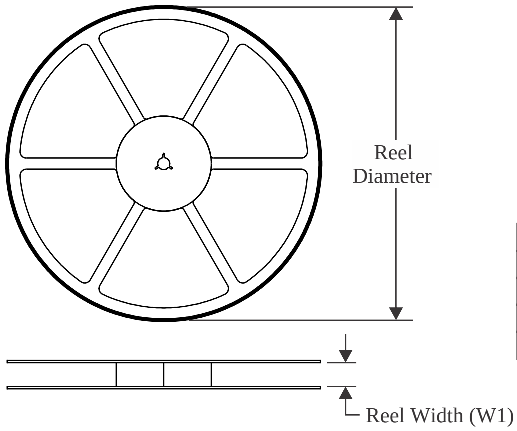
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

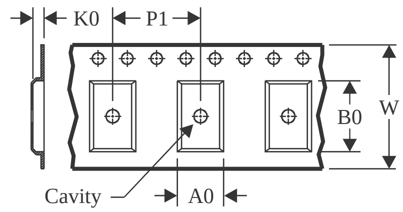
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

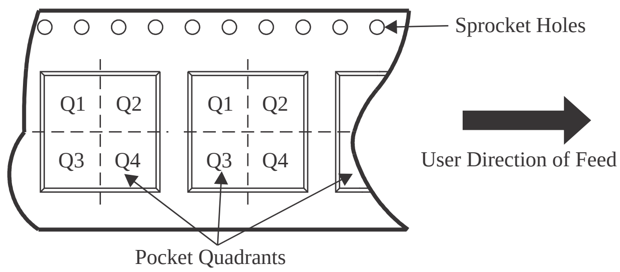


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

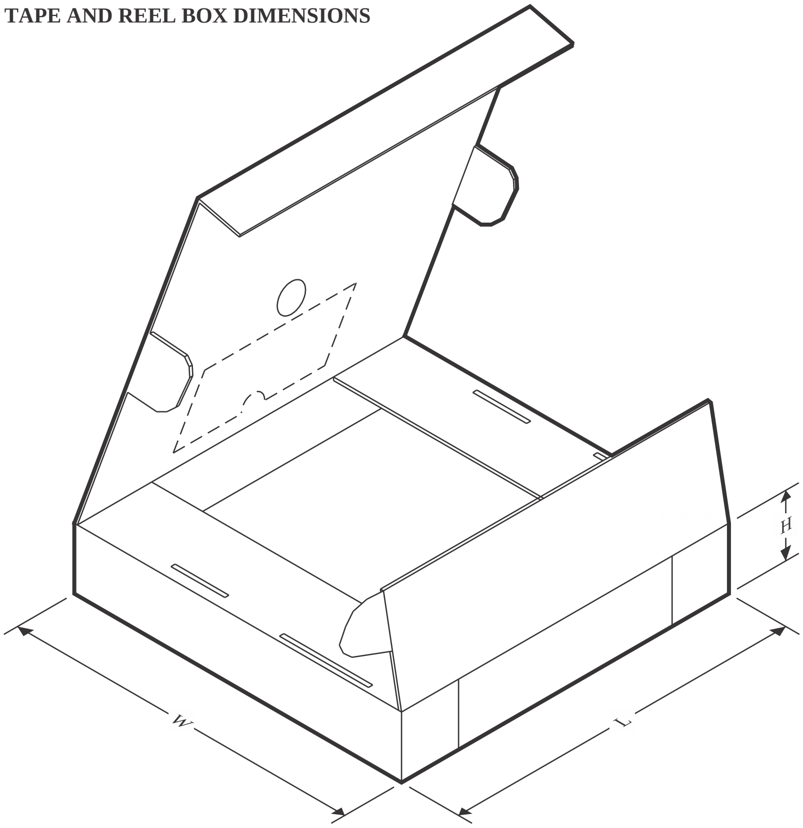
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

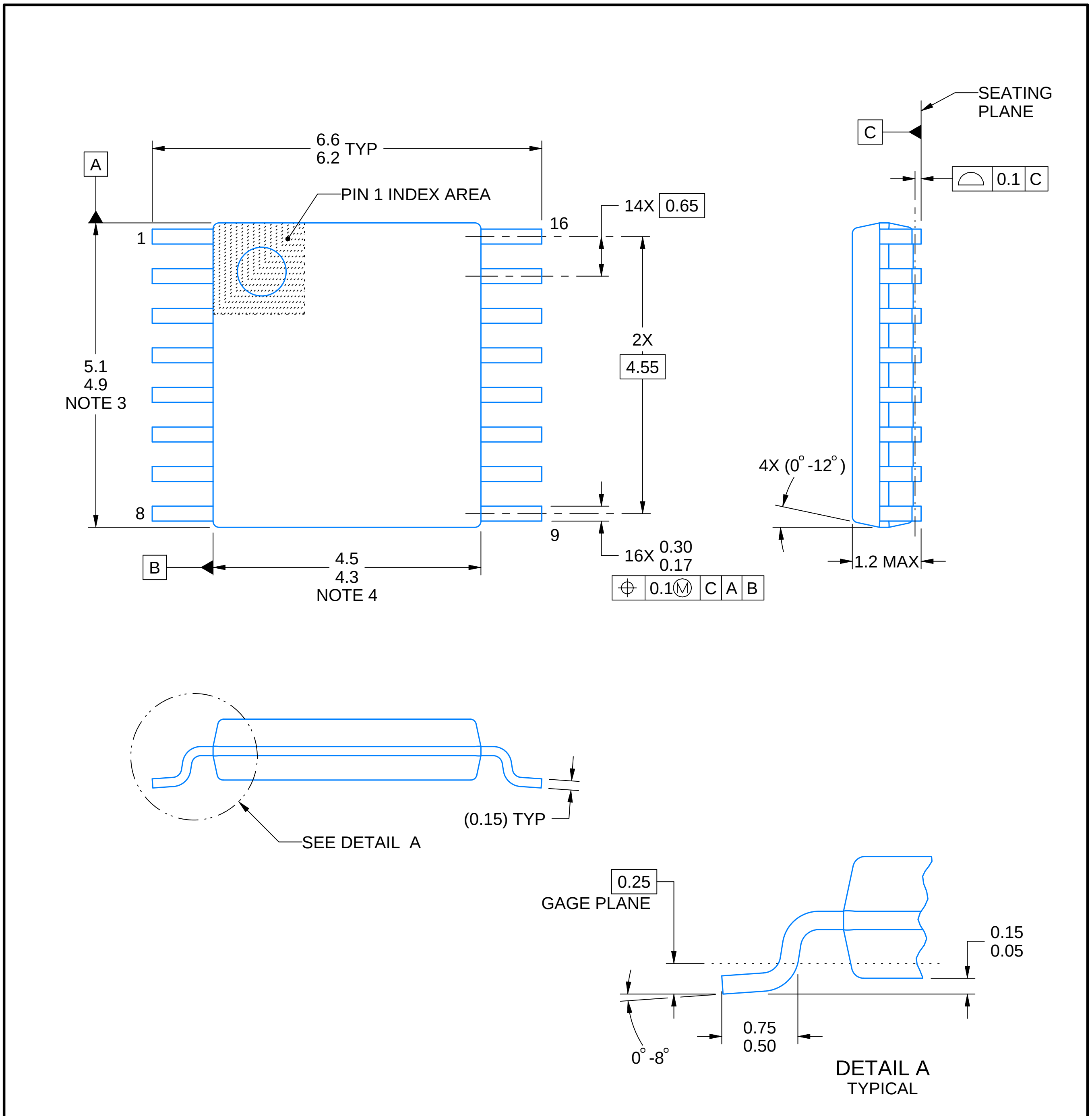
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC128S102PWTSEP	TSSOP	PW	16	250	177.8	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC128S102PWTSEP	TSSOP	PW	16	250	208.0	191.0	35.0



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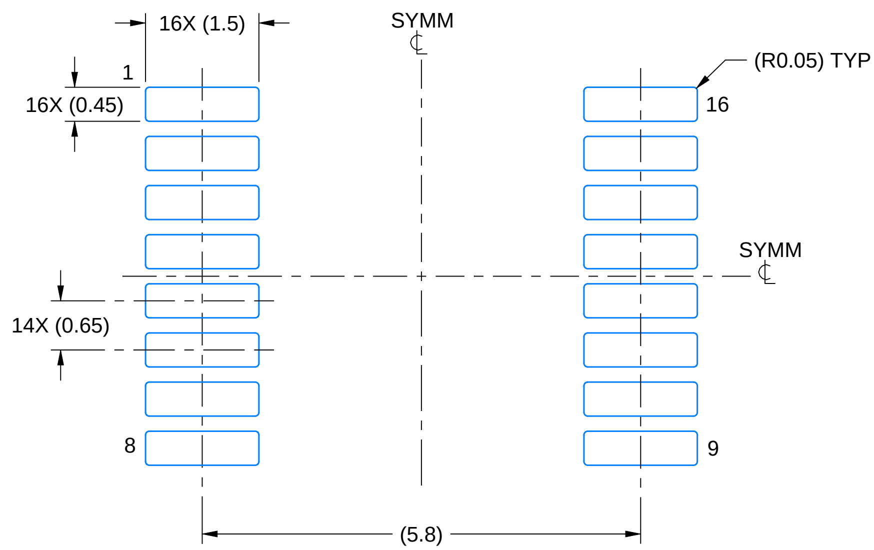
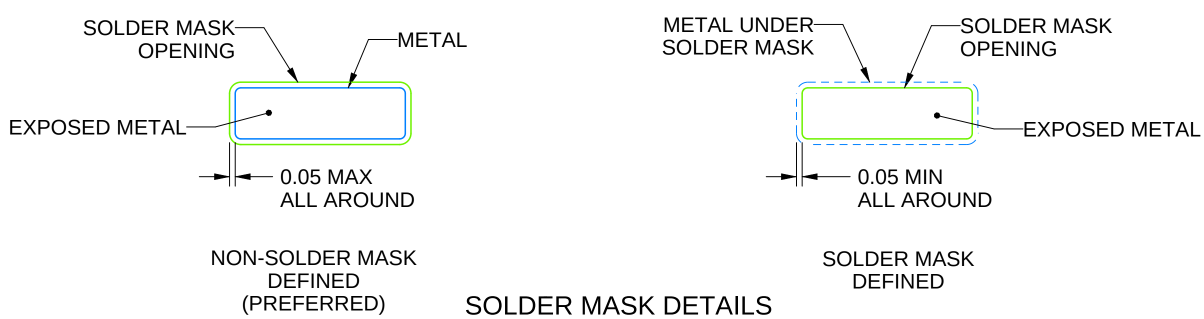
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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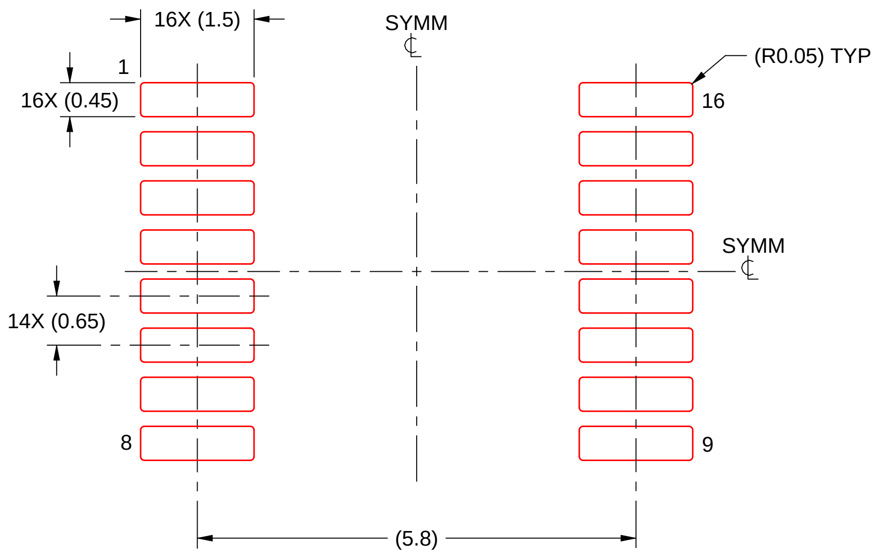
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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