

ADC082S051 2 Channel, 200 ksps to 500 ksps, 8-Bit A/D Converter

Check for Samples: [ADC082S051](#)

FEATURES

- Specified Over a Range of Sample Rates
- Two Input Channels
- Variable Power Management
- Single Power Supply with 2.7V - 5.25V Range

KEY SPECIFICATIONS

- DNL: ± 0.09 LSB (Typ)
- INL: $+ 0.12/-0.062$ LSB (Typ)
- SNR: 49.5 dB (Typ)
- Power Consumption:
 - 3V Supply: 2.2 mW (Typ)
 - 5V Supply 7.1 mW (Typ)

APPLICATIONS

- Portable Systems
- Remote Data Acquisition
- Instrumentation and Control Systems

DESCRIPTION

The ADC082S051 is a low-power, two-channel CMOS 8-bit analog-to-digital converter with a high-speed serial interface. Unlike the conventional practice of specifying performance at a single sample rate only, the ADC082S051 is fully specified over a sample rate range of 200 ksps to 500 ksps. The converter is based on a successive-approximation register architecture with an internal track-and-hold circuit. It can be configured to accept one or two input signals at inputs IN1 and IN2.

The output serial data is straight binary, and is compatible with several standards, such as SPI™, QSPI™, MICROWIRE, and many common DSP serial interfaces.

The ADC082S051 operates with a single supply that can range from +2.7V to +5.25V. Normal power consumption using a +3V or +5V supply is 2.2 mW and 7.1 mW, respectively. The power-down feature reduces the power consumption to just 0.12 μ W using a +3V supply, or 0.35 μ W using a +5V supply.

The ADC082S051 is packaged in an 8-lead VSSOP package. Operation over the industrial temperature range of -40°C to $+85^{\circ}\text{C}$ is ensured.

Table 1. Pin-Compatible Alternatives by Resolution and Speed⁽¹⁾

| Resolution | Specified for Sample Rate Range of: | | |
|------------|-------------------------------------|-------------------|--------------------|
| | 50 to 200 ksps | 200 to 500 ksps | 500 ksps to 1 Msps |
| 12-bit | ADC122S021 | ADC122S051 | ADC122S101 |
| 10-bit | ADC102S021 | ADC102S051 | ADC102S101 |
| 8-bit | ADC082S021 | ADC082S051 | ADC082S101 |

(1) All devices are fully pin compatible.

Connection Diagram

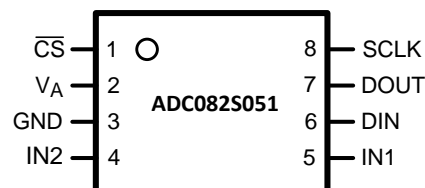


Figure 1. VSSOP Package
See Package Number DGK0008A



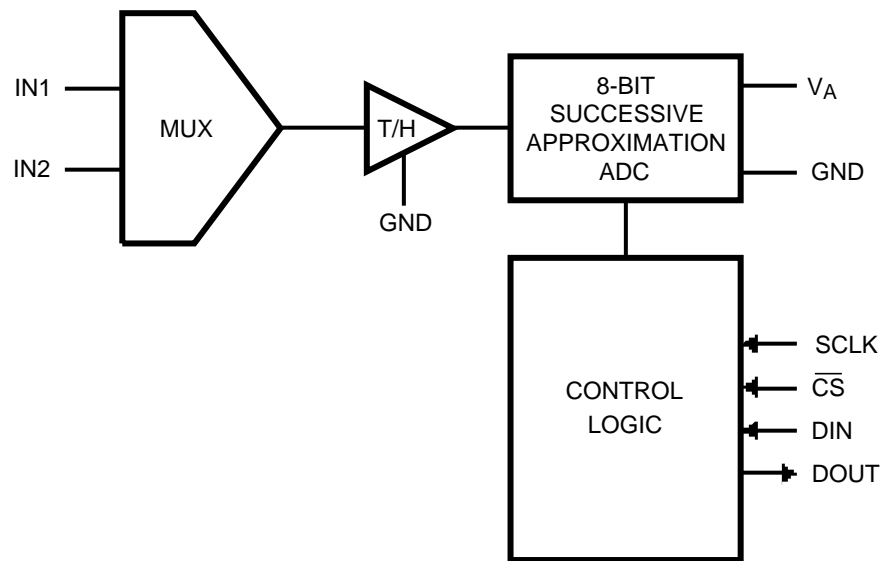
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2004–2013, Texas Instruments Incorporated

Block Diagram



Pin Descriptions and Equivalent Circuits

| Pin No. | Pin Name | Description |
|---------------------|-----------------|---|
| ANALOG I/O | | |
| 5,4 | IN1 and IN2 | Analog inputs. These signals can range from 0V to V _A . |
| DIGITAL I/O | | |
| 8 | SCLK | Digital clock input. This clock directly controls the conversion and readout processes. |
| 7 | DOUT | Digital data output. The output samples are clocked out of this pin on falling edges of the SCLK pin. |
| 6 | DIN | Digital data input. The ADC082S051's Control Register is loaded through this pin on rising edges of the SCLK pin. |
| 1 | \overline{CS} | Chip select. On the falling edge of \overline{CS} , a conversion process begins. Conversions continue as long as \overline{CS} is held low. |
| POWER SUPPLY | | |
| 2 | V _A | Positive supply pin. This pin should be connected to a quiet +2.7V to +5.25V source and bypassed to GND with a 1 μ F capacitor and a 0.1 μ F monolithic capacitor located within 1 cm of the power pin. |
| 3 | GND | The ground return for the die. |



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾⁽³⁾

| | | |
|---|------------------|-----------------------|
| Analog Supply Voltage V_A | | -0.3V to 6.5V |
| Voltage on Any Pin to GND | | -0.3V to $V_A + 0.3V$ |
| Input Current at Any Pin ⁽⁴⁾ | | ± 10 mA |
| Package Input Current ⁽⁴⁾ | | ± 20 mA |
| Power Consumption at $T_A = 25^\circ\text{C}$ | | See ⁽⁵⁾ |
| ESD Susceptibility ⁽⁶⁾ | Human Body Model | 2500V |
| | Machine Model | 250V |
| Junction Temperature | | +150°C |
| Storage Temperature | | -65°C to +150°C |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- (2) All voltages are measured with respect to GND = 0V, unless otherwise specified.
- (3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (4) When the input voltage at any pin exceeds the power supply (that is, $V_{IN} < \text{GND}$ or $V_{IN} > V_A$), the current at that pin should be limited to 10 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two. The Absolute Maximum Rating specification does not apply to the V_A pin. The current into the V_A pin is limited by the Analog Supply Voltage specification.
- (5) The absolute maximum junction temperature (T_{Jmax}) for this device is 150°C. The maximum allowable power dissipation is dictated by T_{Jmax} , the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_{DMAX} = (T_{Jmax} - T_A)/\theta_{JA}$. The values for maximum power dissipation listed above will be reached only when the device is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.
- (6) Human body model is 100 pF capacitor discharged through a 1.5 k Ω resistor. Machine model is 220 pF discharged through zero ohms

Operating Ratings⁽¹⁾⁽²⁾

| | |
|----------------------------------|---|
| Operating Temperature Range | $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ |
| V_A Supply Voltage | +2.7V to +5.25V |
| Digital Input Pins Voltage Range | -0.3V to V_A |
| Clock Frequency | 50 kHz to 16 MHz |
| Analog Input Voltage | 0V to V_A |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- (2) All voltages are measured with respect to GND = 0V, unless otherwise specified.

Package Thermal Resistance⁽¹⁾

| Package | θ_{JA} |
|--------------|---------------|
| 8-lead VSSOP | 250°C / W |

- (1) Soldering process must comply with Reflow Temperature Profile specifications. Refer to www.ti.com/packaging. Reflow temperature profiles are different for lead-free and non-lead-free packages.

ADC082S051 Converter Electrical Characteristics⁽¹⁾

The following specifications apply for $V_A = +2.7V$ to $5.25V$, $GND = 0V$, $f_{SCLK} = 3.2\text{ MHz}$ to 8 MHz , $f_{SAMPLE} = 200\text{ kpsps}$ to 500 kpsps , $C_L = 50\text{ pF}$, unless otherwise noted. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}** ; all other limits $T_A = 25^\circ C$.

| Parameter | | Test Conditions | Typical | Limits ⁽²⁾ | Units |
|-----------------------------------|--|---|---------------------|-----------------------|------------|
| STATIC CONVERTER CHARACTERISTICS | | | | | |
| | Resolution with No Missing Codes | | | 8 | Bits |
| INL | Integral Non-Linearity | | +0.12 | +0.4 | LSB (max) |
| | | | −0.062 | −0.3 | LSB (max) |
| DNL | Differential Non-Linearity | | ±0.09 | ±0.3 | LSB (max) |
| V _{OFF} | Offset Error | | 0.53 | ±0.7 | LSB (max) |
| OEM | Channel to Channel Offset Error Match | | 0.005 | ±0.3 | LSB (max) |
| FSE | Full-Scale Error | | 0.52 | ±0.7 | LSB (max) |
| FSEM | Channel to Channel Full- Scale Error Match | | 0.006 | ±0.3 | LSB (max) |
| DYNAMIC CONVERTER CHARACTERISTICS | | | | | |
| SINAD | Signal-to-Noise Plus Distortion Ratio | V _A = +2.7V to 5.25V, f _{IN} = 40.2 kHz, −0.02 dBFS | 49.5 | 49.1 | dB (min) |
| SNR | Signal-to-Noise Ratio | V _A = +2.7V to 5.25V f _{IN} = 40.2 kHz, −0.02 dBFS | 49.5 | 49.2 | dB (min) |
| THD | Total Harmonic Distortion | V _A = +2.7V to 5.25V, f _{IN} = 40.2 kHz, −0.02 dBFS | −76 | −62 | dB (max) |
| SFDR | Spurious-Free Dynamic Range | V _A = +2.7V to 5.25V f _{IN} = 40.2 kHz, −0.02 dBFS | 68 | 63 | dB (min) |
| ENOB | Effective Number of Bits | V _A = +2.7V to 5.25V | 7.93 | 7.9 | Bits (min) |
| | Channel-to-Channel Crosstalk | V _A = +2.7V to 5.25V f _{IN} = 40.2 kHz | −73 | | dB |
| IMD | Intermodulation Distortion, Second Order Terms | V _A = 5.25V, f _a = 40.161 kHz, f _b = 41.015 kHz | −78 | | dB |
| | Intermodulation Distortion, Third Order Terms | V _A = 5.25V f _a = 40.161 kHz, f _b = 41.015 kHz | −73 | | dB |
| FPBW | -3 dB Full Power Bandwidth | V _A = +5V | 11 | | MHz |
| | | V _A = +3V | 8 | | MHz |
| ANALOG INPUT CHARACTERISTICS | | | | | |
| V _{IN} | Input Range | | 0 to V _A | | V |
| I _{DCL} | DC Leakage Current | | | ±1 | μA (max) |
| C _{INA} | Input Capacitance | Track Mode | 33 | | pF |
| | | Hold Mode | 3 | | pF |
| DIGITAL INPUT CHARACTERISTICS | | | | | |
| V _{IH} | Input High Voltage | V _A = +5.25V | | 2.4 | V (min) |
| | | V _A = +3.6V | | 2.1 | V (min) |
| V _{IL} | Input Low Voltage | | | 0.8 | V (max) |
| I _{IN} | Input Current | V _{IN} = 0V or V _{IN} = V _A | | ±10 | μA (max) |
| C _{IND} | Digital Input Capacitance | | 2 | 4 | pF (max) |

(1) Min/max specification limits are ensured by design, test, or statistical analysis.

(2) Tested limits are ensured to TI's AOQL (Average Outgoing Quality Level).

ADC082S051 Converter Electrical Characteristics⁽¹⁾ (continued)

The following specifications apply for $V_A = +2.7\text{V}$ to 5.25V , $\text{GND} = 0\text{V}$, $f_{\text{SCLK}} = 3.2\text{ MHz}$ to 8 MHz , $f_{\text{SAMPLE}} = 200\text{ kpsps}$ to 500 kpsps , $C_L = 50\text{ pF}$, unless otherwise noted. **Boldface limits apply for $T_A = T_{\text{MIN}}$ to T_{MAX}** ; all other limits $T_A = 25^\circ\text{C}$.

| Parameter | | Test Conditions | Typical | Limits ⁽²⁾ | Units |
|---|--|---|---------------------------|-----------------------|-------------|
| DIGITAL OUTPUT CHARACTERISTICS | | | | | |
| V _{OH} | Output High Voltage | I _{SOURCE} = 200 μA | V _A – 0.03 | V _A – 0.5 | V (min) |
| | | I _{SOURCE} = 1 mA | V _A – 0.1 | | V |
| V _{OL} | Output Low Voltage | I _{SINK} = 200 μA | 0.03 | 0.4 | V (max) |
| | | I _{SINK} = 1 mA | 0.1 | | V |
| I _{OZH} , I _{OZL} | TRI-STATE Leakage Current | | 0.005 | ±1 | μA (max) |
| C _{OUT} | TRI-STATE Output Capacitance | | 2 | 4 | pF (max) |
| | Output Coding | | Straight (Natural) Binary | | |
| POWER SUPPLY CHARACTERISTICS (C _L = 10 pF) | | | | | |
| V _A | Analog Supply Voltage | | | 2.7 | V (min) |
| | | | | 5.25 | V (max) |
| I _A | Supply Current, Normal Mode (Operational, $\overline{\text{CS}}$ low) | V _A = +5.25V, f _{SAMPLE} = 500 ksps, f _{IN} = 40 kHz | 1.35 | 1.9 | mA (max) |
| | | V _A = +3.6V, f _{SAMPLE} = 500 ksps, f _{IN} = 40 kHz | 0.62 | 0.9 | mA (max) |
| | Supply Current, Shutdown ($\overline{\text{CS}}$ high) | V _A = +5.25V, f _{SAMPLE} = 0 ksps | 200 | | nA |
| | | V _A = +3.6V, f _{SAMPLE} = 0 ksps | 200 | | nA |
| P _D | Power Consumption, Normal Mode (Operational, $\overline{\text{CS}}$ low) | V _A = +5.25V | 7.1 | 10 | mW (max) |
| | | V _A = +3.6V | 2.23 | 3.2 | mW (max) |
| | Power Consumption, Shutdown ($\overline{\text{CS}}$ high) | V _A = +5.25V | 0.35 | | μW |
| | | V _A = +3.6V | 0.12 | | μW |
| AC ELECTRICAL CHARACTERISTICS | | | | | |
| f _{SCLK} | Clock Frequency | See ⁽³⁾ | | 3.2 | MHz (min) |
| | | | | 8 | MHz (max) |
| f _S | Sample Rate | See ⁽³⁾ | | 200 | ksps (min) |
| | | | | 500 | ksps (max) |
| t _{CONV} | Conversion Time | | | 13 | SCLK cycles |
| DC | SCLK Duty Cycle | f _{SCLK} = 8 MHz | 50 | 30 | % (min) |
| | | | | 70 | % (max) |
| t _{ACQ} | Track/Hold Acquisition Time | Full-Scale Step Input | | 3 | SCLK cycles |
| | Throughput Time | Acquisition Time + Conversion Time | | 16 | SCLK cycles |

(3) This is the frequency range over which the electrical performance is specified. The device is functional over a wider range which is specified under Operating Ratings.

ADC082S051 Timing Specifications

The following specifications apply for $V_A = +2.7V$ to $5.25V$, $GND = 0V$, $f_{SCLK} = 3.2\text{ MHz}$ to 8 MHz , $f_{SAMPLE} = 200\text{ kps}$ to 500 kps , $C_L = 50\text{ pF}$, **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}** ; all other limits $T_A = 25^\circ C$.

| Parameter | | Test Conditions | | Typical | Limits (1) | Units |
|-----------|--|-----------------|---------------|-----------------------|---|----------|
| t_{CSU} | Setup Time SCLK High to \overline{CS} Falling Edge | See (2) | $V_A = +3.0V$ | -3.5 | 10 | ns (min) |
| | | | $V_A = +5.0V$ | -0.5 | | |
| t_{CLH} | Hold time SCLK Low to \overline{CS} Falling Edge | See (2) | $V_A = +3.0V$ | +4.5 | 10 | ns (min) |
| | | | $V_A = +5.0V$ | +1.5 | | |
| t_{EN} | Delay from \overline{CS} Until DOUT active | | $V_A = +3.0V$ | +4 | 30 | ns (max) |
| | | | $V_A = +5.0V$ | +2 | | |
| t_{ACC} | Data Access Time after SCLK Falling Edge | | $V_A = +3.0V$ | +16.5 | 30 | ns (max) |
| | | | $V_A = +5.0V$ | +15 | | |
| t_{SU} | Data Setup Time Prior to SCLK Rising Edge | | | +3 | 10 | ns (min) |
| t_H | Data Valid SCLK Hold Time | | | +3 | 10 | ns (min) |
| t_{CH} | SCLK High Pulse Width | | | $0.5 \times t_{SCLK}$ | $0.3 \times t_{SCLK}$ | ns (min) |
| t_{CL} | SCLK Low Pulse Width | | | $0.5 \times t_{SCLK}$ | $0.3 \times t_{SCLK}$ | ns (min) |
| t_{DIS} | \overline{CS} Rising Edge to DOUT High-Impedance | Output Falling | $V_A = +3.0V$ | 1.7 | 20 | ns (max) |
| | | | $V_A = +5.0V$ | 1.2 | | |
| | | Output Rising | $V_A = +3.0V$ | 1.0 | | |
| | | | $V_A = +5.0V$ | 1.0 | | |

(1) Tested limits are ensured to TI's AOQL (Average Outgoing Quality Level).

(2) Clock may be either high or low when \overline{CS} is asserted as long as setup and hold times t_{CSU} and t_{CLH} are strictly observed.

Timing Diagrams

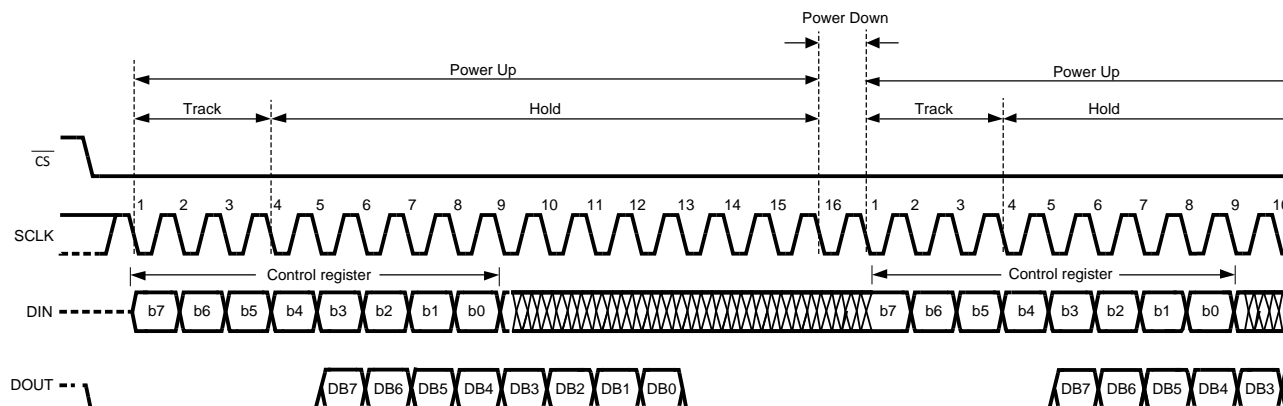


Figure 2. ADC082S051 Operational Timing Diagram

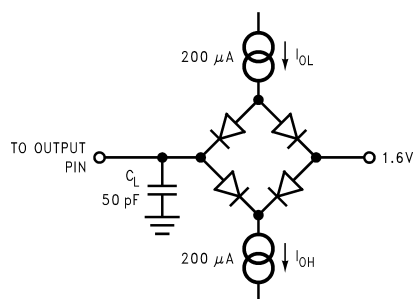


Figure 3. Timing Test Circuit

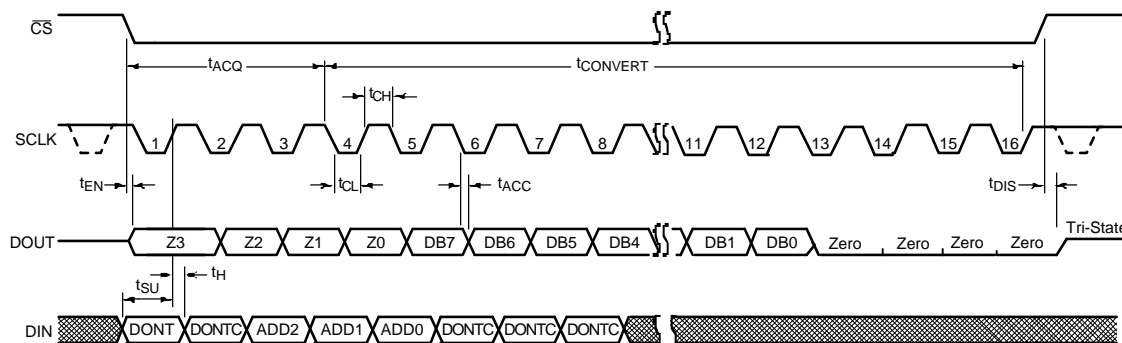


Figure 4. ADC082S051 Serial Timing Diagram

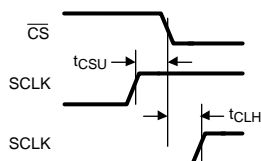


Figure 5. SCLK and \overline{CS} Timing Parameters

Specification Definitions

ACQUISITION TIME is the time required to acquire the input voltage. That is, it is time required for the hold capacitor to charge up to the input voltage.

APERTURE DELAY is the time between the fourth falling SCLK edge of a conversion and the time when the input signal is acquired or held for conversion.

CONVERSION TIME is the time required, after the input voltage is acquired, for the ADC to convert the input voltage to a digital word.

CROSSTALK is the coupling of energy from one channel into the other channel, or the amount of signal energy from one analog input that appears at the measured analog input.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

DUTY CYCLE is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the SCLK.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as $(\text{SINAD} - 1.76) / 6.02$ and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

FULL SCALE ERROR (FSE) is a measure of how far the last code transition is from the ideal $1\frac{1}{2}$ LSB below V_{REF}^+ and is defined as:

$$V_{\text{FSE}} = V_{\text{max}} + 1.5 \text{ LSB} - V_{\text{REF}}^+$$

where

- V_{max} is the voltage at which the transition to the maximum code occurs. FSE can be expressed in Volts, LSB or percent of full scale range. (1)

GAIN ERROR is the deviation of the last code transition (111...110) to (111...111) from the ideal ($V_{\text{REF}} - 1.5$ LSB), after adjusting for offset error.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale ($\frac{1}{2}$ LSB below the first code transition) through positive full scale ($\frac{1}{2}$ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the second and third order intermodulation products to the sum of the power in both of the original frequencies. IMD is usually expressed in dB.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC082S051 is specified not to have any missing codes.

OFFSET ERROR is the deviation of the first code transition (000...000) to (000...001) from the ideal (i.e. GND + 0.5 LSB).

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal at the converter output to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including d.c. or harmonics included in the THD specification.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal where a spurious signal is any signal present in the output spectrum that is not present at the input, excluding d.c.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB or dBc, of the rms total of the first five harmonic components at the output to the rms level of the input signal frequency as seen at the output. THD is calculated as

$$\text{THD} = 20 \cdot \log_{10} \sqrt{\frac{A_{f2}^2 + \dots + A_{f6}^2}{A_{f1}^2}}$$

where

- A_{f1} is the RMS power of the input frequency at the output and A_{f2} through A_{f6} are the RMS power in the first 5 harmonic frequencies. Accurate THD measurement requires a spectrally pure sine wave (monotone) at the ADC input. (2)

THROUGHPUT TIME is the minimum time required between the start of two successive conversion. It is the acquisition time plus the conversion and read out times. In the case of the ADC082S051, this is 16 SCLK periods.

Typical Performance Characteristics

$T_A = +25^\circ\text{C}$, $f_{\text{SAMPLE}} = 200 \text{ kpsps}$ to 500 kpsps , $f_{\text{SCLK}} = 3.2 \text{ MHz}$ to 8 MHz , $f_{\text{IN}} = 40.2 \text{ kHz}$ unless otherwise stated.

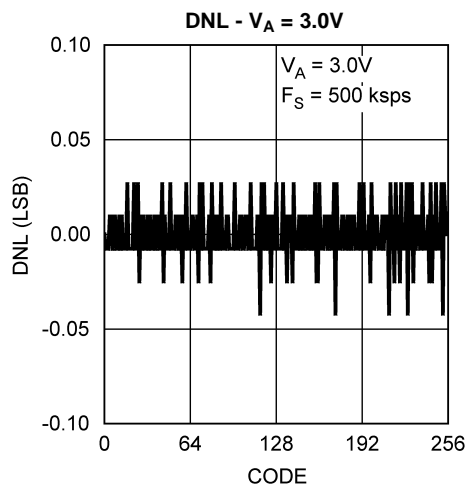


Figure 6.

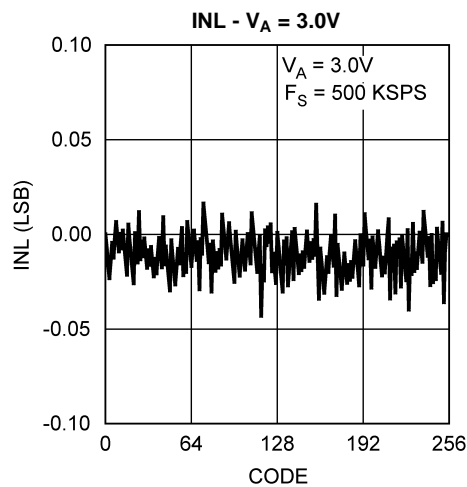


Figure 7.

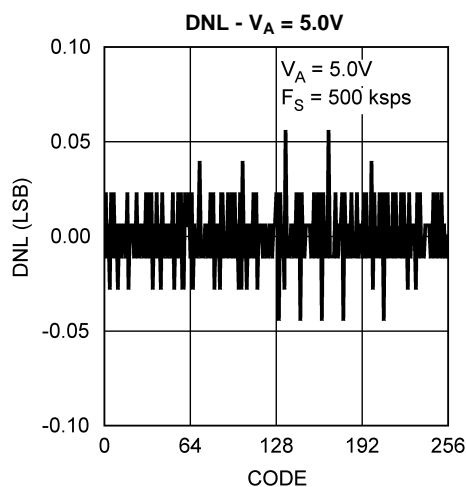


Figure 8.

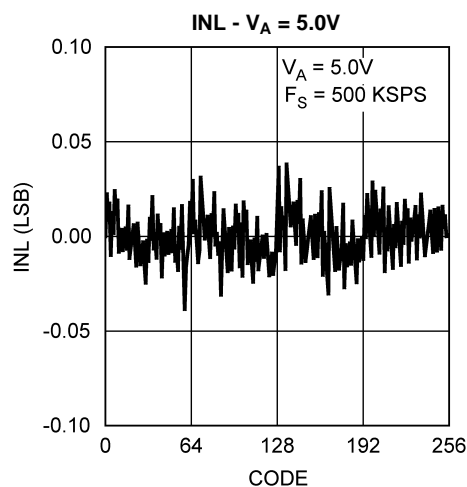


Figure 9.

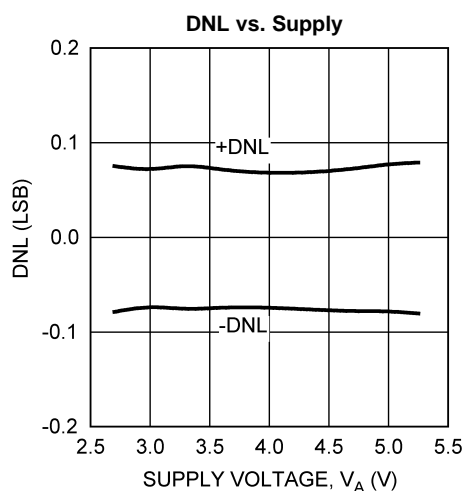


Figure 10.

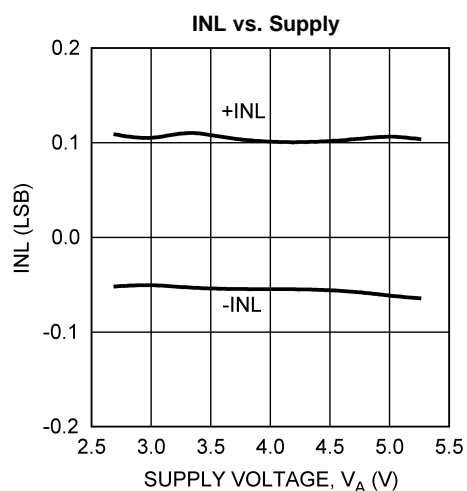


Figure 11.

Typical Performance Characteristics (continued)

$T_A = +25^\circ\text{C}$, $f_{\text{SAMPLE}} = 200 \text{ kps to } 500 \text{ kps}$, $f_{\text{SCLK}} = 3.2 \text{ MHz to } 8 \text{ MHz}$, $f_{\text{IN}} = 40.2 \text{ kHz}$ unless otherwise stated.

DNL vs. Clock Frequency

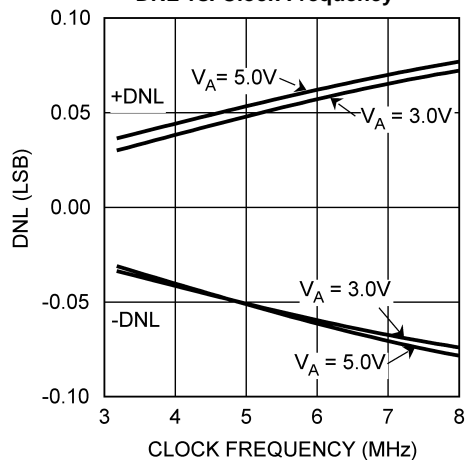


Figure 12.

INL vs. Clock Frequency

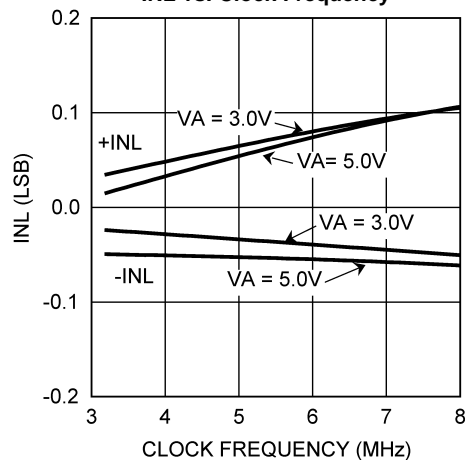


Figure 13.

DNL vs. Clock Duty Cycle

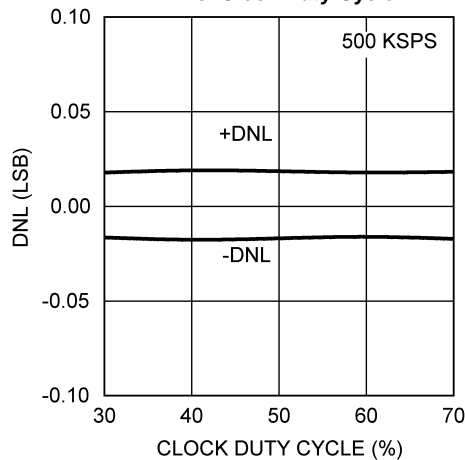


Figure 14.

INL vs. Clock Duty Cycle

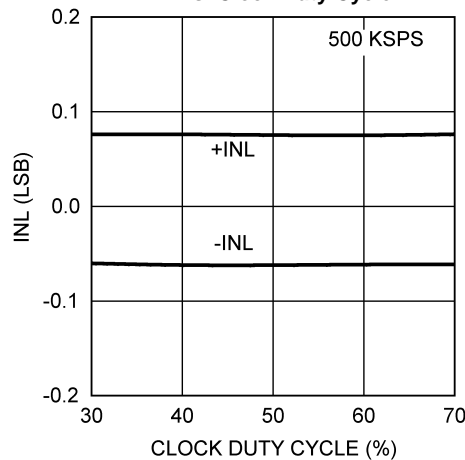


Figure 15.

DNL vs. Temperature

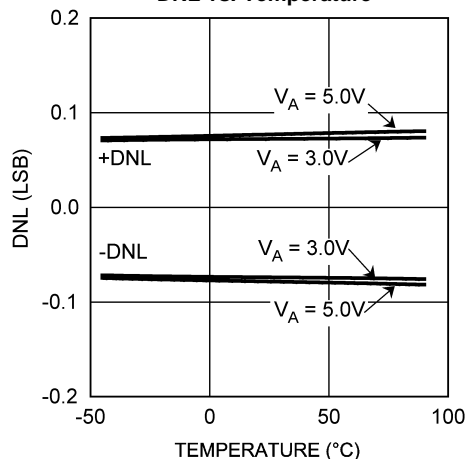


Figure 16.

INL vs. Temperature

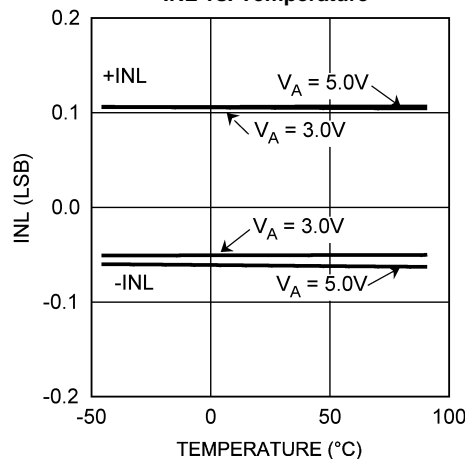


Figure 17.

Typical Performance Characteristics (continued)

$T_A = +25^\circ\text{C}$, $f_{\text{SAMPLE}} = 200 \text{ kpsps}$ to 500 kpsps , $f_{\text{SCLK}} = 3.2 \text{ MHz}$ to 8 MHz , $f_{\text{IN}} = 40.2 \text{ kHz}$ unless otherwise stated.

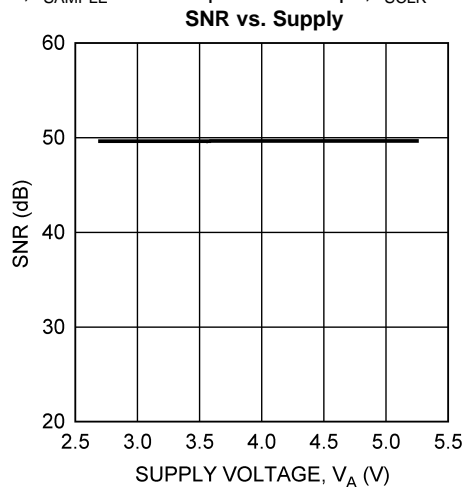


Figure 18.

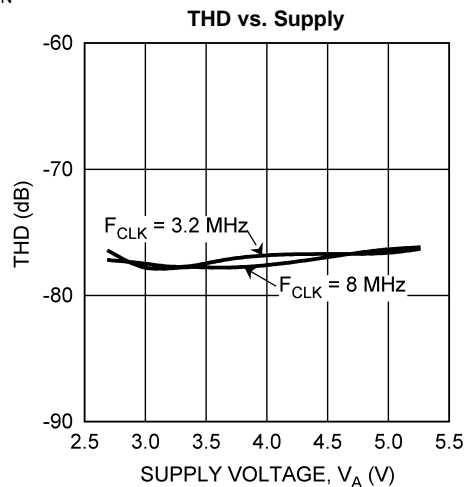


Figure 19.

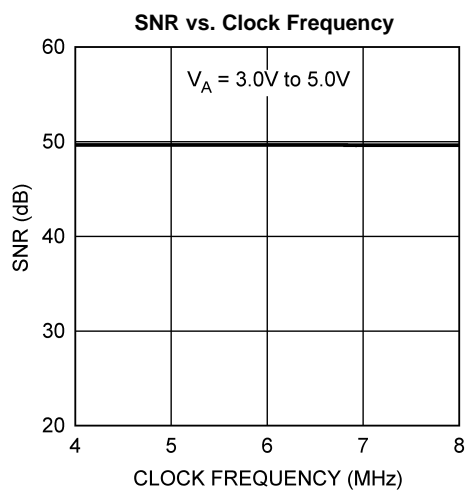


Figure 20.

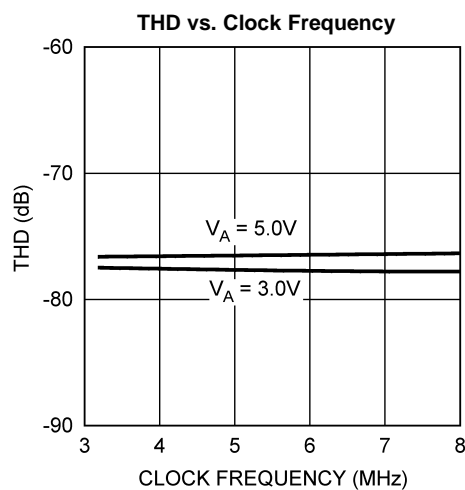


Figure 21.

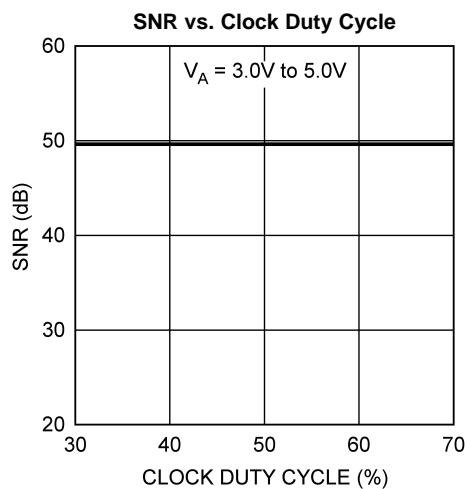


Figure 22.

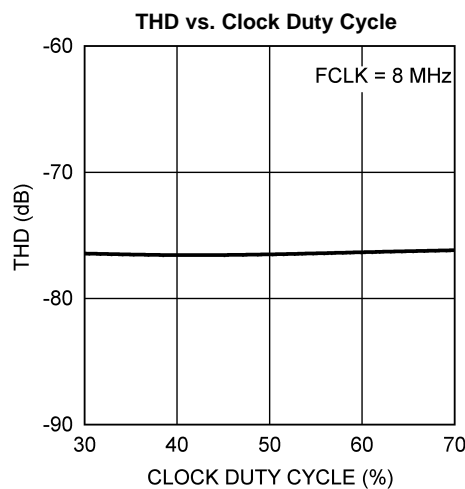


Figure 23.

Typical Performance Characteristics (continued)

$T_A = +25^\circ\text{C}$, $f_{\text{SAMPLE}} = 200 \text{ kpsps}$ to 500 kpsps , $f_{\text{SCLK}} = 3.2 \text{ MHz}$ to 8 MHz , $f_{\text{IN}} = 40.2 \text{ kHz}$ unless otherwise stated.

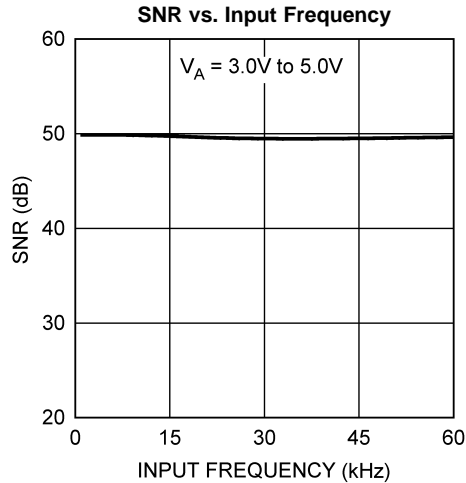


Figure 24.

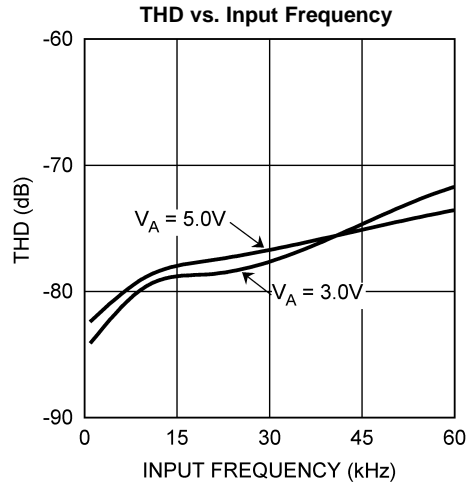


Figure 25.

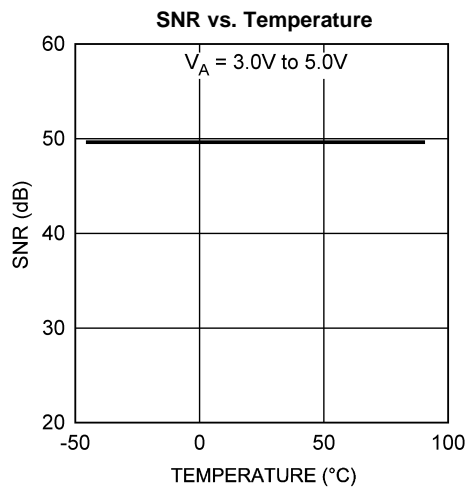


Figure 26.

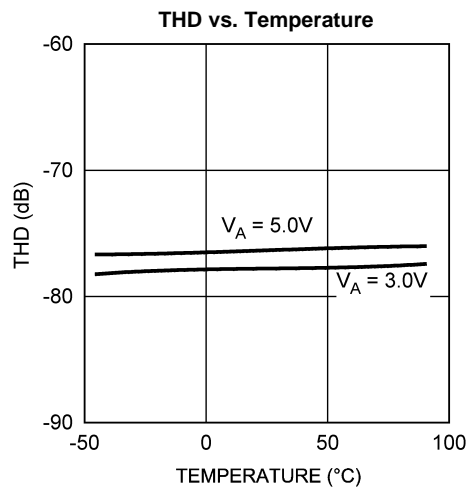


Figure 27.

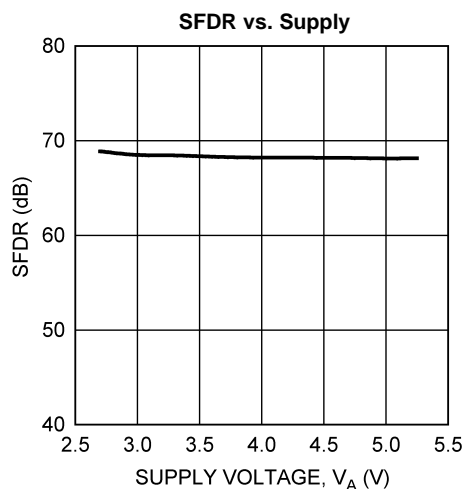


Figure 28.

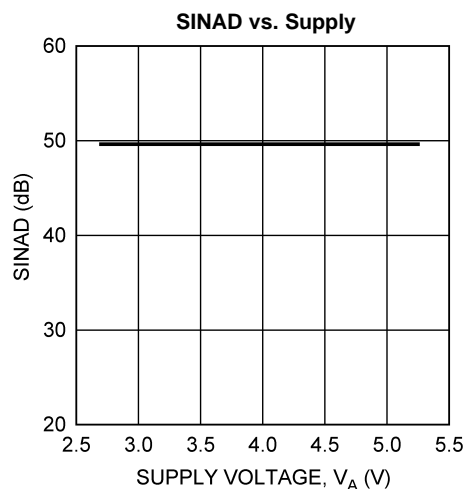


Figure 29.

Typical Performance Characteristics (continued)

$T_A = +25^\circ\text{C}$, $f_{\text{SAMPLE}} = 200 \text{ kpsps to } 500 \text{ kpsps}$, $f_{\text{SCLK}} = 3.2 \text{ MHz to } 8 \text{ MHz}$, $f_{\text{IN}} = 40.2 \text{ kHz}$ unless otherwise stated.

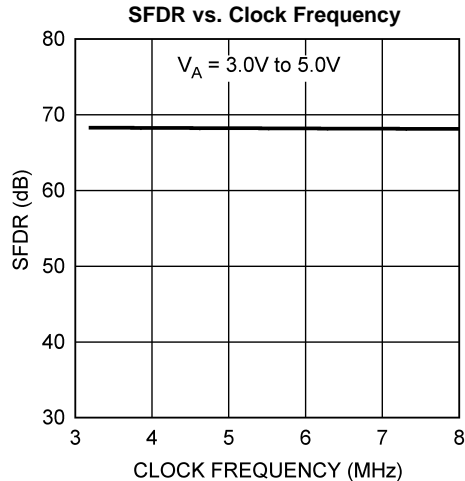


Figure 30.

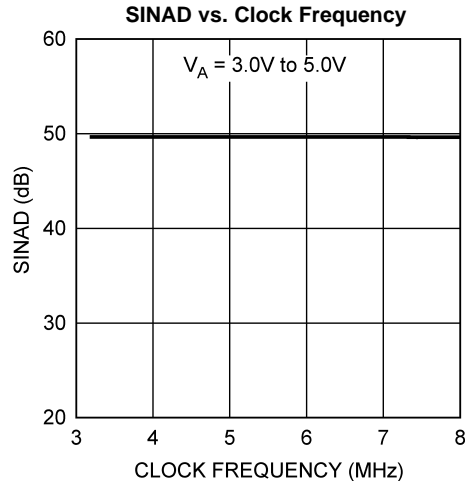


Figure 31.

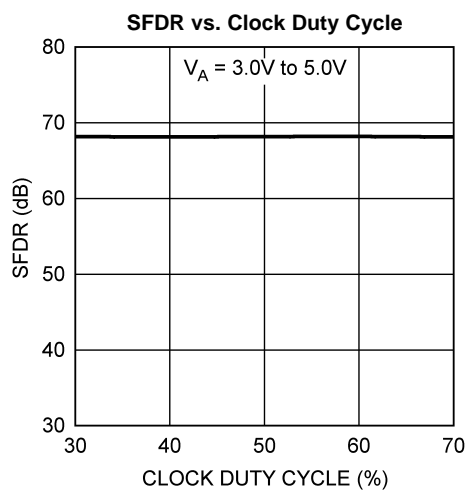


Figure 32.

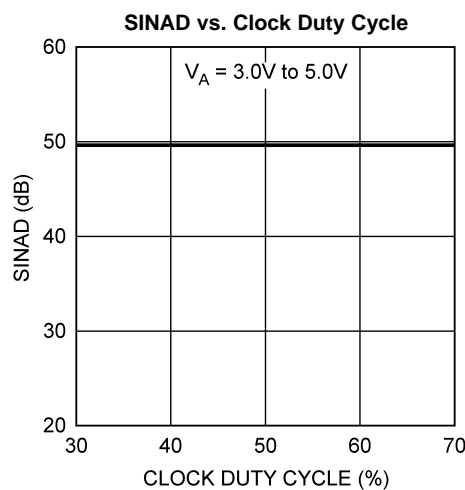


Figure 33.

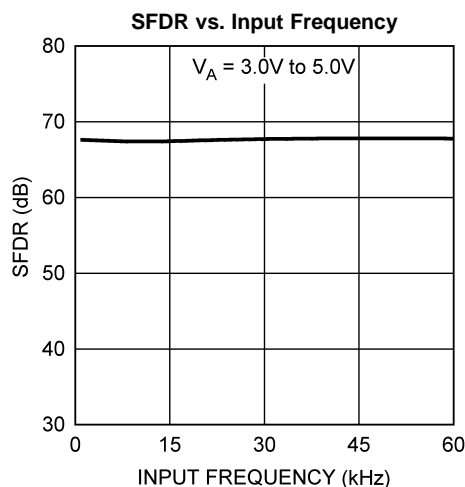


Figure 34.

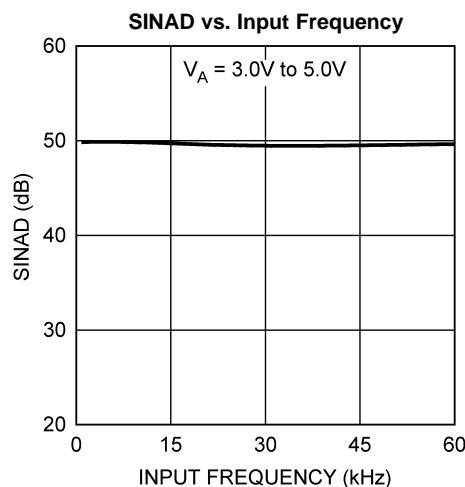


Figure 35.

Typical Performance Characteristics (continued)

$T_A = +25^\circ\text{C}$, $f_{\text{SAMPLE}} = 200 \text{ kps to } 500 \text{ kps}$, $f_{\text{SCLK}} = 3.2 \text{ MHz to } 8 \text{ MHz}$, $f_{\text{IN}} = 40.2 \text{ kHz}$ unless otherwise stated.

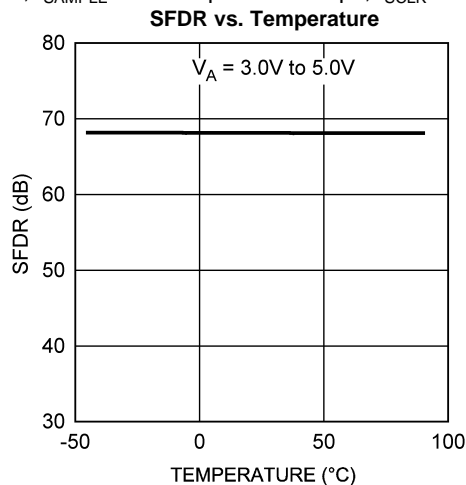


Figure 36.

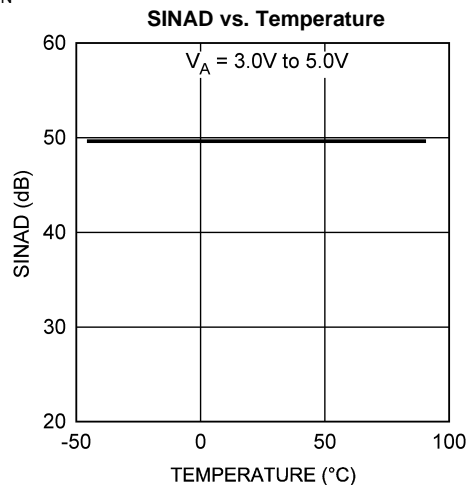


Figure 37.

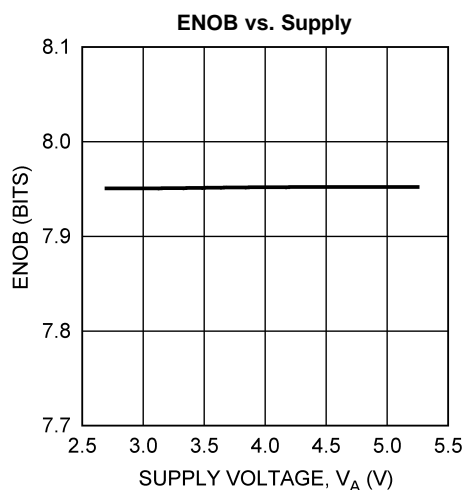


Figure 38.

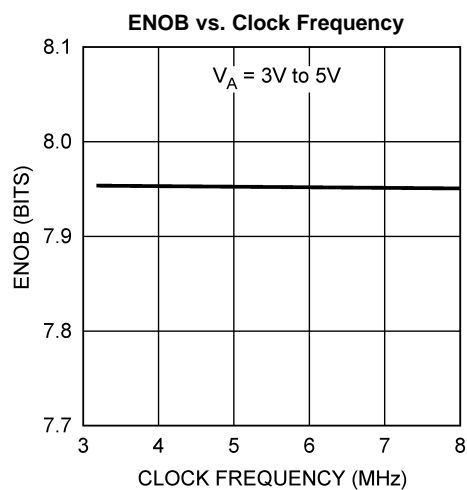


Figure 39.

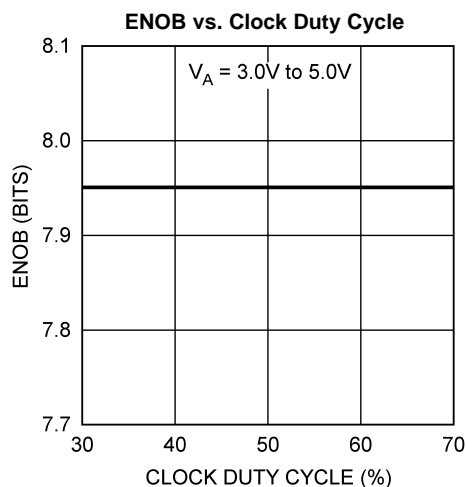


Figure 40.

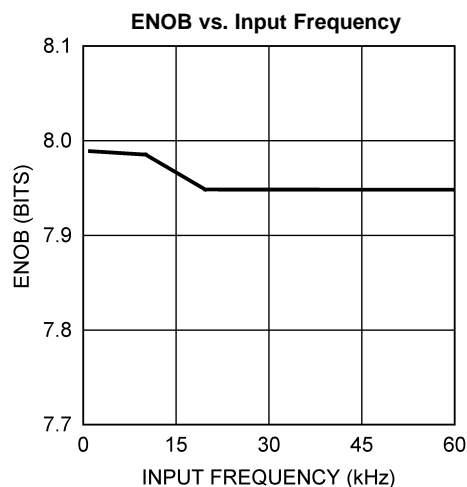


Figure 41.

Typical Performance Characteristics (continued)

$T_A = +25^\circ\text{C}$, $f_{\text{SAMPLE}} = 200 \text{ kpsps}$ to 500 kpsps , $f_{\text{SCLK}} = 3.2 \text{ MHz}$ to 8 MHz , $f_{\text{IN}} = 40.2 \text{ kHz}$ unless otherwise stated.

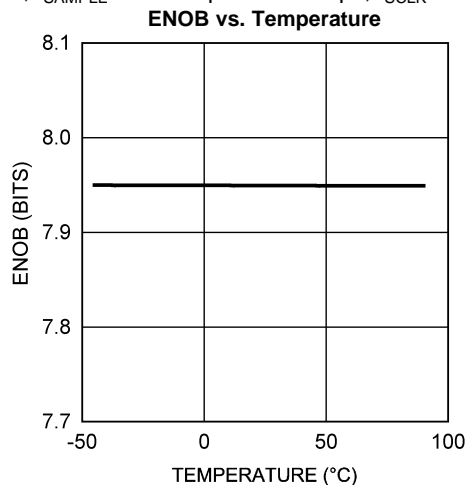


Figure 42.

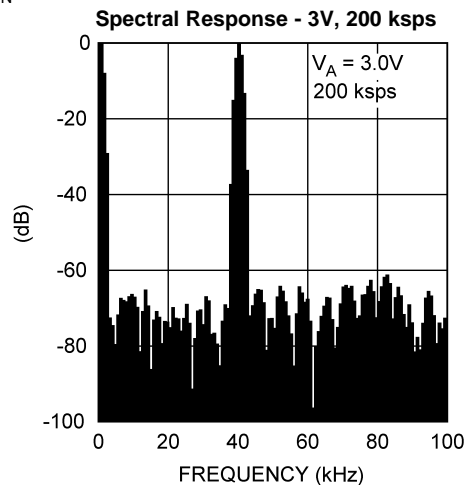


Figure 43.

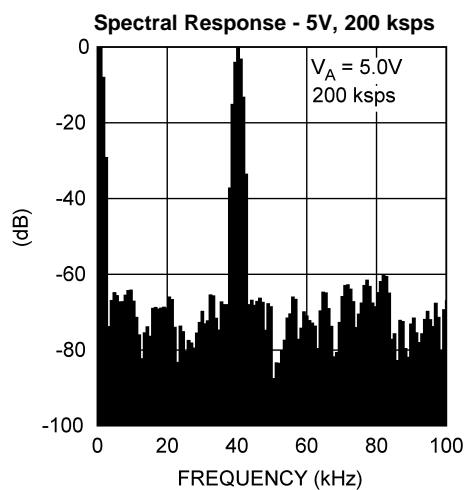


Figure 44.

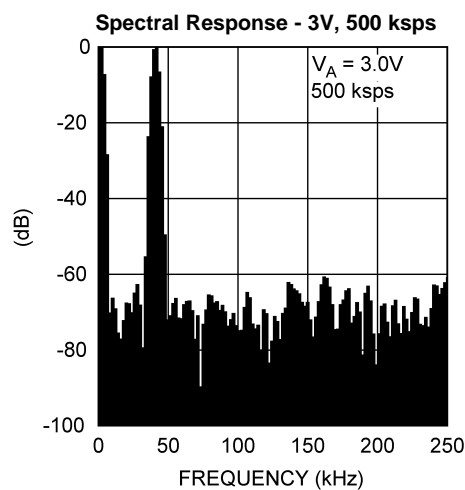


Figure 45.

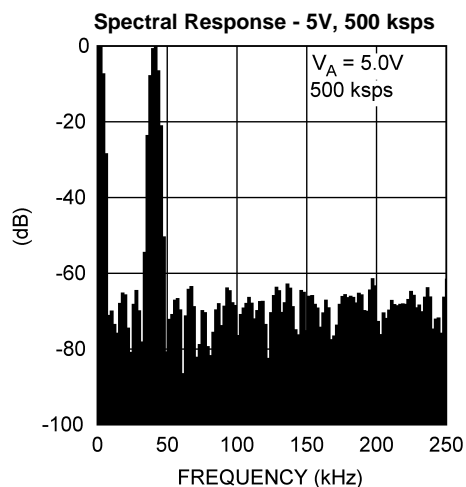


Figure 46.

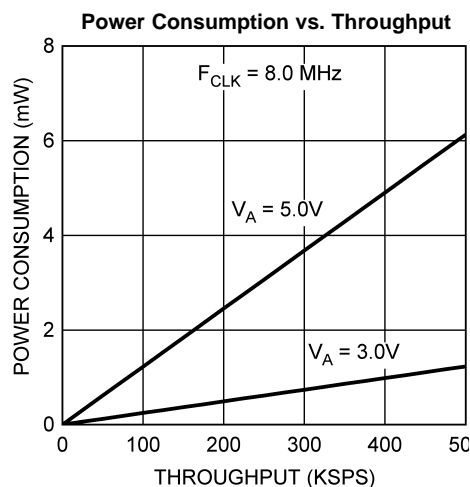


Figure 47.

APPLICATIONS INFORMATION

ADC082S051 OPERATION

The ADC082S051 is a successive-approximation analog-to-digital converter designed around a charge-redistribution digital-to-analog converter. Simplified schematics of the ADC082S051 in both track and hold modes are shown in Figure 48 and Figure 49, respectively. In Figure 48, the ADC082S051 is in track mode: switch SW1 connects the sampling capacitor to one of two analog input channels through the multiplexer, and SW2 balances the comparator inputs. The ADC082S051 is in this state for the first three SCLK cycles after \overline{CS} is brought low.

Figure 49 shows the ADC082S051 in hold mode: switch SW1 connects the sampling capacitor to ground, maintaining the sampled voltage, and switch SW2 unbalances the comparator. The control logic then instructs the charge-redistribution DAC to add fixed amounts of charge to the sampling capacitor until the comparator is balanced. When the comparator is balanced, the digital word supplied to the DAC is the digital representation of the analog input voltage. The ADC082S051 is in this state for the fourth through sixteenth SCLK cycles after \overline{CS} is brought low.

The time when \overline{CS} is low is considered a serial frame. Each of these frames should contain an integer multiple of 16 SCLK cycles, during which time a conversion is performed and clocked out at the DOUT pin and data is clocked into the DIN pin to indicate the multiplexer address for the next conversion.

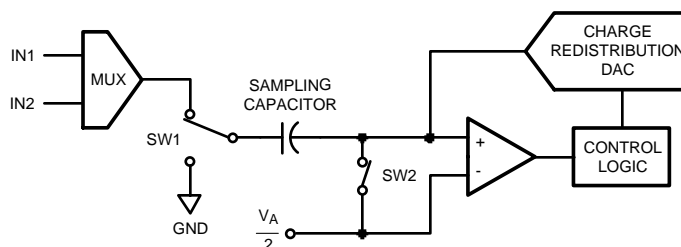


Figure 48. ADC082S051 in Track Mode

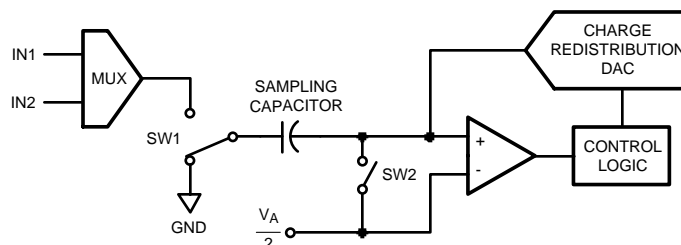


Figure 49. ADC082S051 in Hold Mode

USING THE ADC082S051

An ADC082S051 timing diagram and a serial interface timing diagram for the ADC082S051 are shown in the [Timing Diagrams](#) section. \overline{CS} is chip select, which initiates conversions and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of serial data. DOUT is the serial data output pin, where a conversion result is sent as a serial data stream, MSB first. Data to be written to the ADC082S051's Control Register is placed at DIN, the serial data input pin. New data is written to DIN with each conversion.

A serial frame is initiated on the falling edge of \overline{CS} and ends on the rising edge of \overline{CS} . Each frame must contain an integer multiple of 16 rising SCLK edges. The ADC output data (DOUT) is in a high impedance state when \overline{CS} is high and is active when \overline{CS} is low. Thus, \overline{CS} acts as an output enable. Additionally, the device goes into a power down state when \overline{CS} is high and also between continuous conversion cycles.

During the first 3 cycles of SCLK, the ADC is in the track mode, acquiring the input voltage. For the next 13 SCLK cycles the conversion is accomplished and the data is clocked out, MSB first, starting with the 5th clock. If there is more than one conversion in a frame, the ADC will re-enter the track mode on the falling edge of SCLK after the N*16th rising edge of SCLK, and re-enter the hold/convert mode on the N*16+4th falling edge of SCLK, where "N" is an integer.

When \overline{CS} is brought high, SCLK is internally gated off. If SCLK is stopped in the low state while \overline{CS} is high, the subsequent fall of \overline{CS} will generate a falling edge of the internal version of SCLK, putting the ADC into the track mode. This is seen by the ADC as the first falling edge of SCLK. If SCLK is stopped with SCLK high, the ADC enters the track mode on the first falling edge of SCLK after the falling edge of \overline{CS} .

During each conversion, data is clocked into the ADC at DIN on the first 8 rising edges of SCLK after the fall of \overline{CS} . For each conversion, it is necessary to clock in the data indicating the input that is selected for the conversion after the current one. See [Table 2](#), [Table 3](#), and [Table 4](#).

If \overline{CS} and SCLK go low within the times defined by t_{CSU} and t_{CLH} , the rising edge of SCLK that begins clocking data in at DIN may or may not be one clock cycle later than expected. It is, therefore, best to strictly observe the minimums t_{CSU} and t_{CLH} times given in the Timing Specifications.

There are no power-up delays or dummy conversions required with the ADC082S051. The ADC is able to sample and convert an input to full conversion immediately following power up. The first conversion result after power-up will be that of IN1.

Table 2. Control Register Bits

| Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|
| DONTC | DONTC | ADD2 | ADD1 | ADD0 | DONTC | DONTC | DONTC |

Table 3. Control Register Bit Descriptions

| Bit #: | Symbol: | Description |
|--------------|---------|---|
| 7 - 6, 2 - 0 | DONTC | Don't care. The value of these bits do not affect the device. |
| 3 | ADD0 | These bits determine which input channel will be sampled and converted in the next track/hold cycle. The mapping between codes and channels is shown in Table 4 . |
| 4 | ADD1 | |
| 5 | ADD2 | |

Table 4. Input Channel Selection

| ADD2 | ADD1 | ADD0 | Input Channel |
|------|------|------|--|
| x | 0 | 0 | IN1 (Default) |
| x | 0 | 1 | IN2 |
| x | 1 | x | Not allowed. The output signal at the D _{OUT} pin is indeterminate if ADD1 is high. |

ADC082S051 TRANSFER FUNCTION

The output format of the ADC082S051 is straight binary. Code transitions occur midway between successive integer LSB values. The LSB width for the ADC082S051 is $V_A/256$. The ideal transfer characteristic is shown in Figure 50. The transition from an output code of 0000 0000 to a code of 0000 0001 is at $1/2$ LSB, or a voltage of $V_A/512$. Other code transitions occur at steps of one LSB.

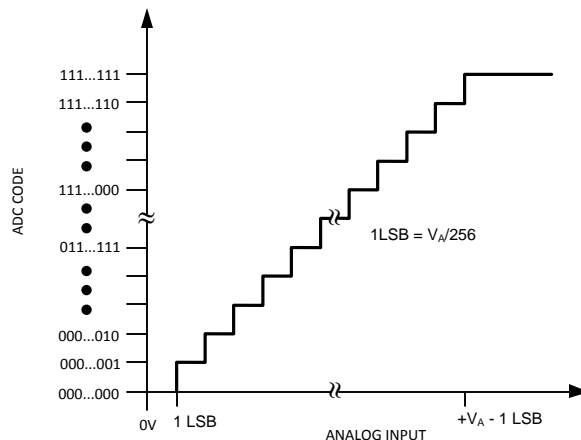


Figure 50. Ideal Transfer Characteristic

TYPICAL APPLICATION CIRCUIT

A typical application of the ADC082S051 is shown in Figure 51. Power is provided, in this example, by the Texas Instruments LP2950 low-dropout voltage regulator, available in a variety of fixed and adjustable output voltages. The power supply pin is bypassed with a capacitor network located close to the ADC082S051. Because the reference for the ADC082S051 is the supply voltage, any noise on the supply will degrade device noise performance. To keep noise off the supply, use a dedicated linear regulator for this device, or provide sufficient decoupling from other circuitry to keep noise off the ADC082S051 supply pin. Because of the ADC082S051's low power requirements, it is also possible to use a precision reference as a power supply to maximize performance. The four-wire interface is shown connected to a microprocessor or DSP.

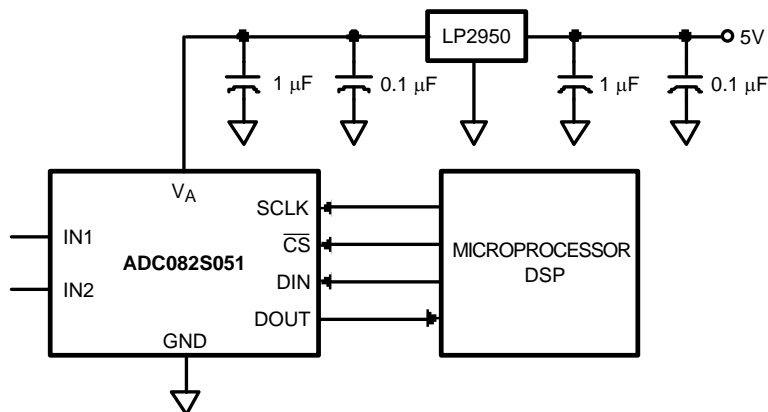


Figure 51. Typical Application Circuit

ANALOG INPUTS

An equivalent circuit for one of the ADC082S051's input channels is shown in [Figure 52](#). Diodes D1 and D2 provide ESD protection for the analog inputs. At no time should any input go beyond ($V_A + 300\text{ mV}$) or ($\text{GND} - 300\text{ mV}$), as these ESD diodes will begin conducting, which could result in erratic operation. For this reason, these ESD diodes should NOT be used to clamp the input signal.

The capacitor C1 in [Figure 52](#) has a typical value of 3 pF, and is mainly the package pin capacitance. Resistor R1 is the on resistance of the multiplexer and track / hold switch, and is typically 500 ohms. Capacitor C2 is the ADC082S051 sampling capacitor and is typically 30 pF. The ADC082S051 will deliver best performance when driven by a low-impedance source to eliminate distortion caused by the charging of the sampling capacitance. This is especially important when using the ADC082S051 to sample AC signals. Also important when sampling dynamic signals is a band-pass or low-pass filter to reduce harmonics and noise, improving dynamic performance.

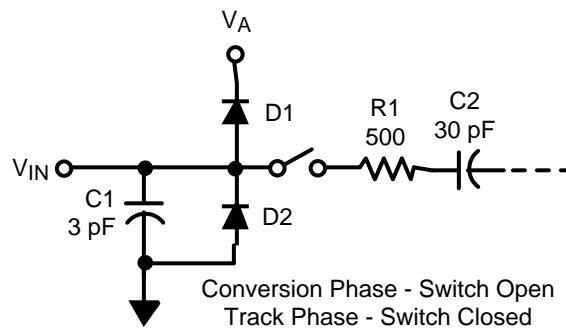


Figure 52. Equivalent Input Circuit

DIGITAL INPUTS AND OUTPUTS

The ADC082S051's digital output DOUT is limited by, and cannot exceed, the supply voltage, V_A . The digital input pins are not prone to latch-up and, although not recommended, SCLK, $\overline{\text{CS}}$ and DIN may be asserted before V_A without any latchup risk.

POWER SUPPLY CONSIDERATIONS

The ADC082S051 is fully powered-up whenever $\overline{\text{CS}}$ is low, and fully powered-down whenever $\overline{\text{CS}}$ is high, with one exception: the ADC082S051 automatically enters power-down mode between the 16th falling edge of a conversion and the 1st falling edge of the subsequent conversion (see [Timing Diagrams](#)).

The ADC082S051 can perform multiple conversions back to back; each conversion requires 16 SCLK cycles. The ADC082S051 will perform conversions continuously as long as $\overline{\text{CS}}$ is held low.

The user may trade off throughput for power consumption by simply performing fewer conversions per unit time. The Power Consumption vs. Sample Rate curve in the [Typical Performance Characteristics](#) section shows the typical power consumption of the ADC082S051 versus throughput. To calculate the power consumption, simply multiply the fraction of time spent in the normal mode by the normal mode power consumption, and add the fraction of time spent in shutdown mode multiplied by the shutdown mode power dissipation.

Power Management

When the ADC082S051 is operated continuously in normal mode, the maximum throughput is $f_{\text{SCLK}}/16$. Throughput may be traded for power consumption by running f_{SCLK} at its maximum 8 MHz and performing fewer conversions per unit time, putting the ADC082S051 into shutdown mode between conversions. A plot of typical power consumption versus throughput is shown in the [Typical Performance Characteristics](#) section. To calculate the power consumption for a given throughput, multiply the fraction of time spent in the normal mode by the normal mode power consumption and add the fraction of time spent in shutdown mode multiplied by the shutdown mode power consumption. Generally, the user will put the part into normal mode and then put the part back into shutdown mode. Note that the curve of power consumption vs. throughput is nearly linear. This is because the power consumption in the shutdown mode is so small that it can be ignored for all practical purposes.

Power Supply Noise Considerations

The charging of any output load capacitance requires current from the power supply, V_A . The current pulses required from the supply to charge the output capacitance will cause voltage variations on the supply. If these variations are large enough, they could degrade SNR and SINAD performance of the ADC. Furthermore, discharging the output capacitance when the digital output goes from a logic high to a logic low will dump current into the die substrate, which is resistive. Load discharge currents will cause "ground bounce" noise in the substrate that will degrade noise performance if that current is large enough. The larger is the output capacitance, the more current flows through the die substrate and the greater is the noise coupled into the analog channel, degrading noise performance.

To keep noise out of the power supply, keep the output load capacitance as small as practical. If the load capacitance is greater than 50 pF, use a 100 Ω series resistor at the ADC output, located as close to the ADC output pin as practical. This will limit the charge and discharge current of the output capacitance and maintain noise performance.

REVISION HISTORY

| Changes from Revision E (March 2013) to Revision F | Page |
|--|--------------------|
| • Changed layout of National Data Sheet to TI format | 21 |

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-------------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| ADC082S051C1MM/NO.A | Active | Production | VSSOP (DGK) 8 | 1000 SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | X04C |
| ADC082S051C1MM/NOPB | Active | Production | VSSOP (DGK) 8 | 1000 SMALL T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | X04C |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ADC082S051C1MM/NOPB | VSSOP | DGK | 8 | 1000 | 177.8 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ADC082S051CIMM/NOPB | VSSOP | DGK | 8 | 1000 | 210.0 | 185.0 | 35.0 |

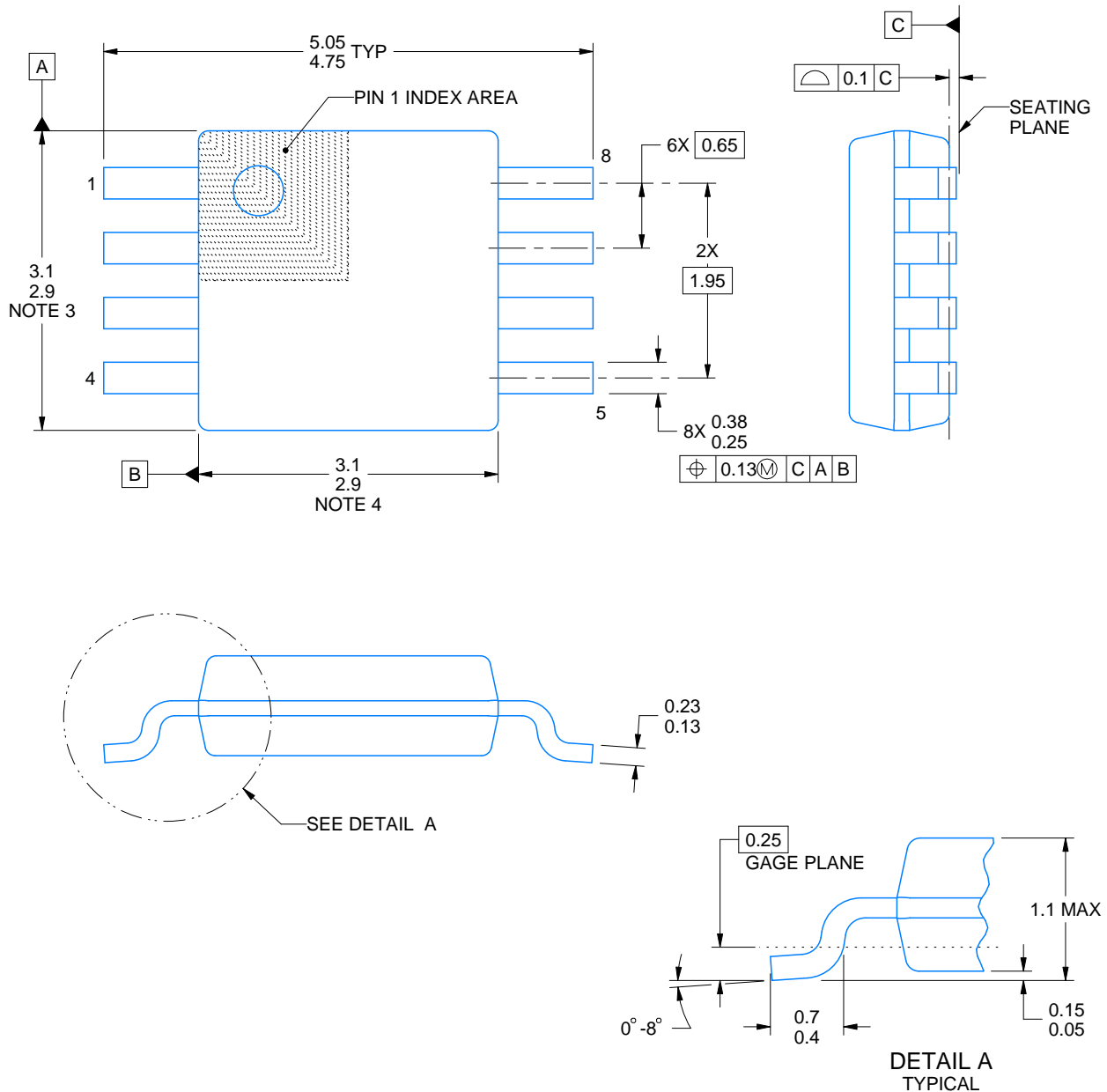
DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated